

Arm® CoreLink™ CMN-600AE Coherent Mesh Network

Revision: r1p0

Technical Reference Manual



Arm® CoreLink™ CMN-600AE Coherent Mesh Network

Technical Reference Manual

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Release Information

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Contents

Arm® CoreLink™ CMN-600AE Coherent Mesh Network Technical Reference Manual

Preface

About this book	8
Feedback	11

Chapter 1

Introduction

1.1 About CMN-600AE	1-13
1.2 Compliance	1-15
1.3 Features	1-16
1.4 Interfaces	1-20
1.5 Configurable options	1-21
1.6 Test features	1-32
1.7 Product documentation and design flow	1-33
1.8 Product revisions	1-35

Chapter 2

Functional description

2.1 Components	2-38
2.2 System configurations	2-45
2.3 CML system configurations	2-48
2.4 Node ID mapping	2-51
2.5 Discovery	2-53
2.6 Addressing capabilities	2-64
2.7 Atomics	2-65

2.8	Exclusive accesses	2-66
2.9	Processor events	2-67
2.10	Quality of Service	2-68
2.11	Barriers	2-76
2.12	DVM messages	2-77
2.13	PCIe integration	2-78
2.14	Reliability, Availability, and Serviceability	2-80
2.15	CCIX Port Aggregation Groups	2-96
2.16	System Address Map	2-97
2.17	RN SAM	2-98
2.18	CXRA SAM	2-104
2.19	HN-F SAM	2-105
2.20	RN and HN-F SAM additional features and programming	2-110
2.21	HN-I SAM	2-119
2.22	Cross chip routing and ID mapping	2-127
2.23	GIC communication over AXI4-Stream ports	2-133
2.24	Clocking	2-134
2.25	Reset	2-139
2.26	Power and clock management	2-140
2.27	RN entry to and exit from Snoop and DVM domains	2-151
2.28	Link layer	2-154
2.29	CML Symmetric Multiprocessor support	2-156

Chapter 3

Functional safety features

3.1	Overview	3-158
3.2	External interface protection	3-161
3.3	Internal interface protection	3-165
3.4	Logic protection	3-167
3.5	Shared RAM protection	3-170
3.6	Memory Protection Unit	3-172
3.7	Hang detector	3-176
3.8	Clock and reset protection	3-177
3.9	FuSa error reporting	3-181
3.10	Fault Management Unit	3-186

Chapter 4

Programmer's model

4.1	About the programmers model	4-189
4.2	Register summary	4-192
4.3	Register descriptions	4-233
4.4	CMN-600AE programming	4-1832
4.5	CML programming	4-1834
4.6	Support for RN-Fs compliant with CHI Issue A specification	4-1845

Chapter 5

SLC memory system

5.1	About the SLC memory system	5-1848
5.2	HN-F configurable options	5-1850
5.3	Basic operation	5-1851
5.4	Cache maintenance operations	5-1852
5.5	Cacheable and Non-cacheable exclusives	5-1853
5.6	TrustZone technology support	5-1854

5.7	Snoop connectivity and control	5-1855
5.8	QoS features	5-1856
5.9	Hardware-based cache flush engine	5-1858
5.10	DataSource handling	5-1860
5.11	Software configurable memory region locking	5-1861
5.12	Software-configurable On-Chip Memory	5-1863
5.13	Source-based SLC cache partitioning	5-1864
5.14	Way-based SLC cache partitioning	5-1865
5.15	Error reporting and software-configured error injection	5-1867

Chapter 6

Debug Trace and PMU

6.1	Debug trace system overview	6-1869
6.2	DT programming	6-1882
6.3	DT usage examples	6-1884
6.4	PMU system overview	6-1889
6.5	PMU system programming	6-1890
6.6	Secure debug support	6-1892

Chapter 7

Performance optimization and monitoring

7.1	Performance optimization guidelines	7-1894
7.2	About the Performance Monitoring Unit	7-1895
7.3	HN-F performance events	7-1899
7.4	RN-I performance events	7-1904
7.5	SBSX performance events	7-1908
7.6	HN-I performance events	7-1912
7.7	DN performance events	7-1916
7.8	XP PMU event summary	7-1917
7.9	Occupancy and lifetime measurement using PMU events	7-1918
7.10	DEVEVENT	7-1919

Appendix A

Signal descriptions

A.1	About the signal descriptions	Appx-A-1921
A.2	Clock and reset signals	Appx-A-1922
A.3	Clock management signals	Appx-A-1923
A.4	Power management signals	Appx-A-1926
A.5	Interrupt and event signals	Appx-A-1928
A.6	Configuration input signals	Appx-A-1929
A.7	Device population signals	Appx-A-1930
A.8	CHI interface signals	Appx-A-1931
A.9	AXI and ACE-Lite interface signals	Appx-A-1937
A.10	CGL interface signals	Appx-A-1947
A.11	Debug, trace, and PMU interface signals	Appx-A-1954
A.12	DFT and MBIST interface signals	Appx-A-1956
A.13	Processor event interface signals	Appx-A-1958
A.14	AXI4-Stream interface signals	Appx-A-1959
A.15	FMU interface signals	Appx-A-1961
A.16	APB interface signals	Appx-A-1962

Appendix B

Revisions

B.1	Revisions	Appx-B-1964
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Preface

This preface introduces the *Arm® CoreLink™ CMN-600AE Coherent Mesh Network Technical Reference Manual*.

It contains the following:

- *About this book* on page 8.
- *Feedback* on page 11.

About this book

This book is for the Arm® CoreLink™ CMN-600AE Coherent Mesh Network product.

Product revision status

The *rm**pn* identifier indicates the revision status of the product described in this book, for example, r1p2, where:

rm Identifies the major revision of the product, for example, r1.

pn Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses Coherent Mesh Network CMN-600AE.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction

This chapter describes the CMN-600AE product.

Chapter 2 Functional description

This chapter describes the functionality of the CMN-600AE product.

Chapter 3 Functional safety features

This chapter describes CMN-600AE safety mechanisms and associated engineering requirements.

Chapter 4 Programmer's model

This chapter describes the memory map and registers, and provides information about programming the device.

Chapter 5 SLC memory system

This chapter describes the SLC memory system.

Chapter 6 Debug Trace and PMU

This chapter describes the *Debug Trace* (DT) and *Performance Monitoring Unit* (PMU) features.

Chapter 7 Performance optimization and monitoring

This chapter describes performance optimization techniques for use by system integrators, and the *Performance Monitoring Unit* (PMU).

Appendix A Signal descriptions

This section describes the CMN-600AE I/O signals.

Appendix B Revisions

This appendix describes the technical changes between released issues of this book.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the *Arm® Glossary* for more information.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

monospace

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

monospace italic

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

monospace bold

Denotes language keywords when used outside example code.

<and>

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

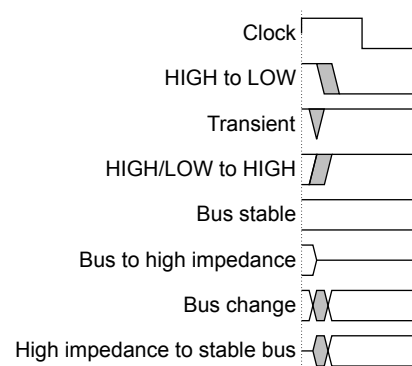


Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

Arm publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *AMBA® AXI and ACE Protocol Specification* (IHI 0022).
- *AMBA® 4 AXI4-Stream Protocol* (IHI 0051).
- *AMBA® 5 CHI Architecture Specification* (IHI 0050).
- *AMBA® CXS Protocol Specification* (IHI 0079).
- *AMBA® Low Power Interface Specification, Q-Channel and P-Channel Interfaces* (IHI 0068).
- *AMBA® APB Protocol Version: 2.0* (IHI 0024).
- *Reliability, Availability, and Serviceability (RAS) Architecture Specification ARMv8, for the ARMv8-A architecture profile* (DDI 0587).
- *Principles of Arm® Memory Maps White Paper* (DEN 0001).

The following non-confidential books are only available to licensees:

- *AMBA® Low Power Interface Specification Issue D Update* (AES 0009).
- *AMBA® Interface Parity Specification AHB, APB and AXI4-Stream* (AES 0010).

The following confidential books are only available to licensees:

- *Arm® CoreLink™ CMN-600AE Coherent Mesh Network Configuration and Integration Manual* (101409).
- *Arm® CoreLink™ CMN-600AE Safety Manual* (101410).
- *Arm® CoreLink™ CMN-600AE Development Interface Report* (101411).
- *Arm® CoreLink™ CMN-600AE Coherent Mesh Network Release Note* (PJDOC-1779577084-26841).
- *Arm® Neoverse™ N1 hyperscale reference design GIC-600 Integration using CMN-600 AXI4-Stream Interfaces White Paper* (PJDOC-1779577084-5931).

Other publications

- *JEDEC Standard Manufacturer's Identification Code*, JEP106, <http://www.jedec.org>.
- *Cache Coherent Interconnect for Accelerators CCIX Base Specification Revision 1.0 Version 0.9*, <https://www.ccixconsortium.com/>

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

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- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:

- The title *Arm CoreLink CMN-600AE Coherent Mesh Network Technical Reference Manual*.
- The number 101408_0100_04_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

————— **Note** —————

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Chapter 1

Introduction

This chapter describes the CMN-600AE product.

It contains the following sections:

- *1.1 About CMN-600AE* on page 1-13.
- *1.2 Compliance* on page 1-15.
- *1.3 Features* on page 1-16.
- *1.4 Interfaces* on page 1-20.
- *1.5 Configurable options* on page 1-21.
- *1.6 Test features* on page 1-32.
- *1.7 Product documentation and design flow* on page 1-33.
- *1.8 Product revisions* on page 1-35.

1.1 About CMN-600AE

The CMN-600AE product is a scalable configurable coherent interconnect with functional safety features designed for Coherent Mesh Network systems that are used in functional safety applications.

CMN-600AE is a scalable mesh interconnect with 1-8 processor compute clusters.

You can configure CMN-600AE using the Arm Socrates™ system IP Tooling platform. Socrates enables you to configure CMN-600AE, and generate a configuration file to send to Arm to be validated and built.

CMN-600AE supports Arm AMBA 5 CHI Issue B, including the following features:

- Far Atomic operations.
- Cache-stashing to improve data locality.
- Direct data transfer to reduce latency.

CMN-600AE provides system-level alignment by providing the following system functionality:

- *Quality of Service* (QoS)
- *Reliability, Availability, and Serviceability* (RAS)
- *Debug and Trace* (DT)

CMN-600AE is compatible with the following types of IP:

- *Generic Interrupt Controller* (GIC)
- *Memory Management Unit* (MMU)
- Armv8.0 and Armv8.2 processors

CMN-600AE provides an optional *Coherent Multichip Link* (CML) feature. CML is compliant with the CCIX standard and allows you to support up to four SoCs in a coherent system.

The following table shows the protocol nodes and devices present in a system built using CMN-600AE.

Table 1-1 Supported protocol nodes and devices

Protocol node or device	Description
<i>Fully coherent Requesting Node</i> (RN-F)	<p>A fully coherent master device that supports:</p> <ul style="list-style-type: none"> • CHI Issue B <p>———— Restriction ————</p> <p>All RN-Fs must be of the same type.</p>
<i>I/O coherent Requesting Node</i> (RN-I)	An I/O-coherent master device. This CHI bridge device acts as an RN-I proxy for one or more AXI or ACE-Lite master devices that connect to it.
<i>I/O coherent Requesting Node with DVM support</i> (RN-D)	An I/O coherent master device that supports acceptance of <i>Distributed Virtual Memory</i> (DVM) messages on the Snoop channel.
<i>Fully coherent Home Node</i> (HN-F)	A device that acts as a Home Node for a coherent region of memory. HN-Fs accept coherent requests from RN-Fs and RN-Is, and generates snoops to all applicable RN-Fs in the system as required to support the coherency protocol.
<i>I/O coherent Home Node</i> (HN-I)	<p>A device that acts as a Home Node for the slave I/O subsystem, responsible for ensuring proper ordering of requests targeting the slave I/O subsystem.</p> <p>HN-I supports AMBA AXI and ACE-Lite protocols.</p>

Table 1-1 Supported protocol nodes and devices (continued)

Protocol node or device	Description
<i>I/O coherent Home Node + DVM Node (HN-D)</i>	<p>A device that includes an HN-I, a <i>Debug Trace Controller (DTC)</i>, <i>DVM Node (DN)</i>, <i>configuration node (CFG)</i>, Global Configuration Slave, and the <i>Power/Clock Control Block (PCCB)</i>.</p> <p>———— Restriction ————</p> <p>Only one HN-D is allowed per CMN-600AE instance.</p> <p>—————</p>
<i>I/O coherent Home Node + DTC (HN-T)</i>	An HN-I with a built-in DTC and ATB.
<i>CHI Slave Node (SN-F)</i>	A device which solely receives CHI commands, limited to fulfilling simple read, write, and CMO requests targeting normal memory.
SBSX	A CHI bridge device that converts and forwards simple CHI read, write, and CMO commands to an AXI or ACE-Lite slave memory device.
CXG	A <i>CCIX Gateway (CXG)</i> device bridges between CHI and CXS (CCIX port).

1.2 Compliance

The CMN-600AE product is compliant with the *AMBA® 5 CHI Issue B Architecture Specification*.

AMBA® 5 CHI architecture

The CMN-600AE product implements the following architecture capabilities:

- Fully compliant with CHI interconnect architecture
- Non-blocking coherence protocol
- Packet-based communication
- Four channel types:
 - *Request* (REQ)
 - *Response* (RSP)
 - *Snoop* (SNP)
 - *Data* (DAT)
- Credited end-to-end protocol-layer flow control with a retry-once mechanism for flexible bandwidth and resource allocation
- Integrated end-to-end *Quality-of-Service* (QoS) capabilities

For more information, see the *Arm® AMBA® 5 CHI Issue B Architecture Specification*.

CCIX architecture

The CML CCIX implementation is compliant with *Cache Coherent Interconnect for Accelerators CCIX Base Specification Revision 1.0 Version 0.9* dated October 20, 2017.

1.3 Features

The CMN-600AE product provides the following key features:

- Highly scalable mesh network topology that is configurable up to a 4×4 mesh
- Custom mesh size and device placement
- Supports a programmable *System Address Map* (SAM)
- Supports up to eight RN-F interfaces for CHI-based compute clusters, accelerators, graphic processing units, or other cache coherent masters
- Supports up to four memory controllers.
- Supports up to eight RN-Is with up to three ACE5-Lite ports each (24 total)

Note

Extra devices are supported by using more levels of interconnect hierarchy, such as the CoreLink NIC-450 Network Interconnect Controller.

- Two 256-bit data channels, one for each direction
- DVM message transport between masters
- QoS regulation for shaping traffic profiles
- A *Performance Monitoring Unit* (PMU) to count performance-related events
- High-performance distributed *System Level Cache* (SLC) and *Snoop Filter* (SF) up to eight HN-Fs with cache sizes of 0-32MB total
- The HN-F includes an integrated *Point-of-Serialization* (PoS) and *Point-of-Coherency* (PoC) and its SLC (also referred to as Agile System Cache) can be used both for compute and I/O caching
- SF with up to 32MB of tag RAM for increased coherency scalability consisting of up to eight partitions (one per HN-F)
- Up to four HN-Is, each with an ACE-Lite master port
- Supports *Device Credited Slices* (DCSs) used for register slices at device interfaces, allowing flexibility in device placement
- Supports *Mesh Credited Slices* (MCSs) used for X-Y register slices, allowing flexibility in mesh floorplanning
- *On-Chip Memory* (OCM) allows for the creation of CMN-600AE systems without physical DDR memory
- RAS features including *Single-Error Correction and Double-Error Detection* (SECDDED) ECC and data poisoning signaling
- Supports up to two CCIX ports, which support one, two, or three CCIX links for chip-to-chip coherent communication. Each CCIX port has a CXS interface that transports CCIX TLP.
- Support for *Address Based Flush* (ABF)
- Support for way-based SLC partitioning
- Support for source-based way locking
- AXI4-Stream support
- *Functional Safety* (FuSa) features, comprising:
 - Selective duplication of logic with lock-step operation
 - Partial duplication of mesh transport logic comprising routers and switches
 - Asynchronous FIFO logic protection in logic blocks implementing clock domain crossing functions
 - RAM protection using ECC with address folding
 - Asynchronous interface checkers
 - Point-to-point parity protection of external interface signals
 - End-to-end protection of internal buses
 - Clock and reset checkers
 - FuSa error logging and reporting using a *Fault Management Unit* (FMU)
 - Dedicated APB interface into FMU for fault diagnostics and control
 - Support for MBIST for latent fault detection
 - Protection against systematic faults:

- Hang detectors flag transaction deadlocks
- *Memory Protection Unit* (MPU) detects illegal access to privileged memory regions

This section contains the following subsections:

- [1.3.1 CXS property support on page 1-17.](#)
- [1.3.2 CCIX property support on page 1-17.](#)
- [1.3.3 CHI feature support for CML on page 1-17.](#)

1.3.1 CXS property support

This section provides CXS information.

The following table contains CXS property settings.

Table 1-2 CXS property support

Property	Support
TX/RX CXSDATAFLITWIDTH	256
TX/RX CXSMAXPKTPERFLIT	2
TX CXSCONTINUOUSDATA	True
RX CXSCONTINUOUSDATA	False
TX/RX CXSErrorFULLPKT	True
TX/RX CXSDATACHECK	None
TX/RX CXSREPLICATION	None

1.3.2 CCIX property support

This section provides CCIX information for CML support.

The following table contains CCIX property settings for CML.

Table 1-3 CCIX property settings for CML

Property	Permitted values	Support
NoCompAck	True, False	False
PartialCacheStates	True, False	False
CacheLineSize	64B, 128B	64B
AddrWidth	48b, 52b, 56b, 60b, 64b	48b
PktHeader	Compatible, Optimized	Both
MaxPacketSize	128B, 256B, 512B	All
NoMessagePack	True, False	Both, the default is True

Restriction

The following CCIX features are not supported:

- Memory expansion. HN-Fs and their associated SN-Fs must be on the same chip
- Snoop chaining outbound
- CCIX snoop multicast, inbound and outbound
- Snoop broadcast outbound

1.3.3 CHI feature support for CML

This section provides CHI information for *Coherent Multichip Link* (CML) support.

The following table contains CHI support for CML settings.

Table 1-4 CHI support for CML

CHI feature	CML support		Comments
	Local	Remote	
Coherency	Yes	Yes	-
Ordering	Yes	Yes	-
Atomics	Yes	Yes	-
Exclusive Accesses	Yes	SMP Mode Only	Remote Support. Only RN-F exclusives are supported and can only target HN-F. In non-SMP mode, any read exclusive access is downgraded to a non-exclusive read and write exclusive is terminated at CXRA and Non-data Error response is sent.
Cache Stashing	Yes	No	-
DVM Operations	Yes	SMP Mode Only	-
Error Handling			
- Response Error	Yes	Yes	-
- Data Check	Yes	No	-
- Poison	Yes	Yes	Mandatory for CMN-600AE
QoS			
- Request	Yes	Yes	-
- Snoop	Yes	No	-
Data Return from Shared Clean	Yes	No	-
<i>Direct Cache Transfer</i> (DCT)	Yes	No	Local support includes local RN-F sending data directly to CCIX gateway block
<i>Direct Memory Transfer</i> (DMT)	Yes	No	Local support includes local SN-F sending data directly to CCIX gateway block
I/O Deallocation Transactions	Yes	Yes	-
CleanSharedPersist CMO	Yes	Yes	-
Prefetch Target	Yes	No	Remote Support. This request is intended to target SN and therefore is not expected at CXRA.
Trace Tag	Yes	SMP Mode Only	-
System Coherency Interface (SYSCOREQ and SYCOACK)	Yes	Yes (using s/w bits)	-
Partial Cache State	Yes	No	CXRA, inside CML block, does not accept the following requests and responses: <ul style="list-style-type: none"> WriteBackPtl WriteCleanPtl SnpRespDataPtl*
Streaming and Optimized Streaming of Ordered WriteUniques	Yes	No	WriteUnique* request with Request Order and ExpCompAck attributes set, RN must send the CompAck when it receives a Comp response for that write request. The RN must not create any dependencies on other outstanding writes.
CHI-A RN-F	No	No	CML configurations do not support CHI-A RN-F nodes

CML requirement

Each CML port requires a minimum of one request and one data credit more than the total number of reservations. This number is enabled through the CXRA configuration control register, `por_cxg_ra_cfg_ctl`.

This requirement applies to each enabled CCIX link at a given CCIX port. For example, by default all the reservations are enabled in the SMP mode. Therefore, a minimum of four request and four data credits are required to be granted per CCIX link. Certain traffic types, such as QoS-15, use these credentials to make progress in a loaded system. For more information, see the configuration register [por_cxg_ra_cfg_ctl](#) on page 4-970.

1.4 Interfaces

The CMN-600AE can be configured with various interfaces.

The following figure shows the interfaces of the CMN-600AE product.

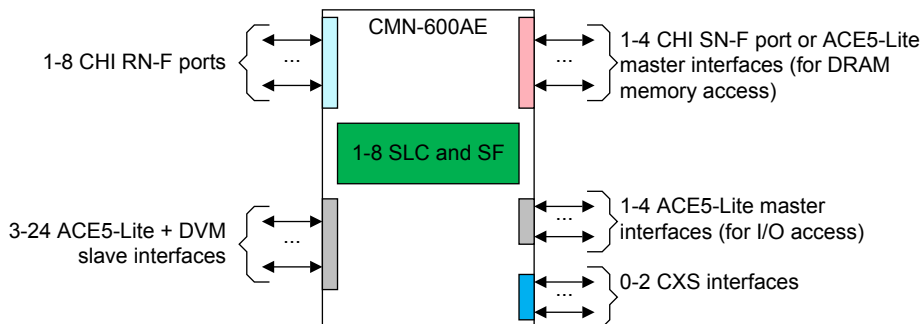


Figure 1-1 CMN-600AE interfaces

Note

All interfaces can be configured to be safe or non-safe.

1.5 Configurable options

The basic structure of CMN-600AE is a configurable rectangular grid that is comprised of network routers referred to as *Crosspoints* (XPs) and CHI-compliant devices. Each XP connects horizontally and vertically to other XPs, creating a two-dimensional mesh structure. Each XP has up to two ports to which CHI-compliant devices can be connected.

CMN-600AE provides several configurable parameters that can be configured to meet system requirements. You can use Socrates IP Tooling to initially auto-populate one or more devices throughout the mesh. Then refine the mesh design and/or device placement keeping in mind these guidelines:

CMN-600AE is configured in three steps:

1. System component selection. In this step, system components are determined, including:
 - The number and type of processors.
 - I/O interfaces.
 - Number of HN-Fs.
 - Amount of SLC.
 - Memory interfaces.
2. Mesh sizing and top-level configuration. This step includes specifying the following:
 - The number of rows and columns.
 - Global configuration parameters.
3. Device placement and configuration. This step involves:
 - Placement of devices and credited repeater slices between XPs based on floorplan needs.
 - Configuration of devices.

This section contains the following subsections:

- [1.5.1 System component selection on page 1-21.](#)
- [1.5.2 Mesh sizing and top-level configuration on page 1-22.](#)
- [1.5.3 Device placement and configuration on page 1-26.](#)

1.5.1 System component selection

The selection of components comprising a CMN-600AE system.

Requesting masters (RNs)

Requesting masters reside outside of the mesh and connect to CMN-600AE ports.

Requesting masters with coherent caches (processors, GPUs, or processing elements with internal caches) are referred to as RN-F devices. They connect directly to the CMN-600AE interconnect mesh using a CHI RN-F port.

I/O requesting masters without coherent caches (I/O masters, processing elements without internal caches, or with internal caches that are not hardware coherent) connect to RN-I bridge devices that are located within CMN-600AE using ACE-Lite ports. The RN-I bridge device is located between the ACE-Lite interface and the internal CHI interface. Each RN-I bridge device has three ACE-Lite interfaces.

While an I/O requesting master can connect directly to a CMN-600AE ACE-Lite port, multiple masters may share a single ACE-Lite port using external AMBA interconnect components. Consider traffic bandwidth requirements and physical floorplan trade-offs to determine whether I/O masters share 1-3 ACE-Lite ports or an RN-I.

Home nodes (HNs)

In CHI, each byte of memory is assigned to a single home node which is responsible for handling all memory transactions that are associated with that byte.

There are two types of home node devices within the CMN-600AE system: HN-F and HN-I.

HN-F device instances are the home nodes for all coherent memory. HN-F also supports non-coherent memory accesses. Memory that is mapped to an HN-F targets DRAM. Each HN-F can contain an SF and an SLC slice. The amount of SLC should determine the number of HN-Fs.

The total amount of SLC needed divided by the number of HN-F instances determines the recommended SLC size for each HN-F instance. Generally, each HN-F partition has the same SLC size.

Note

The amount of SLC and number of HN-Fs are configured separately.

For best performance, the total SF size should be twice the total exclusive cache size for all RN-Fs. For example, for a 32MB RN-F total cache size, the recommended SF size would be 64MB.

HN-I device instances are the home nodes for all memory that is targeted at an ACE-Lite slave device or subsystem. HN-I does not support coherent memory. However, cacheable transactions can be sent to HN-I. Each HN-I instance contains a single ACE-Lite master port to send bus transactions to one or more slaves through an AMBA interconnect. The number of HN-I instances needed should be determined by the total ACE-Lite master bandwidth and slave peripherals' physical placement.

Note

HN-I instances with additional functionality are referred to by different names. For example, an HN-I that has a debug trace controller is called an HN-T. An HN-I that has a debug trace controller, DVM node and configuration slave is called an HN-D. The CMN-600AE interconnect can have zero or more HN-I and HN-T instances. However, it must have exactly one HN-D instance.

CML interfaces

The CMN-600AE interconnect supports up to two CXS (CCIX port) interfaces. A CXG device bridges between CHI and CXS, and contains CCIX *Request Agent* (RA) proxy and *Home Agent* (HA) proxy functionality. The CXG device also contains CXS *Link Agent* (LA) functionality, which is external to the CMN-600AE hierarchy.

Memory interfaces

The CMN-600AE interconnect supports two types of memory interface ports:

1. CHI SN port: Used to connect a native CHI.B for CMN-600AE memory controller such as the CoreLink DMC-620 Dynamic Memory Controller.
2. AXI port: Used to connect an AXI memory controller via an SBSX bridge. See [Table 1-5 Device types on page 1-23](#) for details.

1.5.2 Mesh sizing and top-level configuration

The size of the CMN-600AE mesh primarily depends on the number of connected devices.

The number of devices divided by two (rounded up) determines the minimum number of XPs. Also, the product of the X and Y mesh dimensions must be greater than or equal to the required number of XPs. For example, if seven XPs are required, a 2×4 or 4×2 mesh would be acceptable.

The device types that are supported by CMN-600AE are shown in the following table.

Table 1-5 Device types

Device	Name	Description
RN-I	Request Node I/O.	A non-caching Request Node, bridging I/O master requests from 1-3 AXI, or ACE-Lite interfaces.
RN-D	DVM Request Node.	An RN-I node that can accept DVM messages on the Snoop channel.
RNF_CHIB_ESAM	Request Node Full without a built-in SAM. CHI Issue B compliant.	CHI Issue B compliant processor, cluster, GPU, or other Request Node with a coherent cache but without a built-in SAM.
HN-F	Home Node Full.	A fully coherent Home Node, typically configured with SLC and/or SF.
HN-I	Home Node I/O.	A non-coherent Home Node, bridging I/O slave requests to an ACE-Lite interface.
HN-T	Home Node I/O with debug trace control.	An HN-I with a built-in debug trace controller.
HN-D	DVM Home Node.	An HN-I with a built-in debug trace controller, <i>DVM Node</i> (DN), <i>Configuration Node</i> (CFG), Global Configuration Slave, and the <i>Power/Clock Control Block</i> (PCCB).
SN-F	Slave Node.	A memory controller consisting of a native CHI SN interface.
SBSX	CHI to AXI bridge.	A CHI to AXI bridge that allows an AXI memory controller to be connected to CMN-600AE.
CXG	CHI to CXS (CCIX port) bridge.	<p>A CHI to CXS (CCIX port) bridge that enables CML.</p> <p style="text-align: center;">————— Note —————</p> <p>It comprises two entities: an internal CXRH device, including RA and HA functionality inside the CMN-600AE hierarchy, and an external CXLA device.</p> <p style="text-align: center;">—————</p>

The configurable options for mesh size, component counts, and top-level configuration (including associated parameters) are shown in the following tables.

Table 1-6 Top-level configurable options

Feature	Parameter	Description	Values (Default)	Comments
Mesh dimensions	Mesh X dimension	Number of mesh columns.	1-8	Mesh configurations that are not supported: <ul style="list-style-type: none"> • 1×1. • 1×2. • 2×1. <hr/> Note <hr/> CMN-600AE supports up to 16 XPs that enable a maximum mesh size of 4×4 or equivalent, such as 3×5 . <hr/>
	Mesh Y dimension	Number of mesh rows.	1-8	
	MCSX count	Number of credited slices on an XP-XP mesh link in X dimension.	0-4	This count is per link and can be different for each link.
	MCSY count	Number of credited slices on an XP-XP mesh link in Y dimension.	0-4	
	DCS count	Number of credited slices on a device-XP link.	0-4	

Table 1-6 Top-level configurable options (continued)

Feature	Parameter	Description	Values (Default)	Comments
Global parameter	PA_WIDTH	System physical address width.	34, 44, 48 (48)	-
	REQ_ADDR_WIDTH	Width of Address field in REQ flit.	44, 48 (48)	REQ_ADDR_WIDTH must be set equal to or greater than PA_WIDTH.
	REQ_RSVD_WIDTH	Width of RSVDC field in REQ flit.	0, 4, 8 (8)	-
	DATACHECK_EN	Datacheck enable.	0 (False)	Data check refers to data byte parity checking. ————— Note ————— In CMN-600AE, DATACHECK_EN is not configurable.
	FLIT_PAR_EN	Flit parity enable.	0 (False)	————— Note ————— In CMN-600AE, FLIT_PAR_EN is not configurable.
	NUM_REMOTE_RNF	Number of RN-Fs for CML configurations on all remote chips combined.	0-64 (0)	-
	RNSAM_NUM_ADD_HASHED_TGT	Number of extra hashed target IDs supported by the RN SAM, beyond the local HN-F count.	0, 2, 4, 8, 16, 32 (0)	-
	MPU_NUM_REG	Number of programmable MPU address regions.	0, 8, 16, 24, 32 (16)	-
Processor resources	Number of RN-Fs	The number of RN-Fs in the system.	1-8	-
I/O resources	Number of RN-Is	The number of RN-I instances in the system.	0-8	At least one RN-I or RN-D must be present. The total count of RN-Is and RN-Ds must not exceed eight.
	Number of RN-Ds	The number of RN-D instances in the system.	0-8	
	Number of HN-Is	The number of HN-I instances in the system. This count includes the HN-D which is always present.	1-4	-
Debug resources	Number of DTCs	The total number of Debug Trace Controller domains.	1-4	The number of DTCs must not exceed the number of HN-Is.

Table 1-6 Top-level configurable options (continued)

Feature	Parameter	Description	Values (Default)	Comments
System cache	Number of HN-Fs	The total number of HN-F instances in the system. The number of HN-Fs referred to by a given cache group (hashed entry in the SAM) must be a power of two.	1-8	For more details, refer to Chapter 5 SLC memory system on page 5-1847.
Memory resources	Number of SN-Fs	The number of SN-Fs (CHI interfaces).	0-4	At least one SN-F or SBSX must be present. The total count of SN-Fs and SBSXs must not exceed four.
	Number of SBSXs	The number of SBSX instances (AXI interfaces).	0-4	

1.5.3 Device placement and configuration

When the devices are enumerated and the mesh dimensions are determined, the placement of each device, or node, in the mesh must be specified.

While there are no constraints on the location of a device within the mesh, optimal device placement is driven by floorplanning and performance constraints, and is outside the scope of this document.

Individual CMN-600AE devices can be configured using the options that are shown in the following table.

Table 1-7 CHI device configurable options

Feature	Parameter	Description	Values (Default)	Comments
RN-F port, SN-F port	DEV_POISON_EN	Data poison enable (RN-F port only)	0, 1 (1)	-
	DEV_DATACHECK_EN	Datacheck enable (RN-F port only) ————— Note ————— DEV_DATACHECK_EN must be set to 0 when the global parameter DATACHECK_EN is 0. —————	0 (0)	DEV_DATACHECK_EN is not configurable in CMN-600AE.
	RXBUF_NUM_ENTRIES	Number of receive flit buffers inside CMN-600AE on this port. To achieve full bandwidth operation, this number must equal the CHI credit return latency (in cycles) for flit transfers from RN-F or SN-F to the interconnect. ————— Note ————— <ul style="list-style-type: none">The credit return latency is one cycle in the interconnect. This number must be added to the credit latency in the RN-F or SN-F to arrive at the total credit return latency.When MPU is enabled, an extra cycle of latency is present in the SNP flit path to RN-Fs. —————	2-4 (3)	The minimum value of 2 corresponds to a credit return latency of one cycle in the interconnect and one cycle in the RN-F or SN-F.
	CHI_SAFE_XFACE_DISABLE	Safe CHI interface disable	0, 1 (0)	When safe interface is disabled, the corresponding check signals are removed from the interface.
	A4S_SAFE_XFACE_DISABLE	Safe AXI4-Stream interface disable (RN-F port only)	0, 1 (0)	When safe interface is disabled, the corresponding check signals are removed from the interface.

Table 1-7 CHI device configurable options (continued)

Feature	Parameter	Description	Values (Default)	Comments
RN-I, RN-D	AXDATA_WIDTH	Data width on ACE-Lite/AXI interface	128, 256 (128)	-
	NUM_WR_REQ	Number of Write Request Tracker entries	4, 16, 24, 32, 64 (32)	-
	NUM_RD_REQ	Number of Read Request Tracker entries	4, 32, 64, 96, 128 (32)	-
	NUM_RD_BUF	Number of Read Data Buffers	4, 16, 24, 32, 64, 96, 128 (24)	-
	AXDATAPOISON_EN	Data poison enable on ACE-Lite/AXI interface	0, 1 (0)	-
	FORCE_RDB_PREALLOC	Force Read Data Buffer pre-allocation	0, 1 (0)	-
	ACEL_SAFE_XFACE_DISABLE	Safe ACE-Lite/AXI interface disable. Applicable to all three ports: S0, S1 and S2.	0, 1 (0)	When safe interface is disabled, the corresponding check signals are removed from the interface at all three ports: S0, S1 and S2.
HN-F	SLC_SIZE	Size of system cache	0KB, 128KB, 256KB, 512KB, 1MB, 2MB, 3MB, 4MB (2MB)	-
	SF_SIZE	Size of SF tag RAM	512KB, 1MB, 2MB, 4MB, 8MB (4MB)	-
	SLC_TAG_RAM_LATENCY	Latency of system cache tag RAM	1-3 cycles (2)	Valid Tag:Data RAM latency combinations: <ul style="list-style-type: none"> • 1:2 • 2:2 • 3:3
	SLC_DATA_RAM_LATENCY	Latency of system cache data RAM	2-3 cycles (2)	
	NUM_ENTRIES_POCQ	Number of entries in the POCQ tracker	32, 64 (32)	

Table 1-7 CHI device configurable options (continued)

Feature	Parameter	Description	Values (Default)	Comments
HN-I, HN-D	NUM_AXI_REQS	Number of Request Tracker entries	8, 32, 64 (32)	-
	AXDATA_WIDTH	Data width on ACE-Lite/AXI interface	128, 256 (128)	-
	AXDATAPOISON_EN	Data poison enable on ACE-Lite/AXI interface	0, 1 (1)	-
	DVM_V8_1_EN	Enable Armv8.1A DVMs (HN-D only)	0, 1 (1)	-
	DN_NUM_VMF_PARAM	Number of VMID filter registers	4, 16 (4)	-
	ACEL_SAFE_XFACE_DISABLE	Safe ACE-Lite/AXI interface disable	0,1 (0)	When safe interface is disabled, the corresponding check signals are removed from that interface.
	APB_SAFE_XFACE_DISABLE	Safe APB interface disable (HN-D only)	0,1 (0)	When safe interface is disabled, the corresponding check signals are removed from that interface.
SBSX	AXDATA_WIDTH	Data width on ACE-Lite/AXI interface	128, 256 (128)	-
	AXDATAPOISON_EN	Data poison enable on ACE-Lite/AXI interface	0, 1 (1)	-
	NUM_DART	Number of Tracker entries	64, 128 (64)	-
	NUM_WR_BUF	Number of write buffers	8, 16 (8)	-
	ACEL_SAFE_XFACE_DISABLE	Safe ACE-Lite/AXI interface disable	0,1 (0)	When safe interface is disabled, the corresponding check signals are removed from the interface.

Table 1-7 CHI device configurable options (continued)

Feature	Parameter	Description	Values (Default)	Comments
CXG	CXDB_LCRD_MAX_COUNT	Number of flit credits at CXLA interface	3-15 (4)	-
	SMP_MODE_EN	Enables Symmetric Multiprocessor Mode (SMP) Mode	0, 1 (0)	-
	RA_NUM_REQS	Depth of Request Tracker	64, 128, 256 (256)	-
	RA_NUM_RDBUF	Depth of Read Data Buffer	16, 24, 32 (16)	-
	RA_NUM_WRBUF	Depth of Write Data Buffer	16, 24, 32 (24)	-
	RA_NUM_SNPREQS	Depth of Snoop Tracker	64, 128, 256 (128)	-
	RA_NUM_SNPBUF	Depth of Snoop Data Buffer	16, 24, 32 (32)	-
	HA_NUM_REQS	Depth of request tracker	128, 192, 256 (192)	-
	HA_NUM_WRBUF	Depth of Write Data Buffer	96, 128 (96)	-
	HA_NUM_SNPREQS	Depth of Snoop Tracker. This indicates the number of outstanding snoop request HA can have on CCIX.	96, 128, 256 (96)	-
	HA_NUM_SNPBUF	Depth of Snoop Data Buffer	16, 24, 32 (24)	-
	HA_SSB_DEPTH	This depth indicates the maximum number of remote snoop requests from the local chip that can be sunk at this HA.	96, 128, 256 (96)	This value must be at least as large as HA_NUM_SNPREQS.
	DB_FIFO_DEPTH	FIFO Depth in CXLA Domain Bridges - CXDB, PDB	6, 8 (8)	-

MCS

The CMN-600AE mesh is designed to operate with a single cycle of latency between XPs. However, depending on the fabrication process and the distance between XPs, a single-cycle XP-XP connection may limit frequency. In this case, one or more register slices can be added to lengthen the XP-XP links. Register slices add link transfer latency, but the frequency gained can justify the trade-off.

To add an extra cycle between two XPs, a *Mesh Credited Slice* (MCS) is specified. One to four MCSs can be added to any link between XPs.

An MCS placed between adjacent XPs in the same row is called an MCSX. Similarly, one placed between adjacent XPs in the same column is called an MCSY.

DCS

A credited slice that is placed between a device and an XP is called a *Device Credited Slice* (DCS). One to four DCSs can be added to any link between a device and an XP.

The following figure shows an example configuration including an MCSX, MCSY, and DCS.

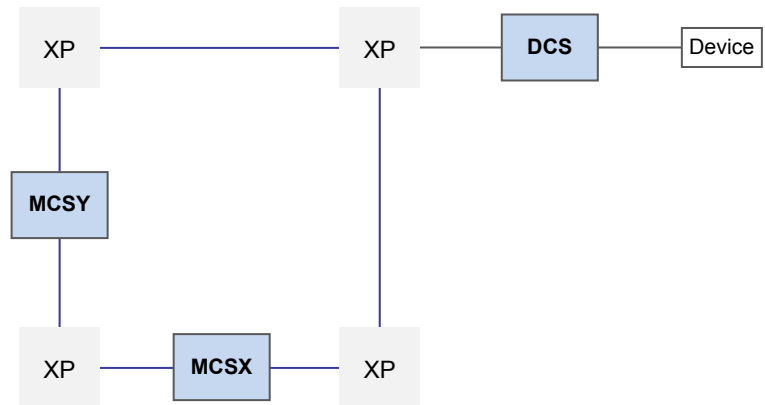


Figure 1-2 Example MCSX, MCSY, and DCS configuration

1.6 Test features

The CMN-600AE product includes several test features.

For information about the test features, see the *Arm® CoreLink™ CMN-600AE Coherent Mesh Network Configuration and Integration Manual*.

1.7 Product documentation and design flow

CMN-600AE product manuals support an effective design flow process.

Documentation

The CMN-600AE product is supported by the following documentation:

Technical Reference Manual

The *Technical Reference Manual* (TRM) describes the functionality and the effects of functional options on the behavior of CMN-600AE. It is required at all stages of the design flow. The choices that you make in the design flow can mean that some behavior that is described in the TRM is not relevant. If you are programming the CMN-600AE product, contact:

- The implementer to determine:
 - The build configuration of the implementation.
 - What integration, if any, was performed before implementing the CMN-600AE product.
- The integrator to determine the pin configuration of the device that you are using.

Configuration and Integration Manual

The *Configuration and Integration Manual* (CIM) describes how to integrate the CMN-600AE product into an SoC. It includes a description of the pins that the integrator must tie off to configure the macrocell for the required integration. Some of the configuration options that are used when implementing the CMN-600AE product include:

- The available build configuration options and related issues in selecting them.
- How to configure the *Register Transfer Level* (RTL) with the build configuration options.
- How to integrate RAM arrays.
- How to run test patterns.
- The processes to sign off the configured design.

The Arm product deliverables include reference scripts and information about using them to implement your design. Reference methodology flows supplied by Arm are example reference implementations. Contact your EDA vendor for EDA tool support.

Safety Manual

The Safety Manual provides additional information on specific features of the CMN-600AE that are relevant to Functional Safety. This information is important for SoC integrators whose final designs target applications where Functional Safety is a concern.

Development Interface Report

The *Development Interface Report* (DIR) describes the activities conducted by Arm that are related to the safety architecture of the CMN-600AE.

Design flow

CMN-600AE is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following processes:

Implementation

The implementer configures and synthesizes the RTL to produce a hard macrocell. This process includes integrating RAMs into the design.

Integration

The integrator connects the implemented design into an SoC. This process includes connecting a memory system and peripherals.

Programming

Programming is the last process. The system programmer develops the software that is required to configure and initialize the CMN-600AE product, and tests the required application software.

Each process can:

- Be performed by a different party.
- Include implementation and integration choices that affect the behavior and features of the CMN-600AE product.

The operation of the final device depends on the following factors:

Build configuration

The implementer chooses the options that affect how the RTL source files are pre-processed. These options usually include or exclude logic that affects one or more of the area, maximum frequency, and features of the resulting macrocell.

Configuration inputs

The integrator configures some features of the CMN-600AE product by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

Software configuration

The programmer configures the CMN-600AE product by programming particular values into registers. The configuration affects the behavior of the CMN-600AE product.

Note

This manual refers to IMPLEMENTATION DEFINED features that are applicable to build configuration options. A reference to a feature that is included means that the appropriate build and pin configuration options are selected. A reference to an enabled feature means one that has also been configured by software.

1.8 Product revisions

There are differences in functionality between successive product revisions of the CMN-600AE product.

r0p0

First release.

r0p0-r1p0

Functional changes are:

- Bug fixes.

Chapter 2

Functional description

This chapter describes the functionality of the CMN-600AE product.

It contains the following sections:

- [2.1 Components](#) on page 2-38.
- [2.2 System configurations](#) on page 2-45.
- [2.3 CML system configurations](#) on page 2-48.
- [2.4 Node ID mapping](#) on page 2-51.
- [2.5 Discovery](#) on page 2-53.
- [2.6 Addressing capabilities](#) on page 2-64.
- [2.7 Atomics](#) on page 2-65.
- [2.8 Exclusive accesses](#) on page 2-66.
- [2.9 Processor events](#) on page 2-67.
- [2.10 Quality of Service](#) on page 2-68.
- [2.11 Barriers](#) on page 2-76.
- [2.12 DVM messages](#) on page 2-77.
- [2.13 PCIe integration](#) on page 2-78.
- [2.14 Reliability, Availability, and Serviceability](#) on page 2-80.
- [2.15 CCIX Port Aggregation Groups](#) on page 2-96.
- [2.16 System Address Map](#) on page 2-97.
- [2.17 RN SAM](#) on page 2-98.
- [2.18 CXRA SAM](#) on page 2-104.
- [2.19 HN-F SAM](#) on page 2-105.
- [2.20 RN and HN-F SAM additional features and programming](#) on page 2-110.
- [2.21 HN-I SAM](#) on page 2-119.
- [2.22 Cross chip routing and ID mapping](#) on page 2-127.
- [2.23 GIC communication over AXI4-Stream ports](#) on page 2-133.

- [2.24 Clocking](#) on page 2-134.
- [2.25 Reset](#) on page 2-139.
- [2.26 Power and clock management](#) on page 2-140.
- [2.27 RN entry to and exit from Snoop and DVM domains](#) on page 2-151.
- [2.28 Link layer](#) on page 2-154.
- [2.29 CML Symmetric Multiprocessor support](#) on page 2-156.

2.1 Components

CMN-600AE is made up of various types of devices, including router modules, CHI nodes, and bridges. The components that you require depend on the requirements of your system and some are optional or only used if certain requirements are met.

CMN-600AE can be integrated into a complete SoC system that includes devices that this section does not describe.

This section contains the following subsections:

- [2.1.1 Crosspoint \(XP\) on page 2-38.](#)
- [2.1.2 I/O coherent Request Node \(RN-I\) on page 2-40.](#)
- [2.1.3 Fully coherent Home Node \(HN-F\) on page 2-40.](#)
- [2.1.4 I/O coherent Home Node \(HN-I\) on page 2-41.](#)
- [2.1.5 AMBA 5 CHI to ACE5-Lite bridge \(SBSX\) on page 2-41.](#)
- [2.1.6 CCIX Gateway \(CXG\) on page 2-41.](#)
- [2.1.7 Configuration node \(CFG\) on page 2-41.](#)
- [2.1.8 Power/Clock Control Block \(PCCB\) on page 2-42.](#)
- [2.1.9 System Address Map \(SAM\) on page 2-42.](#)
- [2.1.10 Debug and Trace Controller \(DTC\) on page 2-42.](#)
- [2.1.11 QoS regulator \(QR\) on page 2-42.](#)
- [2.1.12 Credited Slices \(CSs\) on page 2-43.](#)
- [2.1.13 Mesh Credited Slice \(MCS\) on page 2-43.](#)
- [2.1.14 Device Credited Slice \(DCS\) on page 2-44.](#)
- [2.1.15 CHI Domain Bridge on page 2-44.](#)
- [2.1.16 AMBA® Domain Bridge on page 2-44.](#)

2.1.1 Crosspoint (XP)

The *crosspoint* (XP) is a switch or router logic module. It is the fundamental building block of the CMN-600AE transport mechanism.

Note

The terms XP and MXP are used interchangeably throughout this TRM.

The CMN-600AE mesh interconnect is built using a set of XP modules. Each XP can have six ports: four mesh ports and two device ports. The following figure shows these ports.

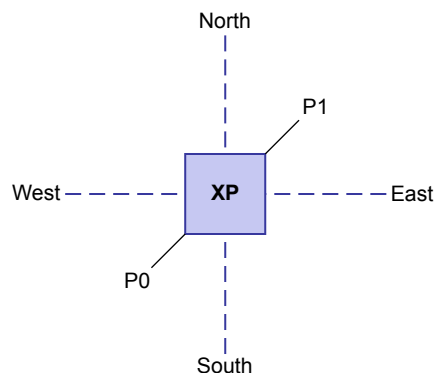


Figure 2-1 Crosspoint

The dashed lines in the preceding figure represent mesh ports. Each XP can connect to up to four neighboring XPs through mesh ports. Each XP also has two device ports, P0 and P1, for connecting devices.

Each XP supports four CHI channels for transporting flits across the mesh from a source device to a destination or target device:

- *Request* (REQ)
- *Response* (RSP)
- *Snoop* (SNP)
- *Data* (DAT)

The XP modules are arranged in a two-dimensional rectangular mesh topology.

The maximum size for the CMN-600AE mesh is 16 XPs arranged in a 4×4 or equivalent rectangular grid. Each XP in the grid is referenced using an (X,Y) coordinate system with (0,0) representing the bottom-left corner. The following figure shows a 4×4 mesh configuration with some (X,Y) coordinate values.

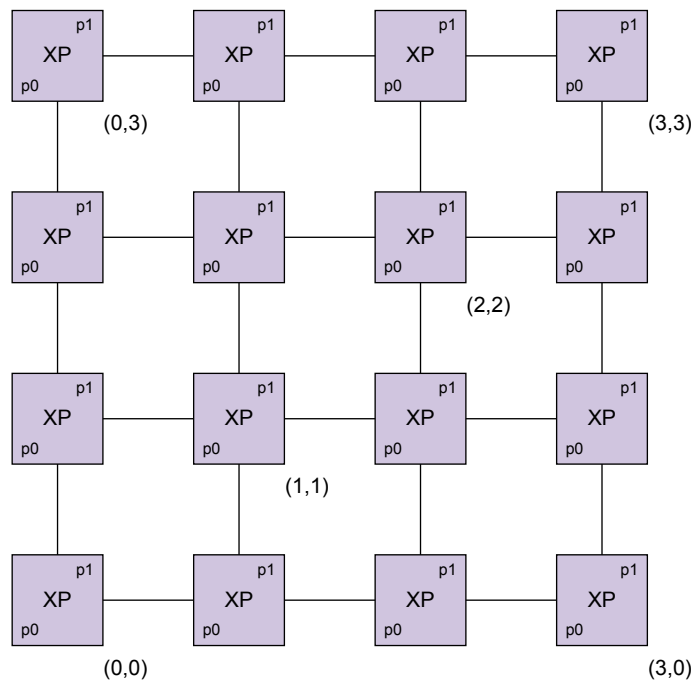


Figure 2-2 4×4 maximum mesh configuration

The following figure shows an example 4×4 mesh configuration, with devices attached to XP ports.

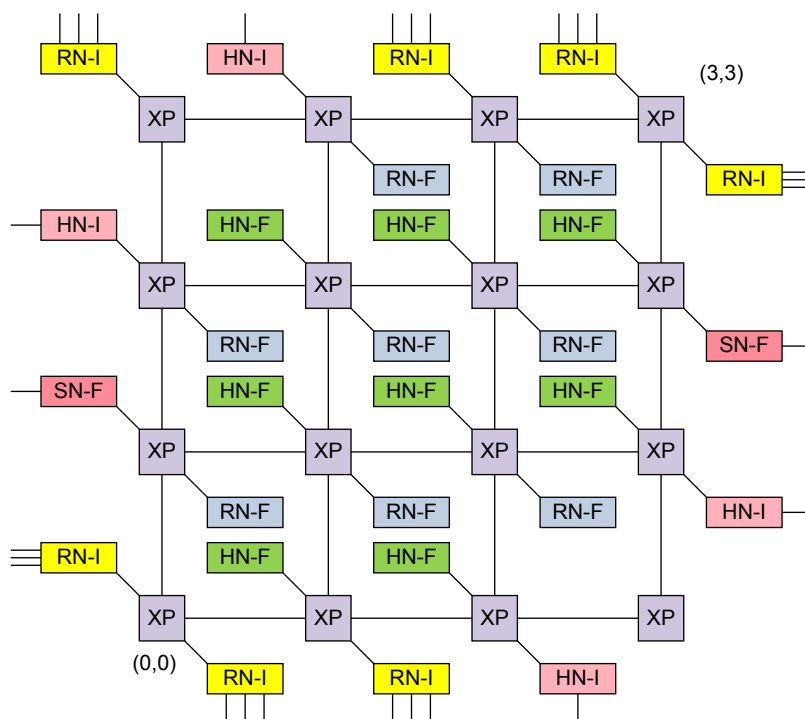


Figure 2-3 Example 4×4 mesh configuration

Note

The x and y coordinates of an XP are also known as the XID and YID respectively.

2.1.2 I/O coherent Request Node (RN-I)

The *I/O-coherent Request Node* (RN-I) connects I/O-coherent AMBA masters to the rest of the CMN-600AE system.

An RN-I bridge includes three ACE-Lite or ACE-Lite-with-DVM slave ports.

The RN-I bridge can act as a proxy only for masters that do not contain hardware-coherent caches. There is no capability to issue snoop transactions to RN-Is.

2.1.3 Fully coherent Home Node (HN-F)

The *Fully coherent Home Node* (HN-F) is responsible for managing part of the address space.

The HN-F consists of the following:

System Level Cache (SLC)

The *System Level Cache* (SLC) is a last-level cache. The SLC allocation policy is exclusive for data lines, except where sharing patterns are detected and pseudo-inclusive for code lines, as indicated by the RN-Fs. All code lines can be allocated into the SLC on the initial request.

Combined Point-of-Serialization (PoS) and Point-of-Coherency (PoC)

The combined *Point-of-Serialization* (PoS) and *Point-of-Coherency* (PoC) is responsible for the ordering of all memory requests sent to the HN-F. Ordering includes serialization of multiple outstanding requests and actions to the same cache line, and request ordering as required by the RN-F.

Snoop Filter (SF)

The *Snoop Filter* (SF) tracks cache lines that are present in the RN-Fs. Using the SF reduces snoop traffic in the system by favoring directed snoops over snoop broadcasts when possible. This approach substantially reduces the snoop response traffic that might otherwise be required.

Each HN-F in the system is configured to manage a specific portion of the overall address space.

The entire DRAM space is managed through the combination of all HN-Fs in the system.

Note

The HN-F is architecturally defined to manage only well-behaved memory, which is memory without any possible side effects. The HN-F includes microarchitectural optimizations to exploit this architectural guarantee.

2.1.4 I/O coherent Home Node (HN-I)

The *I/O coherent Home Node* (HN-I) is an HN for all CHI transactions targeting AMBA slave devices.

The HN-I acts as a proxy for all the RNs of CMN-600AE, converting CHI transactions to ACE5-Lite transactions. The HN-I includes support for the correct ordering of Arm device types.

The HN-I does not support caching of any data read from or written to the downstream ACE5-Lite I/O slave subsystem. Any cacheable request that is sent to the HN-I does not result in any snoops being sent to RN-Fs in the system. Instead, the request is converted to the appropriate ACE5-Lite read or write command and sent to the downstream ACE5-Lite subsystem.

Caution

If an RN-F caches data that is read from or written to the downstream ACE5-Lite I/O slave subsystem, coherency is not maintained. Any subsequent access to that data reads from or writes to the ACE5-Lite I/O slave subsystem directly, ignoring the cached data.

2.1.5 AMBA 5 CHI to ACE5-Lite bridge (SBSX)

The *AMBA 5 CHI to ACE5-Lite bridge* (SBSX) enables an ACE5-Lite slave device such as a CoreLink DMC-400 Dynamic Memory Controller, to be used in a CMN-600AE system.

2.1.6 CCIX Gateway (CXG)

A CXG device bridges between CHI and CXS.

A CXG device contains the following components:

- *CCIX Request Agent* (CXRA) proxy and *CCIX Home Agent* (CXHA) proxy functionality.
- *CXS Link Agent* (CXLA) functionality which is external to the CMN-600AE hierarchy.

2.1.7 Configuration node (CFG)

The *configuration node* (CFG) is co-located with the HN-D node and handles various CMN-600AE configuration, control, and monitoring features.

The CFG carries out the following functions:

- Configuration accesses
- Error reporting and signaling
- Interrupt generation
- Centralized debug and PMU support

The CFG includes the following elements:

- Ports to collect error signals from CHI components within CMN-600AE
- A configuration bus which connects to all the nodes to handle internal configuration register reads and writes

The CFG does not have a dedicated CHI port. It shares a device port with the HN-D node in the mesh.

2.1.8 Power/Clock Control Block (PCCB)

The *Power/Clock Control Block* (PCCB), co-located with the HN-D node, provides separate communication channels. These channels pass information about the power and clock management between the SoC and the network.

The PCCB acts as an aggregator to convey information between the SoC and the other CMN-600AE components, in the following way:

1. The PCCB receives transaction activity indicators from other relevant CMN-600AE components and conveys that information to the external power and clock control units.
2. The PCCB receives power or clock control management requests from the external power or clock control units. Where applicable, it conveys that request to the relevant CMN-600AE components.
3. The PCCB waits for the appropriate responses from the relevant CMN-600AE components, and conveys an aggregated response to the external power and clock control units.

The PCCB does not have a dedicated CHI port. It shares a device port with the HN-D node in the mesh.

2.1.9 System Address Map (SAM)

All CHI commands must include a fully resolved network address. The address must include a source and target ID. Target IDs are acquired by passing a request address through a *System Address Map* (SAM). The SAM effectively maps a memory or I/O address to the target device.

The SAM functionality is required for each requesting device. The SAM consists of two logical units:

RN SAM Allows each RN to map addresses to HN-F, HN-I, HN-D, and HN-T target IDs. The RN SAM supports generation of *Memory Controller* (MC) target IDs, which can be used to issue PrefetchTgt operations from the RN directly to the MC.

HN-F SAM Maps addresses to MC target IDs.

CMN-600AE has software-configurable SAM blocks which allow a single implementation of CMN-600AE to support programmable mappings of addresses to HNs and SNs.

The SAM functionality is required for each requesting device.

2.1.10 Debug and Trace Controller (DTC)

The *Debug and Trace Controller* (DTC) controls distributed *Debug and Trace Monitors* (DTMs) and generates time stamped trace using the ATB interface. DTCs are present in HN-D and HN-T nodes.

The DTC performs the following functions:

- Generates event or PMU-based interrupts
- Receives packets from DTM and packs them into ATB format trace
- Time stamps trace with SoC timer input
- Generates alignment sync for the ATB trace output
- Handles ATB flush requests
- Handles debug and Secure debug external requests
- Provides a consistent view of distributed and central PMU counters
- Handles PMU snapshot requests
- Generates interrupt **INTREQPMU** assertion on overflow of PMU counters

— Important —

Debug and Trace functionality must be disabled during mission critical operation.

2.1.11 QoS regulator (QR)

CMN-600AE supports end-to-end *Quality-of-Service* (QoS) which guarantees using QoS mechanisms that are distributed throughout the system.

The QoS provision uses the QoS field in each RN request to influence arbitration priority at every QoS decision point. The QoS field is then propagated through all subsequent packets that are generated by the transaction. RNs must either:

- Self-modulate their QoS priority depending on how well their respective QoS requirements are met.
- Use the integrated QoS regulators at ingress points to CMN-600AE.

It is possible to include non-QoS-aware devices in the system, but still have these devices meet the QoS modulation requirement of the QoS architecture. To meet this requirement, CMN-600AE includes inline regulators that perform the QoS functionality without the requesting device requiring any awareness of QoS. A *QoS Regulator* (QR) provides an interstitial layer between an RN and the interconnect. The QR monitors how the bandwidth and latency requirements of the RN are met, and does in-line replacement of the RN-provided QoS field. The QR adjusts the QoS field upwards for higher priority in the system and downwards for lower priority.

QoS regulators are present at each RN-I ACE-Lite interface and at each XP device port that is connected to an RN-F.

2.1.12 Credited Slices (CSs)

You can configure various optional credited register slices in your CMN-600AE system. These *Credited Slices* (CSs) can help with timing closure.

CSs enable synchronous but higher latency communication at any point in the system.

CMN-600AE includes the following optional CSs:

Mesh Credited Slice

Placed between XPs. For more information, see [2.1.13 Mesh Credited Slice \(MCS\)](#) on page 2-43.

Device Credited Slice

Placed between a device and a CAL, or a device and an XP. For more information, see [2.1.14 Device Credited Slice \(DCS\)](#) on page 2-44.

The slices are simple repeater-flop structures that are applied across the entire communication boundary. The supported number of CSs of each type is specified in .

The following figure shows where various CSs fit in the structure of the mesh. The example mesh includes two MCSs, which are denoted as MCSX and MCSY according to the X or Y direction of the link, and a DCS.

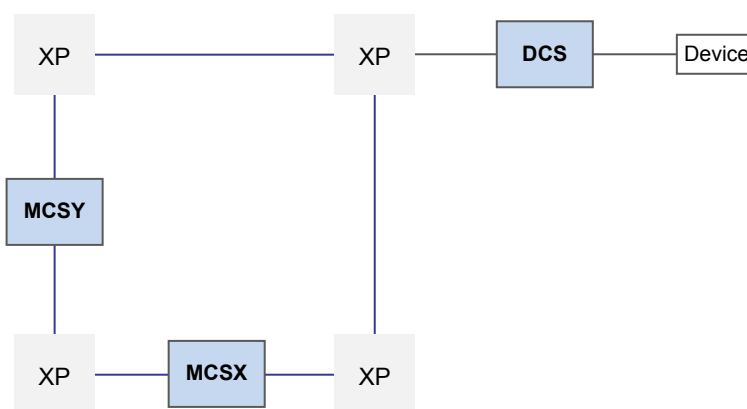


Figure 2-4 Example MCSX, MCSY, and DCS configuration

2.1.13 Mesh Credited Slice (MCS)

You can configure one or more *Mesh Credited Slices* (MCSs) between CMN-600AE XPs. MCSs are optional register slices that can help timing closure in a CMN-600AE system.

The CMN-600AE mesh can operate with a single cycle of latency between XPs. However, depending on the fabrication process and the distance between XPs, a single-cycle XP-XP connection might limit frequency. In this case, one or more MCSs can be added to lengthen the XP-XP links. Register slices add link transfer latency, but also allow certain CMN-600AE implementations to run at higher frequencies.

Each MCS on an XP-XP link adds an extra cycle for transfer between XPs. One to four MCSs can be added to any link between XPs.

An MCS that is placed between adjacent XPs in the same row is called an MCSX. Similarly, an MCS that is placed between adjacent XPs in the same column is called an MCSY.

2.1.14 Device Credited Slice (DCS)

You can configure one or more *Device Credited Slices* (DCSs) on a link between a device and an XP. DCSs help with timing closure in a CMN-600AE system.

DCSs are optional register slices that you can add to your CMN-600AE configuration. You can add up to four DCSs on any link between a device and an XP.

2.1.15 CHI Domain Bridge

The *CHI Domain Bridge* (CDB) bridges two CHI interfaces that operate in two different clock domains, power/voltage domains, or both.

For more information about the CDB, see the *Arm® CoreLink™ CMN-600AE Coherent Mesh Network Configuration and Integration Manual*, which is only available to licensees.

2.1.16 AMBA® Domain Bridge

The *AMBA Domain Bridge* (ADB) bridges two AXI, ACE5-Lite, or ACE5-Lite-with-DVM interfaces that operate in two different clock domains, power/voltage domains, or both.

For more information about the ADB, see the *Arm® CoreLink™ CMN-600AE Coherent Mesh Network Configuration and Integration Manual*, which is only available to licensees.

2.2 System configurations

You can configure CMN-600AE to meet system requirements.

The following figure shows a 1×3 mesh for a small system configuration that contains single instances of RN-F, HN-F, RN-D, SN-F, and HN-D.

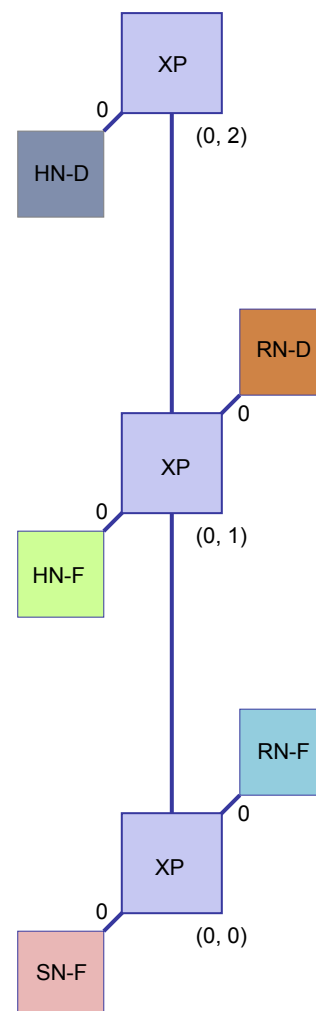


Figure 2-5 Mesh example 1×3

The following figure shows a 4×2 mesh for a medium system configuration with single and multiple instances of RN-F, HN-F, RN-D, SN-F, and HN-D.

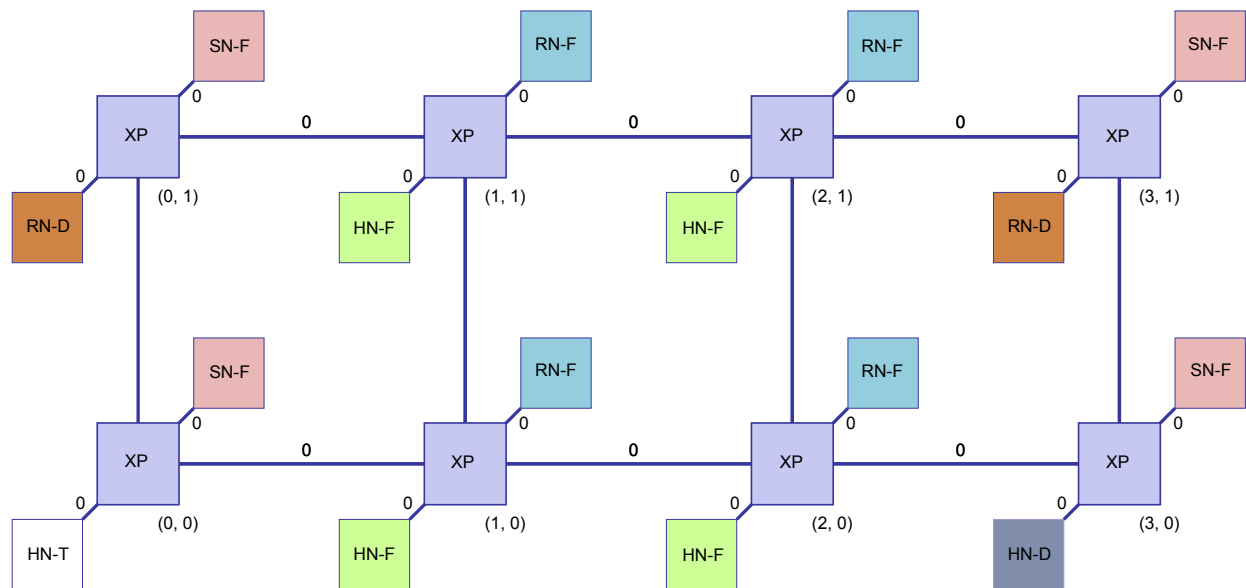


Figure 2-6 Mesh example 4×2

The following figure shows a 3×5 mesh for a large system configuration with multiple instances of RN-F, HN-F, RN-D, HN-I, SN-F, and HN-D.

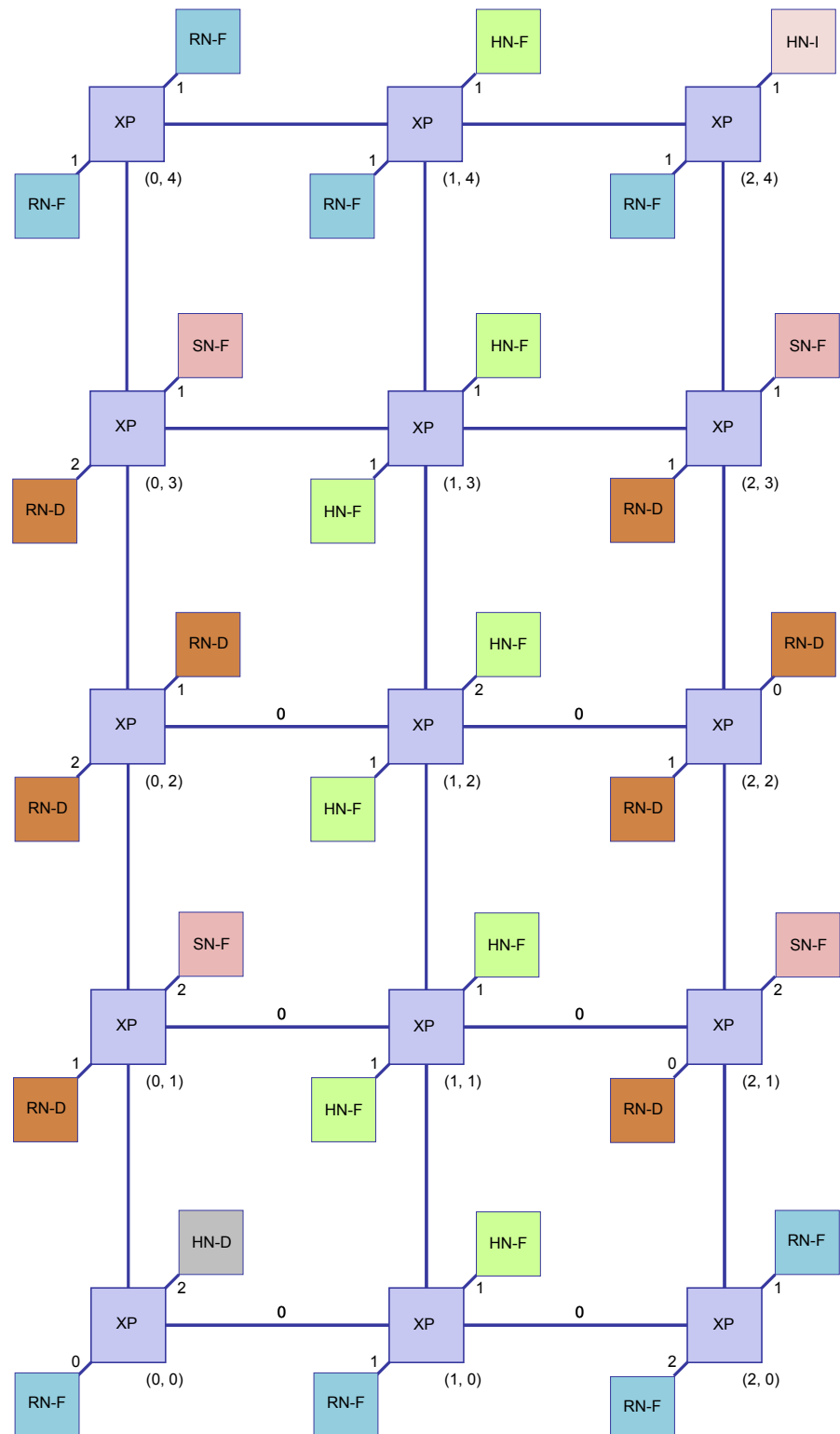


Figure 2-7 Mesh example 3 × 5

2.3 CML system configurations

This section provides CML system configuration examples.

Single CML configuration

The following figure shows a 4×2 mesh with a single CXG instance.

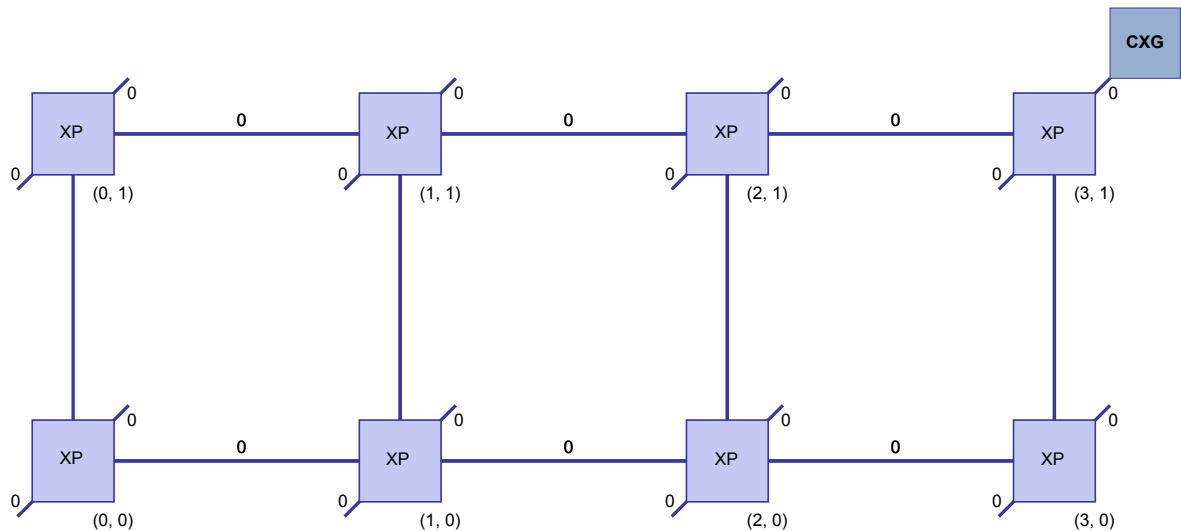


Figure 2-8 4×2 single CML mesh example

Double CML configuration

The following figure shows a 4×2 mesh with two CXG instances.

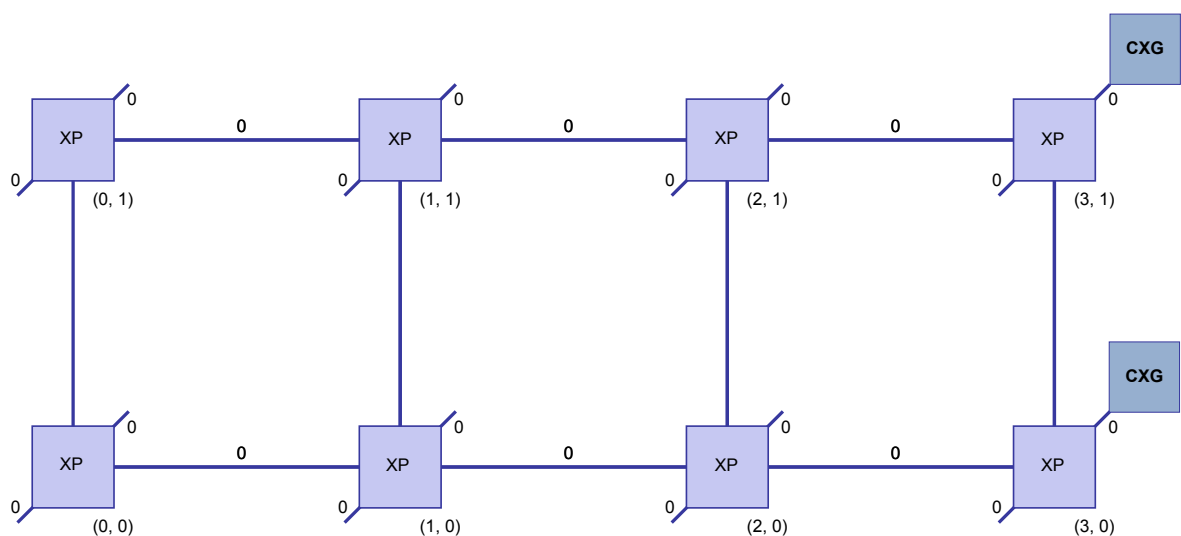


Figure 2-9 4×2 double CML mesh example

CXG components

A CXG device bridges between CHI and CXS. It contains CCIX *Request Agent* (RA) proxy and *Home Agent* (HA) proxy functionality. The CXG device also contains CXS *Link Agent* (LA) functionality, which is external to the CMN-600AE hierarchy. The following figure shows a simple CXG block diagram.

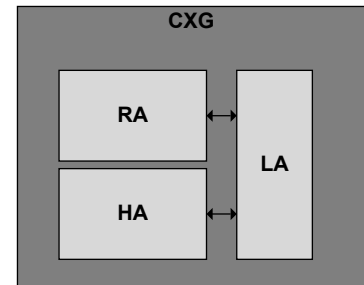


Figure 2-10 CXG block diagram with RA, HA, and LA

CCIX topologies

The following figure shows three simplified CCIX topology examples.

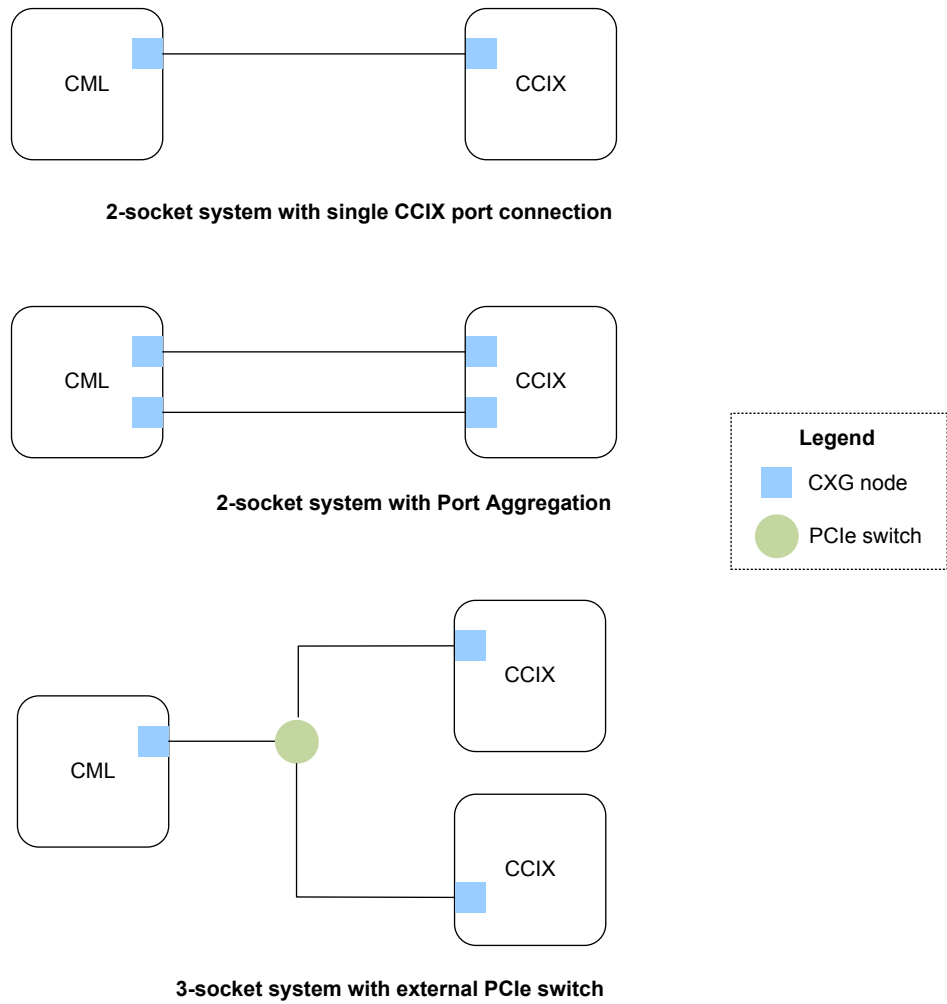


Figure 2-11 CCIX topologies

2.4 Node ID mapping

The physical position of a device in the mesh determines the node ID that the device is mapped to.

The following details determine the physical position of a device in the mesh:

1. The X coordinate of its XP
2. The Y coordinate of its XP
3. The XP device port (0 or 1) that it connects to

Therefore, the device node ID is mapped to (X, Y, Port, Device ID).

Note

1. The size of the node ID field depends on the configured size of the mesh. Larger meshes have larger bit widths for the X and Y parameters.
 2. The naming convention for I/O signals uses decimal values of the node ID. For example, RXREQFLIT_NIDxxx uses xxx values in decimal.
-

The node ID size depends on the X and Y dimensions of the CMN-600AE mesh. The larger of the X and Y dimensions determines the size of the node ID. The following table shows the relationship between mesh X and Y dimensions and the node ID size.

Table 2-1 Node ID size selection

X mesh dimension	Y mesh dimension	Node ID size
4 or less	4 or less	7 bits
5-8	8 or less	9 bits
8 or less	5-8	

Note

On internal CHI interfaces, the NodeID width is set equal to the NodeID size. On external CHI interfaces, the NodeID width is set to 11 bits, where unused bits occupy MSBs and are driven to zeroes.

The following tables contain the different node ID formats, depending on whether the node ID is 7 bits or 9 bits wide.

Table 2-2 7-bit node ID format

[6:5]	[4:3]	[2]	[1:0]
X position	Y position	Port	Device ID

Table 2-3 9-bit node ID format

[8:6]	[5:3]	[2]	[1:0]
X position	Y position	Port	Device ID

The following figure shows a CMN-600AE system with 7-bit node IDs in decimal format.

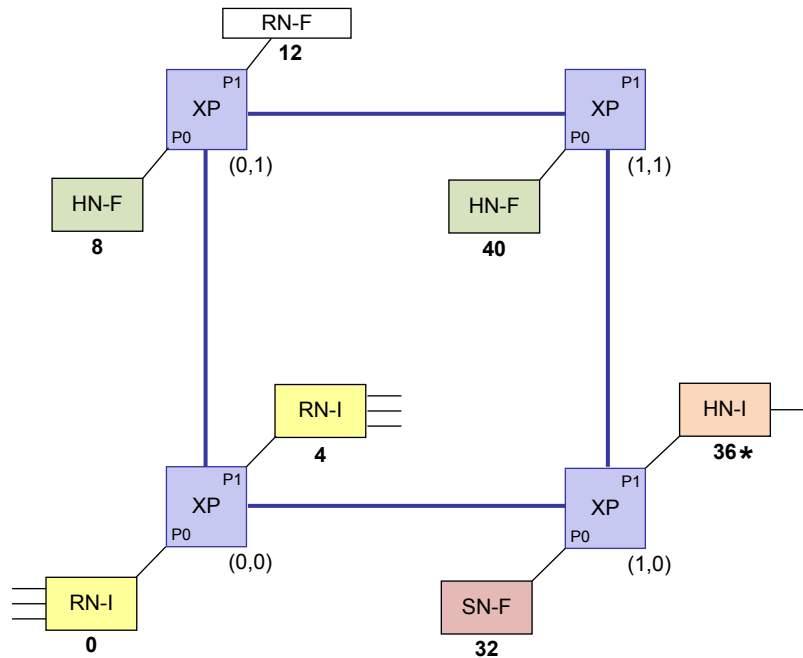


Figure 2-12 Example system with 7-bit node IDs

Example 2-1 7-bit node ID format

For the HN-I connected to XP (1,0), the node ID reads as 36.

The equivalent binary value is `0b0100100`. In other words, the X position value = `0b01`, the Y position value = `0b00`, the device port value = `0b1`, and the device ID value = `0b00`.

2.5 Discovery

Discovery is a software algorithm that is used to discover the configuration of CMN-600AE.

Software uses the discovery mechanism to identify the following properties:

- The CHI node ID and LDID corresponding to all node types

Note

The valid logical node types are DVM, Global CFG, DTC, HN-F, HN-I, RN-D, RN SAM, RN-I, SBSX, and XP. There are other node types for additional functionality:

CML

CXRA, CXHA, and CXLA.

Functional safety

FMU and FDC.

- Whether a discovered node is internal or external to CMN-600AE

The following figure shows an example configuration. In the example, after discovery, software should have enough information to know the location of the following components:

- Global configuration registers
- Configuration registers for each XP
- Configuration registers for the HN-F
- Configuration registers for the RN SAM corresponding to the RN-F

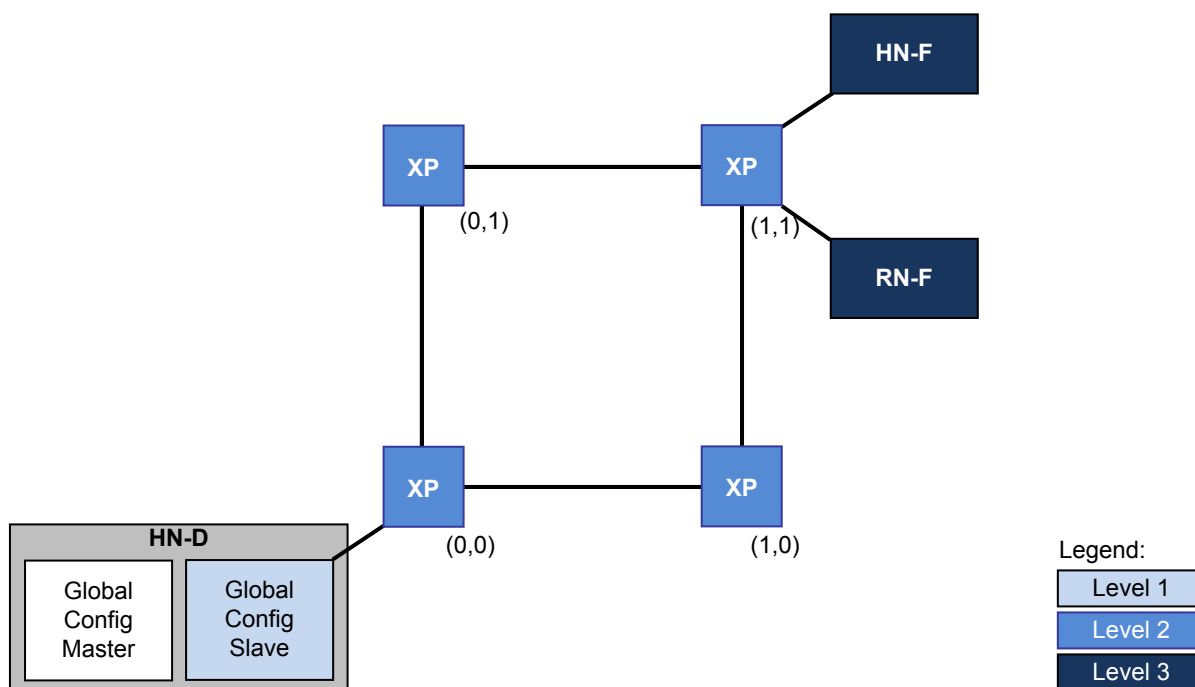


Figure 2-13 2 × 2 register tree example

This section contains the following subsections:

- [2.5.1 Configuration address space organization on page 2-53.](#)
- [2.5.2 Configuration register node structure on page 2-55.](#)
- [2.5.3 Child pointers on page 2-58.](#)
- [2.5.4 Discovery tree structure on page 2-62.](#)

2.5.1 Configuration address space organization

This section contains configuration address space organization information. It describes two system addresses, PERIPHBASE and ROOTNODEBASE, that are required for this process.

PERIPHBASE

The starting address of the range that all CMN-600AE configuration registers are mapped to. For a system where both the X and Y dimensions are eight or less:

- This address should be aligned to 64MB
- The maximum size of the address range is 64MB

ROOTNODEBASE

The address to the Root Node where the discovery process can start. The configuration registers at ROOTNODEBASE contain global and configuration information, and the first level of discovery information for the system components.

Discovery determines specific addresses for individual system blocks that have IMPLEMENTATION DEFINED register spaces, as the following figure shows.

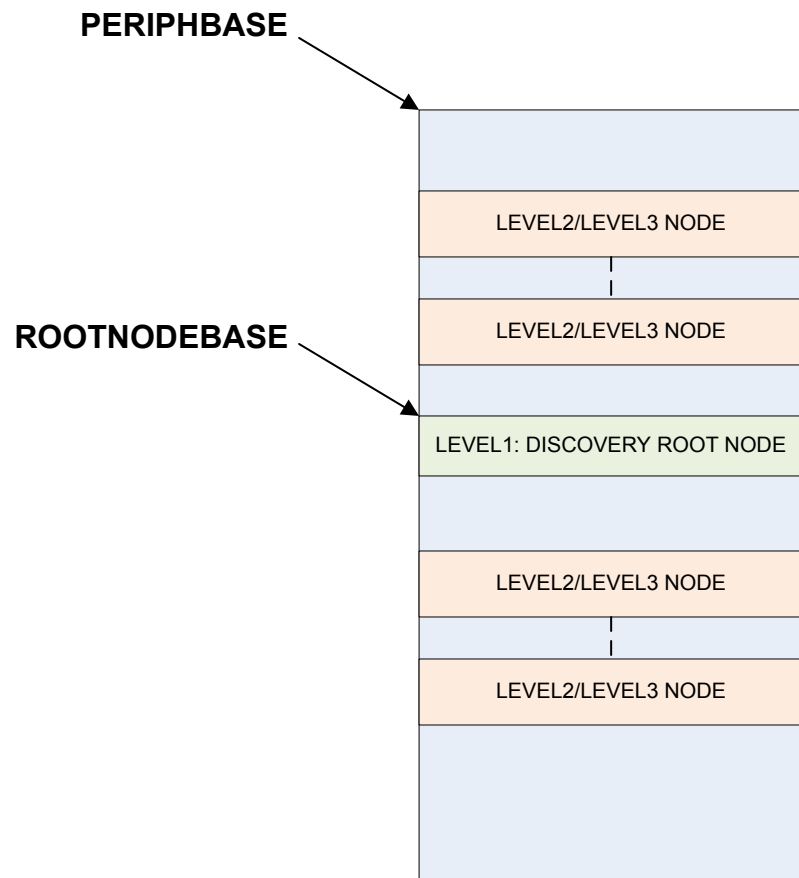


Figure 2-14 PERIPHBASE and ROOTNODEBASE addresses

CMN-600AE supports 4B and 8B software-accessible registers. Register organization consists of software using 32b and 64b register reads.

All registers are organized into several register blocks as nodes. A node:

- Is a register block with the size of 16KB
- Is associated with a logical block in the design
- Has implementation-specific information and configuration for that block

The different types of nodes are:

General Contains device information and has children.

Leaf Contains device information, such as configuration data, but has no children.
Pure hierarchy Has children but contains no device information.

If a node has more than one child, the node provides:

- The number of children
- A pointer to each child

The following figure shows an example for the ROOTNODEBASE structure.

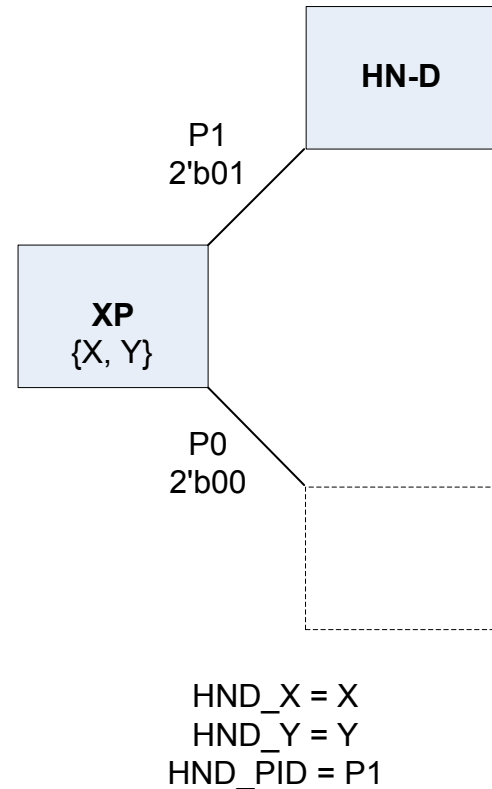


Figure 2-15 ROOTNODEBASE pointer example

The following values define the ROOTNODEBASE structure:

- PERIPHBASE
- Root Node Pointer. If one of the mesh dimensions is greater than four, the node ID is 14 bits. Otherwise, the node ID is 12 bits.
- Register offset. In this example, the register offset is $14'b0$

2.5.2 Configuration register node structure

Read-only registers that are organized into several register blocks are referred to as nodes.

Nodes are aligned on 8B boundaries (16KB aligned). The required registers are:

Node Information register	Identifies the product or node type, and the CHI node ID.
Child Information register	Indicates the child count and offset for the first register containing child node pointers. These optional Child Pointer registers each use 8B.

———— **Important** ————

The Node Information and Child Information registers are at fixed offsets for all nodes.

The following figure shows the basic node structure.

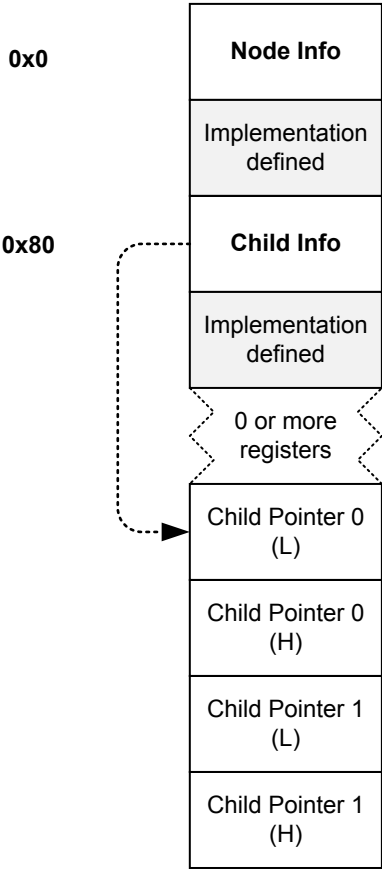


Figure 2-16 Basic node structure

The `child_count` field of the Child Information register indicates the number of children. This value also represents the number of functional units that are connected to the current unit on the next level of the discovery process.

The `child_ptr_offset` field of the Child Information register indicates the Child Pointer 0 register offset, in bytes, from the Node Information register address.

———— **Important** ————

For a leaf node (node with no children), the `child_count` and `child_ptr_offset` fields must be set to zero.

The following figure provides the node structure detail.

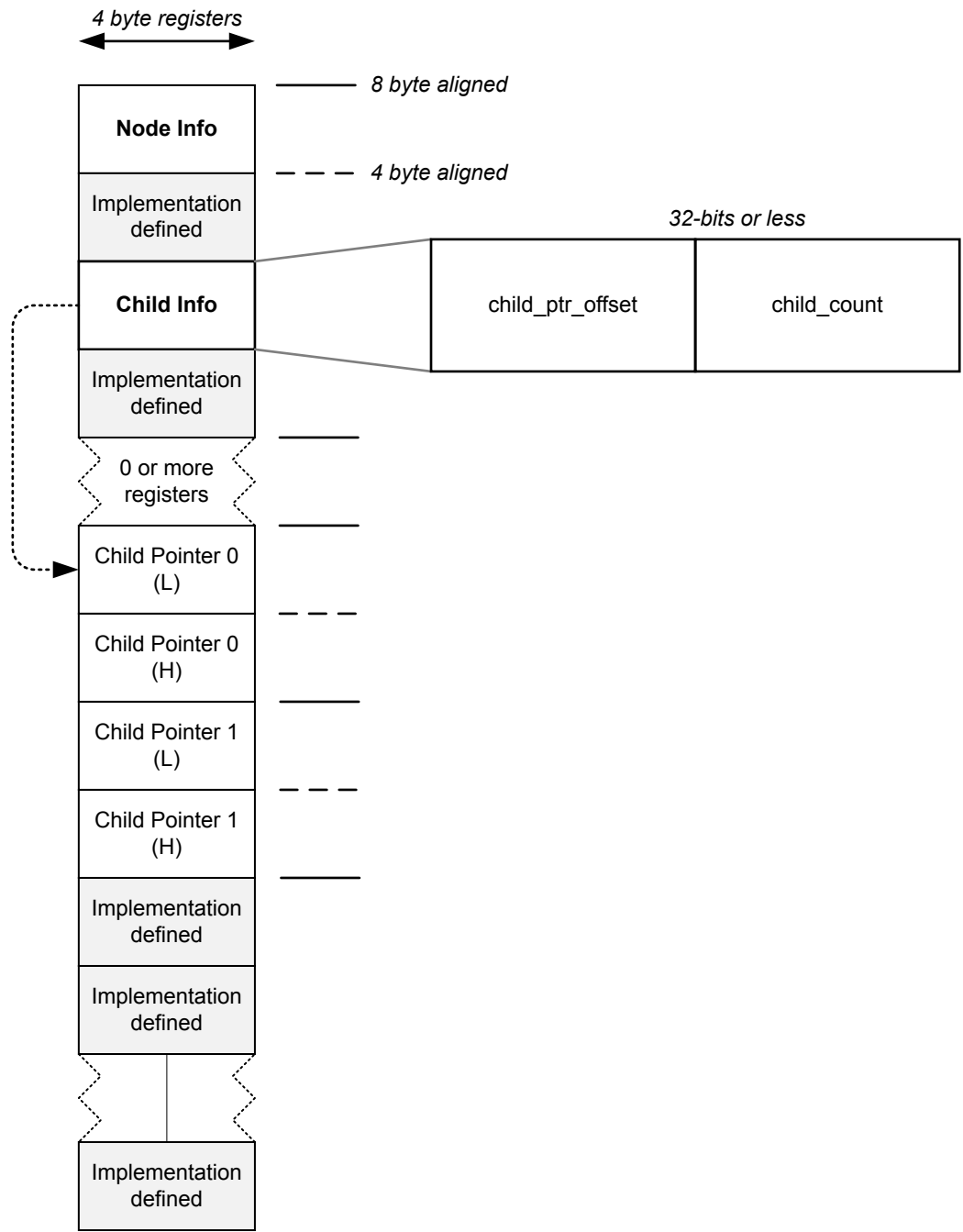


Figure 2-17 Node structure detail

The following table shows the supported node types and the corresponding node_type values in the Node Information register.

Table 2-4 node_type values

Node type	Value
Invalid	16'h0000
DVM	16'h0001
CFG	16'h0002
DTC	16'h0003

Table 2-4 node_type values (continued)

Node type	Value
HN-I	16'h0004
HN-F	16'h0005
XP	16'h0006
SBSX	16'h0007
RN-I	16'h000A
RN-D	16'h000D
RN SAM	16'h000F
CXRA	16'h0100
CXHA	16'h0101
CXLA	16'h0102
FMU	16'h0200
FDC	16'h0201
MPU	16'h0202
MXPMPU	16'h0203

2.5.3 Child pointers

There is one child pointer register per child node.

The address of the register containing the first child pointer is computed as:

Base node address (of the current 16KB block) + the child_ptr_offset value (from the child_info register).

Each subsequent child pointer register is 8 bytes higher. For more information, see [Figure 2-17 Node structure detail on page 2-57](#).

For example:

- Base node address = 0x4000
- Child_ptr_offset in child info register = 0x100
- Address of first child pointer register (child pointer 0) = Base node address + child_ptr_offset = 0x4100
- Address to child pointer 1 = Address of child pointer 0 (0x4100) + 0x8 = 0x4108

Child pointers are 32 bits or less and are contained in the low register. The high register is zero. Child pointer contents include the following:

- The child node address offset from PERIPHBASE, bits [27:0], which is an unsigned integer (positive offset)
- Three reserved bits, bits [30:28]
- An External Child Node indicator, bit 31

For example, address to 16KB block of the child node = PERIPHBASE + child pointer register [27:0].

The child node address offset relative to PERIPHBASE, including Node Pointer and Register Offset values, is held in the Child Pointer register. The following table shows the contents of the Child Pointer register and associated values.

Table 2-5 Child Pointer register

External Child Node	Reserved	Child node address offset relative to PERIPBASE	
31	30:28	27:14	13:0
1 = External, 0 = Internal	Not used	NODE POINTER [13:0]	REGISTER OFFSET[13:0]

The External Child Node, bit 31, behaves as follows:

- 1'b1: Indicates that this CHILD POINTER is pointing to a Config Node external to CMN-600AE
- 1'b0: Indicates that this CHILD POINTER is pointing to a Config Node internal to CMN-600AE

For CMN-600AE, external child nodes are only used for RN SAM and CXLA Config Node. The software performing the discovery can use two pieces of information:

1. The NODE POINTER information (X, Y, port ID (P0 or P1), device ID (D0, D1, D2, or D3)) to determine the CHI NodeID corresponding to the Config child node in question.
2. When the port (P0 or P1) has been determined using the NODE POINTER information, read the corresponding XP register to determine the device type that is connected to that specific port.
 - a. por_mxp_device_port_connect_info_p0
 - b. por_mxp_device_port_connect_info_p1

The device type corresponding to that child node helps the discovery software determine if the child node is RN-F, RN SAM, or CXLA. If the device type is CXRH, CXHA, or CXRA, then the external child node is CXLA, as every CXRH, CXHA, or CXRA node has a corresponding external CXLA node. It is the responsibility of the discovery software to ensure that the external child node is powered ON before sending any config accesses to it.

The NODE POINTER, bits [27:14], is processed as follows:

- If External Child Node is set to 1, then software can use the information in the NODE POINTER to extract the X dimension, Y dimension, port ID, and device ID corresponding to that Child Node.

The REGISTER OFFSET, bits [13:0], is always 0.

Depending on the size of the mesh (X and Y dimensions), CMN-600AE supports two different widths for encoding the X and Y dimension. The number of bits that is required is selected based on the larger of the X and Y values.

Table 2-6 Mesh size and encoding bits

Mesh width in X dimension	Mesh width in Y dimension	Number of bits used to encode X, Y
$X \leq 4$	$Y \leq 4$	2 bits for X, 2 bits for Y
$4 < X \leq 8$	$Y \leq 8$	3 bits for X, 3 bits for Y
$X \leq 8$	$4 < Y \leq 8$	3 bits for X, 3 bits for Y

For mesh widths using two bits each for X,Y encoding, the details of the NODE POINTER structure are provided in the following table.

Table 2-7 Mesh widths using 2 encoding bits

NODE POINTER: XID_WIDTH and YID_WIDTH = 2					
[13:10]	[9]	[8]	[7]	[6]	[5:0]
4'b0	XID[1]	XID[0]	YID[1]	YID[0]	DeviceID

Mapping between NODE POINTER and CMN-600AE NodeID for that processor or cluster:

- NODE POINTER[0] = NodeID[2]
- NODE POINTER[1] = 1'b0
- NODE POINTER[3:2] = NodeID[1:0]
- NODE POINTER[5:4] = 2'b00
- NODE POINTER[7:6] = NodeID[4:3]
- NODE POINTER[9:8] = NodeID[6:5]

Note

If an AXI4-Stream interface is present on an RN-F device, NODE POINTER[5:4] takes the value 2'b11. This only applies to non-ESAM RN-Fs.

For mesh widths using three bits each for X,Y encoding, the details of the NODE POINTER structure are provided in the following table.

Table 2-8 Mesh widths using three encoding bits

NODE POINTER: XID_WIDTH and YID_WIDTH = 3							
[13:12]	[11]	[10]	[9]	[8]	[7]	[6]	[5:0]
2'b0	XID[2]	XID[1]	XID[0]	YID[2]	YID[1]	YID[0]	DeviceID

Mapping between NODE POINTER and CMN-600AE NodeID for that processor or cluster:

- NODE POINTER[0] = NodeID[2]
- NODE POINTER[1] = 1'b0
- NODE POINTER[3:2] = NodeID[1:0]
- NODE POINTER[5:4] = 2'b00
- NODE POINTER[8:6] = NodeID[5:3]
- NODE POINTER[11:9] = NodeID[8:6]

Note

If an AXI4-Stream interface is present on an RN-F device, NODE POINTER[5:4] takes the value 2'b11. This only applies to non-ESAM RN-Fs.

The following figure shows a sample design for child pointers.

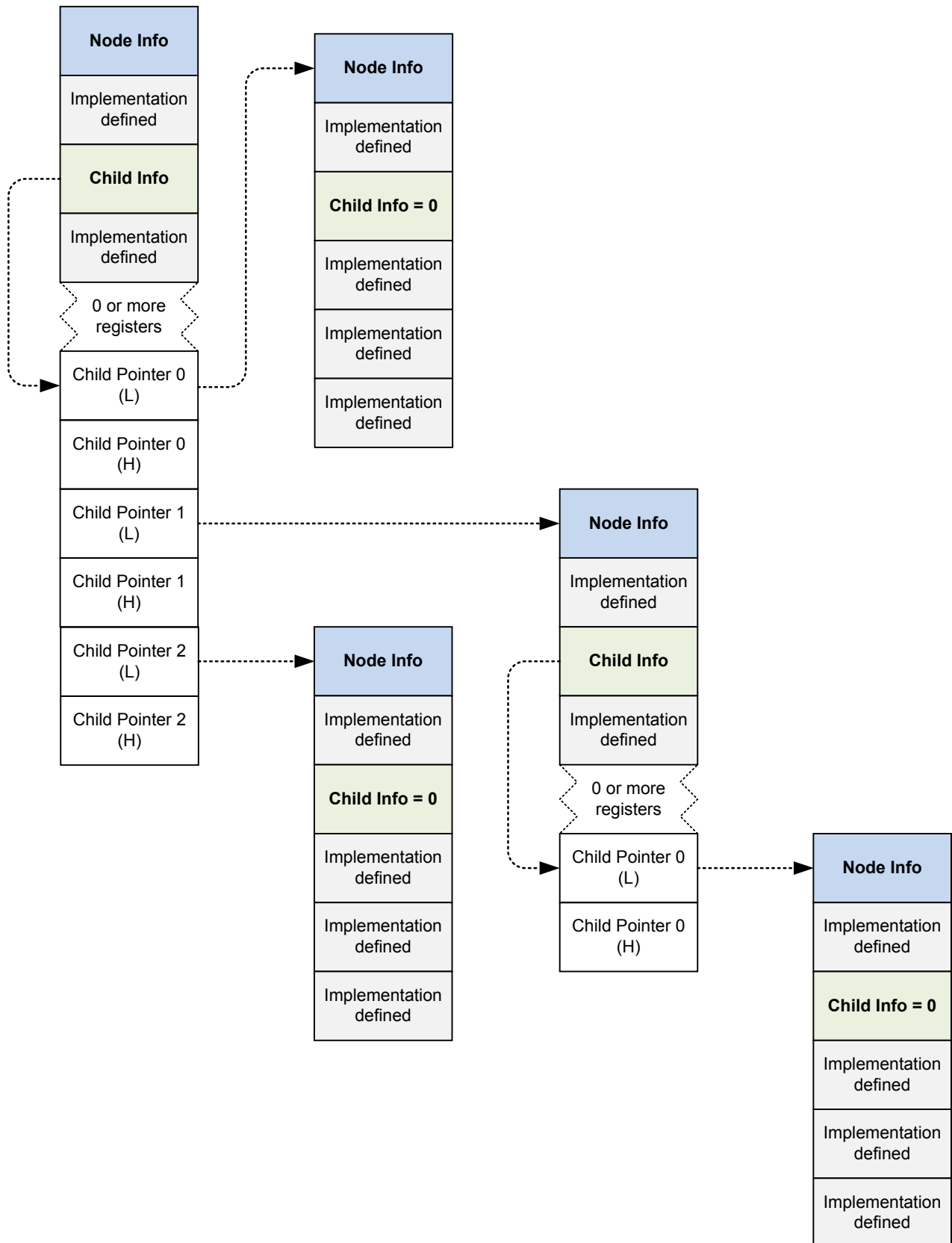


Figure 2-18 Child pointers

2.5.4 Discovery tree structure

The one-time discovery process creates a lookup table that contains the addresses for all CMN-600AE configured devices.

The discovery tree structure consists of three levels:

Level 1 Root Node, or the HN-D containing the Global Configuration Slave.

Level 2 XP layer.

Level 3 Leaf layer with one or two devices.

The following figure shows a 2×2 mesh configuration example with highlighted discovery tree levels.

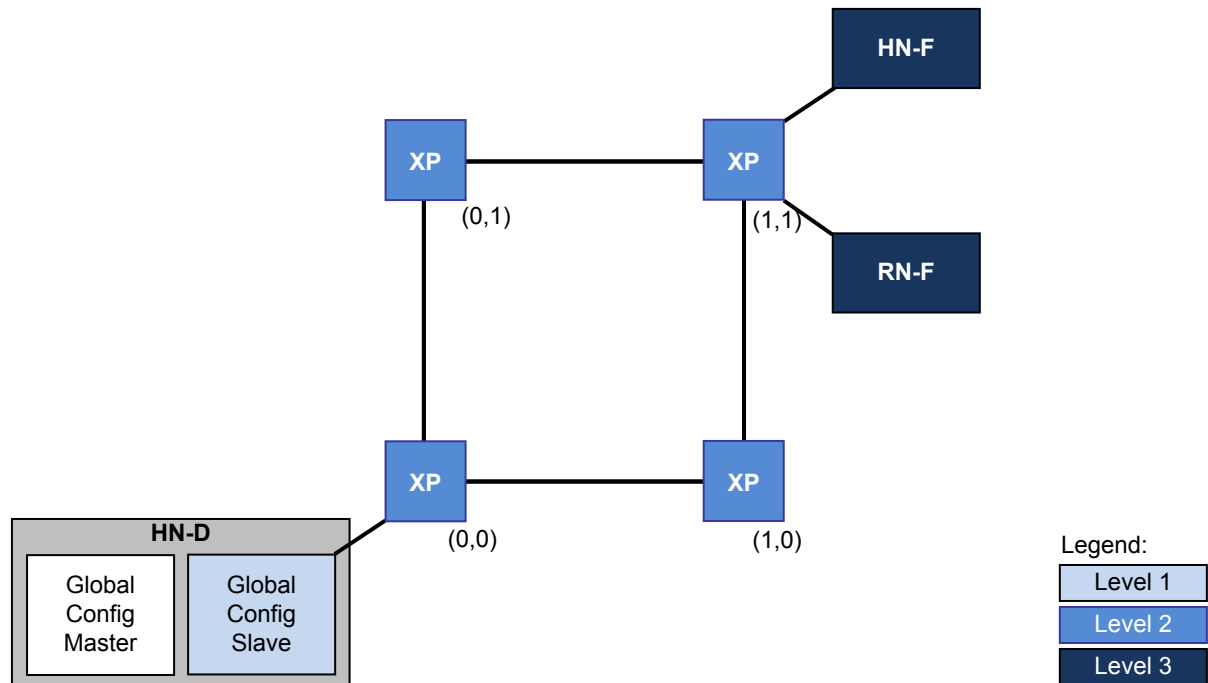


Figure 2-19 2×2 discovery tree example

The following figure shows the discovery tree structure for this 2×2 mesh configuration.

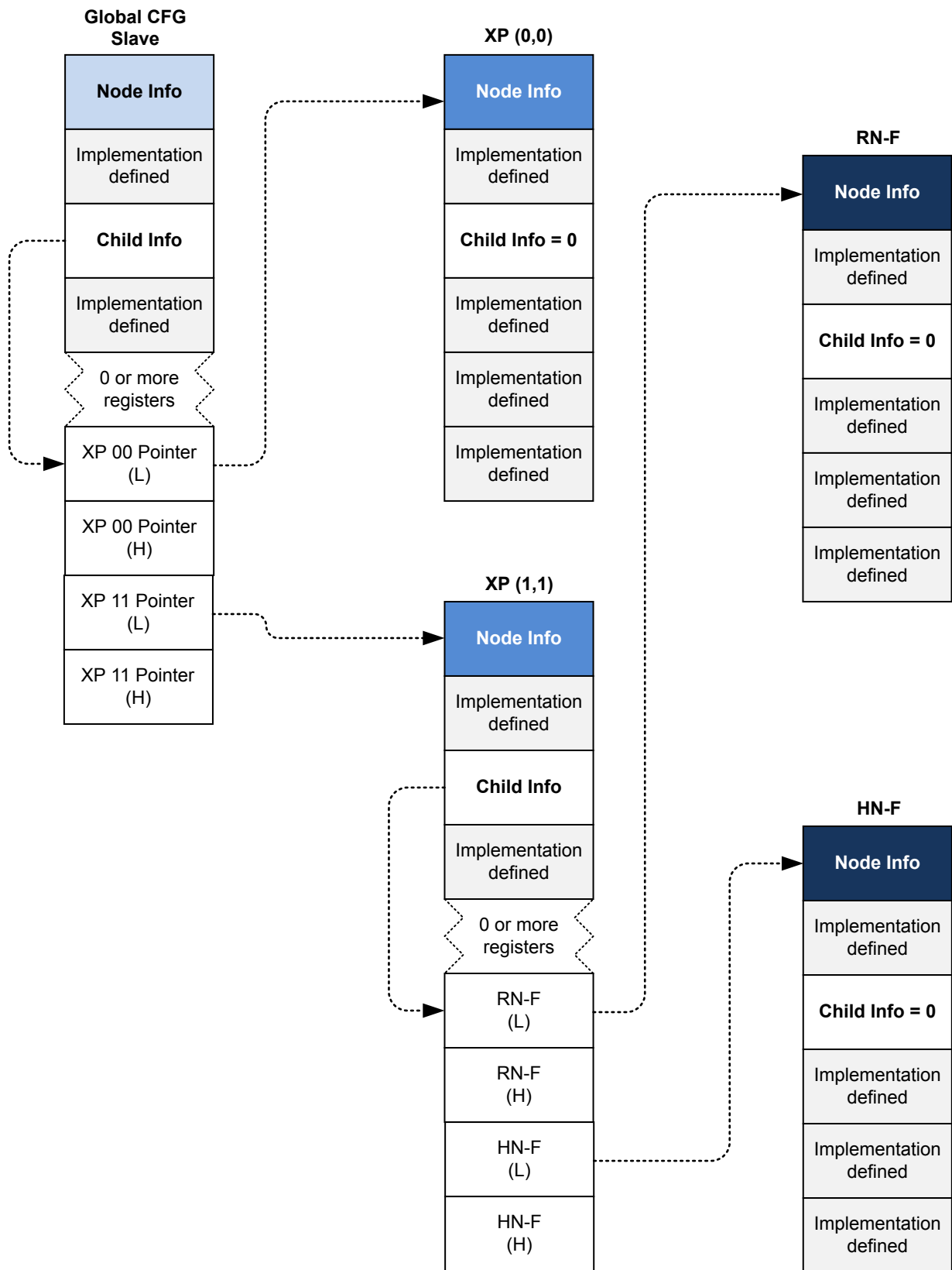


Figure 2-20 2 × 2 discovery tree structure

2.6 Addressing capabilities

CMN-600AE supports a 34-bit, 44-bit, or 48-bit physical address width. This width defines the physical address space for which read and write transactions are supported in the interconnect. Socrates IP Tooling configures these settings and creates the PA_WIDTH global parameter in the CMN-600AE RTL.

CHI interfaces in CMN-600AE support 44-bit and 48-bit address field widths for flits on the REQ channel. Socrates IP Tooling also configures these settings and creates the REQ_ADDR_WIDTH global parameter in the CMN-600AE RTL.

The address field width for flits on the SNP channel is derived automatically based on the REQ_ADDR_WIDTH global parameter.

The following table shows the legal combinations of physical address widths and flit address widths.

Table 2-9 Legal combinations of physical address and flit address widths

Physical address width	REQ flit address width	SNP flit address width (derived)
34-bit	44-bit	41-bit
	48-bit	45-bit
44-bit	44-bit	41-bit
	48-bit	45-bit
48-bit	48-bit	45-bit

The maximum supported physical address width for CMN-600AE is 48 bits. The minimum supported physical address width for CCIX is 48 bits.

If CMN-600AE has a physical address width of less than 48 bits, there is a mismatch between this and other CCIX components in your CML system. A mismatch in physical address widths might cause CMN-600AE to truncate the upper address bits of an incoming CCIX request or snoop. If there is a physical address mismatch, use software to ensure that CCIX components do not present requests and snoops to CMN-600AE with addresses outside of the CMN-600AE physical address range.

2.7 Atomics

CMN-600AE supports atomic accesses to both cacheable and non-cacheable memory locations.

Note

Atomics are not supported at the RN-I interfaces.

This section contains the following subsections:

- [2.7.1 Atomic requests in HN-F on page 2-65.](#)
- [2.7.2 Atomic requests in SN on page 2-65.](#)
- [2.7.3 Atomic requests in HN-I on page 2-65.](#)

2.7.1 Atomic requests in HN-F

The HN-F completes all CHI atomic requests that it receives, both for Cacheable and Non-cacheable transactions.

For Cacheable transactions, the HN-F completes any appropriate coherent actions and, if necessary, obtains the targeted cache line from memory. The HN-F then completes the required atomic operation and issues the appropriate response, with or without data.

For Non-cacheable transactions, the HN-F does not send an atomic request to the SN. As the final PoS/PoC for all memory traffic, the HN-F is able to process the transaction in the following way:

1. Issue a read to the SN
2. Atomically update the copy of the data in the HN-F
3. Write back the result to the SN

This approach means that the SN never receives CHI atomic requests, as the HN-F completely handles the requests.

2.7.2 Atomic requests in SN

The SN node (CHI memory controller or SBSX bridge) does not process atomic requests.

2.7.3 Atomic requests in HN-I

The HN-I does not complete atomic transactions.

On receiving an atomic request, the HN-I generates an appropriate error response to the originating master.

2.8 Exclusive accesses

CMN-600AE supports exclusive accesses to both Shareable and Non-shareable locations.

For more information, see the *Arm® AMBA® 5 CHI Architecture Specification*.

This section contains the following subsections:

- [2.8.1 Exclusive accesses in HN-F on page 2-66.](#)
- [2.8.2 Exclusive accesses in HN-I on page 2-66.](#)
- [2.8.3 CML support for exclusive accesses on page 2-66.](#)

2.8.1 Exclusive accesses in HN-F

The HN-F supports exclusive access on ReadNoSnp, WriteNoSnp, ReadShared, ReadClean, ReadNotSharedDirty, and CleanUnique transactions to any address that maps to the HN-F.

RNs generate ReadNoSnp and WriteNoSnp Exclusives for memory locations that are marked Non-cacheable or Device. ReadShared, ReadClean, ReadNotSharedDirty, and CleanUnique exclusives are used for shareable and coherent memory locations. Each HN-F partition includes 64 exclusive monitors for tracking of these transaction types. Each monitor can act as both a PoC monitor and System monitor, as the *Arm® AMBA® 5 CHI Architecture Specification* defines.

Only 64 unique logical threads, which are designated by a unique combination of SrcID and LPID, can concurrently access the HN-F exclusive monitors.

2.8.2 Exclusive accesses in HN-I

HN-Is support exclusive access on ReadNoSnp and WriteNoSnp transactions to any address that maps to an HN-I.

Each HN-I partition includes 32 exclusive monitors as defined in the *Arm® AMBA® 5 CHI Architecture Specification* for tracking of these transaction types. Only 32 unique logical threads can concurrently access the HN-I system exclusive monitors. These threads can be either processor or device threads, and are designated by a unique combination of SrcID and LPID.

All exclusives targeting the HN-I are terminated at the HN-I and are not propagated downstream. Exclusives are terminated regardless of the value of the HN-I PoS control register and auxiliary control register.

2.8.3 CML support for exclusive accesses

In the SMP mode, CMN-600AE CML supports remote exclusive accesses from RN-Fs.

Constraints include:

- Remote exclusive accesses from an RN-I or RN-D are not supported
- Remote exclusive accesses targeting with an HN-I or HN-D is not supported

Support for remote exclusive accesses in *CCIX Gateway* (CXG) blocks include these constraints:

- CXRA in local CXG block passes Excl and LPID fields of incoming CHI request on CCIX request message USER (Ext) field
- CXHA in the remote CCIX gateway (CXG) block extracts these bits from CCIX request message USER (Ext) field. CXHA then sends these bits on respective CHI Excl and LPID fields. CXHA sets the source type as RN-F based on its RAID to LDID register.
- Exclusive OK (EXOK) response is sent as 0b01 on CCIX RespErr field

Note

0b01 is a reserved encoding in RespErr field and this field is sent as a CCIX extension (Ext6).

HN-Fs monitor exclusives from remote RN-Fs using existing exclusive monitors. To track remote exclusives, the monitors track the LDID and LPID fields of the incoming request.

2.9 Processor events

CMN-600AE supports communicating processor events to all processors in the system.

Refer to the processor event interface signals described in [A.13 Processor event interface signals on page Appx-A-1958](#).

When a processor generates an output event that an SEV instruction triggers, it is broadcast to all processors in the system. Similarly, anytime an exclusive monitor within HN-F or HN-I is cleared, an output event is broadcast to all processors in the system. The event interface signals are also present at RN-I and RN-D nodes, for use by components such as a *System Memory Management Unit* (SMMU).

The logical operator OR is used to combine the EVENT signals, then the result is broadcast to the processors.

2.10 Quality of Service

CMN-600AE includes end-to-end QoS capabilities which support latency and bandwidth requirements for different types of devices.

The QoS device classes are:

Devices with bounded latency requirements

These devices are primarily real-time or isochronous that require some or all of their transactions complete within a specific time period to meet overall system requirements. These devices are typically highly latency-tolerant within the bounds of their maximum latency requirement. Examples of this class of device include networking I/O devices and display devices.

Latency-sensitive devices

The response latency that the transactions of devices incur has a high impact on the performance of these devices. Processors are traditionally highly latency-sensitive devices, although a processor can also be a bandwidth-sensitive device depending on its workload.

Bandwidth-sensitive devices

These devices have a minimum bandwidth requirement to meet system requirements. An example of this class of device is a video codec engine, which requires a minimum bandwidth to sustain real-time video encode and decode throughput.

Bandwidth-hungry devices

These devices have significant bandwidth requirements and can use as much system bandwidth as is made available, to the limits of the system. These devices determine the overall scalability limits of a system, with the devices and system scaling until all available bandwidth is consumed.

Note

A device can be classified into one or more of these classes, depending on its workload requirements.

Support for these different types of devices and their resulting traffic is included in the AMBA 5 CHI protocol and in the entirety of CMN-600AE microarchitecture. Each component in CMN-600AE contributes to the overall QoS microarchitecture.

This section contains the following subsections:

- [2.10.1 Architectural QoS support on page 2-68.](#)
- [2.10.2 Microarchitectural QoS support on page 2-68.](#)
- [2.10.3 QoS configuration example on page 2-74.](#)

2.10.1 Architectural QoS support

The AMBA 5 CHI protocol includes a 4-bit *QoS Priority Value* (QPV) with all message flits.

The QPV of the originating message must propagate for all messages in a transaction. The QPV is defined as higher values being higher priority and lower values being lower priority. All CMN-600AE components use the QPV to provide prioritized arbitration and to prevent Head-of-line blocking based on the QPV.

2.10.2 Microarchitectural QoS support

The QPV of RN requests must be modulated depending on how well or poorly their respective QoS requirements are met.

QoS regulators

QoS-modulation capability can be integrated into the RN. However CMN-600AE enables system designers to include non-QoS-aware devices in the CMN-600AE system, but still have these devices meet the QoS-modulation requirements of the CMN-600AE QoS microarchitecture.

CMN-600AE includes inline QoS regulators that perform QoS modulation without requiring any QoS-awareness by the requesting device. A QoS regulator introduces an interstitial layer between an RN and the interconnect. This interstitial layer monitors whether the bandwidth and latency requirements of the RN are being met. It also performs in-line replacement of the RN-provided QPV field as required, adjusting upwards to increase priority or downwards to reduce priority in the system.

The QoS regulators are present at all entry points into CMN-600AE:

- For CHI ports, the regulator is present in the XP.
- For ACE-Lite and AXI4 slave interfaces, the regulator is present at the ACE-Lite and AXI4 side of the protocol bridge.

CMN-600AE QoS regulators have three operating modes:

- Pass-through.
- Programmed QoS value.
- Regulation.

These operating modes are controlled through memory-mapped configuration registers.

QoS regulator operation

The values of the base QPV, **AxQOS** for AXI and ACE-Lite interfaces or **RXREQFLIT.QOS** for CHI ports, are inputs to the QoS subblock.

When latency regulation or period regulation is enabled, the values generated by the regulators replace the base QPV values. For an RN-F, a single QoS regulator monitors CHI transactions that return data to the RN-F such as reads, atomics, and snoop stash responses. The regulated QPV is applied to all CHI requests from that RN-F. For an RN-I or RN-D, separate QoS regulators exist for AR and AW channels.

The QoS regulators can operate in either latency regulation mode or period regulation mode. The registers to configure the QoS regulators exist in each RN-I, RN-D, and XP.

Latency regulation mode

When configured for latency regulation, the QoS regulator increases the QPV whenever actual transaction latency is higher than the target, and decreases the QPV when it is lower:

- For every cycle that the latency of a transaction is more than the target latency, the QPV increases by a fractional amount. The scale factor K_i determines this amount.
- For every cycle that the latency of a transaction is less than the target latency, the QPV decreases by the same fractional amount. The scale factor K_i determines this amount.

The QoS Latency Target register specifies the target transaction latency in cycles.

The QoS Latency Scale register specifies the scale factor K_i . It is coded in powers of two, so that a programmed value of $0x0 = 2^{-3}$ and a programmed value of $0x7 = 2^{-10}$.

The QoS regulator can be programmed to operate in latency regulation mode by programming the following bits in the QoS Control register:

- Set the qos_override_en bit to 0b1.
- Set the lat_en bit to 0b1.
- Set the reg_mode bit to 0b0.
- Set the pqv_mode bit to 0b0.

Period regulation mode for bandwidth regulation

When configured for period regulation, the QoS regulator increases the QPV whenever the period between transactions is larger than the target, and decreases the QPV when it is lower:

- For every cycle that the period between transactions (as measured at dispatch time) is more than the target period, the QPV increases the scale factor K_i by a fractional amount.
- For every cycle that the period between transactions is less than the target period, the QPV decreases the scale factor K_i by the same fractional amount.

The QoS Latency Target register specifies the target period in cycles.

The QoS Latency Scale register specifies the scale factor K_i . It is coded in powers of two, so that a programmed value of $0 \times 0 = 2^{-3}$ and a programmed value of $0 \times 7 = 2^{-10}$.

The QoS regulator can be programmed to operate in period regulation mode by programming the following bits in the QoS Control register:

- Set the qos_override_en bit to 0b1.
- Set the lat_en bit to 0b1.
- Set the reg_mode bit to 0b1.

There are two modes of period regulation:

Normal mode

The QPV does not increase or decrease when there are zero outstanding transactions.

Quiesce high mode

The QPV increases by a fractional amount, which the scale factor K_i determines, in every cycle where there are zero outstanding transactions.

The mode of period regulation can be selected by programming the pqv_mode bit in the QoS Control register.

RN-I and RN-D bridge QoS support

In addition to the QoS regulators, the RN-I and RN-D bridge provides QoS-aware arbitration mechanisms.

To simplify arbitration logic, all transactions are split into two QoS Priority Classes (QPCs), high and low. QoS-15 transactions make up the high class. All other transactions are considered to be in the low class.

Port multiplexer arbitration

An RN-I and RN-D bridge includes three ACE-Lite and ACE-Lite-with-DVM ports. The RN-I and RN-D bridge selects between these ports for allocation into its transaction tracker. This selection process makes the allocated transaction a candidate for issuing to a Home Node. The port multiplexer is arbitrated using the following strategy:

- High QPC first, then the low QPC.
- Round-robin arbitration among the AMBA ports within a QPC.

Tracker allocation

When transactions are allocated into the tracker, they are scheduled for issuance to a Home Node based on QPC. This strategy is the same strategy as port mux arbitration.

- High QPC first, then the low QPC.
- Round-robin arbitration in a QPC among the transactions for issue.

HN-F QoS support

The HN-F is a key shared system resource that is used for system caching and for communication with the memory controller for external memory access.

The HN-F includes the following QoS support mechanisms:

QoS decoding in HN-F

The HN-F interprets the 4-bit QPV at a coarser granularity, as the following table shows.

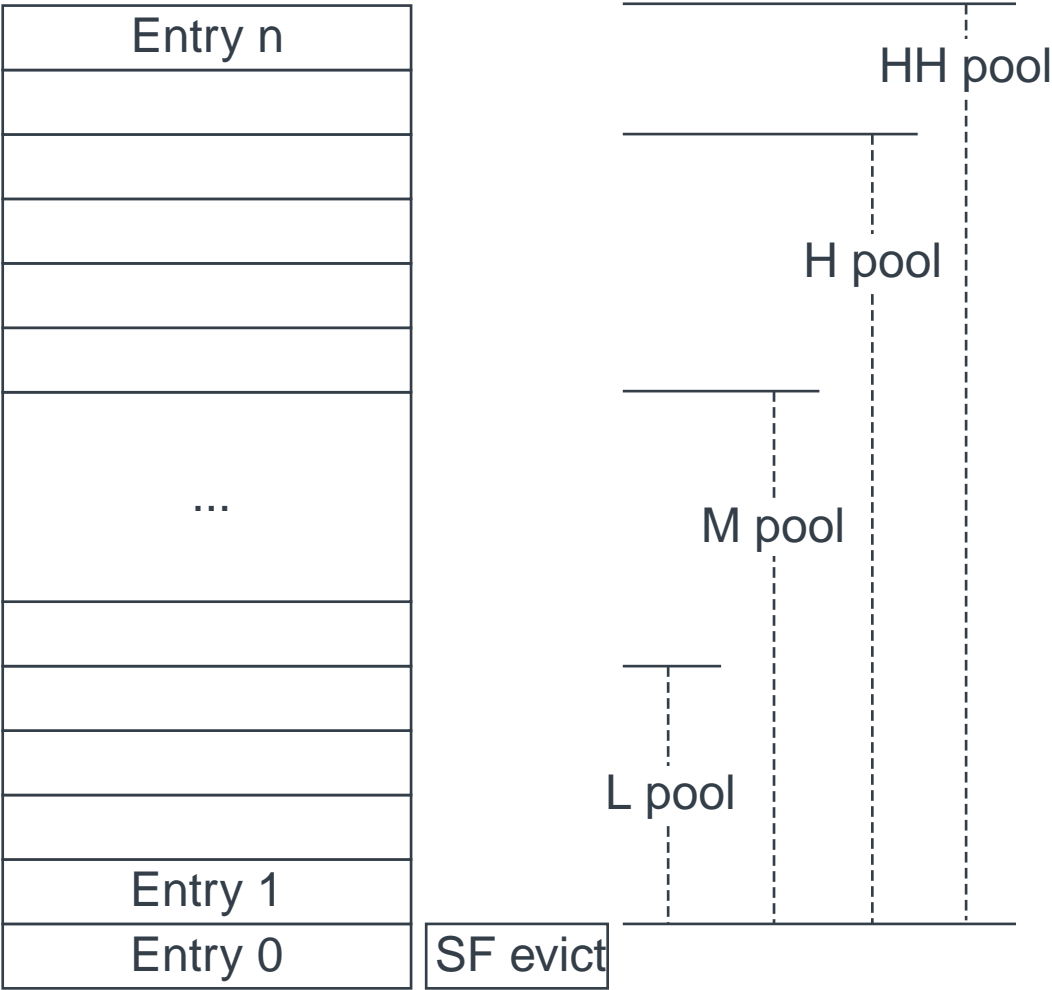
Table 2-10 QoS classes in HN-F

QoS value range	QoS Class	Class mnemonic	Priority
15	HighHigh	HH	Highest
14-12	High	H	High
11-8	Med	M	Medium
7-0	Low	L	Low

QoS class and POCQ resource availability

The HN-F includes a 32-entry or 64-entry structure, the *Point-of-Coherency Queue* (POCQ), from which all transaction ordering and scheduling is performed. The POCQ buffers are shared resources for all QoS classes, with one entry being reserved for internal use. The higher the QoS class, the higher the occupancy availability. As the following figure shows, the POCQ is partitioned so that higher priority requests are able to use a larger percentage of the POCQ buffering. This partitioning ensures bandwidth and latency requirements of higher priority transactions are met.

The number of entries available for use by each QoS class is defined in the HN-F QoS Reservation register, and is software-programmable.



POCQ logical view

Figure 2-21 POCQ availability and QoS classes

The QoS pools are:

- hh_pool** Available for HH class.
- h_pool** Available for H class and HH class.
- m_pool** Available for M class, H class, and HH class.
- l_pool** Available for all classes.
- seq** SF evictions only.

POCQ allocation policies

Allocation into POCQ entries can follow either of two paths:

- Immediate allocation on receipt of the initial request by the HN-F
- Allocation of a retried request after a protocol-layer retry of the initial request

The first case is the expected common case and is always the case in a reasonably uncongested system. If the POCQ has an available buffer corresponding to the QoS class of an arriving request, that request allocates in the POCQ.

However, consider a congested system and a POCQ entry with the QoS class of an arriving request is unavailable at the time of arrival. In this case, the AMBA 5 CHI protocol requires that the arriving request receives a protocol-layer retry. The transaction flow in this case is as follows:

1. A request arrives at a congested HN-F.
2. The HN-F does not have an available POCQ buffer corresponding to the QoS class of the new transaction.
3. The HN-F increments a credit counter for the specific QoS class of the specific RN and sends a RetryAck response to the RN.
4. On receiving a RetryAck response, the RN then waits for a follow-on PCreditGrant response.
5. When a POCQ entry becomes available, the HN-F reserves that buffer for the highest-priority RN with a nonzero credit-counter. It also sends a PCreditGrant response to the selected RN.
6. On receiving a PCreditGrant, the RN re-issues the transaction, which is guaranteed to be allocated into the HN-F.

This mechanism serves as prioritized arbitration based on QoS values for requests that are sent to the HN-F.

POCQ scheduler policies

When transactions are allocated into the POCQ, they are scheduled for issuance based on the QPV as follows, in descending order of priority:

- Starved transactions. These transactions are lower-priority transactions that have made no progress for a specific number of cycles. The number of cycles is specified in the respective fields in the RN Starvation Register.
- Highest QoS class
- Round-robin arbitration within a QoS class among the issuable transactions

HN-I and SBSX QoS support

The HN-I bridge provides QoS-aware arbitration mechanisms for static grants and AMBA requests.

To simplify arbitration logic, all transactions are split into two QPCs: high and low. QoS-15 transactions make up the high class. All other transactions are considered to be in the low class.

Note

SBSX QoS support is identical to that of the HN-I.

Dynamic credit tracker allocation

Requests allocate into the tracker until it is full. After it is full, requests are retried and the HN-I increments a credit counter for the affected RNs in an internal retry bank.

When a tracker entry is cleared, the HN-I checks the retry bank for any retried transactions. If any are present, the newly available tracker entry is reserved and a static credit grant is sent to an RN chosen using the following algorithm:

- Choose an RN marked as high QPC first, then the low QPC.
- Use round-robin arbitration within a QPC.

Scheduling to AMBA interface

When transactions are allocated into the tracker, they are scheduled for issue on the AMBA interface. The scheduling is based on QPC following a similar strategy to static credit allocation:

- Choose high QPC first, then the low QPC.
- Use round-robin arbitration within a QPC.

Write data buffers are also allocated based on QPC class. For write requests that are ready to issue:

- Choose high QPC first, then the low QPC.
- Use round-robin arbitration within a QPC.

2.10.3 QoS configuration example

This example configuration demonstrates the QoS mechanisms and their contribution to the overall QoS solution.

It is the responsibility of the SoC designer and system programmer to configure CMN-600AE to meet the specific requirements of the system and expected workloads.

System operating conditions

The example QoS configuration assumes the following:

- Four processor clusters:
 - Bimodal operation. A processor cluster is latency-sensitive when bandwidth per cluster is $\leq 2\text{GB/s}$, and bandwidth-hungry, and therefore latency-tolerant, when bandwidth per cluster is $> 2\text{GB/s}$.
 - 16 outstanding combined reads and writes.
 - 10GB/s maximum bandwidth per cluster.
 - 25GB/s maximum aggregate bandwidth across all processor clusters.
- Four peripheral devices with bounded latency requirements:
 - Each device is the sole device that is connected to ACE-Lite interface 0 on four different RN-I bridges.
 - 1 microsecond maximum latency requirement.
 - 4GB/s maximum bandwidth per device.
 - 210GB/s maximum aggregate bandwidth across all devices.
- 14 peripheral bandwidth-hungry devices:
 - Connected to all remaining RN-I ACE-Lite interfaces.
 - 12GB/s read or write bandwidth per device, with a combined maximum of 24GB/s.
 - 60GB/s maximum aggregate bandwidth across all devices.
- All devices can be concurrently active.
- 80GB/s maximum aggregate bandwidth across all devices.

HN-F QoS classes

For the QoS ranges and class values in HN-F, refer to [Table 2-10 QoS classes in HN-F on page 2-71](#).

QoS regulator settings

To meet the bandwidth and latency requirements of the described system configuration, CMN-600AE QoS regulators can be configured with the settings as described in the following table.

Table 2-11 QoS regulation settings

Device	Regulation type	Regulation parameter	QoS range	QoS scale
Processor	Latency	60ns max latency	11-13	8-9
Real-time peripheral	Override (constant value)	Constant	15	n/a
High-bandwidth peripheral	Override (constant value)	Constant	8	n/a

The latency specification for real-time peripherals must be sufficiently far below the maximum real-time constraint to allow the control loop in the QoS regulator to adjust based on achieved latency. However, the programmed latency must not violate the maximum latency requirement.

To meet the bandwidth and latency requirements of the described system configuration, HN-F QoS reservation values can be configured as summarized in the following table. The table is based on 32-entry POCQ with one entry for SF back invalidations.

Table 2-12 QoS class and reservation value settings

QoS class	QoS reservation value
HighHigh	31
High	30
Medium	15
Low	5

These settings enable the following system functionality:

- Real-time devices are QPV-15, ensuring their transactions meet their bounded latency requirements.
- The processor QPV is higher than the bandwidth-hungry devices, second only to the real-time devices. Therefore the processor QPV generally achieves minimum latency, except when there is high-bandwidth real-time traffic.
- Real-time devices have all the HN-F POCQ buffering available to them, to prevent bandwidth limitations from impacting achieved latency.
- Real-time devices always have buffering available to them throughout the entirety of CMN-600AE preventing Head-of-line blocking from lower-priority or higher-latency transactions.

2.11 Barriers

Barriers were deprecated from CHI-B onwards. All masters (fully coherent and I/O coherent) must handle barriers at the source.

When memory barrier ordering or completion guarantees are required, masters must wait for the responses from all required previous transactions that are issued into the interconnect. No barrier requests can be issued into the interconnect.

All requesting devices that are attached to an interconnect must have a configuration option or strap that prevents issuing of any barriers. If a barrier is issued into the interconnect, the results are unpredictable.

Note

The DVM_SYNC command, the DVM synchronization that might be initiated by an Arm DSB instruction, is sent to the DVM block, and executes appropriately.

For more information about barriers, see the *Arm® AMBA® 5 CHI Architecture Specification* and the *Arm® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, AXI5, ACE and ACE5*.

2.12 DVM messages

If an RN-F supports *Distributed Virtual Memory* (DVM) messages, it can send DVM requests and receive DVM snoops.

A DVM message from an RN-F is sent to the HN-D. On receiving the DVM message, the HN-D:

- Forwards the DVM message as a snoop to the participating RNs. To do this action, the HN-D uses a static list to replace the DVM Domain Control register used with legacy products.
- Collects the individual snoop responses
- Sends a single response back to the RN-F that originated the DVM message transaction

The **SYSCOREQ/SYSCOACK** mechanism provides proxy snoop responses in scenarios when the RN is powered down. For more **SYSCOREQ/SYSCOACK** information, refer to [2.27 RN entry to and exit from Snoop and DVM domains on page 2-151](#).

Note

- An RN that issues DVM messages must also be able to receive DVM messages. If this requirement is violated, the system must not rely on the DVM message causing any DVM snoops.
 - An RN-F can issue only one outstanding DVMOp (Sync).
-

For more information about DVM messages, see the *Arm® AMBA® 5 CHI Architecture Specification*.

2.13 PCIe integration

CMN-600AE supports integration of a PCIe *Root Complex* (RC) or *EndPoint* (EP).

This section contains the following subsections:

- [2.13.1 PCIe topology requirements on page 2-78.](#)
- [2.13.2 PCIe master and slave restrictions and requirements on page 2-78.](#)
- [2.13.3 System requirements for PCIe devices on page 2-78.](#)
- [2.13.4 RN-I and HN-I PCIe programming sequence on page 2-79.](#)

2.13.1 PCIe topology requirements

There are specific topology rules that you must follow when integrating PCIe components with CMN-600AE.

The following PCIe topology requirements apply:

- PCIe slaves must not be connected to HN-D
- PCIe slaves must not share HN-I with other non-PCIe slaves

2.13.2 PCIe master and slave restrictions and requirements

This section describes the PCIe master and slave restrictions and requirements.

Note

In this section, PCIe HN-I refers to an HN-I which has a PCIe slave connected to it. HN-I refers to all other HN-I.

The general restrictions and requirements are:

- Peer-to-peer PCIe traffic, that is, one PCIe endpoint talking to another PCIe endpoint, must not pass through the CMN-600AE. Requests from the PCIe master can only target memory through the HN-F, CMN-600AE configuration space, or an I/O slave device downstream of the HN-I. These requests must not target any PCIe slave downstream of the HN-I.
- The PCIe master must not create same-**AWID** dependency between *Non-Posted Write* (NPR-Wr) and *Posted Write* (P-Wr) transactions sent on the RN-I AXI/ACE-Lite slave port.

The flow control requirements are:

CMN-600AE to PCIe slave

The PCIe slave must be able to sink at least one NPR-Wr from the CMN-600AE sent on the HN-I AXI/ACE-Lite master port. This requirement guarantees that the HN-I AW channel remains unblocked. Therefore, P-Wrs from PCIe master targeting the downstream slave device can progress, as required by the PCIe ordering rules.

PCIe master to CMN-600AE

If a *System Memory Management Unit* (SMMU) or GIC-ITS is in the path between the PCIe master interface and the RN-I slave interface, there are two possible options:

- *Non-Posted Reads* (NPR-Rd) from the PCIe master must not target any PCIe HN-I.
- Use a separate master interface port in the SMMU and GIC-ITS for translation table walks (TCU in MMU-500/GIC-600 and beyond) and connect this port to a different RN-I which does not send any requests to any PCIe HN-I. None of the masters that are connected to this RN-I can talk to any PCIe HN-I.

2.13.3 System requirements for PCIe devices

There are certain system-level requirements that you must meet when integrating PCIe devices with CMN-600AE. These requirements determine which CMN-600AE devices can handle certain request types and how PCIe and non-PCIe transactions must be handled.

Note

In this section, the term PCIe HN-I refers to an HN-I which has a PCIe slave connected to it. The term HN-I refers to all other HN-Is.

CMN-600AE has the following system requirements for PCIe devices:

- All non-PCIe I/O slave devices must complete all writes without creating any dependency on a transaction in the PCIe subsystem
- Your configuration might have an SMMU in the path between the PCIe master interface and the RN-I slave interface. If using this kind of configuration, table-walk requests from the SMMU can only be sent to memory through the HN-F or non-PCIe HN-I.
- Interrupt translation table walk requests from GIC-ITS can only be sent to memory through the HN-F or non-PCIe HN-I

2.13.4 RN-I and HN-I PCIe programming sequence

To ensure proper PCIe functionality, software must complete the following programming before any non-configuration access to the RN-I or HN-I.

When setting up PCIe RN-Is and HN-Is, the entire PCIe configuration space of an RC must be mapped to a single HN-I address region. HN-I has a SAM that can be configured for up to three address regions. All address regions that are not configured into these three regions are considered to be the default address region. For more information about configuring the HN-I SAM, including example configurations, see [2.21 HN-I SAM on page 2-119](#).

Throughout the following procedure, address region X or address region Y can refer to any of the four address regions (0, 1, 2, or 3).

Procedure

1. If there is a PCIe-RC attached to the RN-I, then set the `pcie_mstr_present` field of the `por_rni_cfg_ctl` register. This programming indicates that one or more PCIe masters are present upstream.
2. Program the `por_hni_sam_addrregion{0,1,2,3}_cfg` registers so that the PCIe configuration space falls under one of the four HN-I address regions. This programmed address region is referred to as address region X.
3. Set only one of the following bits in `por_hni_sam_addrregionX_cfg` for address region X:

ser_devne_wr

Set this bit if the PCIe configuration space is marked as the Arm Device-nGnRnE memory type. If this bit is set, HN-I serializes all Device-nGnRnE writes to address region X. The HN-I does not send any other write requests with the same AWID as an outstanding Device-nGnRnE write.

ser_all_wr

Set this bit if the PCIe configuration space cannot be marked as Arm memory type of Device-nGnRnE. If this bit is set, HN-I serializes all writes targeting Address Region X.

4. Clear the `pos_early_wr_comp_en` bit of the `por_hni_sam_addrregionY_cfg` register for address region Y.

Address region Y is the region in which PCIe EP memory space (posted traffic) is programmed. If the `pos_early_wr_comp_en` bit is cleared, HN-I does not provide early write completions for any write requests targeting address region Y.

2.14 Reliability, Availability, and Serviceability

The CMN-600AE *Reliability, Availability, and Serviceability* (RAS) features are implemented as set of distributed logging and reporting registers and a central interrupt handling unit.

The distributed logging and reporting registers are associated with devices that can detect errors. These devices are XP, HN-I, HN-F, SBSX, and CXHA.

The central interrupt handling logic is located in the HN-D.

Each device that can detect errors logs the error in local registers and sends error information to the central interrupt handling logic in the HN-D. The HN-D contains four error groups, a Secure and Non-secure group for error and fault type errors. Each is represented in an *ERRor Group Status Register* (ERRGSR).

Error group, Secure

por_cfgm_errgsr{0-4}

Fault group, Secure

por_cfgm_errgsr{5-9}

Error group, Non-secure

por_cfgm_errgsr{0-4}_NS

Fault group, Non-secure

por_cfgm_errgsr{5-9}_NS

The following figure shows the four error groups, and the four respective interrupt request signals, with XP connections highlighted. The HN-I, HN-F, SBSX, and CXHA use the same input/output structure.

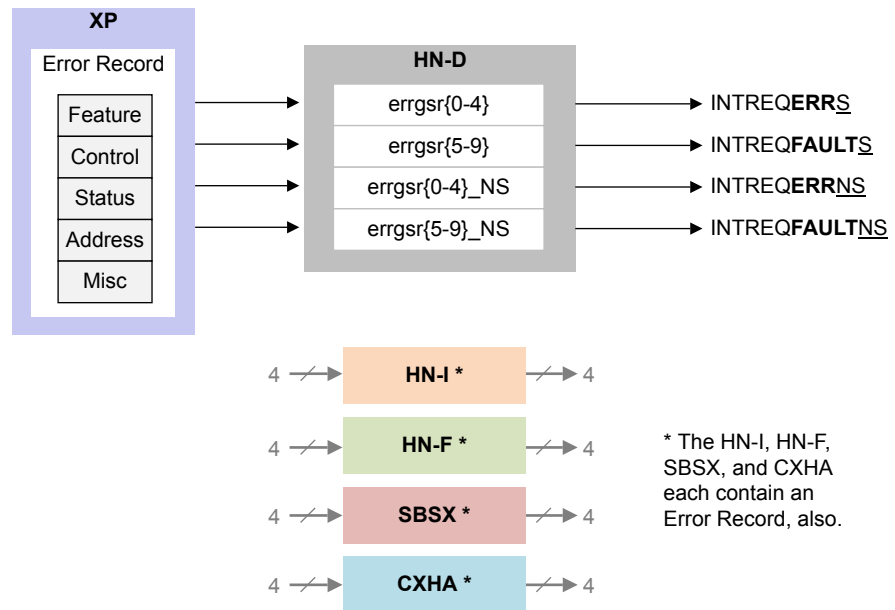


Figure 2-22 Error top-level diagram

Each ERRGSR is partitioned according to device type, with a 64-bit vector representing the logical ID of each device instance. The following figure shows the partitioning.

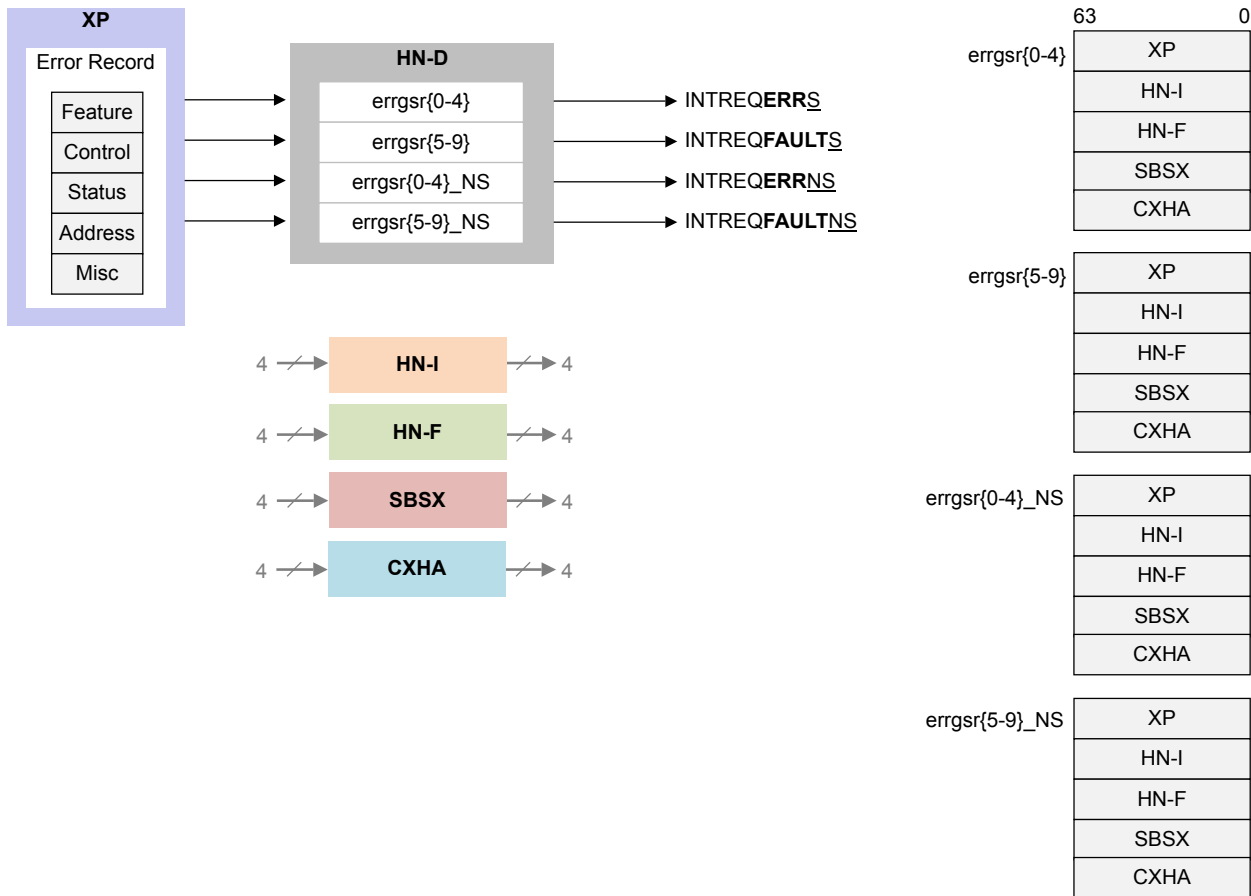


Figure 2-23 256-bit error handling structure

Each device that can detect errors has five Error Record registers that contain the error type, along with other information such as the address and opcode. Error types include *Corrected Error* (CE), *Deferred Error* (DE), and *Uncorrected Error* (UE).

For more information on error types, refer to [2.14.1 Error types on page 2-82](#).

For register details, see [4.3 Register descriptions on page 4-233](#).

Error interrupt handler flow example

The following sequence of events and figure describe the process for determining the error source and type of an HN-I generating an interrupt request:

1. The HN-D generates an interrupt for one of the five error group types.
2. The error group indicates the error source device type, which can be:
 - XP.
 - HN-I, which is used in this case.
 - HN-F.
 - SBSX.
 - CXHA.
3. The bit location within the error group indicates the logical ID of that device type. In this case, it reveals an HN-I error, the HN-I Error Record Status block for this example.
4. The Status block of the Error Record for the specific XP, HN-I, HN-F, SBSX, or CXHA reveals the type of error.
5. The Address and Misc blocks of the Error Record provide further details regarding error root cause, in this case a Corrected Error.

6. The Valid bit is also asserted.
7. To clear the asserted interrupt on the pin, the valid bit of the error status has to be cleared.

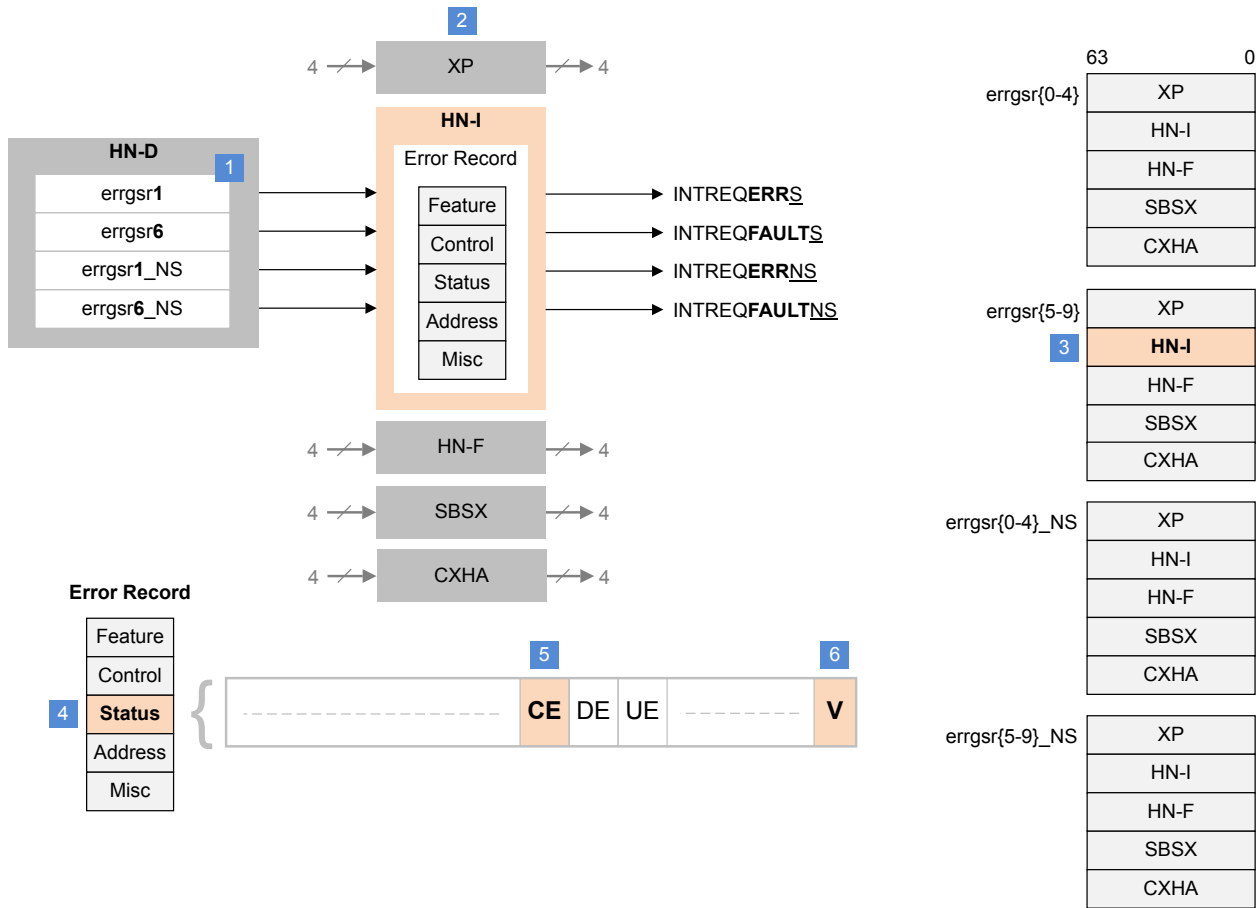


Figure 2-24 Error interrupt handler flow example

This section contains the following subsections:

- [2.14.1 Error types on page 2-82.](#)
- [2.14.2 Error Detection and Deferred Error values on page 2-84.](#)
- [2.14.3 Error detection, signaling, and reporting on page 2-84.](#)
- [2.14.4 Error handling requirements on page 2-89.](#)
- [2.14.5 HN-F error handling on page 2-89.](#)
- [2.14.6 HN-I error handling on page 2-90.](#)
- [2.14.7 SBSX error handling on page 2-93.](#)
- [2.14.8 RN-I error handling on page 2-93.](#)
- [2.14.9 XP error handling on page 2-94.](#)
- [2.14.10 CXHA error handling on page 2-94.](#)
- [2.14.11 CCIX Protocol Error messaging support on page 2-94.](#)

2.14.1 Error types

CMN-600AE supports several error types.

The supported errors are:

- *Corrected Error (CE)*
- *Deferred Error (DE)*
- *Uncorrected Error (UE)*

Note

CEs, DEs, and UEs can occur simultaneously.

There might be cases when an error occurs and sets the status register, but the interrupt reporting is not enabled. For other cases where the interrupt asserts, the interrupt request is generated immediately when enabled. Otherwise, if interrupt reporting is disabled, any interrupt is cleared and the error remains logged with UE, DE, and CE.

Note

If both ERRCTLR.UI (uncorrected interrupt) and ERRCTLR.FI (fault interrupt) are set and a UE occurs, both fault and error interrupts are delivered from CMN-600AE.

Correctable Errors

These errors can be corrected using *Error Correcting Code* (ECC) or other methods. They include:

- A single-bit ECC error
- An error that is recovered by replaying the transaction in the pipeline

The system handles these errors by completing the following steps:

1. Detects the error and increments the ERRMISC.CEC counter. Sets ERRSTATUS.AV and ERRSTATUS.MV. Logs the attributes in the ERRADDR and ERRMISC registers.
2. If CEC counter overflowed, the system updates ERRSTATUS.V and ERRSTATUS.CE, and sets ERRMISC.CECOF.
3. Masks signaling of the error to the *RAS Control Block* (RCB) using ERRCTLR.CFI.
4. If there are multiple CEC overflows, then the system sets ERRSTATUS.OF.

Deferred Errors

These errors are UEs that have the following properties:

- Detected in one node of CMN-600AE, but the data is not used within the same node
- Poison bits are set for the data

The errors can be either fatal or non-fatal errors as described in this section. These errors are not correctable, but the system can operate for a time without being corrupted. These errors can be contained and the system might be able to recover through software intervention. They include:

- A data double bit ECC error in the SLC Data RAM
- Data check error detected in SLC

The system handles these errors by completing the following steps:

1. Logs the error information in the applicable ERRSTATUS, ERRADDR, and ERRMISC registers.
2. Sets ERRSTATUS.V and ERRSTATUS.DE.
3. Masks signaling of the error to the RAS control block using ERRCTLR.FI and ERRCTLR.UI.
4. If there are multiple DEs, then the system sets ERRSTATUS.OF.

Uncorrectable Fatal Errors

These errors are in the control logic at a node. Continuing operation might corrupt the system beyond recovery. They include:

- A double-bit ECC error in SLC tag
- Flit parity error
- *Non-data Error* (NDE) in a response packet

The system handles these errors by completing the following steps:

1. Logs the error information in the applicable ERRSTATUS, ERRADDR, and ERRMISC registers.
2. Sets ERRSTATUS.V and ERRSTATUS.UE.
3. Masks signaling of the error to the RAS control block using ERRCTL.R.UI.
4. If there are multiple UEs, then the system sets ERRSTATUS.OF.

A component might not respond to further messages after an error is signaled. In this case, for the error handling routine to be successful, the component must still respond to configuration access requests from the configuration bus.

CMN-600AE follows the *Arm® Reliability, Availability, and Serviceability (RAS) Specification Armv8, for the Armv8-A architecture profile* for mapping of the different error types to the type of interrupt. The following table summarizes the mapping of various error types to the interrupt type.

Table 2-13 Mapping of error types

Interrupt type	Error type		
	Uncorrected Error	Detected Error	Corrected Error
Fault Handling Interrupt	Yes (if ERRCTL.R.FI==1)	Yes (if ERRCTL.R.FI==1)	Yes (if ERRCTL.R.CFI==1)
Error Recovery Interrupt	Yes (if ERRCTL.R.UI==1)	No	No

2.14.2 Error Detection and Deferred Error values

For XP, the default values of *Error Detection* (ED) and DE depend on build time parameters.

Only the HN-F has CE counters that are implemented in the ERRMISC register. The default values of UI, FI, and CFI are 2'b10, which enables control for the interrupt generation. The following table contains default values of ED and DE for XP.

Table 2-14 Default values of ED and DE for XP

POR_FLIT_PAR_EN	POR_DATACHECK_EN	MXP_DEV_DATACHECK_EN		ED	DE
		P0	P1		
0	0	0	0	2'b00	2'b00

For SBSX, if the AXDATAPOISON_EN parameter is not set, the default values of ED and DE are 2'b01. If the parameter is set, the default values are 2'b00.

For HN-I and HN-F, the default values of ED and DE are always 2'b01.

All fields are required, even though only HN-F has CE counters that are implemented in ERRMISC.

The default values of UI, FI, and CFI must be 2'b10, indicating that the interrupt generation is controllable.

2.14.3 Error detection, signaling, and reporting

Each CMN-600AE component that is connected to a configuration bus can be included in the local error reporting mechanism.

The error handling protocol is as follows:

- Error overflow
- ERRSTATUS.OF value after errors
- ERRMISC fields and register bits

Error overflow

The overflow is set when different types of errors are detected. It is also asserted when multiple errors of equal priority are detected.

0b1 More than one error has been detected.

0b0 Only one error of the most significant type that ERRSTATUS.{UE, CE, DE} describes has been detected.

This bit is read/write-one-to-clear.

Note

ERRSTATUS.OF is only for the highest priority error. For example, if another DE follows the first DE, ERRSTATUS.OF is set. When the next UE happens, ERRSTATUS.OF is cleared. ERRSTATUS.OF is cleared because UE is the highest priority error in the system, and is the first occurrence of UE.

The following table shows the value of ERRSTATUS.OF after errors occur at t0, t1, and t2.

Table 2-15 ERRSTATUS.OF value after errors

Error at			Status of OF after error		
t0	t1	t2	t0	t1	t2
CE	CE	CE	0	1	1
CE	CE	DE	0	1	0
CE	CE	UE	0	1	0
CE	DE	CE	0	0	0
CE	DE	DE	0	0	1
CE	DE	UE	0	0	0
CE	UE	CE	0	0	0
CE	UE	DE	0	0	0
CE	UE	UE	0	0	1
DE	CE	CE	0	0	0
DE	CE	DE	0	0	1
DE	CE	UE	0	0	0
DE	DE	CE	0	1	1
DE	DE	DE	0	1	1
DE	DE	UE	0	1	0
DE	UE	CE	0	0	0
DE	UE	DE	0	0	0
DE	UE	UE	0	0	1
UE	CE	CE	0	0	0

Table 2-15 ERRSTATUS.OF value after errors (continued)

Error at			Status of OF after error		
t0	t1	t2	t0	t1	t2
UE	CE	DE	0	0	0
UE	CE	UE	0	0	1
UE	DE	CE	0	0	0
UE	DE	DE	0	0	0
UE	DE	UE	0	0	1
UE	UE	CE	0	1	1
UE	UE	DE	0	1	1
UE	UE	UE	0	1	1

ERRMISC fields

ERRMISC is the Secondary Error Syndrome Register. The fields of this register differ for ECC, parity, and other errors. The following table summarizes the valid fields for each unit.

Table 2-16 ERRMISC register bit mapping for error reporting units

Bit	Component						
	XP	HN-I	HN-F	SBSX	CXHA		
63	-	-	CECOF	-	-		
62			SETMATCH				
61			-				
60			ERRSET[12:0]				
59							
58	TGTID[10:0]	LPID[4:0]			ERRSET[7:0]		
57							
56							
55							
54							
53							
52							
51	-						
50							
49	ORDER[1:0]						
48							
47	-	-			CEC[15:0]	-	-
46							
45							
44							
43							
42							
41							
40							
39							
38							
37							
36							
35							
34							
33							
32							

Table 2-16 ERRMISC register bit mapping for error reporting units (continued)

Bit	Component						
	XP	HN-I	HN-F	SBSX	CXHA		
31	-	-	-	-	-		
30		SIZE[2:0]		SIZE[2:0]			
29							
28							
27						MEMATTR[3:0]	MEMATTR[3:0]
26							
25							
24							
23		-		-			
22							
21						OPCODE[5:0]	OPCODE[5:0]
20							
19							
18							
17	OPTYPE[1:0]	OPTYPE					
16							
15	-	-	-	-			
14	SRCID[10:0]	SRCID[10:0]	SRCID[10:0]	SRCID[10:0]	SRCRAID[5:0]		
13							
12							
11							
10							
9							
8							
7							
6							
5							
4							
3						-	ERRSRC[3:0]
2	ERRSRC[2:0]						
1							
0							

Error log clearing

In addition to the Error Syndrome Registers, each component has a write-only Error Syndrome Clear Register. Write the applicable mask bits to clear the `first_err_vld` and `mult_err` bits of the Error Syndrome 0 Register.

2.14.4 Error handling requirements

This section describes the specific error handling behaviors of CMN-600AE.

Error reporting rules

CMN-600AE uses specific error reporting rules, concerning which errors must be reported and propagated.

The rules regarding error reporting in CMN-600AE are:

- Any error originating in CMN-600AE is reported
- Any error originating outside CMN-600AE but corrupting CMN-600AE is reported
- If a response packet from outside CMN-600AE does not propagate the response any further, the HN-I can report an error in the response packet
- All non-posted write errors are propagated where possible

2.14.5 HN-F error handling

Errors are reported at the HN-F for various reasons.

The HN-F detects:

- ECC errors in SF Tag, SLC Tag, and Data RAMs.
- Data check and poison errors on DAT flits.
- *Non-data Errors* (NDEs) on responses.

ECC errors in SF Tag, SLC Tag, and Data RAMs

HN-F detects single-bit and double-bit ECC errors in the SF Tag, SLC Tag, and Data RAMs. It can correct single-bit ECC errors. Such errors are logged and reported as CEs.

The source of the double-bit ECC errors determines how they are handled.

SLC Data RAM

- Logged and reported as DEs.
- Propagated to the data consumer in the form of data poison.

SF Tag RAM

- Logged and reported as DEs.
- Not propagated to the requestor.
- The SF Tag RAM in the HN-F is disabled following the first occurrence of the double-bit ECC error.

SLC Tag RAM

- Fatal error.
- Logged and reported as UEs.
- Propagated to the requestor as NDEs in the responses.

Poison errors on DAT flits

If the HN-F allocates data, then it detects poison errors on the data flits.

If `por_hnf_aux_ctl.hnf_poison_intr_en == 1`, then the poison errors originating from HN-F are logged and reported as UEs.

NDEs on responses

HN-F can receive NDEs from other data and response sources such as RN-F, RN-I, and SN-F. If the cache line was allocated in SLC Data RAM, it is logged and reported as a UE. If the cache line is not allocated in HN-F SLC, it propagates the errors to the requestor as an NDE.

MPU access violations

HN-F can detect address access violations from an RN through a read or write request. It logs the requestor information in the `por_hnf_erraddr(_NS)` and `por_hnf_errmisc(_NS)` error logging registers. These access violations are also logged as UEs in the `por_hnf_errstatus(_NS)` registers.

In addition to logging the errors, HN-F always reports NDE in the responses to coherent requests. For non-coherent operations where `BUS_ERROR` was requested, HN-F reports NDE on responses.

HN-F can also detect MPU access violations through Snoop responses, which prevents any data intervention from an RN with insufficient access permissions.

2.14.6 HN-I error handling

Errors are reported at the HN-I for various reasons.

Request errors at HN-I

The HN-I detects errors on receiving various request types and sends an NDE response to the requesting RN.

The HN-I logs request information in the error logging registers, `por_hni_erraddr(_NS)` and `por_hni_errmisc(_NS)`. They are marked as DEs in the error status register, `por_hni_errstatus(_NS)`. The HN-I detects errors on receiving the following request types:

- Coherent Read
- CleanUnique/MakeUnique
- Coherent/CopyBack Write
- Atomic
- Illegal Configuration Read or Write, HN-D only

The `reqerr_cohreq_en` configuration bit in the `por_hni_cfg_ctl` register enables or disables the sending of NDE responses and logging of error information for following request types. By default, this bit is enabled. It can only be programmed during boot time to any one of the following:

- Coherent Read
- CleanUnique/MakeUnique
- Coherent/CopyBack Write

The following table lists all the requests that an HN-I detects as errors and the support of `reqerr_cohreq_en`.

Table 2-17 HN-I request errors and support for configuration bit

Request type	Reqerr_cohreq_en controls sending of NDE and log error
Coherent Read	Yes
CleanUnique/MakeUnique	Yes
Coherent/CopyBack Write	Yes
Atomics	No
Illegal Configuration Read or Write	No

- Coherent reads are downgraded to ReadNoSnp and sent downstream, AXI or ACE-Lite slave
- Coherent and Copyback writes are downgraded to WriteNoSnp and sent downstream, AXI or ACE-Lite slave

- Illegal Configuration Read is sent as ReadNoSnp to downstream, AXI or ACE-Lite slave
- CleanUnique, MakeUnique, atomics, and Illegal Configuration Writes are handled within HN-I
- StashOnceShared, StashOnceUnique, and PrefetchTgt are completed within HN-I without any errors

Data Errors at HN-I

The HN-I only detects errors on write data if it does not detect an error on that request.

The following provides an overview of AXI and ACE-Lite write requests and configuration write requests, with no request error:

- For AXI and ACE-Lite write requests with no request error, when they receive Poison error on data, the HN-I detects the error. If downstream does not support poison, the HN-I logs the request information in `por_hni_erraddr(_NS)` and `por_hni_errmisc(_NS)`. The write requests are marked as UEs in the error status register, `por_hni_errstatus(_NS)`.
- For configuration write requests with no request error, on receiving write data with Partial ByteEnable error, Data check error, or Poison, HN-I detects and sends an NDE response to the requesting RN. It logs the SrcID and TxnID of the request and drops the write. They are marked as DEs in the error status register, `por_hni_errstatus(_NS)`.

————— **Note** —————

StashOnceShared, StashOnceUnique, and PrefetchTgt are completed within HN-I without any errors.

Response Errors at HN-I

The HN-I only detects errors on write response if it does not detect an error on that request.

To summarize:

- For AXI or ACE-Lite write requests with early completions from HN-I and no request error, HN-I detects the error when it receives the following error response types on the downstream write response (**BRESP**):
 - *Slave Error* (SLVERR)
 - *Decode Error* (DECERR)

HN-I logs request information in `por_hni_erraddr(_NS)` and `por_hni_errmisc(_NS)`. They are marked as UEs in the error status register, `por_hni_errstatus(_NS)`.

- For AXI or ACE-Lite write requests with downstream completions and no request error, SLVERR, or DECERR on downstream write response (**BRESP**) are passed on to the requesting RN as CHI DEs or NDEs
- For AXI or ACE-Lite read requests, SLVERR and Poison (if supported by downstream) are both converted to Poison within the CMN-600AE system. This conversion occurs independent of error on request. DECERRs on downstream read responses are passed on to the requesting RN.

Illegal MPU Access Errors

The HN-I detects errors for illegal MPU accesses.

It logs request information in the error logging registers, `por_hni_erraddr(_NS)` and `por_hni_errmisc(_NS)`. They are marked as UEs in the Error Status Register, `por_hni_errstatus(_NS)`.

The HN-I sends NDE if an illegal MPU access is detected and one of the following conditions is true:

- The request type is one of the following:
 - Coherent Read.
 - Coherent Write.
 - CleanUnique/MakeUnique.
 - StashOnce*.
 - Atomic.
- BUS_ERROR is requested for all other Ops.

The error is logged if an illegal MPU access is detected and `por_hni_aux_ctl.disable_mpu_err_logging` is set to 0.

HN-I summary on sending NDE and DE

The HN-I sends NDE scenarios for certain situations.

The HN-I sends NDE in the following cases:

- Request Error:
 - Coherent Read, if `reqerr_cohreq_en` is set to 1
 - CleanUnique/MakeUnique, if `reqerr_cohreq_en` is set to 1
 - Coherent/CopyBack Write, if `reqerr_cohreq_en` is set to 1
 - Atomic
 - Illegal Configuration Read or Write, HN-D only

————— **Note** —————

For the legal format of configuration read/write request, refer to [4.1.5 Requirements of configuration register reads and writes on page 4-190](#).

- Write Data Error for Configuration Write request, HN-D only:
 - Partial ByteEnable Error
 - Data Check Error
 - Poison
- AXI or ACE-Lite Response Error:
 - DECERR on *downstream write response*, **BRESP**, for writes with downstream completions
 - DECERR on *downstream read response*, **RRESP**
- Illegal MPU Access Error:
 - Coherent Read
 - Coherent Write
 - CleanUnique
 - MakeUnique
 - StashOnce*
 - Atomic

————— **Note** —————

The HN-I sends NDE regardless of whether `BUS_ERROR` was requested.

The HN-I sends DE in the following cases:

- AXI or ACE-Lite Response Error:
 - SLVERR on **BRESP** for writes with downstream completions

HN-I summary on logging errors

The HN-I logs an error as deferred or uncorrected in certain conditions.

The HN-I logs errors for all illegal MPU accesses detected. To disable this behavior, set `por_hni_aux_ctl.disable_mpu_err_logging` to 0.

Deferred Errors

The HN-I logs an error as deferred in the following cases:

- Request error:
 - Coherent Read, if `reqerr_cohreq_en` is set to 1
 - CleanUnique/MakeUnique, if `reqerr_cohreq_en` is set to 1
 - Coherent/CopyBack Write, if `reqerr_cohreq_en` is set to 1

- Atomic
- Illegal Configuration Read or Write

————— **Note** —————

For the legal format of a Configuration Read or Write request, see [4.1.5 Requirements of configuration register reads and writes on page 4-190](#).

- Write Data Error for Configuration Write request:
 - Partial ByteEnable Error
 - Data Check Error
 - Poison Error

Uncorrected Errors

The HN-I logs an error as uncorrected in the following cases:

- Write Data Error for AXI or ACE-Lite write requests:
 - Poison Error on data if downstream does not support poison
- AXI or ACE-Lite Write Response Error:
 - SLVERR or DECERR on BRESP for writes that were sent early completions

CML configuration with HN-I

In CML configuration, HN-I must be configured to report NDE response on coherent requests.

This requirement is met by setting `por_hni_cfg_ctl.reqerr_cohreq_en`. This action is required in CML mode so that NDE error responses are not missed on CCIX because of early completion responses from the CXG block.

2.14.7 SBSX error handling

This section describes how errors are handled at the SBSX.

If the following circumstances are both true, then the SBSX detects and logs errors:

- The AXI memory controller downstream of SBSX does not support POISON, indicated by `por_sbsx_unit_info.axdata_poison_en = 0`
- CHI Write Data has Poison set

If `por_sbsx_cfg_ctl.sbsx_rpt_err_on_poison_rd = 1`, and if SBSX receives Poison on read data from downstream, then SBSX detects and logs this error.

————— **Note** —————

SBSX does not have opcode-based Request and Response Error class as does HN-I.

The following table shows the SBSX summary on sending an NDE or DE.

Table 2-18 SBSX summary on sending NDE or DE

Case number	Source of error	SBSX error response
1	Decode Error on RDATA from AXI side	NDE on COMP_DATA on CHIE side
2	Slave Error on RDATA from AXI side	Poison on COMP_DATA on CHIE side
3	Decode Error on BRESP from AXI side	NDE on COMP for CMOs or Writes with EWA = 0
4	Slave Error on BRESP from AXI side	DE on COMP for CMOs or Writes with EWA = 0

2.14.8 RN-I error handling

RN-I does not report any RAS errors.

Coherent transactions that are received at RN-I from AXI and ACE-Lite masters which are targeted for HN-I are downgraded to non-coherent transactions. For example:

- ReadOnce is downgraded to ReadNoSnp
- WriteUnique is downgraded to WriteNoSnp

2.14.9 XP error handling

The XP does not report any RAS errors.

2.14.10 CXHA error handling

Errors are reported at the CXHA for various reasons.

CXHA uses RAMs as buffers for storing the Read and Write data. The contents of the RAM are protected using byte parity. CXHA reports errors if there is an error that is detected when the contents of the Data RAMs are read. These detected errors are of two types:

- Parity error on *Byte-Enable* (BE) fields of the Write Data RAM
- Parity error on Data and Poison fields of the Read and Write Data RAM

Parity error on BE fields of the Write Data RAM

The Write Data buffer RAM stores BE. Parity errors that are detected on BE are treated as UEs. On detecting an error, CXHA does the following:

- Logs the error as UE

Parity error on Data and Poison fields of the Read and Write Data RAM

The Read and Write data buffer RAMs contain the Data and Poison fields. Errors that are detected on these fields are treated as DEs. If an error is detected on Data fields, then the CXHA does the following:

- Logs the error as DE
- Poisons the data by setting the corresponding poison bit of the data. For more information about data poisoning, see the *Arm® AMBA® 5 CHI Architecture Specification*.

If an error is detected on Poison fields, then the CXHA does the following:

- Logs the error as DE
- All Poison bits are set to 1

2.14.11 CCIX Protocol Error messaging support

CMN-600AE CML supports sending of CCIX *Protocol Error* (PER) message to the CCIX Error Agent present on the Host chip.

CMN-600AE includes configuration registers, present in CXLA, and a mechanism to trigger a CCIX PER message. It is expected that an external Error Aggregator/Handler present outside CMN-600AE collects and consolidates all the errors and uses these registers to trigger a CCIX PER message to the CCIX Error Agent.

CXLA Configuration Registers:

- CCIX PER Message Payload:
 - por_cxla_permmsg_pyld_0_63
 - por_cxla_permmsg_pyld_64_127
 - por_cxla_permmsg_pyld_128_191
 - por_cxla_permmsg_pyld_192_255
- CCIX PER Message Control:
 - por_cxla_permmsg_ctl
- CCIX Error Agent ID:
 - por_cxla_err_agent_id

Mechanism:

- Error Aggregator external to CMN-600AE:
 - Writes the PER payload in CCIX PER Message Payload registers, `por_cxla_permsg_pyld_*`
 - Sets `per_msg_vld_set` bit in CCIX PER Message Control register, `por_cxla_permsg_ctl`. When set, a PER message is sent on the given CCIX link that is determined by the Target ID.

It is the responsibility of CCIX discovery software to program CCIX Error Agent ID in CCIX Error Agent ID `por_cxla_err_agent_id` register. This programming should happen during initial system bring up and the programmed ID is used as the target ID on CCIX PER message.

By default, *Error SourceID* (ESID) field from PER message payload, bits [53:48], are used as source ID on PER message. `per_msg_srcid_ovrd` and `per_msg_srcid` fields in CCIX PER message control register, `por_cxla_permsg_ctl`, can be used to override source ID sent on PER message.

———— **Note** ————

CMN-600AE CML does not implement a CCIX Error Agent. It can accept the incoming PER messages, but these messages are dropped at CXLA.

—————

2.15 CCIX Port Aggregation Groups

The CMN-600AE CML configuration supports up to two CXGs. These CXGs can be grouped into one *CCIX Port Aggregation Group* (CPAG).

This feature can be used when connecting two chips together with multiple ports between the chips. For example, the following figure shows two chips that are connected by two CXGs that are grouped into one CPAG.

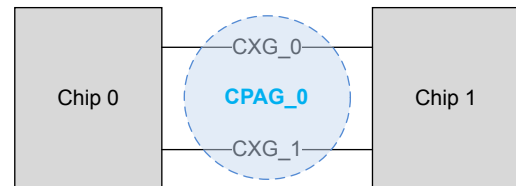


Figure 2-25 CCIX Port Aggregation Groups

To enable CPAG, both RN SAM and HN-F registers must be programmed accordingly in each chip.

2.16 System Address Map

Every master that is connected to CMN-600AE has the same view of memory.

The entire addressable space can be partitioned into subregions, and each partition must be designated as one of the following:

- I/O space. HN-I, HN-D, and HN-T service requests to I/O space.
- DDR space. HN-F, SN-F, and SBSX service requests to DDR space.

Note

Unmapped addresses are routed to the HN-D.

Each HN-F covers a mutually exclusive portion of the system address space. The options and constraints for HN-Fs are:

- Each HN-F can contain an SLC.
- HN-Fs can be combined into *System Cache Groups* (SCGs).
- Each HN-F in an SCG must have the same SLC partition size.
- An address hash function determines the target HN-F within an SCG.

All CHI transactions require a target ID to route packets from source to destination. For addressable requests, a *System Address Map* (SAM) determines the target ID. Each node that can generate a CHI addressable request contains a SAM:

RN SAM

Present in all RNs and CXHA nodes. Generates a target ID for requests to HN-F, HN-I, HN-D, HN-T, SBSX, and SN-F.

CXRA SAM

Present in all CXRA nodes. Generates a target ID for requests to CXHA nodes.

HN-F SAM

Present in all HN-Fs. Generates a target ID for requests to SN-F and SBSX.

HN-I SAM

Present in all HN-Is. Maps the address of the incoming CHI request to an I/O subregion for ordering purposes.

2.17 RN SAM

Transactions from an RN must pass through an RN SAM to generate a CHI target ID.

CMN-600AE RN-Is and CXHAs use an RN SAM that is internal to the interconnect.

CHI RN-Fs can use an RN SAM that is either internal or external to the interconnect. For CHI.A RN-Fs, there is a configuration option to instantiate a SAM that is internal to the interconnect. If this option is not selected, an external SAM must be created and integrated. It must be configurable without relying on the use of the CMN-600AE programmable register space. Arm does not provide such an external RN SAM for CHI.A masters.

This section contains the following subsections:

- [2.17.1 Target IDs on page 2-98.](#)
- [2.17.2 Memory region requirements on page 2-99.](#)
- [2.17.3 System Cache Groups on page 2-100.](#)
- [2.17.4 PrefetchTgt RN SAM on page 2-103.](#)

2.17.1 Target IDs

This section describes how the Default target ID, *Generic Interrupt Controller* (GIC) target ID, and DVM target ID are determined in CMN-600AE.

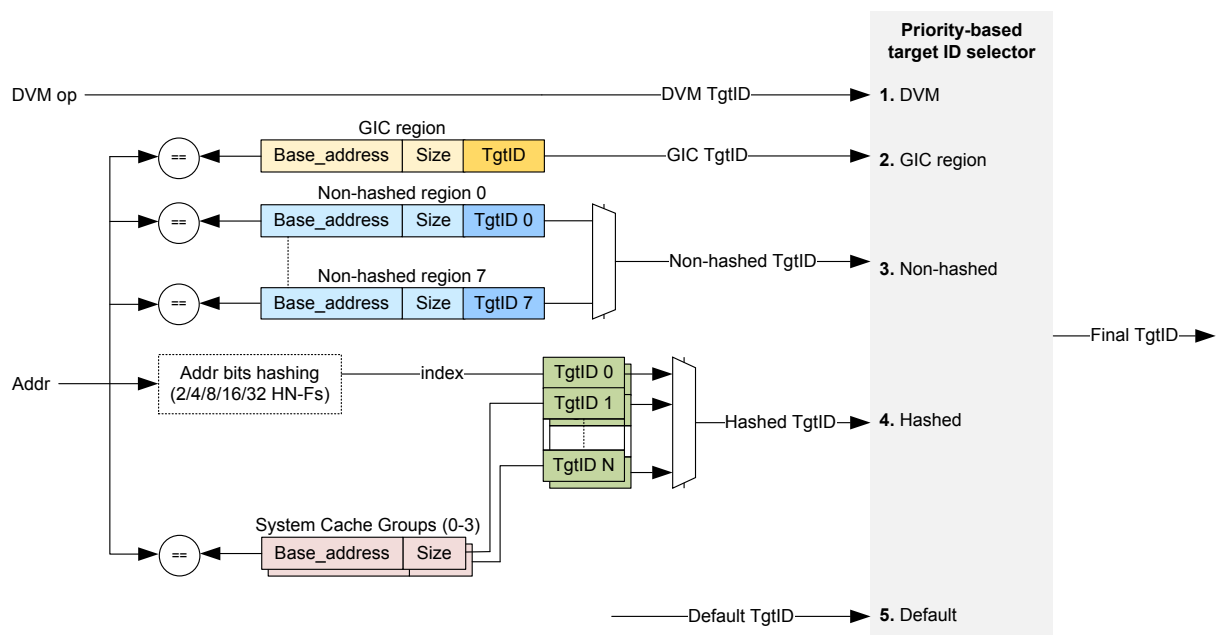


Figure 2-26 RN SAM target ID selection policy

Default target ID

Until the RN SAM has been fully programmed, all addressable transactions use the default target ID. RN SAMs that are internal to CMN-600AE define the HN-D node ID as their default target ID. RN SAMs that are external to CMN-600AE must be configured with a default target ID, which is programmable. When the RN SAM has been programmed, the default target ID is selected only for addressable requests that do not fall within one of the programmed address regions.

Hashed and non-hashed regions

A given memory partition can be either:

- Distributed (hashed) across many target devices
- Assigned to an individual device (non-hashed)

A hashed region can overlap with a non-hashed region. Whether a given region is configured as hashed or non-hashed affects the target ID selection policy for that address range. The SCG region registers support up to four hashed regions. The non-hashed region registers support up to eight non-hashed regions.

The I/O space (HN-I, HN-D, and HN-T) is intended to be the target of non-hashed regions. The DRAM space (HN-F), however, can be the target of either non-hashed or hashed regions. It is also possible to classify a region that only targets one HN-F as hashed. Extra configuration scenarios include:

- Using an SCG region register for an HN-I, HN-D, and HN-T target. This scenario might be useful if all the non-hashed region registers have already been used. The region can optionally be classified as a non-hashed region, except for SCG region 0.
- Using a non-hashed region register for an HN-F target. This scenario might be useful if all the SCG region registers have already been used. For target ID selection purposes, this HN-F is classified as a non-hashed region.

GIC target ID

RN SAMs also support a *Generic Interrupt Controller* (GIC) memory region which can be used to select GIC-related addresses to a specific target ID. The GIC region can overlap with hashed and non-hashed regions.

RN SAM target ID selection policy

RN SAMs support priority-based target ID selection. The order of priority is when selecting a target ID is:

1. GIC memory region, highest priority
2. Non-hashed memory region
3. Hashed memory region
4. Default memory region, lowest priority

DVM target ID

DVM transactions are assigned the DVM target ID. RN SAMs that are internal to CMN-600AE define the nodeID of the HN-D as the DVM target ID. RN SAMs that are external to CMN-600AE must be configured with a DVM target ID, which is programmable.

2.17.2 Memory region requirements

To set up the RN SAM, you must specify which of the memory region types are associated with specific memory ranges in your system memory map. You specify these regions in the RN SAM registers, and there are specific requirements for the regions.

Each of the programmed region sizes must be a power of two and the partition must be size-aligned. The region size can range from 64KB–256TB. For example, a 1GB partition must start at a 1GB-aligned boundary.

It is possible to support complex memory maps where DRAM region sizes are not a power of two or are not size-aligned. For example, the following figure shows a memory map where the entire address is assigned to a hashed region. Then, non-hashed regions can be individually programmed, because of their higher target ID selection priority. Software must prevent accesses to addresses in a hashed region that are not actually backed by physical memory. For more information, see the *Principles of Arm® Memory Maps White Paper*.

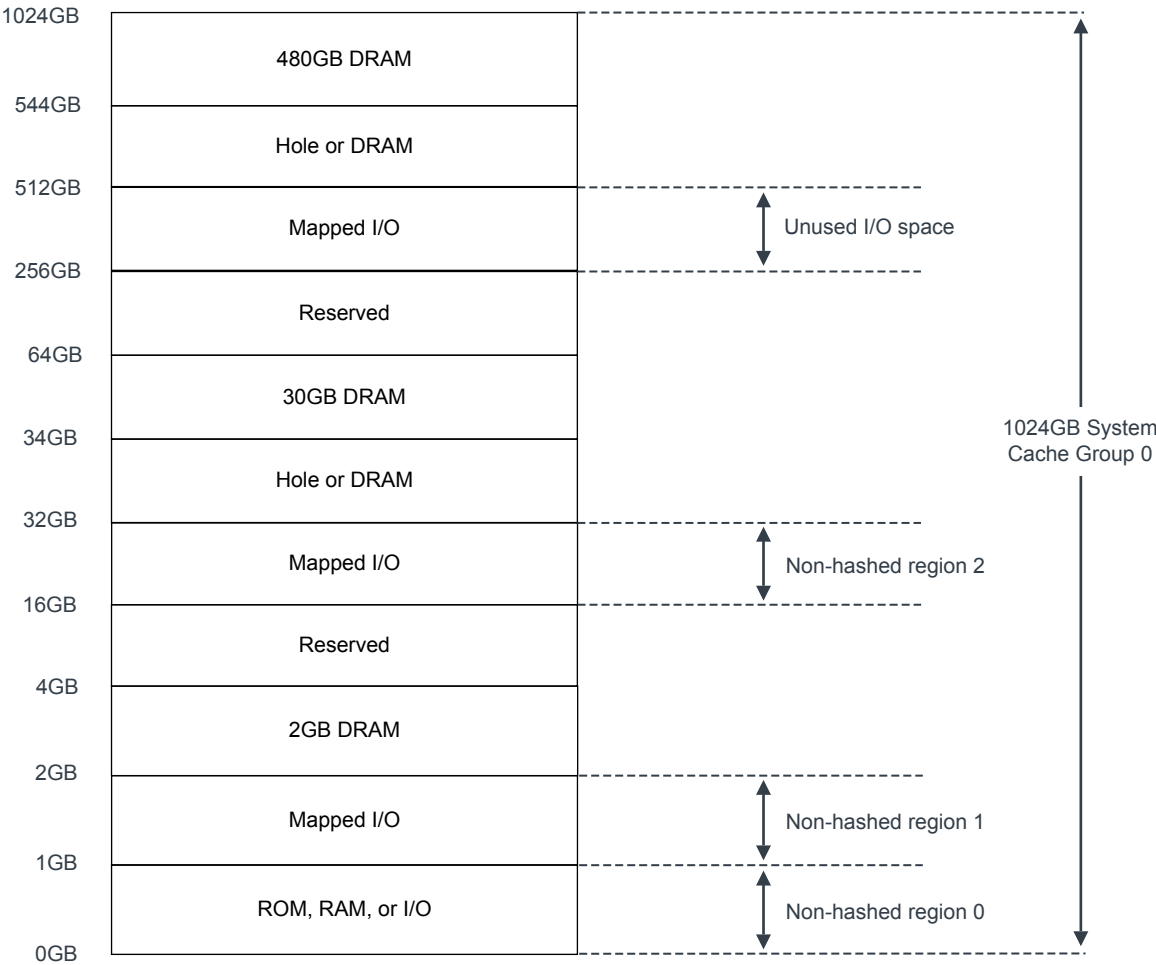


Figure 2-27 Example memory map

For more information about RN SAM configuration register memory partition sizes, see [2.20.2 SAM memory region size configuration on page 2-112](#).

2.17.3 System Cache Groups

A System cache Group is a group of HN-Fs that share a contiguous address region.

Although they share a contiguous address region, the addresses covered by each HN-F in an SCG are mutually exclusive. An HN-F belonging to an SCG is selected as the target based on a hash function.

An SGC supports hashing over one, two, four, eight, 16, or 32 HN-Fs. The hash function uses bits [MSB:6] of the physical address of the request. If CMN-600AE has been configured to implement fewer than 48 physical address bits, the unused upper bits are assumed to be zero. The hash algorithm calculates a pointer in the HN-F ID table in the RN SAM. The hash function is explicitly given below. All the numbers on the right-hand side of the equations below are bit positions within the physical address. For example, 17 corresponds to physical address bit [17]. In the equations, ^ represents XOR.

- Two HN-Fs

Number of bits in select: 1
select [0] = (6^7^8^...^47)
- Four HN-Fs

Number of bits in select: 2
select [0] = (6^8^10^...^46)
select [1] = (7^9^11^...^47)

Eight HN-Fs	Number of bits in select: 3 $\text{select}[0] = (6^9 12^{\dots} 45)$ $\text{select}[1] = (7^{10} 13^{\dots} 46)$ $\text{select}[2] = (8^{11} 14^{\dots} 47)$
16 HN-Fs	Number of bits in select: 4 $\text{select}[0] = (6^{10} 14^{\dots} 46)$ $\text{select}[1] = (7^{11} 15^{\dots} 47)$ $\text{select}[2] = (8^{12} 16^{\dots} 44)$ $\text{select}[3] = (9^{13} 17^{\dots} 45)$
32 HN-Fs	Number of bits in select: 5 $\text{select}[0] = (6^{11} 16^{\dots} 46)$ $\text{select}[1] = (7^{12} 17^{\dots} 47)$ $\text{select}[2] = (8^{13} 18^{\dots} 43)$ $\text{select}[3] = (9^{14} 19^{\dots} 44)$ $\text{select}[4] = (10^{15} 20^{\dots} 45)$

SCG configuration

Up to four SCGs are supported, depending on the number of HN-Fs in each SCG. The following table shows the restrictions on SCG selection.

Table 2-19 Permitted allocation of HN-Fs into SCGs

SCG	HN-F count					
	1	2	4	8	16	32
SCG0	Y	Y	Y	Y	Y	Y
SCG2	Y	Y	Y	Y	Y	N
SCG1	Y	Y	Y	Y	N	N
SCG3	Y	Y	Y	Y	N	N

The following table shows how hashed target IDs are programmed in each SCG. For example, if SCG0 has 32 HN-Fs, then it uses all the available node ID registers and other SCGs cannot be used. However, if SCG0 is only using 16 HN-Fs, then SCG2 and SCG3 can still be used with eight HN-F target IDs each. This table is also applicable to the SN-F target ID registers if PrefetchTgt is supported in the RN SAM.

Table 2-20 Target ID programming

Target ID Register (32 hashed targets)	Number of HN-Fs per SCG			
	32	16	8	4/2/1
scg_nodeid_reg0	SCG0_NIDs	SCG0_NIDs	SCG0_NIDs	SCG0_NIDs
scg_nodeid_reg1				-
scg_nodeid_reg2			SCG1_NIDs	SCG1_NIDs
scg_nodeid_reg3				-
scg_nodeid_reg4		SCG2_NIDs	SCG2_NIDs	SCG2_NIDs
scg_nodeid_reg5				-
scg_nodeid_reg6			SCG3_NIDs	SCG3_NIDs
scg_nodeid_reg7				-

Example 2-2 SCG configuration

The following table contains a mapping example of 25 HN-Fs to three SCGs.

Table 2-21 Mapping example for 25 HN-Fs and three SCGs

SCG	Number of HN-Fs	Node ID
SCG0	16	NID{0-15}
SCG2	8	NID{16-23}
SCG3	1	NID24

The following table contains a programming example for the 25 HN-Fs.

Table 2-22 Programming example for 25 HN-Fs

Target ID Registers	Number of HN-Fs per SCG			
	32	16	8	1
scg0_nodeid_reg0	-	SCG0 NID{0-15}	-	-
scg0_nodeid_reg1				
scg1_nodeid_reg0				
scg1_nodeid_reg1				
scg2_nodeid_reg0	-	-	SCG2 NID{16-23}	SCG3 NID24
scg2_nodeid_reg1				
scg3_nodeid_reg0			-	
scg3_nodeid_reg1			-	

2.17.4 PrefetchTgt RN SAM

The RN SAM supports CHI PrefetchTgt operations.

These operations are sent from RN-F directly to SN-F, bypassing the HN-F. To support such requests, the RN SAM integrates the functionality of HN-F SAM to determine the appropriate SN-F target ID for a given address. RN-Fs that integrate the PrefetchTgt RN SAM only use the SN-F target ID for PrefetchTgt requests. The PrefetchTgt RN SAM programming must match the HN-F SAM for SN-F target IDs.

The registers that are used for programming the PrefetchTgt RN SAM are:

- `por_rnsam_sys_cache_grp_sn_attr`
- `por_rnsam_sys_cache_grp_sn_nodeid_reg{0-7}`
- `por_rnsam_sys_cache_grp_sn_sam_cfg{0-1}`

2.18 CXRA SAM

All *CCIX Requesting Agents* (CXRA) in CMN-600AE require a *CCIX Requesting Agent System Address Map* (RA SAM) to determine the target *CCIX Home Agent ID* (HAID). This HAID is used as the target ID to route the CCIX request.

The RA SAM uses configuration registers to specify address regions and corresponding target HAIDs. You configure the address regions by programming the base address and corresponding size of the address region, or programming the address limit. Each valid address region is marked using a valid bit. The incoming address is compared against programmed valid address regions to generate a specific HAID.

The following figure shows a CCIX RA SAM block diagram.

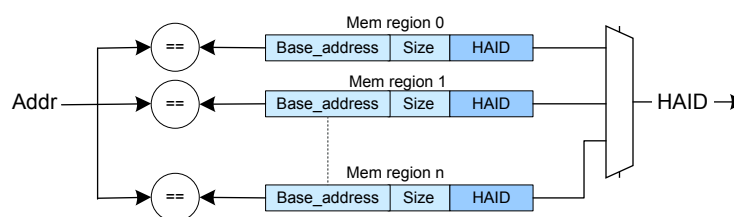


Figure 2-28 RA SAM block diagram

Address region requirements

Each of the programmed address region sizes must be a power of two and must be naturally-aligned to its size. For example, a 1GB partition must start at 1GB boundary. That is, 0GB-1GB or 1GB-2GB, and so forth, but it cannot start from 1.5GB or 2.5GB.

For information about how CCIX messages are routed based on the CXRA SAM programming, see [2.22 Cross chip routing and ID mapping](#) on page 2-127.

2.19 HN-F SAM

Transactions from an HN-F to an SN must pass through an HN-F SAM to generate a CHI target ID.

The following figure shows how the target ID is determined from the HN-F SAM.

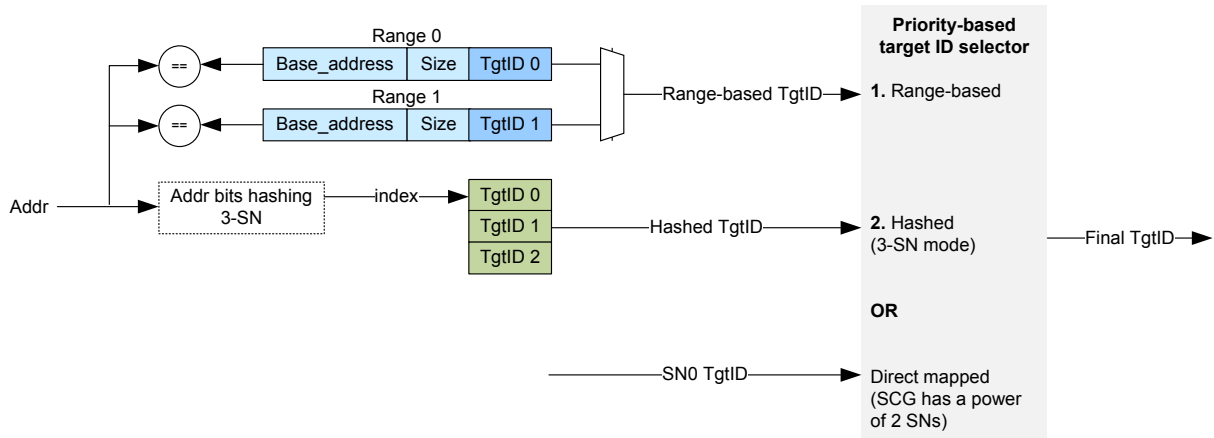


Figure 2-29 HN-F SAM target ID selection policy

As the preceding figure shows, the HN-F SAM has three mapping policies to generate target IDs for transactions:

- Range-based
- Hashed
- Direct mapping

An HN-F cannot use both hashed mapping mode and direct mapping mode. To map transactions that fall in the range-based part of the HN-F SAM, HN-F SAMs support priority-based target ID selection. The order of priority when selecting a target ID is:

1. Range-based mapping, highest priority
2. Striped target ID, 3-SN mode, or direct mapped target ID, SCG has a power of 2 SNs

Range-based mapping

Range-based mapping is an address-based target ID generation policy. Up to two address regions can be created, each targeting a single HN. This mode is useful where a partition of memory from the global DRAM is mapped explicitly to an individual SN, for example, an on-chip SRAM.

Hashed mapping

The HN-F SAM supports 3-SN address striping mode for SN target ID selection, which can only be used when the SCG targets three SNs. Addresses from a given HN-F are striped across three SNs.

Addresses within the address range of the SCG are striped at a 256B granularity between the selected SNs. The stripe function uses address bits [16:8], and an extra two user-defined address bits.

Direct mapping

Direct SN mapping is used if the SCG targets 1, 2, or 4 SNs. In this case, the transaction uses the SN0 target ID. Distributing accesses across the SNs targeted by the SCG is achieved by programming the SN0 field of each HN-F to the SN node ID it targets. For example, if an SCG with four HN-Fs targets four SNs, the SN0 field of each HN-F would be programmed with a different SN node ID. If that same SCG with four HN-Fs targets four SNs instead, every two HN-F nodes would have the same SN0 field value.

This section contains the following subsections:

- [2.19.1 HN-F SAM 3-SN memory striping mode on page 2-106.](#)
- [2.19.2 SN contiguous address spaces on page 2-109.](#)

2.19.1 HN-F SAM 3-SN memory striping mode

The CMN-600AE HN-F SAM supports 3-SN memory striping mode. In this mode, the HN-F SAM stripes addresses across three SN-Fs.

In 3-SN mode, a stripe function ensures that traffic is distributed evenly among the three SNs. The stripe function is based on PA[16:8] and two higher bits in the PA. The two higher PA bits are referred to as `top_address_bit1` and `top_address_bit0`. The top address bits are selected so that:

- Three of the four combinations of the top address bits appear evenly in the selected address space.
- The fourth combination never appears.

Note

In some situations, a top bit can be the inverse of the selected PA bit.

For each physical address, one of the three SNs is selected using the following formula:

$$SN = \{ ADDR[10:8] + ADDR[13:11] + ADDR[16:14] + ((top_addr_bit1 \ll 1) | top_addr_bit0) \} \% 3$$

General SN distribution behavior example

For a simple case with a 3GB flat address space starting at address `0x0`, `top_address_bit1` is PA[31], and `top_address_bit0` is PA[30]. With increasing physical address, the function steps between SNs at a 256-byte granularity. As the physical address iterates from 0-128KB, with `top_address_bit1` = `top_address_bit0` = 0, the first three terms distribute the traffic relatively evenly among the SNs. Of the 512 blocks (256B each) in the first 128KB, the distribution is:

SN[0]	170 blocks 33.2%
SN[1]	171 blocks 33.4%
SN[2]	171 blocks 33.4%

This pattern repeats over each 128KB until 1GB, where `top_address_bit0` toggles. With `top_address_bit1` = 0 and `top_address_bit0` = 1, the pattern is shifted. For each 128KB:

SN[0]	171 blocks 33.4%
SN[1]	170 blocks 33.2%
SN[2]	171 blocks 33.4%

At 2GB, when `top_address_bit1` = 1 and `top_address_bit0` = 0, the pattern shifts again:

SN[0]	171 blocks 33.4%
SN[1]	171 blocks 33.4%
SN[2]	170 blocks 33.2%

Over the full 3GB, the same number of lines are distributed to each SN.

The HN-F uses the `hn_cfg_three_sn_en` bit in its `por_hnf_sam_control` register to enable routing to three SNs. In the `por_hnf_sam_control` register, the `hn_cfg_sam_top_address_bit0` and `hn_cfg_sam_top_address_bit1` fields must be configured at boot time. These two address bits are decoded, and used with a hashing function to determine the target SN-F.

3-SN configurations

The valid top address bits for Arm PDD Memory Map are shown in the following table. For more information, refer to the *Principles of Arm® Memory Maps White Paper*. This configuration ensures equal distribution of requests across all SN-Fs and prevents memory aliasing. The SAM also provides an

inv_top_address_bit configuration bit, which can be used with top address bits as shown in the following table:

Table 2-23 3-SN mode top address bits [bit 1, bit 0]

Combination 1 (inv_top_address_bit set to 0b0)	Combination 2 (inv_top_address_bit set to 0b0)	Combination 3 (inv_top_address_bit set to 0b1)	Combination 4 (inv_top_address_bit set to 0b1)
[0, 0]	[1, 1]	[0, 0]	[0, 0]
[0, 1]	[0, 1]	[1, 0]	[0, 1]
[1, 0]	[1, 0]	[1, 1]	[1, 1]

Note

When inv_top_address_bit=1, it forces the SAM to invert the top most significant top address bit. For 3-SN mode, top_address_bit1 is inverted.

Example 2-3 Example for PDD memory map

Assume that a system supports three SN-Fs with 32GB of DRAM at each SN-F port and all three SN-Fs are used for SCG 0. Since the DRAM space is non-contiguous in this memory map (2GB + 30GB + 480GB), the base addresses for each DRAM partition are:

1. a. 000_8000_0000 to 000_FFFF_FFFF (2GB)
b. 008_8000_0000 to 00F_FFFF_FFFF (30GB)
2. 088_0000_0000 to 08F_FFFF_FFFF (32GB)
3. 090_0000_0000 to 097_FFFF_FFFF (32GB)

The first two regions together comprise a 32GB region, while the remaining two regions are 32GB each. The following table breaks down the address bits for the regions that are shown in the preceding list.

Table 2-24 Address region example bit settings: 3-SN example

Region	39	38	37	36	35	34	33	32	31
1	0	0	0	0	0	0	0	0	1
1	0	0	0	0	1	x	x	x	1
2	1	0	0	0	1	x	x	x	x
3	1	0	0	1	0	x	x	x	x

From the address bit breakdown, the selected top address bits must make sure both regions that are marked as Region 1 have the same values. This requirement ensures no aliasing in memory. For this memory map and DRAM size, there are no address bits that directly give Combination 1 or Combination 2 as shown in . However, if bits [39, 36] are used along with inv_top_address_bit = 1, then Combination 3 is possible. This approach ensures that the memory requests are equally distributed across the three SN-Fs without memory aliasing.

The following figure shows the Arm proposed memory map.

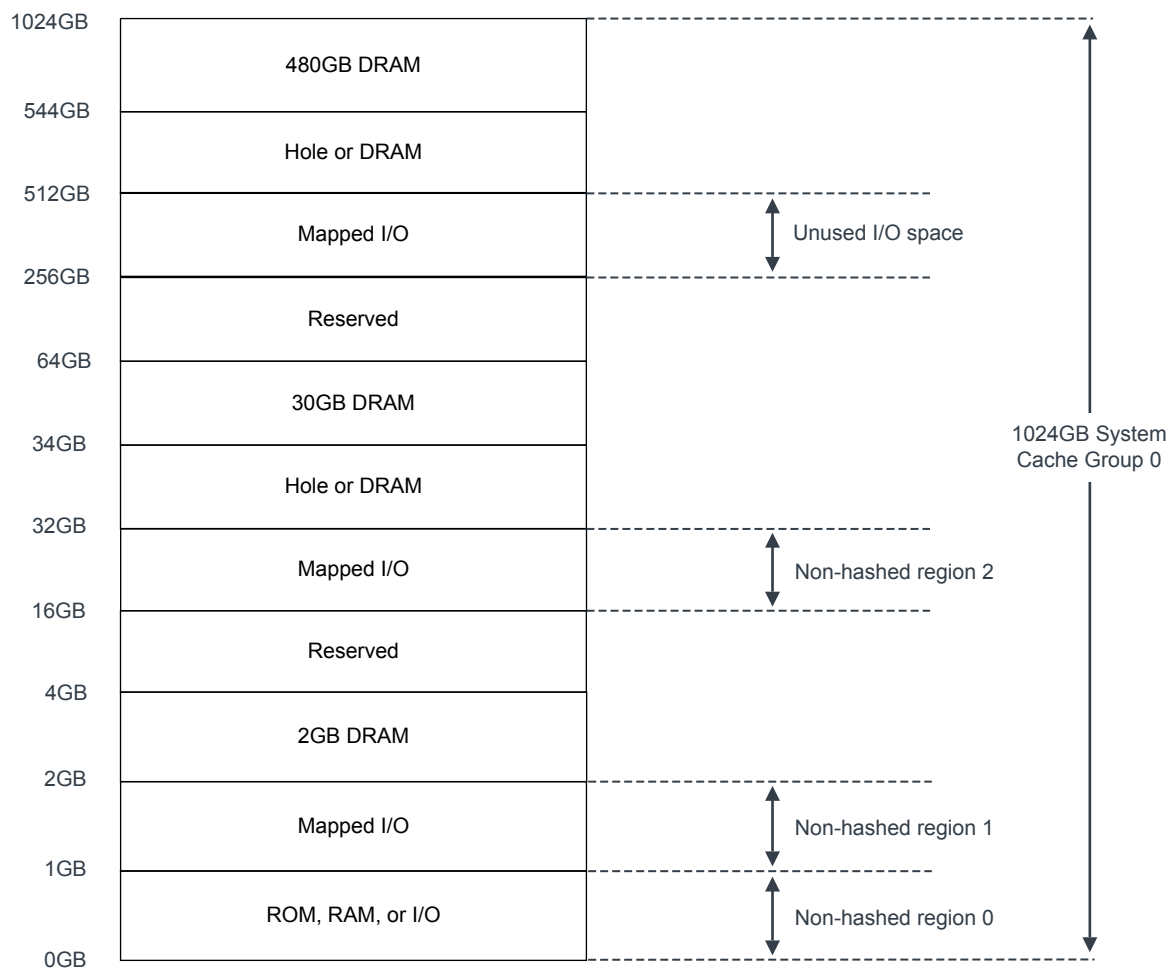


Figure 2-30 Example memory map programming

The following table provides example address bits that are known to provide equal distribution of memory across all SN-Fs in 3-SN mode.

Table 2-25 3-SN DRAM size settings

3-SN DRAM size at each SN-F port	Top address bits [bit 1, bit 0]	Inv_top_address_bit value
1GB (Total 3GB)	[35, 30]	0b0
2GB (Total 6GB)	[35, 31]	0b0
4GB (Total 12GB)	[33, 32]	0b0
8GB (Total 24GB)	[34, 33]	0b0
16GB (Total 48GB)	[39, 34]	0b0
32GB (Total 96GB)	[39, 36]	0b1
64GB (Total 192GB)	[37, 36]	0b0
128GB (Total 384GB)	[38, 37]	0b0

2.19.2 SN contiguous address spaces

This section describes which physical address bits must be connected to an SN-F for various configurations.

If all HN-Fs send their cache misses to a single SN-F, that SN-F sees the full address space. However, it is common for a system to have two or more SN-Fs, with each HN-F sending its cache misses to a single SN-F. In this scenario, each SN-F receives only part of the address space. SN-F typically removes one or more address bits to retain a contiguous address map. The full physical address is presented to each SN-F for every request so that any SN-F based memory protection logic can function. However, the actual mapping to RAM locations can be done with the modified address. The address modification depends on multiple factors:

- Number of HN-Fs in the cache group
- Number of SN-Fs in the cache group
- Which HN-Fs share SN-Fs

2ⁿ-SN address striping

The following table provides HN-F and SN-F combinations that are supported within a cache group, along with the address bits that should be removed.

Table 2-26 HN-F and SN-F combinations supported within a cache group

Number of HN-Fs	Number of SN-Fs	Bits to strip from full PA
2	1	None
	2	[6]
4	1	None
	2	[7]
	4	[7, 6]
8	1	None
	2	[8]
	4	[8, 7]

The method that is used to calculate the bits stripped is as follows:

1. The highest bit removed is the least significant address bit used in the XOR function for the most significant bit of the HN-F select hash function.

Eight HN-Fs	PA[8]
Four HN-Fs	PA[7]
Two HN-Fs	PA[6]

2. The number of bits stripped is $\log_2(\text{number of SN-Fs})$, sequentially below the highest bit.

This approach to bit stripping assumes that HN-Fs that share SN-Fs are sequential in the RN SAM cache group HN-F table. For example, if there are four HN-Fs and two SN-Fs, the bottom two HN-Fs in the RN SAM table would share an SN-F. The top two HN-Fs would share an SN-F.

3-SN address striping

3-SN address hashing mode implements a modulo function according to the top address bits used. Therefore, the SN-F must remove these bits, `top_address_bit1` and `top_address_bit0`, to achieve a contiguous memory map in the DRAM.

2.20 RN and HN-F SAM additional features and programming

This section describes the additional features that RN SAM and HN-F SAM support.

These features are:

- Secondary memory regions for each SCG
- Address bit masking for hashing and range comparison

Secondary memory regions for SCGs

Each SCG supports two memory regions. If the incoming address matches either of the two programmed valid regions, the RN SAM selects the target ID of the corresponding SCG from the target ID table.

Restriction

- Secondary memory region sizes must be size-aligned and a power of two
 - If the primary region for an SCG is set to non-hashed mode, the secondary region must also be set to non-hashed mode
-

Address bit masking

RN SAM supports masking of address bits that are used for range comparison and address hashing. To enable this support, program the `rnsam_hash_addr_mask_reg` and `rnsam_region_cmp_addr_mask_reg` registers.

When comparing the incoming address against the programmed ranges, RN SAM uses address bits:

- [47:26] for hashed and non-hashed memory regions
- [47:16] for GIC memory regions

To mask off the incoming address and the programmed address ranges before comparison, program the select bits in `rnsam_region_cmp_addr_mask_reg` to 0. This region mask is applied to hashed, non-hashed, and GIC memory regions.

RN SAM hashes all address bits [47:6] to equally distribute the requests across all target devices, HN-F and SN-F. To remove address bits from the hashing logic, program the select bits in `rnsam_hash_addr_mask_reg` to 0. This feature is only applicable to hashed memory regions.

HN-F SAM uses all address bits [47:26] when comparing the incoming address against the programmed ranges. To mask off the incoming address and the programmed address ranges before comparison, program the select bits in `hnf_sam_region_cmp_addr_mask_reg` to 0. This region mask is only applicable to region-based memory partitioning in the HN-F. Therefore the mask is not applied to the hashing scheme in 3-SN mode.

HN-F SAM supports masking of address bits used for 3-SN address hashing. To enable this feature, program the `hn_sam_hash_addr_mask_reg` register.

Restriction

- If 3-SN or mode is enabled, address bits [16:7] and the `top_addr_bits` are essential in distributing the addresses between memory. Arm recommends that these bits are masked carefully to avoid memory aliasing.
 - The range comparison mask cannot mask off bits that represent the size of the region. For example, if any region has a size of 64MB, address bit [26] cannot be masked. Similarly, if any region has a size of 512MB, address bit [29] cannot be masked.
 - The address bits masked in HN-F and RN SAM must be consistent. This consistency ensures that PrefetchTgt requests from an RN-F to SN-F are addressed by the same SN-F as an SLC miss from the HN-F to SN-F.
-

This section contains the following subsections:

- [2.20.1 Program the SAM on page 2-111.](#)
- [2.20.2 SAM memory region size configuration on page 2-112.](#)

- [2.20.3 Example memory map programming on page 2-114.](#)
- [2.20.4 Support for CCIX Port Aggregation on page 2-117.](#)

2.20.1 Program the SAM

The SAM must be programmed using a specific sequence. An RN-F or master that is connected to an RN-I must perform this sequence during the configuration of CMN-600AE at boot.

There are several configuration decisions that must be made when setting up the SAM. For more information, see the following sections:

- [2.17 RN SAM on page 2-98](#)
- [2.19 HN-F SAM on page 2-105](#)

Prerequisites

This sequence is part of the overall CMN-600AE boot configuration process. There are steps that must occur at boot-time before SAM programming. For more information about the full process, see [4.4.1 Boot-time programming sequence on page 4-1832.](#)

Procedure

1. Define the following memory map regions:
 - Hashed memory regions, which target HN-Fs. The hashed memory regions can be partitioned into SCGs, if applicable.
 - Non-hashed memory regions, which likely target HN-I or HN-D.
 - Non-hashed regions with HN-I or HN-D mapping. If a single HN-F is the target, HN-F can also be used in non-hashed mode.
 - GIC memory region, if present.
 - HN-F SAM memory regions, if applicable.
 - Mapping of HN-Fs to SN-Fs. This mapping can be direct, or 3-SN mode.
2. Ensure that the memory map meets the following requirements:
 - Non-hashed memory regions must not overlap.
 - Hashed memory regions must not overlap.
 - The memory regions must be size-aligned.
3. Program the following attributes and registers for each HN-F SAM:
 - a. Program the appropriate properties for each SN-F ID, according to the features that are supported in the `por_hnf_sam_sn_properties` register.
These properties provide the interface width as either 128-bit or 256-bit, CMO support, and PCMO support.
 - b. Program the HN-F to SN-F mapping, which depends on the mapping schemes that are used:
 - If the HN-F is directly mapped to an SN-F, program the SN0 target ID and corresponding attributes.
 - If the HN-F is in 3-SN mode, program the following:
 - All SN-F target IDs and the attributes for each SN-F.
 - The mode of operation as 3-SN.
 - The top address bits.
 - If the HN-F uses range-based SN-F partitioning for a particular memory region, program the memory region registers, including the target ID that is associated with each region.
4. Complete the following programming for the RN-F RN SAM:
 - a. Program the following attributes and registers for each SCG:
 - Memory region registers.
 - HN-F count registers.
 - HN-F target ID registers.
 - If PrefetchTgt operations are enabled:

- SN-F target ID registers for SCG.
 - SN-F target ID selection mode for SCG.
 - If 3-SN mode is enabled, program the top address bits.
 - b. Program the non-hashed memory region registers.
 - c. Program the non-hashed target ID registers.
 - d. Program the rnsam_status register to disable the default target ID mode.
5. Complete the following programming for each RN-I RN SAM and RN-D RN SAM:
- a. Program the following registers for each SCG:
 - Memory region registers.
 - HN-F count registers.
 - HN-F target ID registers.
 - b. Program the non-hashed memory region registers.
 - c. Program the non-hashed target ID registers.
 - d. Program the rnsam_status register to disable the default target ID mode.

2.20.2 SAM memory region size configuration

Hashed, non-hashed, and GIC memory regions support various sizes. Each memory partition must be individually programmed in the SAM registers.

RN SAM and HN-F SAM support the following memory partition sizes:

Hashed and non-hashed	64MB to maximum addressable space (2^{48}).
GIC	64KB, 128KB, 256KB, and 512KB.

The following table shows the memory partition size encodings to program the RN SAM and HN-F SAM registers.

Table 2-27 RN SAM and HN-F SAM configuration register memory partition sizes

Memory partition size		regionX_size value
GIC	Hashed and non-hashed	
64KB	64MB	5'b00000
128KB	128MB	5'b00001
256KB	256MB	5'b00010
512KB	512MB	5'b00011

Table 2-27 RN SAM and HN-F SAM configuration register memory partition sizes (continued)

Memory partition size		regionX_size value
GIC	Hashed and non-hashed	
N/A	1GB	5'b00100
	2GB	5'b00101
	4GB	5'b00110
	8GB	5'b00111
	16GB	5'b01000
	32GB	5'b01001
	64GB	5'b01010
	128GB	5'b01011
	256GB	5'b01100
	512GB	5'b01101
	1TB	5'b01110
	2TB	5'b01111
	4TB	5'b10000
	8TB	5'b10001
	16TB	5'b10010
	32TB	5'b10011
	64TB	5'b10100
	128TB	5'b10101
	256TB	5'b10110

The RN SAM also outputs the target type of the device along with the target ID for the RN to use in various optimizations. The target type encodings are listed in the following table.

Table 2-28 Device target types

Device type	Target type
HN-F	2'b00
HN-I	2'b01
CXRA	2'b10
Reserved	2'b11

The following table contains RA SAM configuration register memory partition sizes and encodings.

Table 2-29 RA SAM configuration register memory partition sizes

Memory partition size	regionX_size value
64KB	6'b000000
128KB	6'b000001
256KB	6'b000010
512KB	6'b000011

Table 2-29 RA SAM configuration register memory partition sizes (continued)

Memory partition size	regionX_size value
1MB	6'b000100
2MB	6'b000101
4MB	6'b000110
8MB	6'b000111
16MB	6'b001000
32MB	6'b001001
64MB	6'b001010
128MB	6'b001011
256MB	6'b001100
512MB	6'b001101
1GB	6'b001110
2GB	6'b001111
4GB	6'b010000
8GB	6'b010001
16GB	6'b010010
32GB	6'b010011
64GB	6'b010100
128GB	6'b010101
256GB	6'b010110
512GB	6'b010111
1TB	6'b011000
2TB	6'b011001
4TB	6'b011010
8TB	6'b011011
16TB	6'b011100
32TB	6'b011101
64TB	6'b011110
128TB	6'b011111
256TB	6'b100000

2.20.3 Example memory map programming

This section describes an example memory map and how to program it in the RN SAM and HN-F SAM.

The following figure shows an example memory map with 1024GB addressable size. It is based on the Arm 40-bit proposed address map. It has three separate DRAM regions (in the address ranges from 2-4GB, 34-64GB and 544-1024GB) and four I/O regions, which must be mapped to specific targets. It is assumed that the I/O region 256-512GB is unused and no requests are sent to this address.

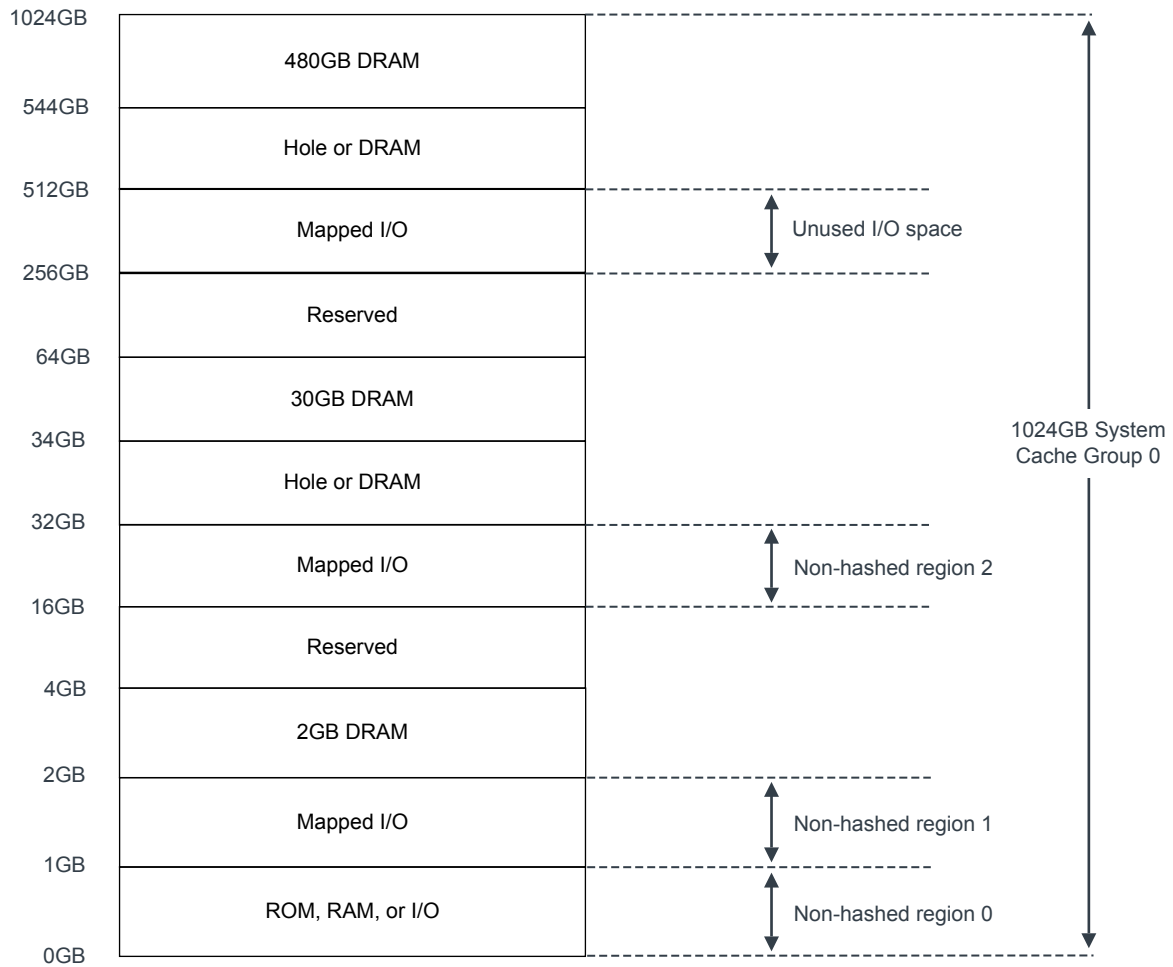


Figure 2-31 CMN-600AE example memory map

It is assumed that there are eight HN-Fs in the system and all HN-Fs are being used for one SCG (group 0). To program the RN SAM, follow these steps:

1. Map the full 1024GB memory map to the system cache group. Arm recommends this mapping because DRAM regions are non-contiguous and the entire DRAM space is assigned to one SCG.
2. Carve out each of the non-hashed regions from the full 1024GB memory map as shown in the preceding figure. Assign each non-hashed region to individual non-hashed targets.
3. When the RN SAM programming is done, turn ON the region-based target ID selection by disabling the default mode of the RN SAM.

The following table shows the RN SAM registers and the corresponding programmed values.

Table 2-30 RN SAM registers and programmed values

Register	Field	Value	Description
sys_cache_grp_region_reg0	region0_base_address	0x0_0000	Base address [47:26]
	region0_size	5'b01110	1024GB size
	region0_target_type	2'b00	HN-F target type
	region0_valid	1'b1	Region 0 is valid

Table 2-30 RN SAM registers and programmed values (continued)

Register	Field	Value	Description
sys_cache_grp0_nodeid_reg0	nodeid_0	<hnf0_node_id>	Physical node IDs of the HN-Fs in the system from HN-F 0 to HN-F 7
	nodeid_1	<hnf1_node_id>	
	nodeid_2	<hnf2_node_id>	
	nodeid_3	<hnf3_node_id>	
sys_cache_grp0_nodeid_reg1	nodeid_4	<hnf4_node_id>	
	nodeid_5	<hnf5_node_id>	
	nodeid_6	<hnf6_node_id>	
	nodeid_7	<hnf7_node_id>	
sys_cache_group_hnf_count	scg0_num_hnf	0x08	Total of eight HN-Fs in this system cache group
non_hash_mem_region_reg0	region0_base_address	0x0_0000	1GB from [47:26] 0x0_0000_0000
	region0_size	5'b00100	1GB size
	region0_target_type	2'b01	HN-I target type
	region0_valid	1'b1	Region 0 is valid
	region1_base_address	0x0_0010	1GB region from 0x0_4000_0000
	region1_size	5'b00100	1GB size
	region1_target_type	2'b01	HN-I target type
	region1_valid	1'b1	Region 1 is valid
non_hash_mem_region_reg1	region2_base_address	0x0_0100	16GB region from 0x4_0000_0000
	region2_size	5'b01000	16GB size
	region2_target_type	2'b01	HN-I target type
	region2_valid	1'b1	Region 2 is valid
non_hash_tgt_nodeid0	nodeid_0	<hni0_node_id>	Node ID of HN-I 0 corresponding to non-hashed region 0
	nodeid_1	<hni1_node_id>	Node ID of HN-I 1 corresponding to non-hashed region 1
	nodeid_2	<hni2_node_id>	Node ID of HN-I 2 corresponding to non-hashed region 2
rnsam_status	ninstall_req	1'b1	Uninstall any operations that are dependent on SAM programming.
	default_target	1'b0	Disable default mode and use the programmed ranges for new incoming addresses.

Similarly to RN SAM, HN-F SAM must also be programmed so that it can select the correct SN-F target ID. All HN-F SAMs within SCG 0 must have the same programming, as the following table shows, including the attributes of each SN-F.

Table 2-31 HN-F programming information

Register name	Field name	Value	Description
por_hnf_sam_control	hn_cfg_sn0_nodeid	<sn0_node_id>	Node ID of SN-F 0
	hn_cfg_sn1_nodeid	<sn1_node_id>	Node ID of SN-F 1
	hn_cfg_sn2_nodeid	<sn2_node_id>	Node ID of SN-F 2
	hn_cfg_three_sn_en	1'b1	Enable 3-SN mode.
	hn_cfg_sam_top_address_bit1	39	Bit 39 of address
	hn_cfg_sam_top_address_bit0	36	Bit 36 of address
	hn_cfg_sam_inv_top_address_bit	1'b1	Invert top address bit.

2.20.4 Support for CCIX Port Aggregation

RN SAM supports *CCIX Port Aggregation* (CPA).

Requests from an RN to a remote chip can be striped across multiple CCIX gateway blocks based on address bits. The following figure shows this functionality.

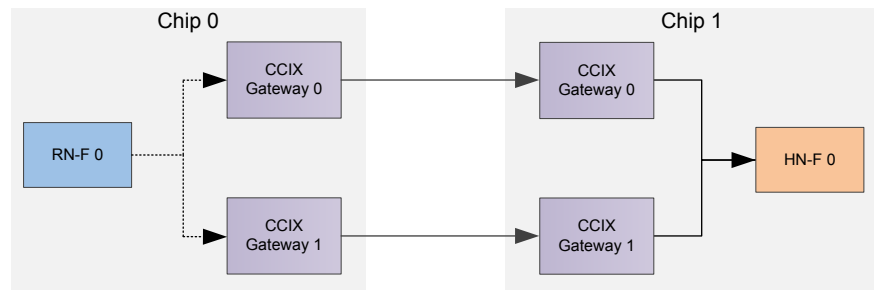


Figure 2-32 RN SAM CCIX Port Aggregation

This striping is achieved by hashing physical address bits[47:6]. The RN SAM CCIX can hash incoming addresses across two or four gateway blocks forming a *CCIX Port Aggregation Group* (CPAG). RN SAM can support up to two CPAGs. RN SAM also has an address mask for each CPA which can be used to remove certain bits from the hashing. For example, to stripe the incoming address at 512B granularity, the address mask bits[47:6] can be set to 0x3FFFFFFF8. With this mask setup, the logical operator AND is applied to all incoming addresses before hashing the address bits. For details on programming, see the RN SAM registers.

HN-F support for CPA

HN-F also supports CPA for snoop requests going to a remote chip. HN-F uses the same hashing as RN SAM so that a given address always goes to the same CCIX gateway block. HN-F uses the ID of the RN-F to determine if CPA is enabled. To enable CPA for the ID of each RN-F, refer to the logical to physical ID conversion registers in HN-F.

To determine if CPA is enabled, RN SAM uses the address ranges and HN-F SAM uses the logical ID of the RN-F. As explained in [2.22 Cross chip routing and ID mapping on page 2-127](#), HN-F contains the *Logical ID* (LDID) to physical node ID conversion table as shown in [2.22 Cross chip routing and ID mapping on page 2-127](#) in the Example Programming table. This table, along with the CHI node ID and valid fields, also contains remote, cpa_en, and cpa_grpid bits. By using these bits, HN-F can determine if the RN-F is enabled to use CPA, and sends the snoops through appropriate ports by hashing the address bits.

Guidelines for enabling CPA in RN SAM and HN-F

Certain rules apply when enabling the CPA in RN SAM and HN-F:

- The CPA is only applicable to SCG and non-hashed ranges.
- Each non-hashed memory range can be explicitly enabled to use CPA or use a single non-hashed target ID.
- The target ID of each SCG can be explicitly enabled to use CPA.
- The HN-F, when participating as a CPA target for traffic from a remote RN-F, must not receive non-CPA traffic from the same remote RN-F. In other words, an RN-F cannot send CPA and non-CPA traffic to the same remote HN-F.
- Each SCG in RN SAM can contain only one CPA group along with local HN-F target IDs.

2.21 HN-I SAM

To simplify mapping and ordering of downstream endpoint address space, the HN-I SAM maps an incoming address to a target endpoint that is connected downstream behind HN-I.

The endpoint can be one of the following:

- Peripheral with memory-mapped I/O space, such as UART or GPIO
- Physical memory, such as SRAM or FLASH

Restriction

Arm recommends that the HN-I SAM is only programmed during the boot process.

To map and order the address space of these endpoints, the HN-I SAM supports:

- Up to three Address Regions

Restriction

Address Regions 1, 2, and 3 must not overlap.

- One Order Region of configurable size for each Address Region
- A default Address Region, Address Region 0

Each Address Region can be programmed as either peripheral or physical memory.

Note

By default, each Address Region is mapped to peripheral memory.

Physical

- Follows normal memory ordering guarantees
- Order Region programming function output does not matter

Peripheral

- Follows device memory ordering guarantees
- These Address Regions can be further divided into smaller address spaces that are known as Order Regions. Device memory ordering guarantees are maintained within each Order Region.
- To enforce strict ordering for a specific Address Region, program its Order Region size to 6'b111111

Caution

An Address Region register must be disabled if the following are true:

- There is potential for new requests to fall into the Address Region register that is newly configured
 - These new requests require ordering regarding the existing outstanding requests
-

The minimum address granularity for Address Regions and Order Regions is 4KB. This size is equivalent to the minimum slave address space granularity in AXI and ACE-Lite. Therefore, the base address in the Address Region {1, 2, 3} Configuration Registers only includes bits [REQ_ADDR_WIDTH-1:12].

Address Region 0

By default, the entire address space of a given HN-I is mapped to Address Region 0. All transactions to this region are kept in order.

The default Order Region size in Address Region 0 is 6'b111111, which covers the entire HN-I address space. The Order Region size can also be configured to:

- 6'b100100 when REQ_ADDR_WIDTH==48
- 6'b100000 when REQ_ADDR_WIDTH==44

Address Region 0 is always valid. Therefore, the Address Region 0 Configuration Register does not define a Valid bit.

For more information, see [por_hni_sam_addrregion0_cfg](#) on page 4-614.

This section contains the following subsection:

- [2.21.1 HN-I SAM example configuration](#) on page 2-120.

2.21.1 HN-I SAM example configuration

This example system configuration for HN-I SAM uses three Address Regions and an Order Region within each Address Region.

The following figure shows the high-level configuration of the address space and the base addresses of each Address Region.

HN-I address space	Base address
Address Region 0 (Default Region)	
Address Region 3	0x0000_0020_0000
Address Region 0 (Default Region)	0x0000_0004_0000
Address Region 2	0x0000_0002_0000
Address Region 0 (Default Region)	0x0000_0000_4000
Address Region 1	0x0000_0000_2000
Address Region 0 (Default Region)	0x0000_0000_0000

Figure 2-33 HN-I address space example

Note

In each Address Region Configuration Register, the following bitfields use the default value:

- ser_all_wr
- ser_devne_wr
- pos_early_wr_comp_en
- pos_early_rdack_en

Address Region 0

The following figure shows the example configuration for Address Region 0.

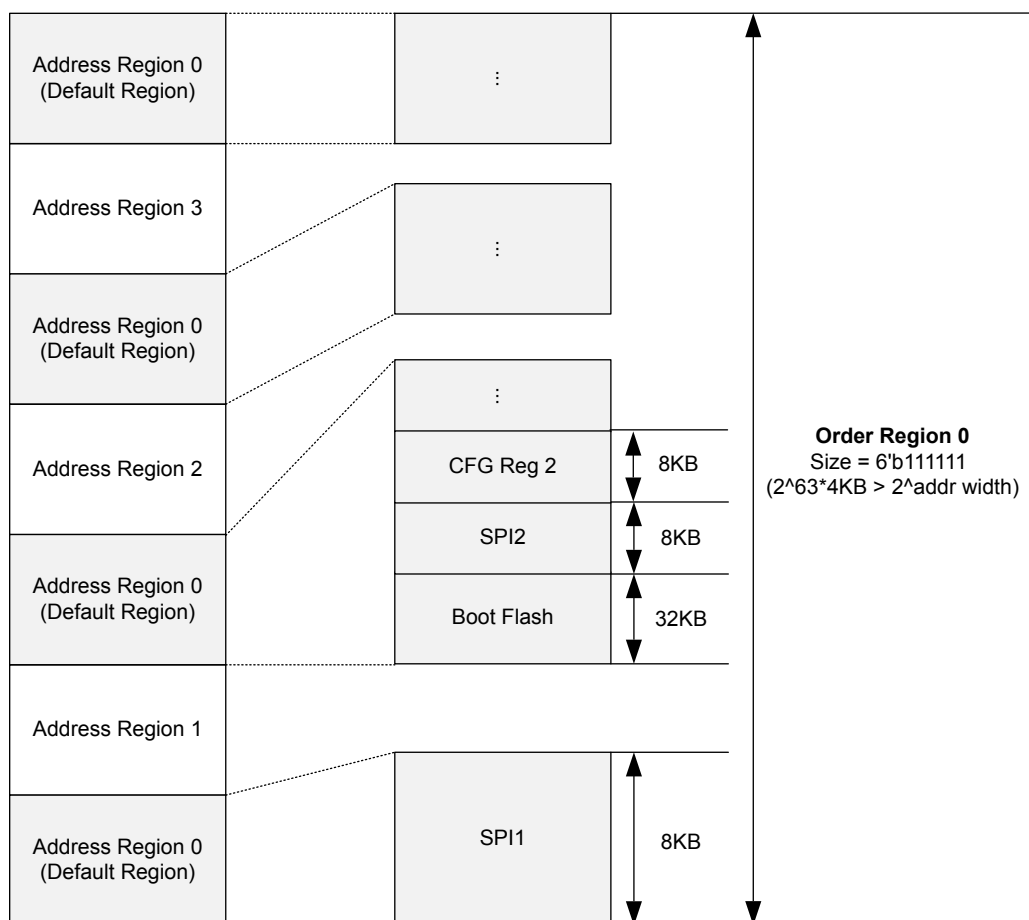


Figure 2-34 Address Region 0 configuration

The size of the maximum peripheral address space in Address Region 0 is 32KB (Boot Flash). Requests targeting this Boot Flash must be kept in order. By configuring the Order Region 0 size to 32KB, requests with addresses from 0x0000_0000_0000 to 0x0000_0000_8000 are ordered. However, since Boot Flash is not aligned to the 32KB boundary (0x0000_0000_4000 to 0x0000_0000_C000), requests might be out of order and cause issues. To ensure all requests to Boot Flash are ordered, the Order Region 0 size must be configured to at least 64KB. In this configuration, requests to SPI1, SPI2, and CFG Reg 2 are also ordered with respect to requests to Boot Flash. Instead, to optimize performance:

- Address Region 0 can have a SAM with Boot Flash aligned to the 32KB boundary.
- The Order Region 0 size can be configured to 32KB.

The following table shows the configured values for the Address Region 0 Configuration Register, `por_hni_sam_addrregion0_cfg`.

Table 2-32 Address Region 0 Configuration Register

Bits	Field name	Configured value
[5:0]	<code>order_reg_size</code>	6'h4
[58]	<code>physical_mem_en</code>	1'b0
[59]	<code>ser_all_wr</code>	1'b0
[60]	<code>ser_devne_wr</code>	1'b0
[61]	<code>pos_early_rdack_en</code>	1'b1
[62]	<code>pos_early_wr_comp_en</code>	1'b1

Address Region 1

The following figure shows the example configuration for Address Region 1.

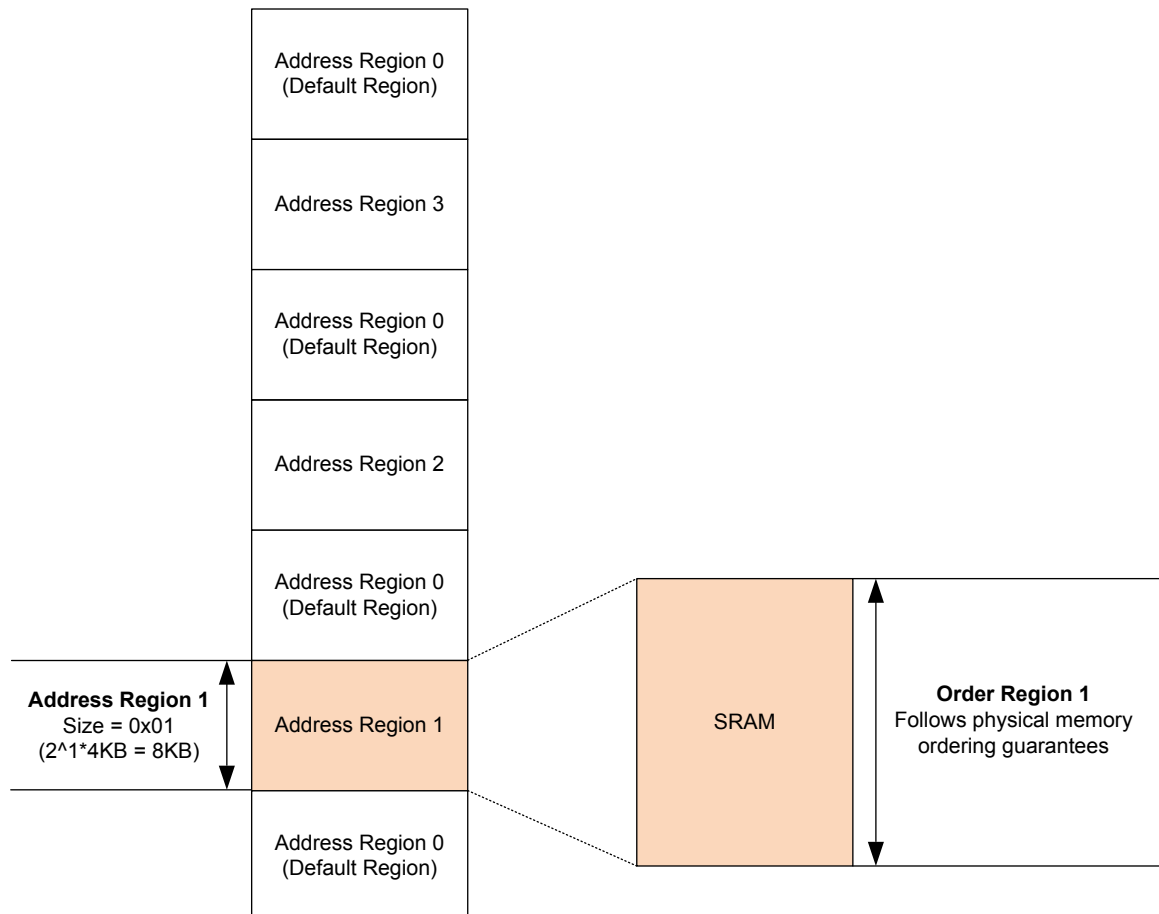


Figure 2-35 Address Region 1 configuration

Address Region 1 starts at base address `0x0000_0000_2000` and is 8KB in size. Because there is SRAM behind this region, it is mapped as physical memory. The entire Address Region 1 is considered as one

Order Region. Therefore, ordering is maintained between all requests to the overlapping cache line region (64B).

The following table shows the configured values for the Address Region 1 Configuration Register, `por_hni_sam_addrregion1_cfg`.

Table 2-33 Address Region 1 configuration

Bits	Field name	Configured value
[5:0]	order_reg_size	6'h1
[15:10]	addr_region_size	6'h1
[55:20]	base_addr	36'h0000_0000_2
[58]	physical_mem_en	1'b1
[59]	ser_all_wr	1'b0
[60]	ser_devne_wr	1'b0
[61]	pos_early_rdack_en	1'b1
[62]	pos_early_wr_comp_en	1'b1
[63]	valid	1'b1

Address Region 2

The following figure shows the example configuration for Address Region 2.

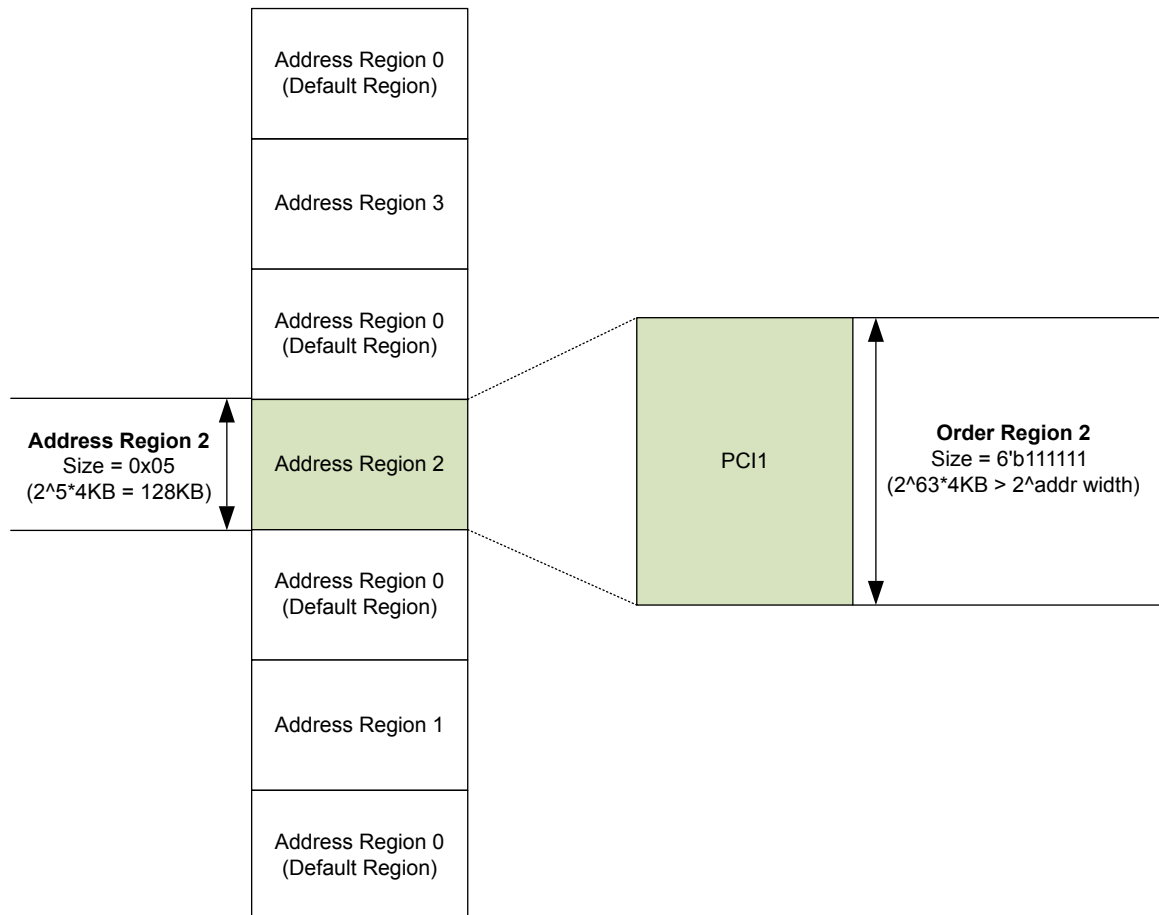


Figure 2-36 Address Region 2 configuration

Address Region 2 starts at base address `0x0000_0002_0000` and is 128KB in size. The Order Region 2 size ($2^6 \times 4\text{KB}$) is configured to the maximum value (`6'b111111`), so Address Region 2 is considered as one Order Region. PCI1 occupies the entire Order Region, so all PCI1 requests are ordered.

The following table shows the configured values for the Address Region 2 Configuration Register, `por_hni_sam_addrregion2_cfg`.

Table 2-34 Address Region 2 configuration

Bits	Field name	Configured value
[5:0]	<code>order_reg_size</code>	<code>6'b111111</code>
[15:10]	<code>addr_region_size</code>	<code>6'h5</code>
[55:20]	<code>base_addr</code>	<code>36'h0000_0002_0</code>
[58]	<code>physical_mem_en</code>	<code>1'b0</code>
[59]	<code>ser_all_wr</code>	<code>1'b0</code>
[60]	<code>ser_devne_wr</code>	<code>1'b0</code>
[61]	<code>pos_early_rdack_en</code>	<code>1'b1</code>

Table 2-34 Address Region 2 configuration (continued)

Bits	Field name	Configured value
[62]	pos_early_wr_comp_en	1'b1
[63]	valid	1'b1

Address Region 3

The following figure shows the example configuration for Address Region 3.

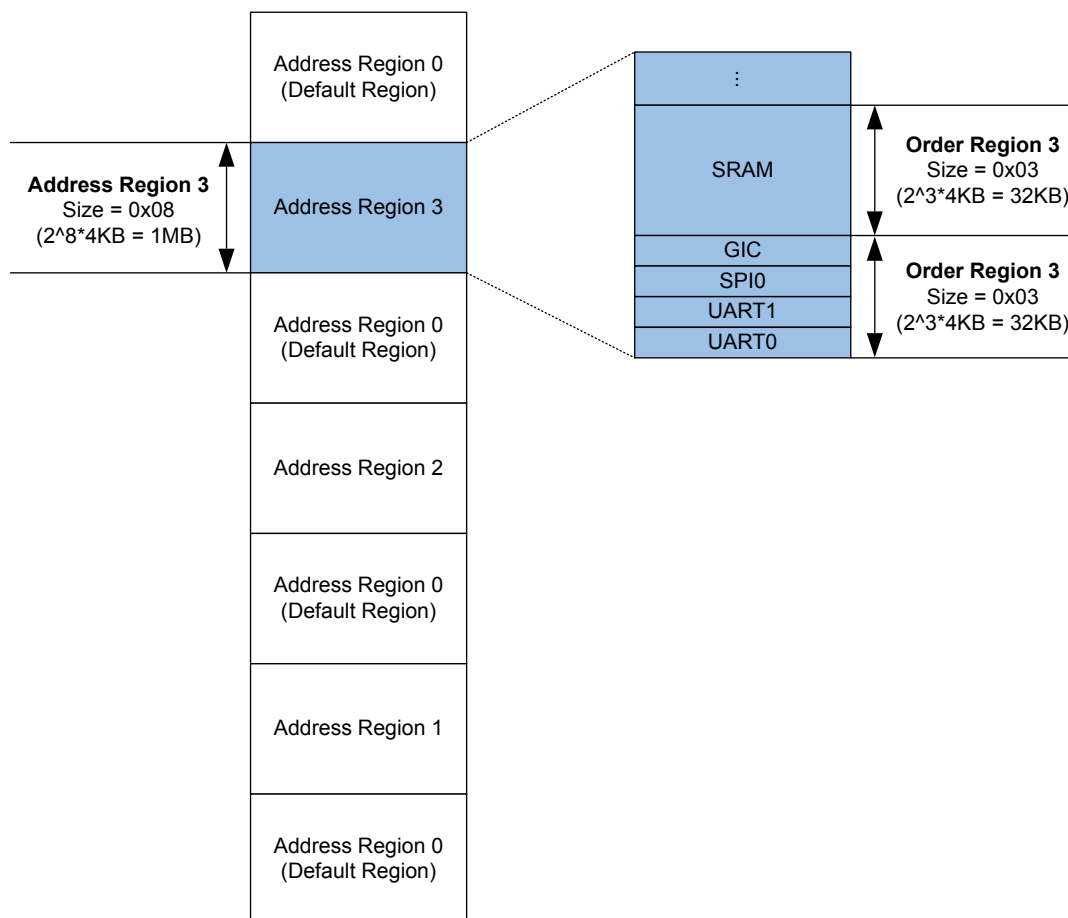


Figure 2-37 Address Region 3 configuration

Address Region 3 starts at base address 0x0000_0020_0000 and is 1MB in size. The Order Region 3 size of 32KB is less than the Address Region 3 size of 1MB, resulting in a total of 32 Order Regions. GIC, SPI0, UART1, and UART0 map to one Order Region, therefore all requests to these peripherals are ordered. SRAM also maps to one Order Region, therefore all requests to SRAM are ordered. Because SRAM maps to a separate Order Region from GIC, SPI0, UART1, and UART0, the following request types are not ordered:

- Requests to SRAM
- Requests to GIC, SPI0, UART1, and UART0

The following table shows the configured values for the Address Region 3 Configuration Register, `por_hni_sam_addrregion3_cfg`.

Table 2-35 Address Region 3 configuration

Bits	Field name	Configured value
[5:0]	order_reg_size	6'h3
[15:10]	addr_region_size	6'h8
[55:20]	base_addr	36'h0000_0020_0
[58]	physical_mem_en	1'b0
[59]	ser_all_wr	1'b0
[60]	ser_devne_wr	1'b0
[61]	pos_early_rdack_en	1'b1
[62]	pos_early_wr_comp_en	1'b1
[63]	valid	1'b1

2.22 Cross chip routing and ID mapping

IDs are generated and used to route protocol messages across multiple chips.

This section covers ID generation and the methods that are used to route CCIX protocol messages across multiple chips. RA SAM-related acronyms include:

- *CCIX Request Agent ID (RAID)*.
- *CCIX Home Agent ID (HAID)*.
- *Logical Device ID (LDID)*.

LDIDs are uniquely assigned within a device type. For example, RN-Fs in the system could be assigned LDIDs 0-n, while RN-Is could be assigned LDIDs 0-m, and RN-Ds could be assigned LDIDs 0-k.

The following rules apply:

- RAID usage:
 - Is confined to CCIX gateway devices only.
 - All non-CCIX CMN-600AE components use and operate on sequentially assigned LDIDs. CXG devices bidirectionally map each CCIX RAID to an LDID.
- RN-F LDID assignment:
 - Local RN-Fs are assigned LDIDs from 0-n, sequentially.
 - Remote RN-Fs must be assigned LDIDs n+1 and above by the discovery software.

The following figure shows a basic multi-chip block diagram.

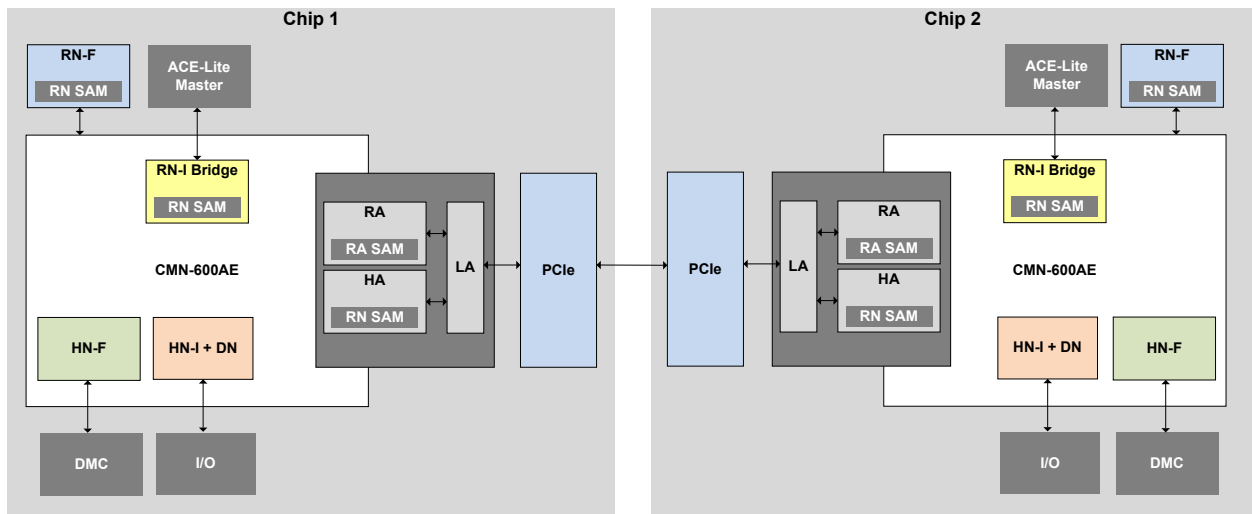


Figure 2-38 Multi-chip block diagram

Request from an RN-F to a remote HN-F

The following figure shows all IDs generated and used to route a request from a local RN-F on Chip 1 to a remote HN-F on Chip 2.

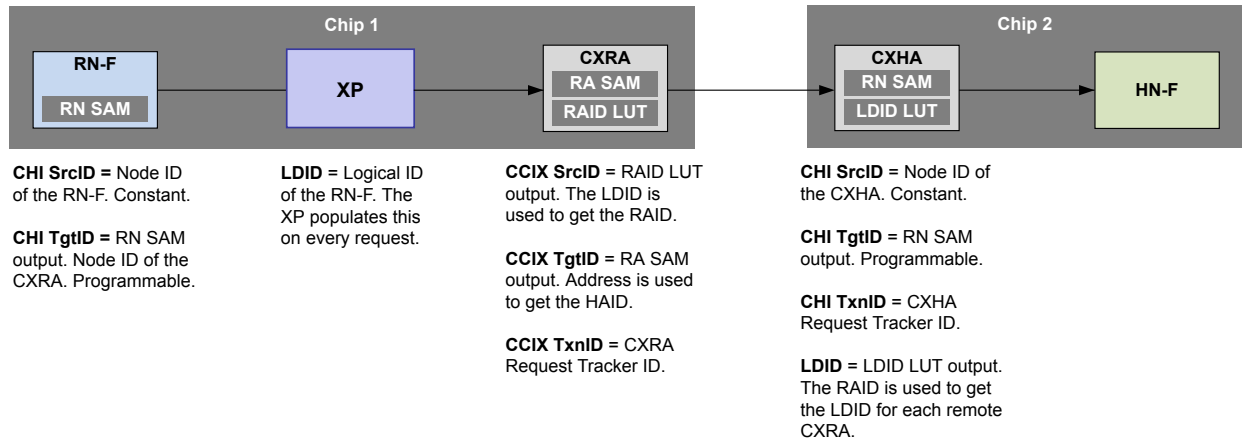


Figure 2-39 RN-F to remote HN-F IDs

The flow for this process is as follows:

- The RN-F looks up the programmable RN SAM to populate the CHI target ID on a request.
- The XP populates the RN-F LDID on this request.
- RN-Is and RN-Ds are internal to CMN-600AE and get their logical ID assigned during CMN-600AE generation. The RN-I or RN-D sends this LDID on every request.
- The CXRA contains programmable lookup tables, RAID LUTs, for each class of local RN (RN-F, RN-I, and RN-D). CCIX discovery software discovers all local RN-Fs, RN-Ds, and RN-Is, and programs their corresponding RAID IDs in these LUTs. The LDID of the incoming request is used to look up these RAID LUTs and determine the CCIX RAID. CXRA also has CCIX RA SAM. This CCIX RA SAM is used to generate the HAID. This HAID is used as the target ID to route the CCIX request message.
- The LDIDs for local RN-Fs must not be changed. The build-time LDID assignments are discovered by reading any one of the HN-F por_hnf_rn_physid registers. A few cycles after reset, these registers are prepopulated with the LDIDs for local RN-Fs within that chip.

The following figure shows the programmable registers during CCIX Discovery.

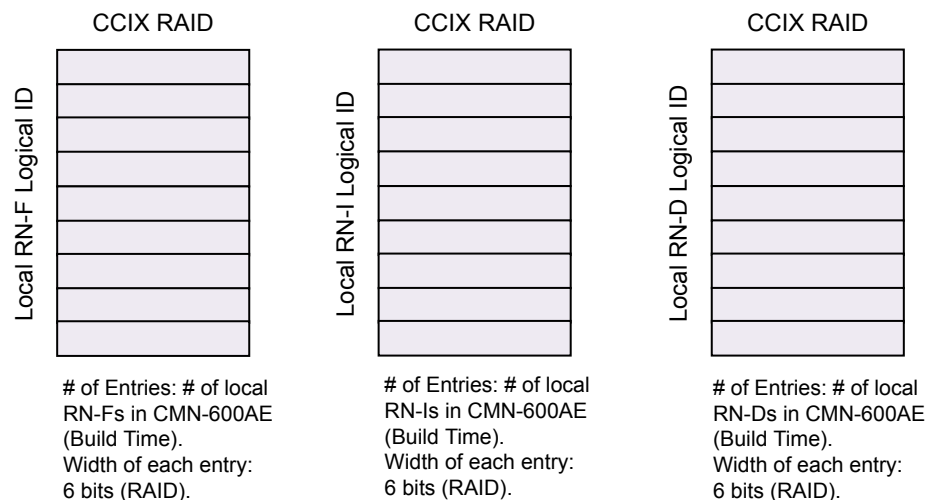


Figure 2-40 Programmable registers during CCIX Discovery

The CXHA contains a programmable register to program the local LDID for each remote CCIX RAID that communicates with local CHI HNs on a given chip or socket. Each entry in the programmable

register also contains an RN-F bit to identify whether the remote CXRA is a caching agent (RN-F) or not. HN-Fs on the local chip use this LDID to track a line in its SF. Therefore a unique LDID assignment is required for each remote requesting caching agent. These unique LDIDs must not overlap with LDIDs assigned to local RN-Fs. It is assumed that these IDs are assigned after CCIX Discovery is complete. For example, all the CXRAs are discovered and assigned an RAID.

The following figure shows the programmable register for RAID to LDID during CCIX Discovery.

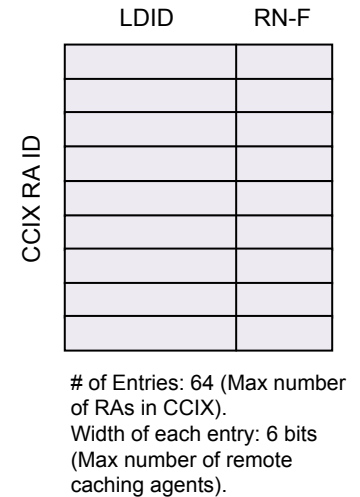


Figure 2-41 RAID to LDID during CCIX Discovery

With the LDID passed to HN-F in all CHI REQ flits, HN-F uses this LDID as the true logical ID for SF tracking purposes. HN-F uses a logical ID vector in the SF, with its size based on the total number of RN-Fs in the entire system (local and remote RN-Fs). The size is assigned when CMN-600AE is generated. This value controls the SF efficiency, therefore set the value according to the total number of caching agents found in the entire system. If the exact number is not known, the value must be set to support the maximum number of caching agents that the entire system can have. CCIX supports a maximum of 64 CXRAs in the entire system.

The following figure shows all generated IDs used to route a response from a remote HN-F on Chip 2 to an RN-F on Chip 1.

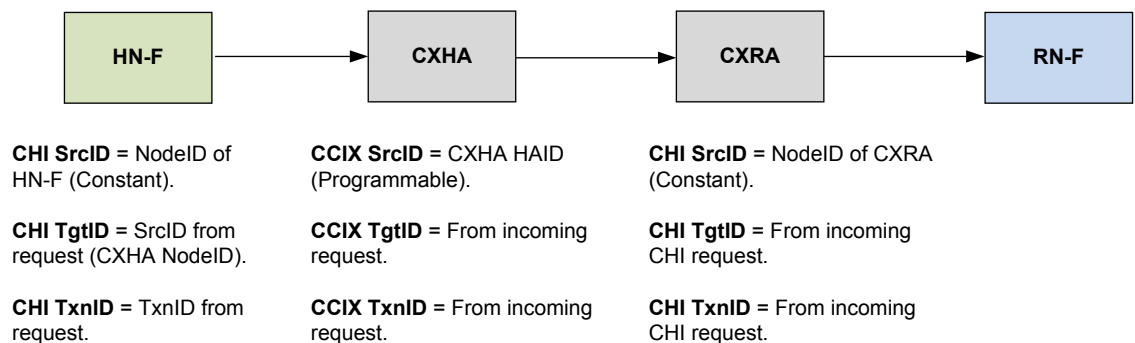


Figure 2-42 Remote HN-F to RN-F IDs

The following figure shows the flow of a snoop from an HN-F to a remote RN-F.

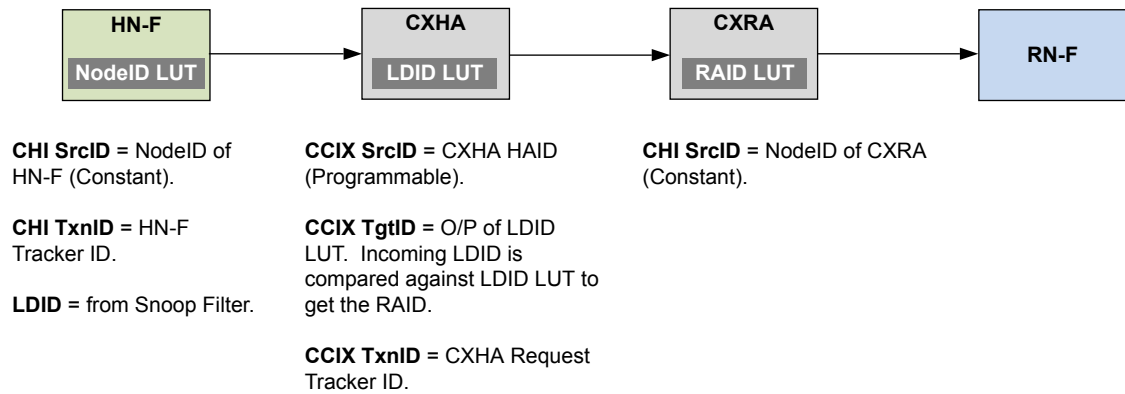


Figure 2-43 Snoop from HN-F to remote RN-F

The HN-F contains the following programmable LUT to program the CXHA node ID of each remote caching agent. HN-F uses the unique LDID from the snoop vector to look up the physical CHI node ID of the CXHA where snoops are sent to. The following table shows an example programming where logical IDs 0-7 are assigned to the local RN-Fs. The logical IDs 8-15 are assigned to the remote RN-Fs. Software assigns these IDs during the Discovery process.

Table 2-36 Example program

Logical ID as index	HN-F programmable register	
	CHI node ID	ID valid
0	Local RN-F 0	1
1	Local RN-F 1	1
2	Local RN-F 2	1
...
7	Local RN-F 7	1
8	CXHA	1
9	CXHA	1
...
15	CXHA	1
16	Not programmed	0
...	Not programmed	0
n	Not programmed	0

The CXHA uses the LDID from incoming CHI snoop to perform a content match against the entries of programmable CCIX RAID to local LDID LUT. This content match results in the CCIX RAID sending a CCIX snoop, as the following figure shows.

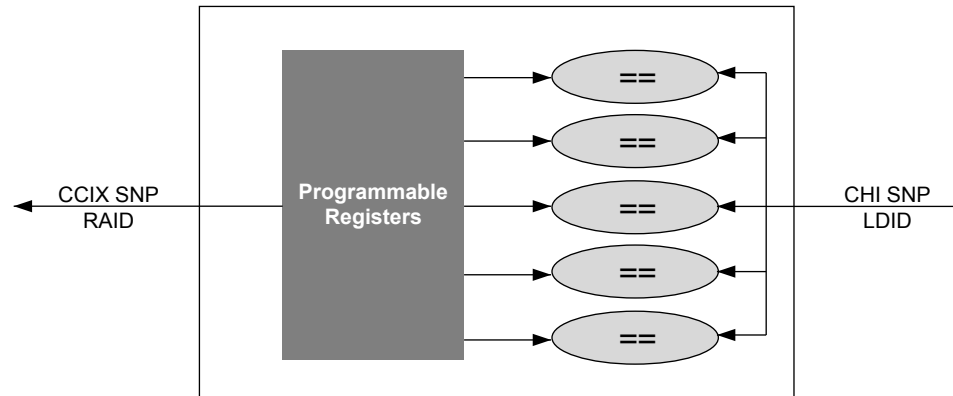


Figure 2-44 CHI SNP LDID to CCIX SNP RAID flow

The following figure shows the number of entries at build time.

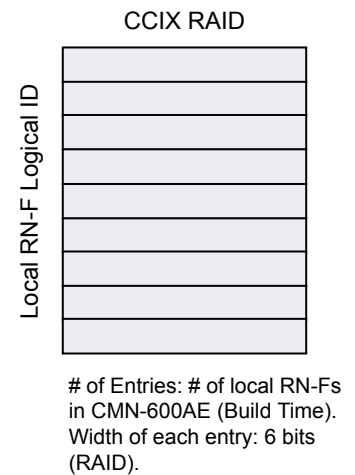


Figure 2-45 Number of entries at build time

The following figure shows the detailed flow of a CHI SNP LDID to CCIX SNP RAID conversion.

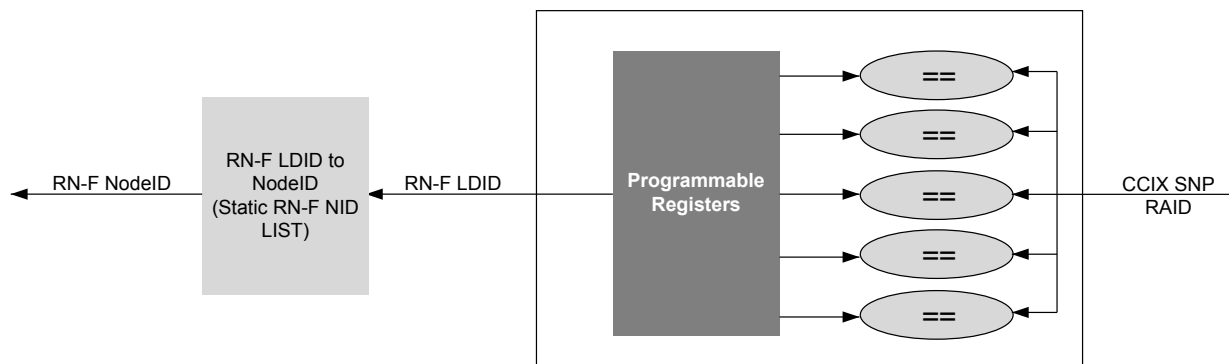


Figure 2-46 CHI SNP LDID to CCIX SNP RAID detailed flow

The following figure shows all generated IDs used to route a snoop response from a remote RN-F on Chip 1 to an HN-F on Chip 2.

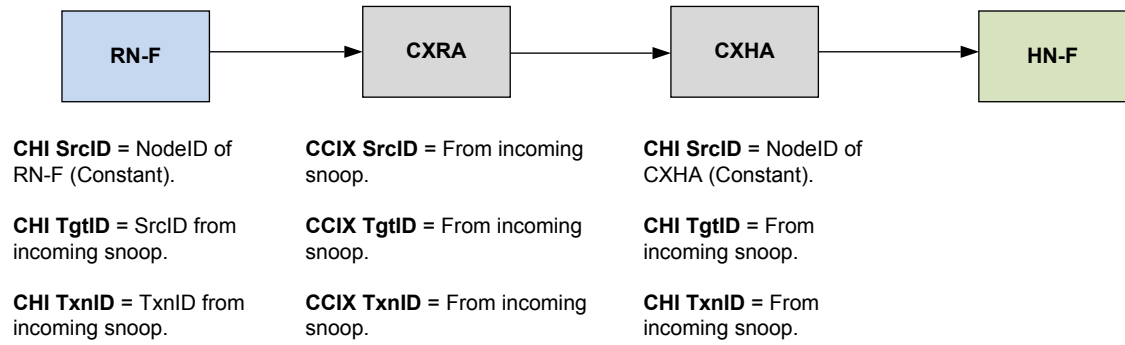


Figure 2-47 Remote RN-F to HN-F with all IDs generated

2.23 GIC communication over AXI4-Stream ports

CMN-600AE supports optional master/slave *AXI4-Stream* (A4S) ports on RN-I, RN-D, and SMXP RN-F ports for communication between a *Generic Interrupt Controller* (GIC) and CPUs. Certain requirements apply to the A4S routing and signaling.

CMN-600AE also supports transmission of GIC information across CCIX links for CML SMP configurations.

More system-level information is available in the *Arm® Neoverse™ N1 hyperscale reference design GIC-600 Integration using CMN-600 AXI4-Stream Interfaces White Paper* on request.

A4S routing

The A4S ports are addressed according to Logical ID, which are assigned sequentially from 0 to the number of A4S ports. To send a packet from one A4S port to the destination A4S port, the TDEST should be assigned to the Logical ID of the target A4S port, or the Logical ID of the CXRH for GIC traffic targeting the other chip. The discovery process returns the number of A4S ports and Logical ID information for each A4S port by reading corresponding RN-I, RN-D, and XP unit information registers. For more information about the discovery process, see [2.5 Discovery on page 2-53](#).

Other requirements

- The **PUB_DESTID** associated with the GICD A4S port must drive the **CXRH GICD_DESTID** input. GICD drives the CMN-600AE **RXA4STRI[7:0]** input (8 MSB bits of **GICD ICDRTDEST**), indicating the CCIX link of the target chip, in addition to the **RXA4STDEST[7:0]** (8 LSB bits of **GICD ICDRTDEST**) of CXRH for CML SMP configurations.

————— **Note** —————

This requirement only applies to 2-chip configurations. Contact *Arm®* for information on three or more chip configurations.

- The A4S master must assert **valid** irrespective of **ready** state to transmit data.

2.24 Clocking

The following sections describe the CMN-600AE clock domains, inputs, and hierarchy.

This section contains the following subsections:

- [2.24.1 Clock domains on page 2-134.](#)
- [2.24.2 CML clock inputs on page 2-135.](#)
- [2.24.3 Clock hierarchy on page 2-136.](#)
- [2.24.4 Clock enable inputs on page 2-137.](#)

2.24.1 Clock domains

CMN-600AE has a single, fully synchronous clock domain. This clock domain is supplied by a single global clock signal, which is known as **GCLK0**.

The following figure shows an example mesh topology and the boundaries of the CMN-600AE clock domain.

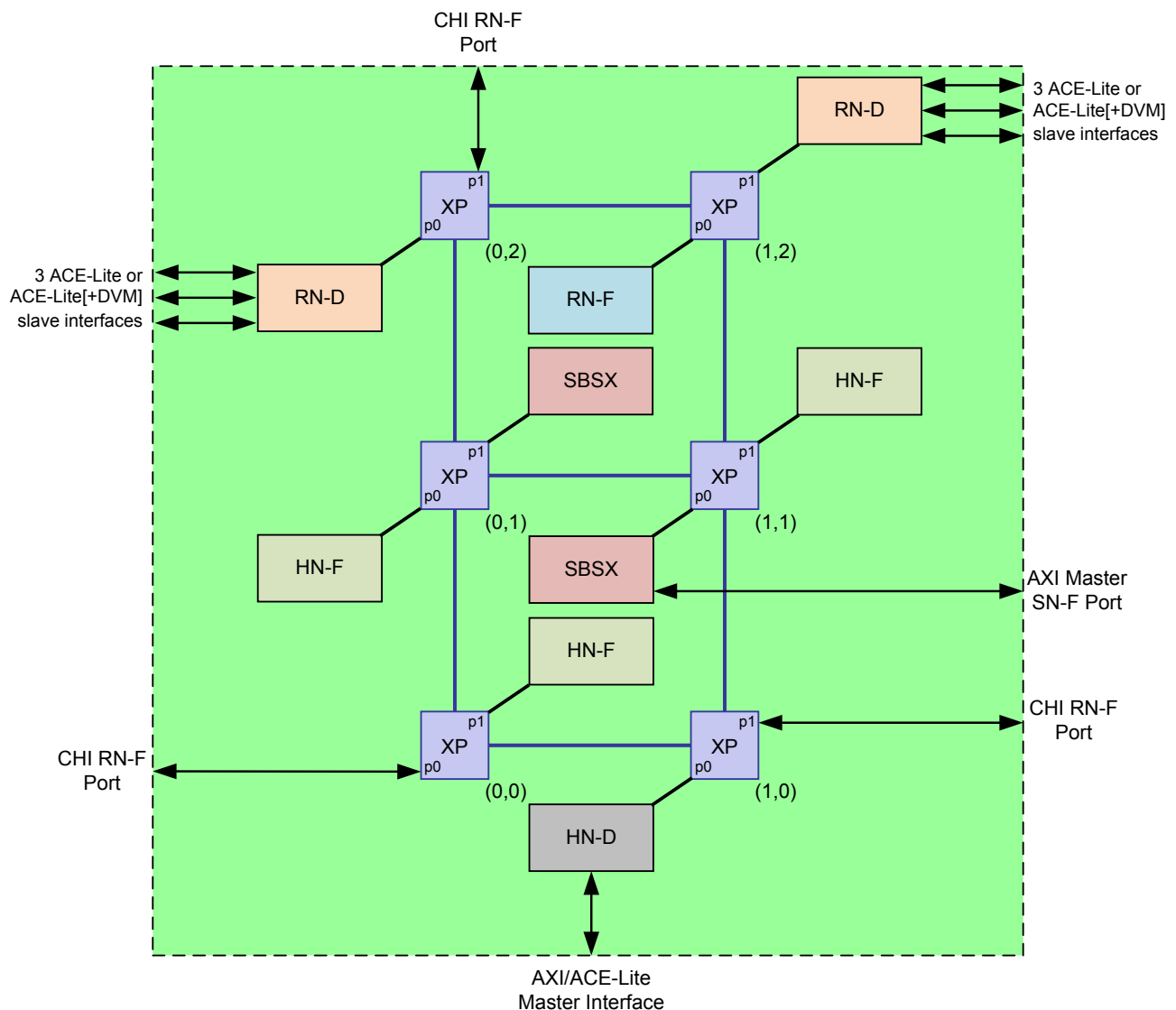


Figure 2-48 CMN-600AE fully synchronous clock domain

2.24.2 CML clock inputs

There are two extra clock inputs for CML configurations: **CLK_CGL** and **CLK_CXS**.

CLK_CGL is a copy of the CMN clock input used by the CXRH node associated with the CXLA, **GCLK0**. A separate clock input is provided to allow gating of the CGL clock domain independent of the **GCLK0** domain. **CLK_CXS** clocks the CXS interface logic, and can be synchronous or asynchronous to **GCLK0**. **CLK_CXS** can be driven with **CLK_CGL** for synchronous configurations, as the following figure shows.

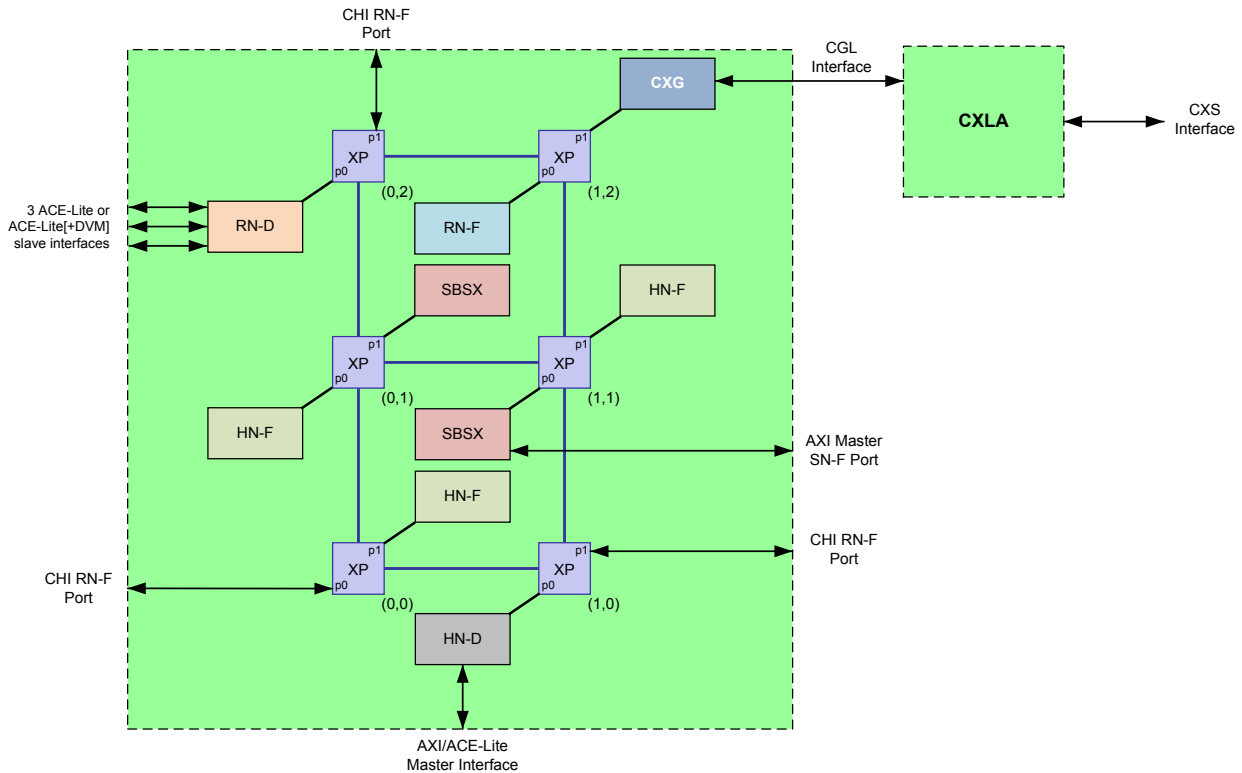


Figure 2-49 CMN-600AE clock domains with synchronous CXS domain

The CXLA block contains an asynchronous domain bridge for configurations where the **CLK_CXS** domain is asynchronous to the **CLK_CGL** domain, as the following figure shows.

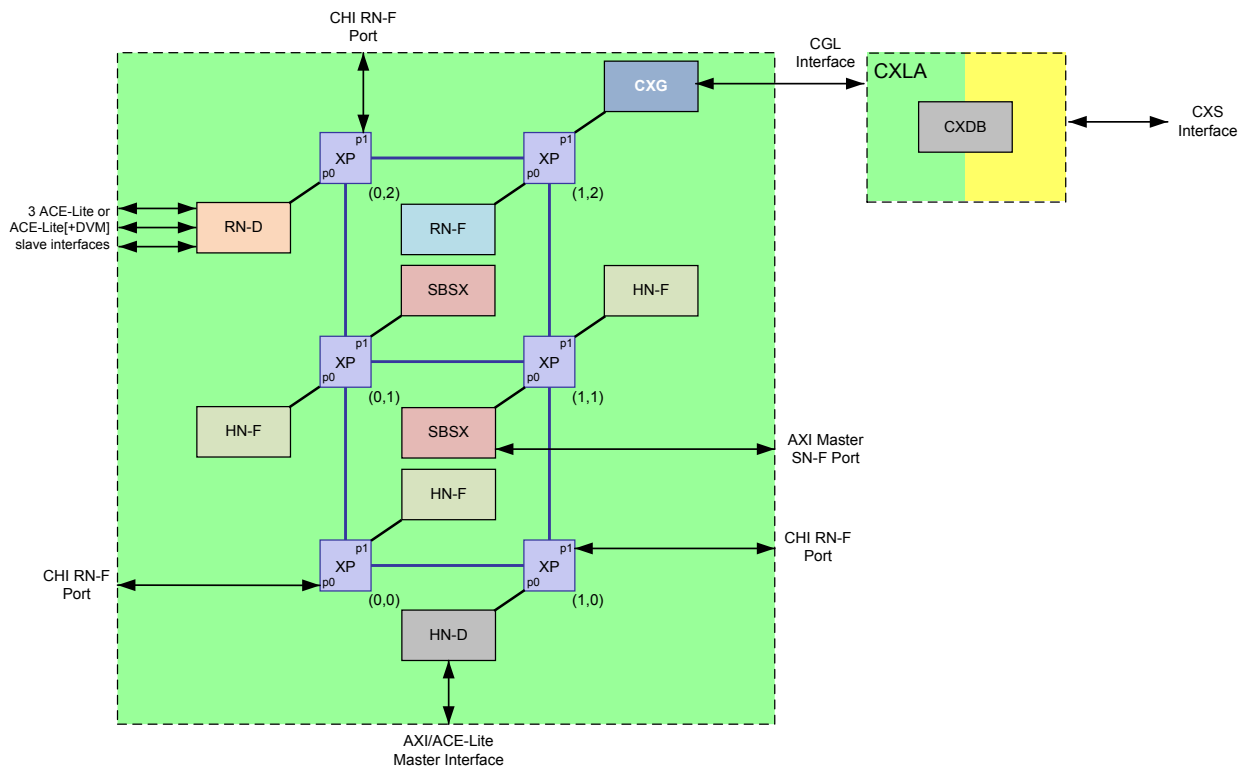


Figure 2-50 CMN-600AE clock domains with asynchronous CXS domain

2.24.3 Clock hierarchy

The clocking delivery and clock gating architecture are hierarchical.

Within the clock gating hierarchy, three levels of clocks are defined:

- | | |
|------------------------|--|
| Global clock | The global clock is the clock input to the CMN-600AE system. Another level of clock gating or clock control outside of the system is likely to control the global clock that is provided by the SoC. Although it is not a system requirement, CMN-600AE includes support for external clock control. |
| Regional clocks | Regional clocks are created as an output of regional clock gaters that include a coarse enable for coarse-grained clock gating under idle or mostly idle conditions. Regional clock gaters can shutdown the clock network between regional and local gaters. Therefore, this level of hierarchy enables greater power reduction than is possible using local clock gating. The regional clock gaters are instantiated in and controlled by the CMN-600AE RTL. The exact set of regional clocks is internal to CMN-600AE and is not described in this book. |
| Local clocks | <p>Local clocks are created according to the following hierarchy:</p> <ol style="list-style-type: none"> 1. RTL creates fine-grained enable signals. 2. Fine-grained enable signals control local clock gaters. 3. Local clock gaters output local clock signals. <p>Local clock signals are used to directly clock sequential elements in CMN-600AE. The exact set of local clocks is internal to CMN-600AE and is not described in this manual.</p> |

The following figure shows the clocking hierarchy.

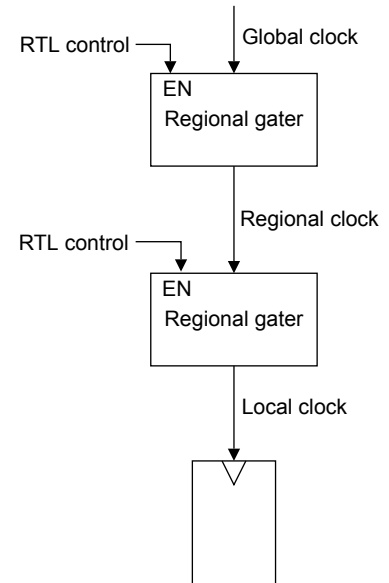


Figure 2-51 Clocking hierarchy

2.24.4 Clock enable inputs

CMN-600AE includes several clock enable inputs, enabling synchronous communication with slower SoC logic.

The clock enable input signals are:

- ACLKEN_S** This input is present on each AMBA slave interface.
- ACLKEN_M** This input is present on each AMBA master interface.
- ATCLKEN** This input is present on each debug and trace ATB interface.

All clock enable signals, shown here as ***CLKEN***, have identical functionality: they enable their respective interface to run at integer fractions of **GCLK0**. In other words, the clock enable signals run slower than **GCLK0**. **ACLKEN_S** and **ACLKEN_M** can run at any integer ratio from 1:1 to 4:1 of the frequency of **GCLK0**. **ATCLKEN** is limited to 1:1, 2:1, and 4:1 integer ratios.

CLKEN asserts one **GCLK0** cycle before the rising edge of the SoC clock, **SoC-CLK**. SoC control logic can change the ratio of **GCLK0** frequency to **SoC-CLK**, frequency dynamically using ***CLKEN***.

The following figure shows a timing example of a ***CLKEN*** ratio change. In the example, ***CLKEN*** changes the ratio of the relevant interface frequency respective to **GCLK0** from 3:1 to 1:1.

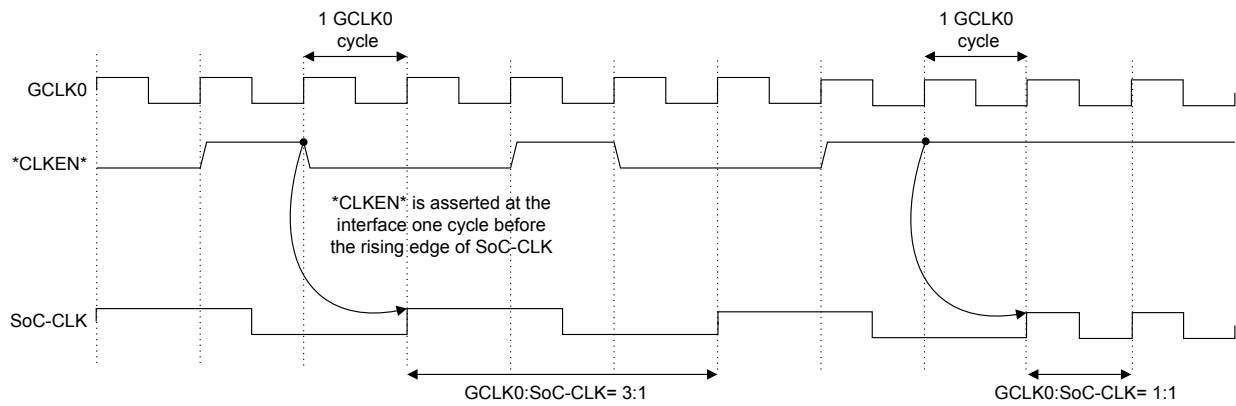


Figure 2-52 *CLKEN* with GCLK0:SoC-CLK ratio changing from 3:1 to 1:1

2.25 Reset

CMN-600AE has a single global reset input signal, **nSRESET**.

nSRESET is an active-LOW signal that can be asynchronously or synchronously asserted and deasserted.

When asserted, **nSRESET** must remain asserted for 72 clock cycles. Likewise, when deasserted, **nSRESET** must remain deasserted for 72 clock cycles. This requirement ensures that all internal CMN-600AE components enter and exit their reset states correctly.

All CMN-600AE clock inputs must be active during the required 72-cycle, or larger, period of **nSRESET** assertion. The clock inputs must also remain active for at least 72 cycles following deassertion of **nSRESET**.

This section contains the following subsection:

- [2.25.1 CML reset on page 2-139](#).

2.25.1 CML reset

There are two extra reset inputs for the CML configuration: **nRESET_CGL** and **nRESET_CXS**.

Both **nRESET_CGL** and **nRESET_CXS** are active-LOW signals that can be asynchronously or synchronously asserted and deasserted.

When asserted, **nRESET_CGL** and **nRESET_CXS** must remain asserted for 20 **CLK_CGL** and **CLK_CXS** clock cycles respectively. Likewise, when deasserted, **nRESET_CGL** and **nRESET_CXS** must remain deasserted for 20 **CLK_CGL** and **CLK_CXS** clock cycles respectively. This requirement ensures that all CML components enter and exit their reset states correctly.

Both **CLK_CGL** and **CLK_CXS** must be active during the required 20-cycle, or larger, period of **nRESET_CGL** and **nRESET_CXS** assertion respectively and must remain active for at least 20 cycles following deassertions.

For more relationship information between the CXS and CGL domains, refer to [2.24.2 CML clock inputs on page 2-135](#).

Note

There is no sequencing requirement between the CMN-600AE **nSRESET** and the CML resets. However, the CML domains must exit reset before CXLA functionality is required.

2.26 Power and clock management

CMN-600AE includes several power management and clock management capabilities, that are either externally controllable or are assisted by the SoC.

The power management and clock management capabilities are:

- High-level Clock Gating that indicates inactivity in the system, enabling an External Clock Controller to disable global clock inputs during periods of inactivity. This capability significantly reduces dynamic power consumption.
- Several distinct predefined power states, including states in which all, half, or none of the SLC Tag and Data RAMs can be powered up, powered down, or in retention:
 - A state in which only the HN-F SF is active.
 - A state in which the SLC RAMs and SF RAMs are inactive.

These power states reduce static and dynamic power consumption.

- Support for static retention in HN-F in which the SoC places SLC and SF RAMs in a retention state. This capability reduces static power consumption.
- Support for in-pipeline low-latency Data RAM retention control, in which a programmable idle counter can be used to put the SLC RAMs in retention.

This section contains the following subsections:

- [2.26.1 High-level Clock Gating \(HCG\) on page 2-140.](#)
- [2.26.2 Power domains on page 2-142.](#)
- [2.26.3 Power domain control on page 2-143.](#)
- [2.26.4 P-Channel on device reset on page 2-144.](#)
- [2.26.5 CXS power domain on page 2-144.](#)
- [2.26.6 HN-F Memory retention mode on page 2-145.](#)
- [2.26.7 HN-F power domains on page 2-145.](#)
- [2.26.8 HN-F RAM Power Control State Machine interface on page 2-149.](#)
- [2.26.9 HN-F power domain completion interrupt on page 2-149.](#)

2.26.1 High-level Clock Gating (HCG)

The PCCB supports a *High-level Clock Gating* (HCG) mechanism. This mechanism notifies the SoC when CMN-600AE is inactive and therefore reduces dynamic power consumption.

HCG enables an external SoC clock control unit, the *External Clock Controller* (ExtCC), to stop the **GCLK0** clock inputs. For more information about the ExtCC, see [External Clock Controller \(ExtCC\) on page 2-140.](#)

CMN-600AE includes a Q-Channel interface that enables CMN-600AE and the SoC to communicate to achieve HCG functionality through the PCCB. For more information, see the *Arm® AMBA® Low Power Interface Specification Arm® Q-Channel and P-Channel Interfaces.*

External Clock Controller (ExtCC)

The *External Clock Controller* (ExtCC) is used to control the HCG flow.

The following figure shows an example of how the ExtCC controls the clock gating flow. This example clock gating sequence begins and ends with the Q-Channel in either of the following states:

Q_STOPPED

Quiescent state, where **QREQn** and **QACCEPTn** are asserted.

Q_RUN

Active state, where **QREQn** and **QACCEPTn** are deasserted.

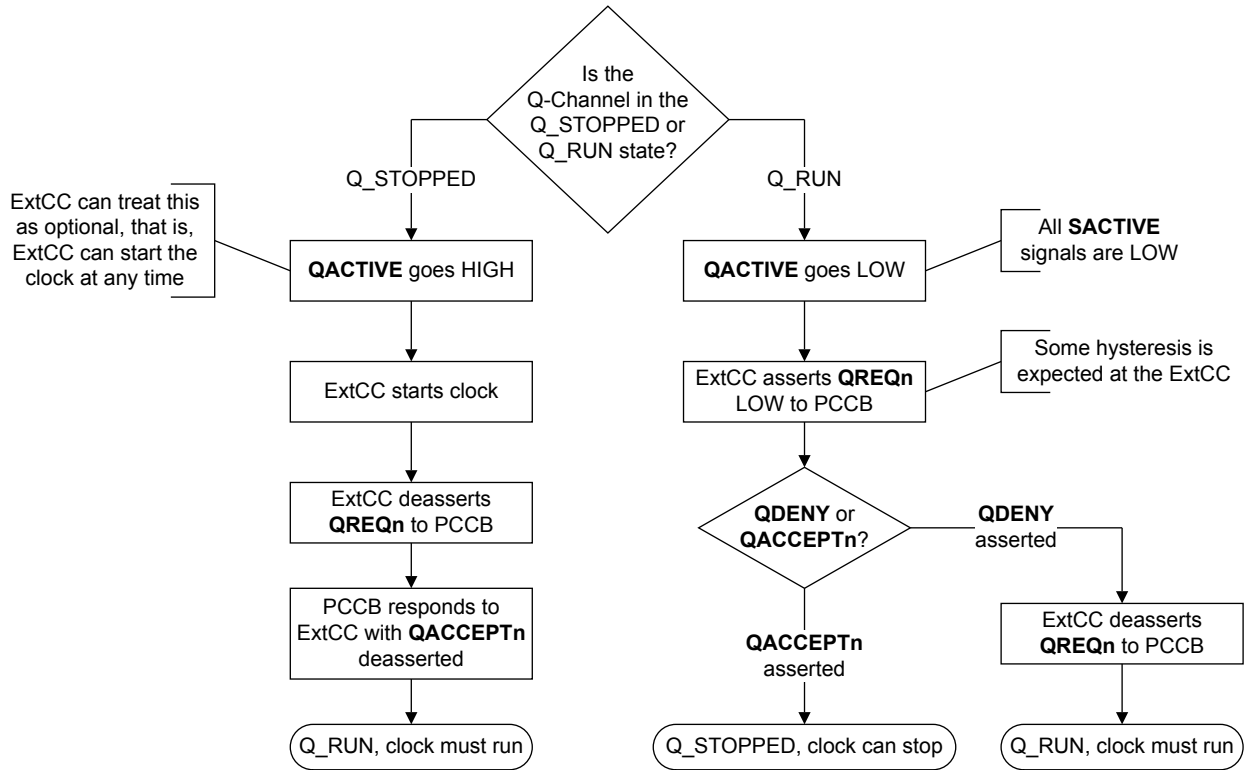


Figure 2-53 Clock gating control using ExtCC

The requirements of the ExtCC are as follows:

- It must supply a clock to CMN-600AE when the Q-Channel is in any state other than Q_STOPPED.
- The ExtCC can either:
 - Choose to gate the clock to CMN-600AE when the Q-Channel is in the Q_STOPPED state.
 - Choose to run the clock at any time.
- ExtCC is responsible for bringing the Q-Channel to Q_RUN state after reset deassertion.
- This manual does not describe the exact behavior of the ExtCC and its usage of **QREQn** in response to **QACTIVE** deassertion. However, the design of the ExtCC is likely to include a control loop with some hysteresis. Therefore HCG is enabled when the system is inactive for long periods, but is not enabled for short periods of inactivity. If the clocks are stopped in response to short periods of inactivity, performance of CMN-600AE can be negatively affected.
- It is the responsibility of the SoC designer to fully control the clock management Q-Channel. If you require a control or configuration bit to completely enable or disable HCG functionality, it must exist outside of CMN-600AE. CMN-600AE has no internal means of disabling HCG.

CML clock management

CMN-600AE CML configurations add two extra clock domains and corresponding Q-Channel interfaces for each CXG instance and corresponding CXS interface:

- CLK_CGL Q-Channel: Manages the CGL link and CGL domain logic in the CXG and CXLA devices.
- CLK_CXS Q-Channel: Manages the CXS link interface and CXS clock domain logic in the CXLA.

The following table shows the possible clock states for the CMN-600AE and CML device clocks, where N denotes multiple CXS interfaces:

Table 2-37 CMN-600AE and CML device clock states

GCLK0	CLK_CGL[N]	CLK_CXS[N]	Description
RUN	RUN	RUN	CMN-600AE and CXS[N] interface active
RUN	RUN	STOP	CXS[N] domain gated
RUN	STOP	RUN	CGL[N] inactive, transitory state
RUN	STOP	STOP	CXS[N] interface fully gated
STOP	STOP	RUN	CXS[N] active, others inactive, transitory state
STOP	STOP	STOP	CMN-600AE fully gated, all CXS[N] interfaces inactive

2.26.2 Power domains

The power domains in CMN-600AE are divided into logic domains and domains for the RAMs in the HN-F partitions.

CMN-600AE has the following power domains:

Logic

All logic except HN-F SLC tag and data RAMs and HN-F SF RAMs.

SLC RAM0

SLC tag and data RAMs way[7:0] within HN-F partitions. The RAMs in each HN-F partition can be independently controlled.

SLC RAM1

SLC tag and data RAMs way[15:8] within HN-F partitions. The RAMs in each HN-F partition can be independently controlled. For 3MB SLC size configurations, the RAM1 domain includes way[11:8].

Snoop filter only mode

SF RAMs within HN-F partitions. The RAMs in each HN-F partition can be independently controlled.

The following figure shows an example power domain configuration.

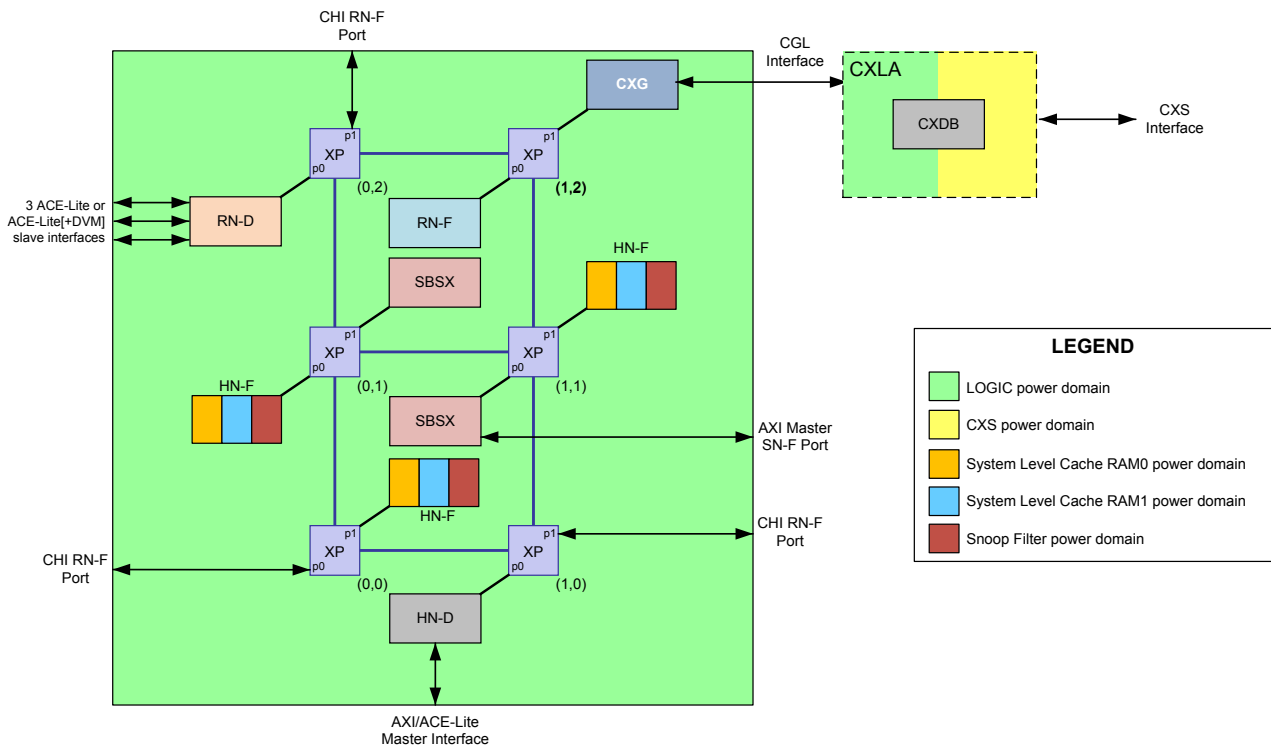


Figure 2-54 CMN-600AE power domain example

2.26.3 Power domain control

The CMN-600AE logic P-Channel controls all power domains except for the RAM and CXS power domains.

In addition to controlling the logic domain, the logic P-Channel allows synchronization between the HN-F software-controlled power domains and the logic domain. This synchronization is achieved through a CONFIG state, as the following figure shows.

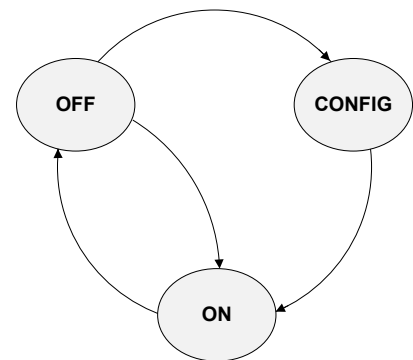


Figure 2-55 Logic domain states

There are two paths for transitioning from the OFF to ON state:

Cold reset

The logic PSTATE OFF to ON transition also initiates NOSFSLC to FAM transition for all HN-F partitions.

Exit from HN-F static retention state

The logic PSTATE transitions from OFF to CONFIG, indicating that CMN-600AE is exiting a memory retention state. The transition does not initiate any HN-F partition power transitions.

The following table contains the power modes of components within the domain and the associated PSTATE values.

Table 2-38 Power mode configurations and PSTATE values

Power mode	PSTATE	CMN-600AE logic	HN-F
OFF	0b00000	OFF	OFF/MEM_RET
CONFIG	0b11000	ON	ANY
ON	0b01000	ON	ANY

For an introduction to HN-F states, see [2.26.7 HN-F power domains on page 2-145](#).

For P-Channel signal information, see [A.4 Power management signals on page Appx-A-1926](#).

CXS power gating

CML systems contain an extra power domain, the CXS power domain. CXS logic is controlled by a combination of the CXS power Q-Channel and the CXS Q-Channel that controls the clocks. Unless both the CXS power Q-Channel and the CXS Q-Channel are in the OFF state, power must be provided.

2.26.4 P-Channel on device reset

This section shows how to initialize the power state of a power domain.

Certain device power states might power down the control logic. When powering this control logic back on, the power controller must indicate the state that the device must power up. The device detects the required state by sampling **PSTATE** when **nSRESET** deasserts. The **PSTATE** inputs must be asserted before the deassertion of reset and remain after the deassertion of **nSRESET**, to allow reset propagation within CMN-600AE. The power controller must ensure that the reset sequence is complete before transitioning **PSTATE**, otherwise the device might sample an undetermined value. The following figure shows the state initialization on reset.

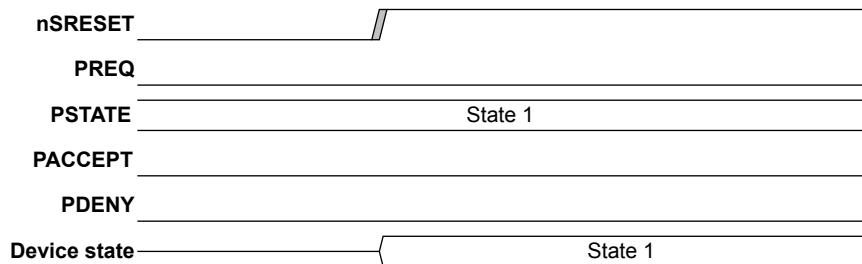


Figure 2-56 Reset state initialization

For an introduction to HN-F states, see [2.26.7 HN-F power domains on page 2-145](#).

2.26.5 CXS power domain

CML systems contain an extra power domain, the CXS power domain. The CMN-600AE CXS Power Q-Channel controls the CXS power domain.

Note

If the CXS interface is inactive, the CXS power domain can be shut off.

The following table shows the possible CMN-600AE LOGIC and CXS power states, where N denotes multiple CXS interfaces:

Table 2-39 CMN-600AE LOGIC and CXS power states

LOGIC state	CXS[N] state	Description
ON	ON	CMN-600AE and CXS[N] interface active.
ON	OFF	CXS[N] interface inactive.
OFF	ON	CXS[N] domain active, transitory state.
OFF	OFF	Shut down, all CXS[N] interfaces inactive.

2.26.6 HN-F Memory retention mode

When isolating the CMN-600AE outputs, handshake protocols on certain interfaces must be followed. This section describes the steps to take to enter and exit HN-F Memory retention mode.

Entering HN-F Memory retention mode

1. Program the HN-Fs to enter the required power state.
2. Quiesce the interconnect, and wait for **QACTIVE** to drop.
3. Place CMN-600AE in the LOGIC_OFF state through the logic P-Channel.
4. Isolate the CMN-600AE outputs. If the logic on the other side of the interface is being powered down or reset, this step might not be needed.
5. Turn off power to CMN-600AE.

Exiting HN-F Memory retention mode

1. Apply power to CMN-600AE.
2. Assert reset.
3. Enable clocks.
4. Disable isolation of the CMN-600AE outputs.
5. Deassert reset.
6. Place CMN-600AE in LOGIC_CONFIG state through the logic P-Channel.
7. Reprogram the por_hnf_ppu_pwpr register to the retention mode the HN-F was in before turning off power.
8. Reprogram the por_hnf_ppu_pwpr register to ON.
9. Reprogram the CMN-600AE configuration registers, including the RN SAM and any other registers that are written during cold boot.
10. Place CMN-600AE in the LOGIC_ON state through the P-Channel.
11. Resume traffic and normal operation.

2.26.7 HN-F power domains

The HN-F has various power states. Transitioning between different states enables or disables different parts of the HN-F.

The HN-F has the following classes of power states:

1. Operational states, where logic is on and enabled RAMs are operating as normal
2. Functional retention states, where logic is on, and enabled RAMs are in retention
3. Memory retention states, where logic is off and enabled RAMs are in retention

Within these power states, the HN-Fs in an SCG operate in four modes:

<i>Full Associativity Mode (FAM)</i>	The SF and the entire SLC are enabled.
<i>Half Associativity Mode (HAM)</i>	The SF is enabled but the upper half of the SLC ways are disabled and powered off.
<i>Snoop Filter Only Mode (SFONLY)</i>	The SF is enabled but the whole SLC is powered off.
<i>No SLC Mode (NOSFSLC)</i>	The SF and SLC are disabled and powered off.

The following constraints apply to the power states and transitions:

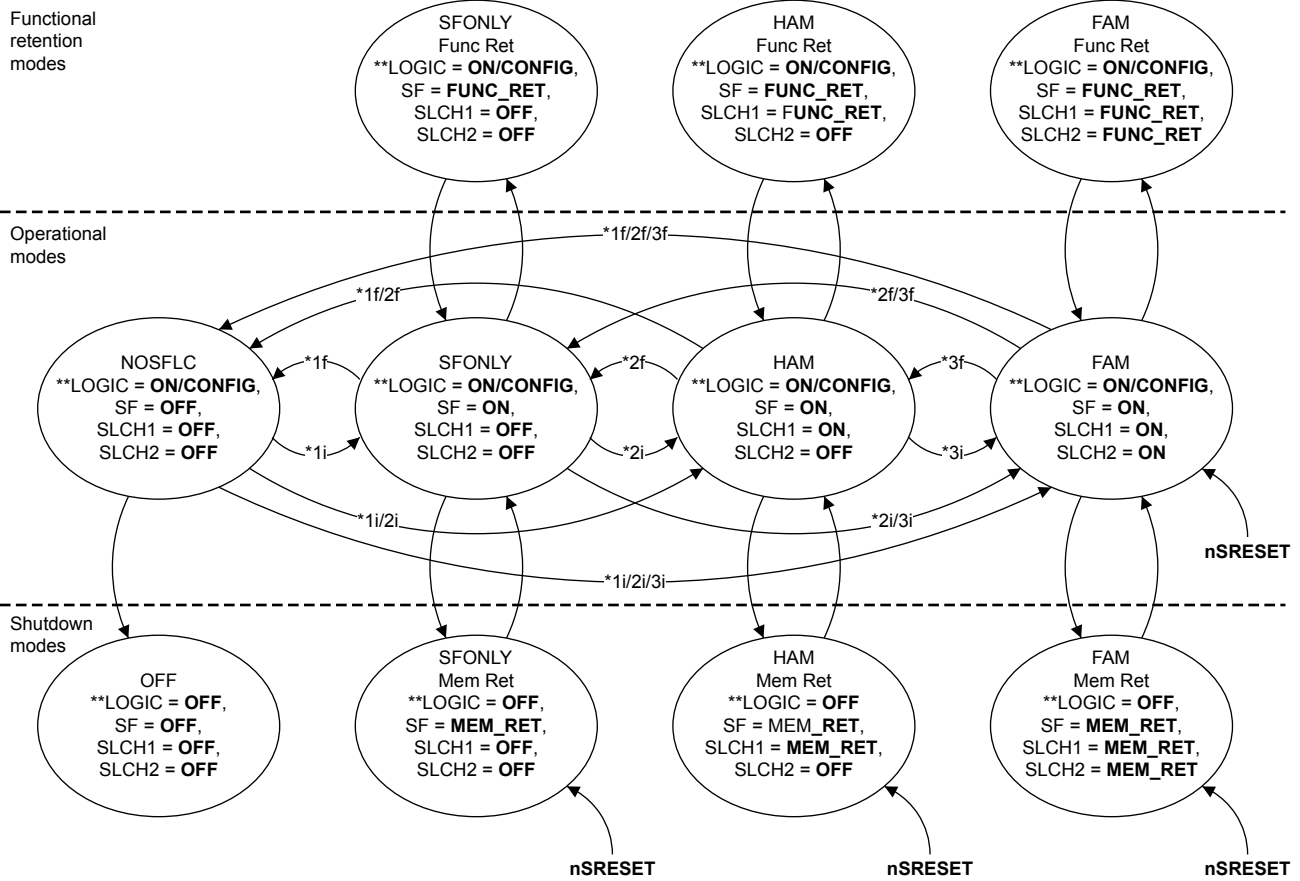
- If SLC size is 0KB, the HN-F does not support transitions to FAM or HAM modes.
- After initialization, the power status register indicates FAM instead of SFONLY for 0KB SLC configurations.
- When a power transition is initiated, another must not be initiated until the first one completes.

The following table shows the valid HN-F power states and their requirements.

Table 2-40 HN-F power states

State	Description	Control logic	SF power state	SLC way[7:0] power state	SLC way[15:8] power state
FAM	Full Run mode	On	On	On	On
HAM	Run mode with SLCH2 (SLC upper ways) disabled.	On	On	On	Off
SF	Run mode with SLCH1 and SLCH2 disabled.	On	On	Off	Off
NOSFSLC	Run mode with SLCH1, SLCH2, and SF disabled.	On	Off	Off	Off
FAM FUNC_RET	Run mode with SLCH1, SLCH2, and SF in dynamic retention.	On	Retention	Retention	Retention
HAM FUNC_RET	Run mode with SLCH1 and SF in retention, and SLCH2 in power down.	On	Retention	Retention	Off
SF FUNC_RET	Run mode with SF in retention, and SLCH1 and SLCH2 in power down.	On	Retention	Off	Off
FAM MEM_RET	Shut down with SLCH1, SLCH2, and SF in retention	Off	Retention	Retention	Retention
HAM MEM_RET	Shut down with SLCH1 and SF in retention, and SLCH2 in power down	Off	Retention	Retention	Off
SF MEM_RET	Shut down with SF in retention, and SLCH1 and SLCH2 in power down	Off	Retention	Off	Off
OFF	Shutdown	Off	Off	Off	Off

The following figure shows the valid power states and transitions for a CMN-600AE system.



Note: **BOLD** text shows the required power state.

- * Automatic initialization and flushing actions:
- 1i: Initialize snoop filter RAMs.
 - 2i: Initialize lower ways of tag RAMs.
 - 3i: Initialize upper ways of tag RAMs.
 - 1f: Flush (force back-invalidations as necessary and invalidate) snoop filter RAMs.
 - 2f: Flush (clean/invalidate) lower ways of tag/data RAMs.
 - 3f: Flush (clean/invalidate) upper ways of tag/data RAMs.

** All designations refer to P-state values required to enter the respective state.

Figure 2-57 Power state transitions

These HN-F power states are transitioned using configuration register writes that must target all HN-Fs in the SCG region. Also, the logic domain P-Channel interface can initiate a NOSFSLC→FAM transition.

To transition HN-F partitions to a required power state, write to the following `por_hnf_ppu_pwpr` register fields:

- `policy`
- `op_mode`

When the power state transition is complete, the following `por_hnf_ppu_pwsr` register fields are updated:

- `pow_status`
- `op_mode_status`

If either the SLC, the SF, or both are flushed as part of a power transition, then the power state transition can take many thousands of clock cycles. Also, the **INTREQPPU** interrupt output can be used to indicate the completion of the HN-F power state transitions.

From the FAM, HAM, or SFONLY modes, the HN-F can enter a dynamic retention mode using configuration register writes, where:

- The logic power is on
- The voltage to the RAMs is on, but is reduced to a level that is sufficient for bitcell retention but insufficient for normal operation
- The array pipeline is blocked, and a handshake occurs to allow array access when exiting the retention state

These dynamic power transitions are executed autonomously within each HN-F partition. Each HN-F has a programmable idle cycle counter and initiates a P-Channel handshake with the corresponding RAMs to enter the dynamic retention state. The pipeline then blocks transactions that target the HN-F RAMs. A coherent transaction triggers an exit from the dynamic retention state, initiates another P-Channel handshake, and takes the RAMs out of dynamic retention mode.

From these states, the SLC can also enter a Memory retention mode, where:

- The logic power is turned off
- The voltage to the RAMs is on, but is reduced to a level that is sufficient for bitcell retention but insufficient for normal operation
- Reset deassertion is essential when exiting retention after logic power down

A P-Channel interface controls the CMN-600AE logic domain power state. This P-Channel interface also interacts with the HN-F power control logic using an internal bus. The HN-F power control logic waits for a command on the deassertion of **nSRESET**, depending on the overall power state transition that is required. For the Cold reset HN-F FAM transition case, the PCCB block initiates the HN-F NOSFSLC→FAM command. To exit static retention cases, the SCP initiates configuration register writes to the HN-F to indicate the HN-F power state.

The circumstances where the HN-F enters dynamic retention modes or static retention modes are different. Dynamic retention is entered because of a dynamic activity or inactivity indicator from the HN-F to the SoC. This indicator is an output of the HN-F, and is used to determine periods of inactivity long enough to warrant entering retention mode. However the inactivity is either not long enough or not the type of inactivity to make the SoC place the SLC and SF into static retention. In addition to the static retention modes, the control logic can be powered down from the NOSFSLC state, at which point CMN-600AE is fully off.

The HN-Fs automatically perform all activity that is required to enable safe transition between the respective power states in response to input P-Channel PSTATE transitions. It is not necessary for the SoC logic to perform any extra activity to enable transitions between power states. For example, the HN-F performs clean and invalidation of half of the ways of the SLC and clean and invalidation of all ways of the SLC. This clean and invalidation activity occurs as required by the respective power state transitions.

Note

CMN-600AE cannot make any power transitions while the control logic is powered off. Consider a transition from FAM static retention to OFF. To complete this transition, the power state must first move through FAM and NOSFSLC states while the LOGIC power domain is on. These transitions allow the SLC and SF to be flushed.

The following table shows the PSTATE encodings for the HN-F and power domains including RAM configurations for the different operational modes.

Note

HN-F cannot process any transactions while in static retention (FUNC_RET or MEM_RET). HN-F must be in the ON state before sending any transactions to HN-F in this case. If HN-F is in dynamic retention, any activity autonomously takes HN-F out of dynamic retention.

Table 2-41 Power modes, operational modes, and RAM configurations

Operational mode	Power mode	PSTATE	Bank 0 RAM	Bank 1 RAM	SF RAM
FAM	ON	11_1000	ON	ON	ON
	FUNC_RET	11_0111	RET	RET	RET
	MEM_RET	11_0010	RET	RET	RET
HAM	ON	10_1000	ON	OFF	ON
	FUNC_RET	10_0111	RET	OFF	RET
	MEM_RET	10_0010	RET	OFF	RET
SFONLY	ON	01_1000	OFF	OFF	ON
	FUNC_RET	01_0111	OFF	OFF	RET
	MEM_RET	01_0010	OFF	OFF	RET
NOSFSLC	MEM_OFF	00_0110	OFF	OFF	OFF
	OFF	00_0000	OFF	OFF	OFF

2.26.8 HN-F RAM Power Control State Machine interface

Each HN-F RAM interface contains a *Power Control State Machine* (PCSM).

The following items depend on the completion of all P-Channel transactions:

- Each PCSM P-Channel interface that can be used to convert power state transitions into technology-specific controls
- The overall HN-F partition power state transition

The following table lists the valid **PSTATE** values for this interface.

Table 2-42 PSTATE Encodings

PSTATE	Value
ON	0b1000
FUNC_RET	0b0111
MEM_RET	0b0010
OFF	0b0000

Note

This interface does not have a **PDENY** signal.

2.26.9 HN-F power domain completion interrupt

The PCCB can be configured to generate an **INTREQPPU** interrupt on completion of power state transitions for a collection of HN-Fs.

The PCCB contains a global status register, `por_ppu_int_status`, which indicates HN-F power state transition completion. The PCCB also contains a mask register, `por_ppu_int_mask`, which allows filtering on all or a subset of the HN-Fs in the CMN-600AE configuration. The bit positions in the `por_ppu_int_status` and `por_ppu_int_mask` registers correspond to the logical ID of the HN-Fs.

INTREQPPU asserts when the HN-F power transition completion sets all `por_ppu_int_status` register bits and the corresponding `por_ppu_int_mask` register bit.

To deassert **INTREQPPU**, write 1 to the bits of the `por_ppu_int_status` register that correspond to the masked group of HN-Fs that completed the power transitions.

2.27 RN entry to and exit from Snoop and DVM domains

CMN-600AE includes a feature that allows RNs to be included or excluded from the system coherency domain. This domain is also known as the Snoop domain or DVM domain. This feature ensures correct operations of Snoops and DVMs when:

- An RN is taken out of reset.
- An RN is powered down and then later powered up.

RN-Fs behave as follows:

- If an RN-F is included in the system coherency domain, it must respond to Snoop and DVM requests from CMN-600AE.
- If an RN-F is excluded from the system coherency domain, it does not receive Snoop or DVM requests from CMN-600AE.

RN-Ds behave as follows:

- If an RN-D is included in the system coherency domain, it must respond to DVM requests from CMN-600AE.
- If an RN-D is excluded from the system coherency domain, it does not receive DVM requests from CMN-600AE.

This section contains the following subsections:

- [2.27.1 Hardware interface on page 2-151.](#)
- [2.27.2 Software interface on page 2-152.](#)

2.27.1 Hardware interface

This section describes the hardware interface for RN inclusion into and exclusion from system coherency domain.

CMN-600AE provides two signals for RN system coherency entry and exit:

- **SYSCOREQ** input (to CMN-600AE)
- **SYSCOACK** output (from CMN-600AE)

These two signals implement a four-phase handshake between the RN and CMN-600AE with four states. The following table describes this handshake.

Table 2-43 RN system coherency states

SYSCOREQ	SYSCOACK	State
0	0	DISABLED
1	0	CONNECT
1	1	ENABLED
0	1	DISCONNECT

Coming out of reset, the RN is in the DISABLED system coherency state.

CONNECT

To enter system coherency, an RN must assert **SYSCOREQ** and transition to the CONNECT state. The RN must be ready to receive and respond to Snoop and DVM requests in this state.

ENABLED

Next, CMN-600AE asserts **SYSCOACK** and transitions to the ENABLED state. The RN is now included in the system coherency domain. The RN can receive and must respond to Snoop and DVM requests in this state.

DISCONNECT

When the RN is ready to exit system coherency, it must deassert **SYSCOREQ** and transition to the DISCONNECT state. The RN continues to receive and must respond to Snoop and DVM requests in this state.

DISABLED

When all outstanding Snoop and DVM responses have been received, CMN-600AE deasserts **SYSCOACK** and transitions to the DISABLED state. In this state, no snoop or DVM transactions are sent to the RN which can now be powered down.

The following rules must be obeyed to adhere to the four-phase handshake protocol.

- When **SYSCOREQ** is asserted, it must remain asserted until **SYSCOACK** is asserted.
- When **SYSCOREQ** is deasserted, it must remain deasserted until **SYSCOACK** is deasserted.

2.27.2 Software interface

This section describes the software interface for RN inclusion into and exclusion from system coherency domain.

CMN-600AE provides two configuration registers for system coherency entry and exit:

- | | |
|-------------|---|
| RN-F | <ul style="list-style-type: none"> • <code>por_mxp_p{1,0}_syscoreq_ctl</code> • <code>por_mxp_p{1,0}_syscoack_status</code> |
| RN-D | <ul style="list-style-type: none"> • <code>por_rnd_syscoreq_ctl</code> • <code>por_rnd_syscoack_status</code> |

Reading and writing to these configuration registers provides a software alternative to the four-phase hardware handshake.

————— Note —————

It is possible the configuration registers contain multiple bits where each bit corresponds to a different RN. The following description is about the read and write of the configuration register bit that corresponds to a given RN. When configuring the system coherency entry or exit for a given RN, software must adopt a Read-Modify-Write strategy. This strategy ensures configuration register bits corresponding to other RNs are not modified when writing into the `syscoreq_ctl` configuration register.

Coming out of reset, both configuration registers are cleared, indicating DISABLED state.

CONNECT

To initiate an RN entry into the system coherency domain, software must first poll both configuration registers. This poll ensures the configuration register bits corresponding to that RN are set to 0. When the RN is ready to receive and respond to Snoop and DVM requests, software must write a 1 into the corresponding bit in the `syscoreq_ctl` configuration register. This write process transitions the RN to CONNECT state.

ENABLED

Next, CMN-600AE indicates a transition to ENABLED state by setting the corresponding configuration register bit in the `syscoack_status` register to 1. The RN is now inside the system coherency domain. Software can poll the `syscoack_status` register to determine this state transition.

DISCONNECT

To initiate an RN exit from the system coherency domain, software must first poll both configuration registers. After ensuring that the configuration register bits corresponding to that RN are set, software must clear the corresponding `syscoreq_ctl` bit to transition the RN to DISCONNECT state. The RN continues to receive and must respond to Snoop and DVM requests in this state.

DISABLED

When all outstanding Snoop and DVM responses have been received, CMN-600AE clears the corresponding syscoack_status bit indicating the transition to DISABLED state. In this state, no Snoop or DVM transactions are sent to the RN. Software must poll the syscoack_status register to ensure that this state transition has occurred before initiating RN powerdown.

Note

To adhere to the four-phase handshake protocol, the following rules apply:

- The hardware interface is intended as the primary interface. The software interface is provided as an alternative for legacy RN devices and systems that do not support the hardware interface.
 - Either the hardware interface or the software interface must be used, but not both. Coming out of reset, the hardware interface is enabled by default. The first write into the syscoreq_ctl register disables the hardware interface and enables the software interface. There must be a reset to re-enable hardware interface.
 - When the software interface is employed, **SYSCOREQ** must remain deasserted.
 - When the hardware interface is employed, software must not write to the syscoreq_ctl configuration register.
-

2.28 Link layer

CMN-600AE provides link initialization, flow-control, and link deactivation functionality at the RN-F and SN-F device interfaces.

This functionality comprises the following mechanisms:

- A link initialization mechanism by which the receiving device communicates link layer credits, on each CHI channel that is present, to a transmitting device.
- A flow-control mechanism by which the transmitting device uses link layer credits to send CHI flits. The transmitting device uses one credit per flit. The receiving device sends these credits back to the transmitting device, one at a time, after processing each flit. Subsequent flit transfers can then occur.

Note

This section refers to the credit roundtrip latency. This latency is measured in clock cycles, and is between:

1. The time a transmitting device uses a link layer credit to send a flit to the receiving device.
2. The earliest time when the transmitting device can receive that credit back from the receiving device and send a subsequent flit.

- A link deactivation mechanism. The transmitting device sends all unused link layer credits on each CHI channel back to the receiving device by sending corresponding link flits.

On flit upload channels, RN-F or SN-F is the transmitting device and CMN-600AE is the receiving device. On flit download channels, CMN-600AE is the transmitting device and RN-F or SN-F is the receiving device.

For a description of the functional requirements of the CHI link layer, see the *Arm® AMBA® 5 CHI Architecture Specification*.

This section contains the following subsection:

- [2.28.1 Flit buffer sizing requirements on page 2-154](#).

2.28.1 Flit buffer sizing requirements

There are specific size requirements for the CMN-600AE flit buffers.

Flit buffer sizing at a receiving device is based on the following two factors:

1. A transmitting device must be able to send flits continuously in a pipelined fashion without stalling due to insufficient link layer credits from the receiving device. This requirement ensures that the system can achieve the full link bandwidth. For a specific system, there is a minimum number of link layer credits that are required so that pipeline stalls can be prevented. You can use the credit roundtrip latency between the transmitting device and receiving device as a measure of the required number of link layer credits.
2. A receiving device must be able to accept and process as many flits as the number of link layer credits it has outstanding at the transmitting device. Therefore, the number of link layer credits that a receiving device sends must not exceed its flit buffering and processing capabilities.

Therefore, flit buffer sizing and corresponding link layer crediting must reflect the credit roundtrip latency. If this requirement is met, the system can achieve optimal flit transfer bandwidth between transmitting and receiving devices. For more information about flit buffer sizing and link layer crediting for flit uploads and downloads at RN-F and SN-F interfaces, see the following sections:

- [Flit uploads from RN-F or SN-F on page 2-154](#)
- [Flit downloads at RN-F or SN-F on page 2-155](#)

Flit uploads from RN-F or SN-F

For flit uploads, the `RXBUF_NUM_ENTRIES` parameter specifies the number of flit buffers in CMN-600AE.

For more information about `RXBUF_NUM_ENTRIES`, refer to .

For optimal flit transfer bandwidth, this parameter must be set equal to the upload credit roundtrip latency, UpCrdLat<ch>. Use the following equation to calculate UpCrdLat<ch>:

$UpCrdLat<ch> = UpCrdLatInt<ch> + UpCrdLatExt<ch>$, where:

- <ch> is the CHI channel (REQ, RSP, SNP, or DAT).
- UpCrdLatInt<ch> is the upload credit latency inside CMN-600AE. This latency is measured in clock cycles between the following time points:
 1. The time that the RN-F or SN-F asserts the RX<ch>FLITV input for a flit that is uploaded to CMN-600AE.
 2. The earliest time when CMN-600AE asserts the RX<ch>LCRDV output to the RN-F or SN-F after the flit is processed and the credit sent back.
 At the RN-F and SN-F interfaces, UpCrdLatInt<ch> = 1 on all CHI channels.
- UpCrdLatExt<ch> is the upload credit latency outside CMN-600AE. This latency is measured in clock cycles between the following time points:
 1. The time that CMN-600AE asserts the RX<ch>LCRDV output when the credit is sent back to the RN-F or SN-F.
 2. The earliest time when the RN-F or SN-F asserts the RX<ch>FLITV input when the credit is used to send a subsequent flit.

Flit downloads at RN-F or SN-F

For optimal flit downloads, the RN-F or SN-F must size its input buffers to reflect the download credit roundtrip latency, DnCrdLat<ch>.

Use the following equation to calculate DnCrdLat<ch>:

$DnCrdLat<ch> = DnCrdLatInt<ch> + DnCrdLatExt<ch>$, where:

- <ch> is the CHI channel (REQ, RSP, SNP, or DAT)
- DnCrdLatInt<ch> is the download credit latency inside CMN-600AE. This latency is measured, in clock cycles, between the following time points:
 - The time that the RN-F or SN-F asserts the RX<ch>LCRDV input to CMN-600AE
 - The earliest time when CMN-600AE asserts the RX<ch>FLITV output to the RN-F or SN-F for a flit using that credit. At the RN-F or SN-F interfaces, DnCrdLatInt<ch> = 2 on all CHI channels.
- DnCrdLatExt<ch> is the download credit latency outside CMN-600AE. This latency is measured, in clock cycles, between the following time points:
 - The time that CMN-600AE asserts the RX<ch>FLITV output for a flit downloaded to the RN-F or SN-F
 - The earliest time when RX<ch>LCRDV input is asserted when the RN-F or SN-F returns the corresponding credit to CMN-600AE

Note

When MPU is enabled, an extra cycle of latency is present in the SNP flit path to RN-Fs.

2.29 CML Symmetric Multiprocessor support

A *Symmetric Multiprocessor* (SMP) allows for a shared, common OS and memory to operate on multiple chips.

CML supports SMP systems if the systems were built using CMLs generated by CMN-600AE.

When set, the provided SMP mode option enables DVM, GIC-D, Exclusives, and CPU-Event communication across CCIX links using micro-architected mechanism.

Microarchitecture support for propagating Trace Tag across CCIX links (called Remote Trace Tag) is also enabled in SMP mode only. Propagation of Remote Trace Tag is achieved by the sender CXG only on the outgoing CCIX request, and by the receiving CXG only from the incoming CCIX request. This feature ensures all subsequent CCIX messages that are part of the same transaction use the same CCIX TxnID. Similarly, the sender CXG only completes propagation of remote Trace Tag on the outgoing CCIX Snoop, and the receiving CXG only from the incoming CCIX snoop.

Chapter 3

Functional safety features

This chapter describes CMN-600AE safety mechanisms and associated engineering requirements.

It contains the following sections:

- [3.1 Overview on page 3-158.](#)
- [3.2 External interface protection on page 3-161.](#)
- [3.3 Internal interface protection on page 3-165.](#)
- [3.4 Logic protection on page 3-167.](#)
- [3.5 Shared RAM protection on page 3-170.](#)
- [3.6 Memory Protection Unit on page 3-172.](#)
- [3.7 Hang detector on page 3-176.](#)
- [3.8 Clock and reset protection on page 3-177.](#)
- [3.9 FuSa error reporting on page 3-181.](#)
- [3.10 Fault Management Unit on page 3-186.](#)

3.1 Overview

CMN-600AE provides several *Functional Safety* (FuSa) features to detect random hardware faults, systematic faults, and latent faults.

The FuSa features and the associated safety mechanisms are described here. The fault detection and reporting times of the safety mechanisms are specified in the *Arm® CoreLink™ CMN-600AE Safety Manual*.

The following figure shows an overview of the CMN-600AE functional safety features.

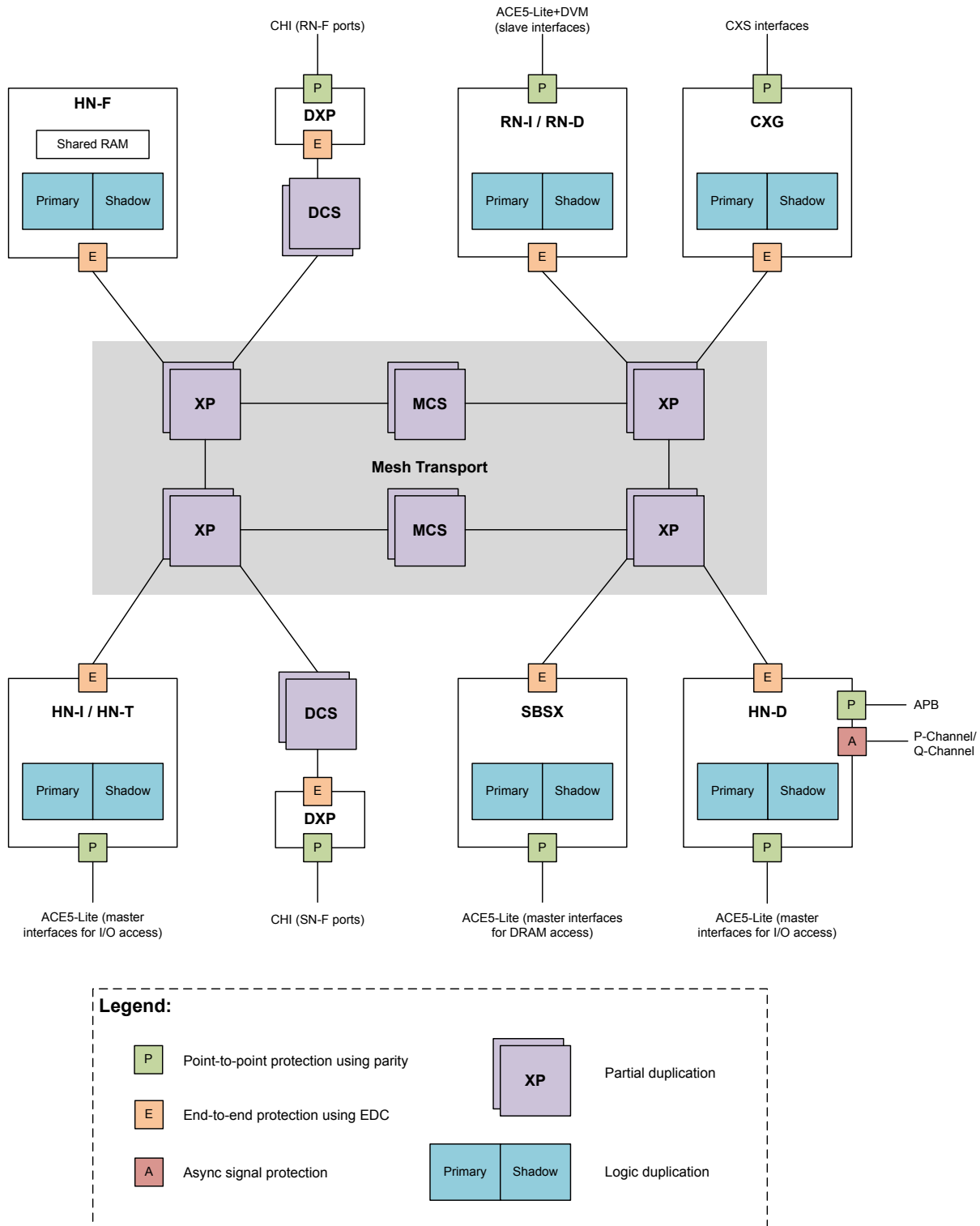


Figure 3-1 CMN-600AE functional safety features

The key functional safety features are summarized into the following categories:

Random hardware faults

The following functional safety features provide protection against random hardware faults that include transient and permanent hardware faults:

- Point-to-point protection of external interfaces.
- End-to-end protection of internal interfaces.
- Asynchronous signal protection.
- Logic protection through duplication and delayed lockstep operation.
- RAM protection using SECDED ECC with address folding.

Systematic faults

The following functional safety features provide protection against systematic faults:

- *Memory Protection Unit* (MPU).
- Transaction hang detector.

Latent faults

The following functional safety features provide protection against latent faults:

- Checker duplication.
- MBIST for RAMs.
- *Fault Management Unit* (FMU) that supports redundancy in FuSa error reporting.

3.2 External interface protection

This section describes the protection of AMBA interfaces, asynchronous interface signals, debug trace and PMU, and strap input signals.

This section contains the following subsections:

- [3.2.1 AMBA interfaces on page 3-161.](#)
- [3.2.2 Asynchronous interface signals on page 3-161.](#)
- [3.2.3 Debug trace and PMU interface on page 3-163.](#)
- [3.2.4 Strap input signals on page 3-163.](#)

3.2.1 AMBA interfaces

All external AMBA interfaces on CMN-600AE are protected as defined by the AMBA Parity Extensions. These interfaces include CHI, ACE5-Lite, AXI4-Stream, APB, and CXS interfaces.

Point-to-point protection

Point-to-point protection is sufficient for wires and buffers that cannot cause *Multiple Bit Errors* (MBEs). An example of an interconnect component that can cause MBEs is a switch. A single fault on a switch mux input can switch the wrong data, causing multiple bits to fail.

CMN-600AE supports interface parity protection for point-to-point connections from CMN-600AE to another functionally safe IP or FuSa interconnect. Interface parity errors are reported as FuSa errors.

Note

CMN-600AE can be configured with AMBA interface protection disabled to work with IPs that do not support interface parity.

Assumptions of use

Arm expects that:

- CMN-600AE is directly connected to the far-end IP with only wires and repeater buffers.
- No complex logic gates or cross bar switches exist in the path, as they could be a source of MBEs.
- The far-end IP checks the parity bits generated by CMN-600AE.
- The far-end IP generates the incoming parity bits compliant with AMBA Parity Extensions.

Details of AMBA interface signals and the corresponding parity check signals can be found in [Appendix A Signal descriptions on page Appx-A-1920](#) under the following subsections:

- [A.8 CHI interface signals on page Appx-A-1931.](#)
- [A.9 AXI and ACE-Lite interface signals on page Appx-A-1937.](#)
- [A.14 AXI4-Stream interface signals on page Appx-A-1959.](#)
- [A.16 APB interface signals on page Appx-A-1962.](#)

Details of external interface signals for the CXS interface can be found in the *AMBA® CXS Protocol Specification*.

3.2.2 Asynchronous interface signals

Asynchronous interface signals are protected by duplication with inverse polarity. The duplicated signal is referred to as the CHK signal.

Async checker

The async checker checks for faults on the asynchronous signal (**SIG**) and its CHK duplicate (**SIGCHK**). It ensures that the signal is transmitted to the primary and shadow functional blocks only when **SIG** and **SIGCHK** are both asserted or both deasserted.

Transient faults

Transient assertions or deassertions of either **SIG** or **SIGCHK** are treated as transient faults. These faults are filtered by the async checker for reliability. The protection logic prevents these faults from reaching mission mode logic and causing errors.

Permanent faults

Stuck-At Faults (SAFs) on **SIG** or **SIGCHK** are permanent faults. These faults are detected by the async checker using a SAF timeout mechanism and flagged as FuSa errors.

The functionality of the async checker is shown in the following figure.

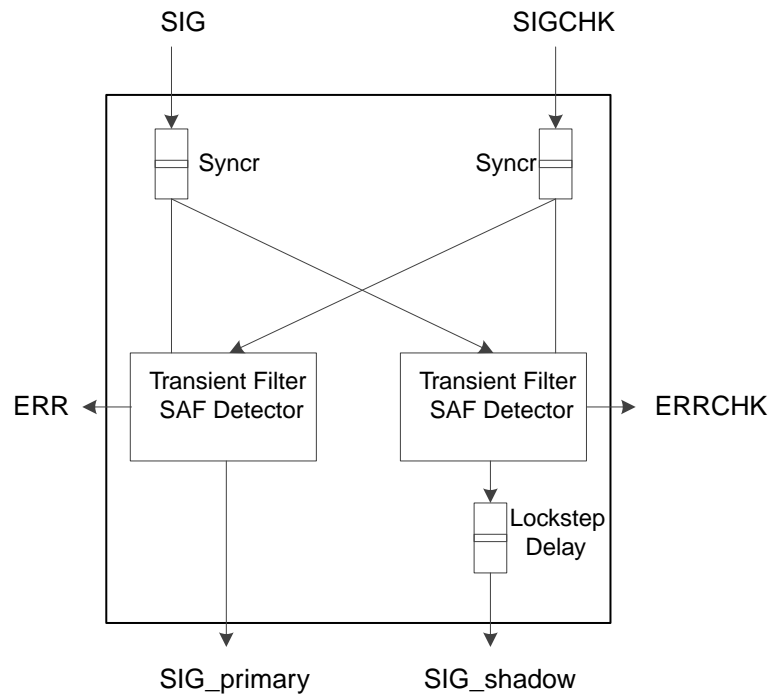


Figure 3-2 Asynchronous interface protection

CHK signal timing

The timing skew between **SIG** and **SIGCHK** must be less than the maximum that the SAF detection logic allows. The skew depends on the following factors.

Lockstep delay (D1)

Temporal skew between lockstep primary and shadow logic blocks. On CMN-600AE, the lockstep delay is set to two cycles.

SAF timeout count (T2)

SAF detector timeout count. On CMN-600AE, SAF timeout count is set to 256.

Synchronizer uncertainty delay (U2)

Uncertainty in the synchronizer delay used to synchronize **SIG** and **SIGCHK**.

Clock Ratio (CR)

Equal to (CMN-600AE clock frequency) / (external controller clock frequency).

The permitted maximum implementation skew ($S1_{max}$) between **SIG** and **SIGCHK** in external controller clock cycles is calculated as $S1_{max} = ((T2 - U2)/CR) - D1$.

Example

Assume that:

- CMN-600AE clock frequency = 2000MHz.
- External controller frequency = 50MHz.
- Synchronizer uncertainty delay (U_2) = 2.

Based on these frequencies, the CR is calculated as $CR = 2000\text{MHz}/50\text{MHz} = 40$.

The allowable skew that is permitted is:

$$S1_{\max} = ((T_2 - U_2)/CR) - D1 = ((256 - 2)/40) - 2 = \sim 4 \text{ external controller clock cycles}$$

Therefore, the SoC integrator is allowed no more than four cycles for implementation skew between **SIG** and **SIGCHK**.

Assumptions of use

Arm expects that on asynchronous interfaces:

- CMN-600AE is directly connected to the external controller or external IP block with only wires and repeater buffers.
- No complex logic gates or cross bar switches exist in the path, as they could be a source of MBEs.
- The external controller or external IP block has an async checker that checks the CHK bits generated by CMN-600AE.
- The inbound **SIG** and **SIGCHK** bits are driven within the permitted maximum implementation skew.
- FuSa error reporting is disabled before clock gating asynchronous domain crossing logic (CDB, ADB, and CXDB) to avoid spurious FuSa errors from async checkers.
- The External Clock Controller factors in both **QACTIVE** and **QACTIVECHK** signals in making clock wakeup decisions to ensure clocks are active in the presence of faults.

————— Note —————

For a valid comparison of **QACTIVE** and **QACTIVECHK** outputs, the CMN-600AE clocks must be ON.

CMN-600AE asynchronous interface signals include the following:

- [A.3 Clock management signals on page Appx-A-1923.](#)
- [A.4 Power management signals on page Appx-A-1926.](#)
- [A.5 Interrupt and event signals on page Appx-A-1928.](#)
- [A.13 Processor event interface signals on page Appx-A-1958.](#)
- [A.15 FMU interface signals on page Appx-A-1961.](#)

3.2.3 Debug trace and PMU interface

The debug trace and PMU interface signals do not have protection.

The debug trace and PMU functions must be turned off during mission critical operation and the corresponding interface signals must be in their quiescent state. Violations of these requirements are detected and reported as FuSa errors.

Assumptions of use

Arm makes the following assumptions of use:

- Debug trace and PMU functions are turned off during mission critical operation.
- Debug trace and PMU interface signals remain at their quiescent values during mission critical operation.

3.2.4 Strap input signals

All strap input signals are protected by duplication with inverse polarity.

The strap signal and its CHK equivalent are sent to the primary and shadow functional blocks, respectively. Faults on strap signals manifest themselves as output mismatches between the primary and shadow blocks.

Assumptions of use

Arm expects that strap input signals do not transition during mission critical operation.

3.3 Internal interface protection

This section describes the protection mechanisms for internal interfaces.

Mesh interfaces

Mesh components comprise XP, MCS, DCS, and DXP. They transport message flits from source devices to destination devices.

Mesh interfaces comprise interfaces that are:

- Between two mesh components. Examples include XP to XP, XP to MCS, XP to DCS, XP to DXP, and DCS to DXP.
- Between a mesh component and an internal device. Examples include XP to HN-F and DCS to RN-D.

The mesh interface consists of flit payload and routing control signals.

Flit payload protection

Flit payload signals are protected through a combination of duplication and CRC. A few predefined fields of the flit payload are duplicated and the others are protected using CRC. The signals representing the duplicated flit fields and the CRC are collectively referred to as the flit EDC. Because most of the flit is protected using CRC, the EDC width is smaller than the corresponding flit width.

Routing control protection

Routing control signals are protected by duplication.

End-to-end protection

The source device generates the flit payload and routing control. The routing control information is used by the mesh transport logic to route the flit payload through the primary mesh network to the destination device.

In parallel, the source device generates the flit EDC and duplicates the routing control. The flit EDC travels through the shadow mesh network to the destination device in lockstep with a two-cycle delay relative to the flit payload.

Checkers at the destination device compare the flit payload that is received from the primary mesh network with the flit EDC that is received from the shadow mesh network. Mismatches are flagged as FuSa errors.

Therefore, the source and destination devices on the mesh network serve as endpoints in implementing end-to-end flit payload protection through the mesh transport network.

The following figure shows the end-to-end protection on the mesh interfaces.

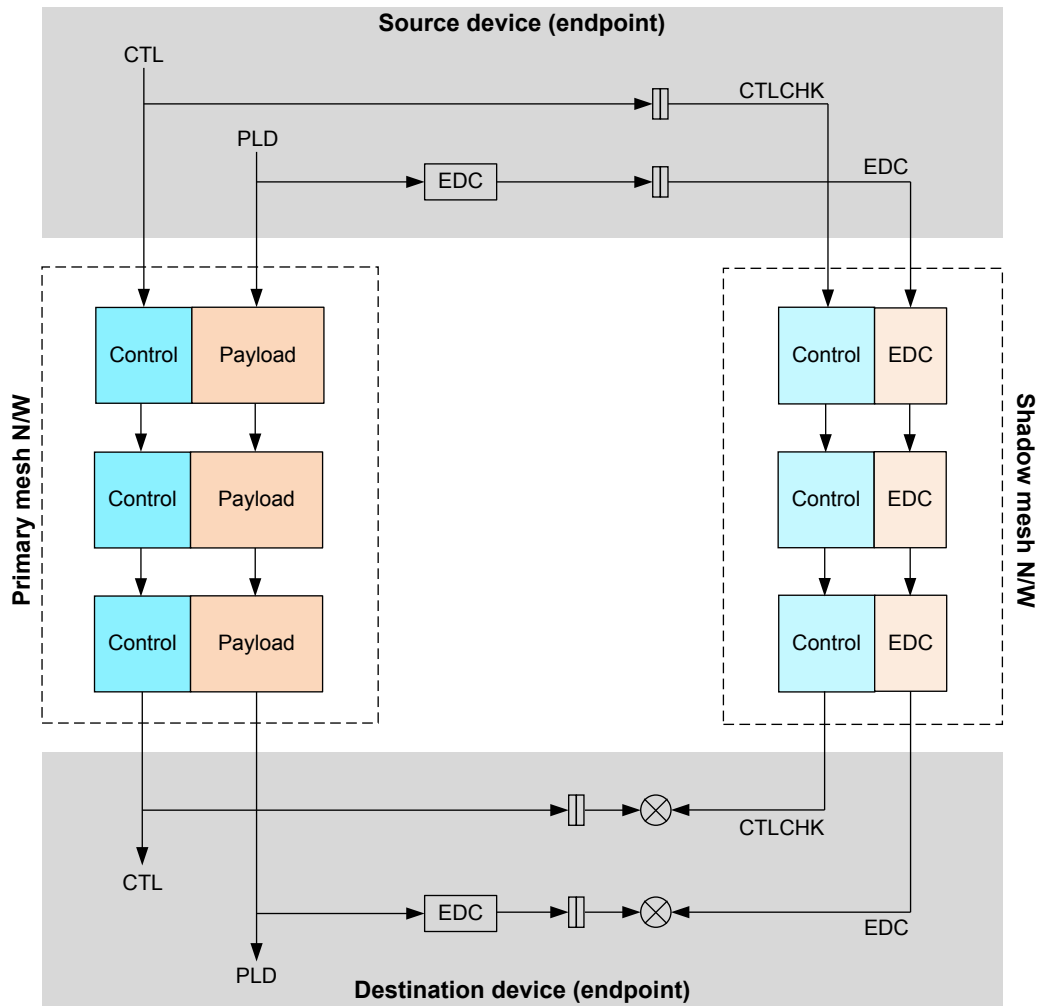


Figure 3-3 Mesh interface end-to-end protection

3.4 Logic protection

CMN-600AE functional logic is protected by duplication and lockstep checking.

The functional block is duplicated. The original block is designated as the primary block while the duplicated block is designated as the shadow block. The shadow block is operated in lockstep with the primary block, with a fixed delay of two clock cycles. The outputs of the shadow block serve as reference outputs against which the primary block outputs are checked.

The clocking and reset are also duplicated. To provide redundancy in the reset and clock trees, the primary and shadow blocks have separate clock and reset inputs. If a branch of the reset or clock tree fails in either the primary domain or the shadow domain, the other domain detects it.

For more information on reset assumptions and requirements that are related to lockstep logic and FuSa, see [3.8.2 Reset protection on page 3-178](#).

Checkers

The lockstep checkers consist of an XOR tree for comparing the outputs of the primary and shadow blocks. The same parameterized checker component is instantiated throughout the design to promote uniformity.

The checkers are known to be power hungry. To mitigate this condition, payload outputs from primary and shadow blocks are compressed into their respective 8-bit CRC values which are then compared. In addition, qualification is used wherever possible so they only check the outputs when necessary. For instance, an AXI bus checker checks the bus payload only when the valid bits are asserted. This methodology is necessary to:

- Prevent flagging errors on benign glitches on the bus payload when nothing is reading the bus.
- Prevent false error from being asserted because of UNKNOWN values on the bus, from RAMs or from uninitialized datapath flops.

Non-resettable flops

All non-resettable flops that could not be proven benign have been changed to resettable versions.

This section contains the following subsections:

- [3.4.1 Full duplication on page 3-167](#).
- [3.4.2 Duplication with shared RAM on page 3-168](#).
- [3.4.3 Partial duplication with EDC on page 3-169](#).

3.4.1 Full duplication

In this scheme, the functional block is duplicated in its entirety, including payload, datapath, and control logic.

The following figure shows the duplication of the functional block.

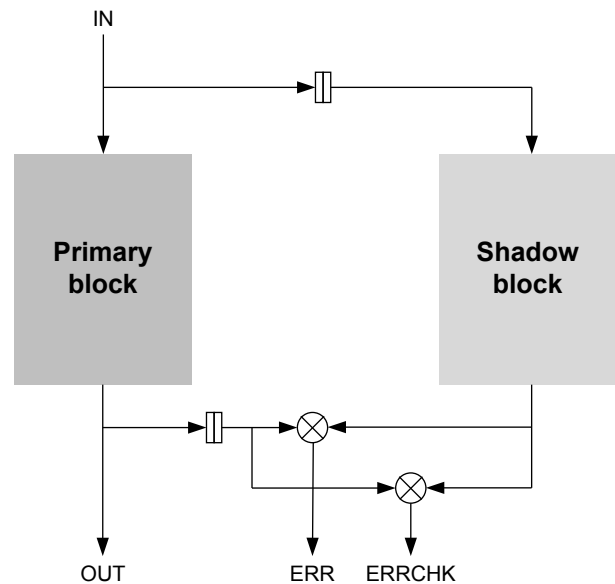


Figure 3-4 Full duplication

3.4.2 Duplication with shared RAM

This scheme is implemented in the HN-F device that contains large RAM blocks.

The HN-F functional block is repartitioned into NORAM and RAM blocks.

NORAM block Contains all functional logic, excluding the RAM instances. It is duplicated as primary and shadow blocks.

RAM block Contains all RAM instances. It is shared between the primary and shadow NORAM blocks.

The following figure shows the duplicated blocks and shared RAM.

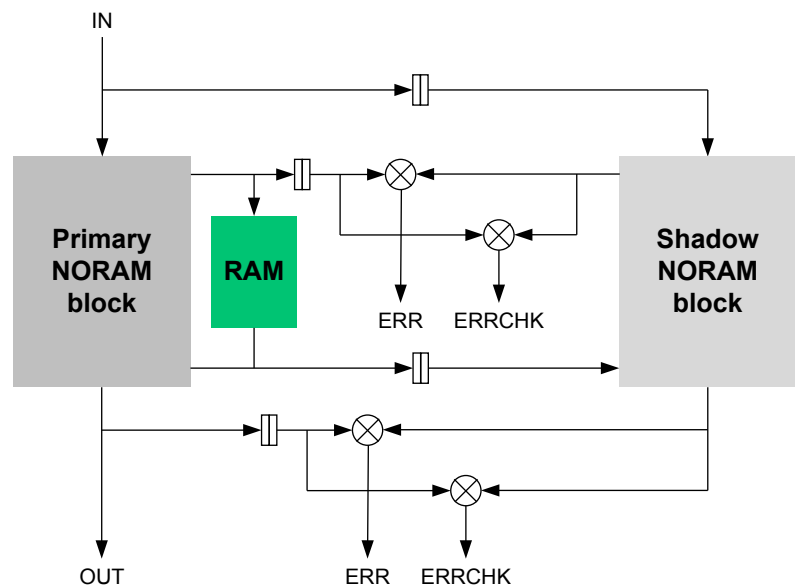


Figure 3-5 Duplication with shared RAM

The RAM blocks are protected by other means that are described in [3.5 Shared RAM protection](#) on page 3-170.

3.4.3 Partial duplication with EDC

Partial duplication with *Error Detection Code* (EDC) uses a primary block and a shadow block.

Primary block Contains the original flit payload datapath logic and routing control logic.

Shadow block Contains the EDC logic and duplicated control logic.

The following figure shows partial duplication with EDC.

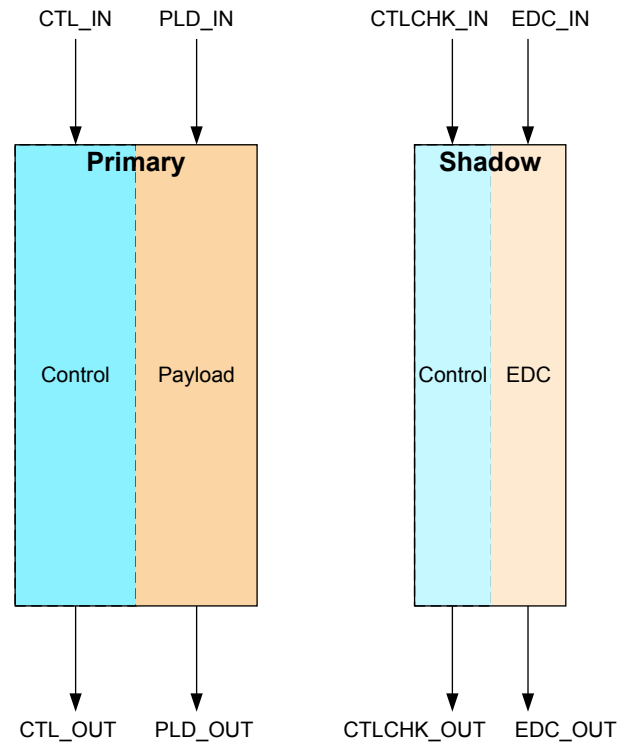


Figure 3-6 Partial duplication with EDC

Because the EDC logic is smaller than the flit payload logic, the shadow block is smaller than the primary block, which provides savings in area and power consumption.

This scheme is applicable to the XP, MCS, DCS, and DXP mesh components.

Note

Checkers for payload and control are implemented at the endpoints as shown in [Figure 3-3 Mesh interface end-to-end protection](#) on page 3-166

3.5 Shared RAM protection

The CMN-600AE HN-F RAMs inherit SECDED ECC protection from CMN-600. The address is not protected on CMN-600, so this protection is added on CMN-600AE.

Note

Shared RAM protection does not apply to CXHA RAMs, which are fully duplicated.

This section contains the following subsections:

- [3.5.1 SECDED ECC data protection on page 3-170.](#)
- [3.5.2 Address protection on page 3-170.](#)

3.5.1 SECDED ECC data protection

ECC protection is provided for HN-F RAMs that include SLC Tag RAM, SF Tag RAM, and SLC Data RAM. HN-F provides *Single-Bit Error* (SBE) correction and *Double-Bit Error* (DBE) detection.

Corrected error reporting

A corrected error (ECC_CE) can be reported to the FMU as critical or non-critical. Because the SECDED ECC algorithm cannot reliably distinguish between correctable SBEs and MBEs, ECC_CE is reported as a critical error by default. If this behavior is not required, ECC_CE reporting can be configured as non-critical by programming the FDC registers in the XP accordingly which results in the FMU generating an FHI interrupt instead of an ERI interrupt. On an FHI interrupt, error handling software can query the corrected ECC error count in the HN-F and handle the FHI as an ERI interrupt when the count exceeds a critical error threshold value.

3.5.2 Address protection

Address protection includes the protection of address decoders within the RAM decoder macro.

Because the RAM is shared, the address decoders need protection. Otherwise, faults within the RAM macro address decoder cause a *Common Mode Failure* (CMF). To achieve this protection, the ECC generation process factors in the address bits. The ECC generation for protecting the:

- SLC and SF Tag RAMs only factors in the Set Address.
- SLC Data RAMs factors in the Set Address and Way Address.

The following figure shows the address decoder protection for the SLC and SF Tag RAMs.

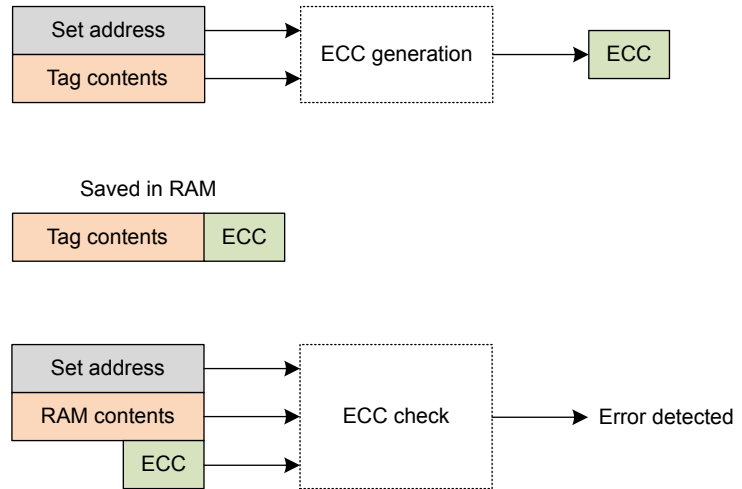


Figure 3-7 Address decoder protection for SLC and SF Tag RAMs

The following figure shows the address decoder protection for the SLC Data RAMs.

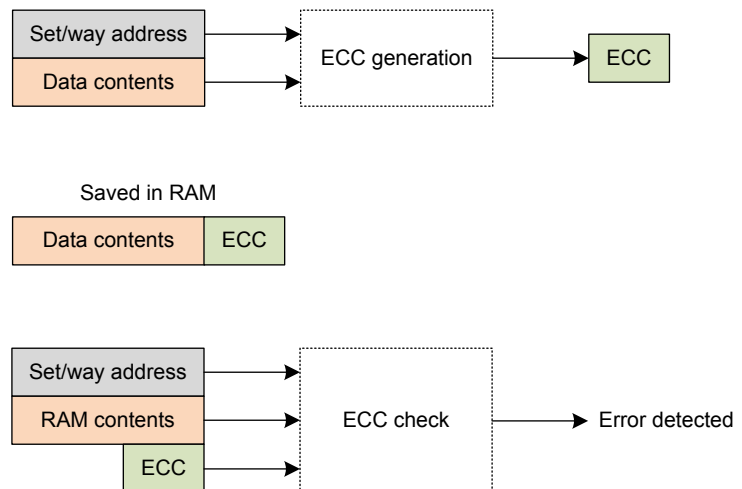


Figure 3-8 Address decoder protection for SLC Data RAMs

3.6 Memory Protection Unit

Memory Protection Units (MPUs) provide memory protection in functional safety systems that contain bus masters of different *Safety Integrity Levels* (SILs).

MPUs implement a sandbox for each unsafe bus master so that they can only access memory regions in physical address space for which they have appropriate access permissions and attributes. Virtual address space is managed by MMUs, so multiple virtual regions can exist within a single physical region.

MPUs offer protection against corrupt but protocol conforming transactions that are initiated by low integrity bus masters while maintaining system coherence. Unauthorized memory read requests are completed by returning null data while unauthorized write requests are dropped. This feature preserves the data integrity of safety critical memory in the system, allowing low integrity masters to coexist with high integrity masters in the same system without compromising the safety goals. In addition, unauthorized accesses are reported as FuSa errors or bus errors or both.

In CMN-600AE, memory protection functionality is implemented by MPU and the HNs. The MPU assigns memory access rights to individual masters which allow control of read and write access in the home nodes. In functional safety systems, MPUs can be used to assign restrictive access rights to low integrity masters to protect safety critical memory.

This section contains the following subsections:

- [3.6.1 MPU implementation on page 3-172.](#)
- [3.6.2 MPU programmers model on page 3-173.](#)
- [3.6.3 MPU programming on page 3-174.](#)
- [3.6.4 MPU with data coherence on page 3-175.](#)

3.6.1 MPU implementation

Memory Protection Units (MPUs) are located at all CMN-600AE master interfaces.

The MPUs consist of:

- Local masters at RN-F, RN-I, and RN-D interfaces.
- Remote masters at CCIX gateway (CXRH).

The location of the MPUs in an example interconnect topology is shown in the following figure.

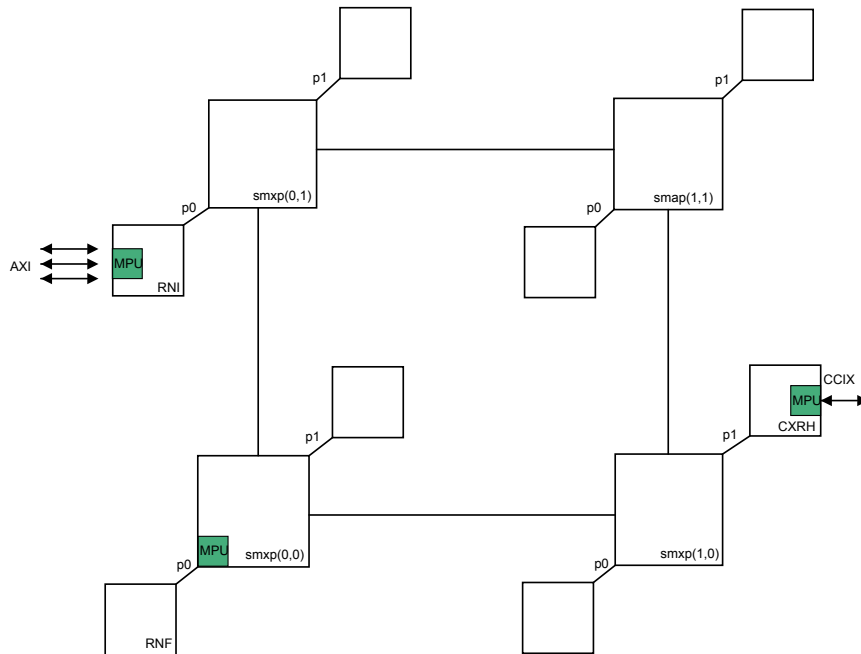


Figure 3-9 Location of MPUs in an example CMN-600AE topology

Memory access permissions can be individually configured for local masters that are connected to each RN port. For example, MPUs at RN-I and RN-D interfaces can be individually configured for three masters. In a multichip system that is built using CCIX links, MPU located in CXRH can be configured for remote masters that are based on the SMP mode as follows:

In SMP mode

Memory protection is provided by MPUs at local master interfaces (RNs) in each chip. CXRH MPU has no function.

In non-SMP mode

Memory protection from remote RNs is provided by MPU located in CXRH. In this scenario, all remote masters that are connected to that CXRH instance have the same access permissions as programmed in the CXRH MPU.

3.6.2 MPU programmers model

Memory Protection Units (MPUs) are programmable by the Safety Island.

The programmable registers within the MPU are accessible using safe APB. There is an override option to allow CHI accesses using secure override. You can program error reporting action to raise an interrupt to the Safety Island and respond with a bus error to the requestor master.

Programmable address regions

The MPU supports multiple address regions per unsafe bus master. The MPU can be configured to support 8, 16, 24, or 32 address regions. These regions can have different sizes and memory attributes. Two registers define each programmable address region:

PRBAR

The *MPU Region Base Address Register* (PRBAR) contains the fields for the lower bound address and access attributes of the region.

PRLAR

The *MPU Region Limit Address Register* (PRLAR) contains the fields for upper bound address and enables or disables control for the region.

There are N sets of these registers for the N maximum address regions that the MPU supports. Address regions are defined at 4K granularity, and range from 4KB to the maximum memory size that the system supports. The following equation provides the address that is permissible within a region:

$$\{\text{PRBAR.BASE}, 0x000\} \leq \text{Address} \leq \{\text{PRLAR.LIMIT}, 0xFFF\}$$

Primary and Background regions

A programmable address region can be one of two types. This feature enables more regions to be specified than the number of programmable regions that the MPU supports.

Background

Larger address regions with one set of attributes.
Background regions can overlap with primary regions, but must not overlap with other Background regions.

Primary

Subregions with a different set of attributes.
Primary regions must not overlap with each other. This allows carving of specific regions within the Background regions.
Primary regions have priority over Background regions.

The following figure shows two highlighted regions, pr0 and pr1. These regions can be programmed as Primary regions in two PRBAR/LRBAR register sets. The rest of the memory can be programmed as a Background region in a third register set. This method enables five different regions to be specified.

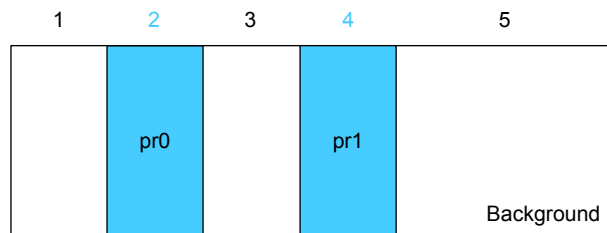


Figure 3-10 MPU Primary and Background regions

The *MPU register descriptions* section of the *Arm® CoreLink™ CMN-600AE Coherent Mesh Network Technical Reference Manual* defines the MPU configuration registers.

3.6.3 MPU programming

This section describes how to program the MPU.

The MPU can be programmed:

- At boot time.
- After the bus master is flushed and quiesced.

By default, MPUs are disabled and all masters have full access permissions. To program the MPU for a given bus master, follow these steps:

1. Determine the MPU instance corresponding to the bus master via discovery software.
2. Program the Base Address and Limit Address Registers for each address region, assigning access rights for that bus master.
3. Program the MPU control register with the error action to be taken on unauthorized access and enable the MPU.

When the MPU is enabled, subsequent transactions from that master are processed based on the programmed access permissions.

3.6.4 MPU with data coherence

In CMN-600AE, home nodes implement the MPU functionality by protecting against illegal Read or Write transactions.

For normal memory regions, where multiple CPUs (high integrity and low integrity) are coherently operating together, HN-F further protects the high integrity master from being exposed to clean or dirty data from a low integrity master. This exposure could be in the form of Snoop data intervention where the HN-F snoops a low integrity master to service a request from the high integrity master. HN-F also drops any clean victim writes from a low integrity master as they may be consumed by high integrity masters in future accesses.

For invalidating types of request opcodes, such as MakeInvalid, ReadOnceMakeInvalid and MakeUnique, HN-F converts these opcodes to non-invalidating type requests if the requestor does not have sufficient permission to the cache line. For example, MakeInvalid is converted to CleanInvalid, ReadOnceMakeInvalid is converted to ReadOnceCleanInvalid and MakeUnique is converted to CleanUnique.

3.7 Hang detector

The *hang detector* is a transaction timeout detection mechanism that is based on transaction tracker occupancy.

This mechanism detects transaction hang conditions and addresses systematic faults that are caused by incorrect programming or design errors. Hang detectors are duplicated for latent fault protection. One instance is connected to the primary block while the other instance is connected to the shadow block.

A transaction timeout value can be specified independently for each device by programming the corresponding FDC configuration register.

The following table shows the devices that use hang detectors and the corresponding transaction trackers with hang detection.

Table 3-1 Device transaction trackers with hang detection

Device	Transaction trackers
HN-F	PoC queue
HN-D	Request Tracker, Request Dispatch Tracker, DN RCB
HN-I	Request Tracker, Request Dispatch Tracker
HN-T	Request Tracker, Request Dispatch Tracker
RN-I	Read Request, Write Request
RN-D	Read Request, Write Request, Snoop queue
SBSX	Request Tracker, Dispatched ACE Request Tracker
CXG	RA Request, RA Snoop, HA Request, HA Snoop

3.8 Clock and reset protection

This section describes clock and reset protection.

This section contains the following subsections:

- [3.8.1 Clock protection on page 3-177.](#)
- [3.8.2 Reset protection on page 3-178.](#)

3.8.1 Clock protection

The clock signal is protected by a duplicate reference clock.

Clock tree duplication

Primary and shadow logic blocks within a device have their own clock trees.

Clock checker

The primary and shadow clock trees share a common root, which is the main clock input to the device, **GCLK0**. If a permanent stuck-at fault occurs on the main clock signal that is driving the clock tree root, it can affect both the primary and shadow clock trees identically.

To address this common mode issue, there is a reference clock input, **GCLK0CHK**. A clock checker uses the reference clock to check for stuck-at faults on the primary clock. If a transition is not observed within the specified timeout window, the clock checker reports a clocking error.

Note

The clock checker timeout is set to 72 cycles.

The following figure shows the clock protection mechanism.

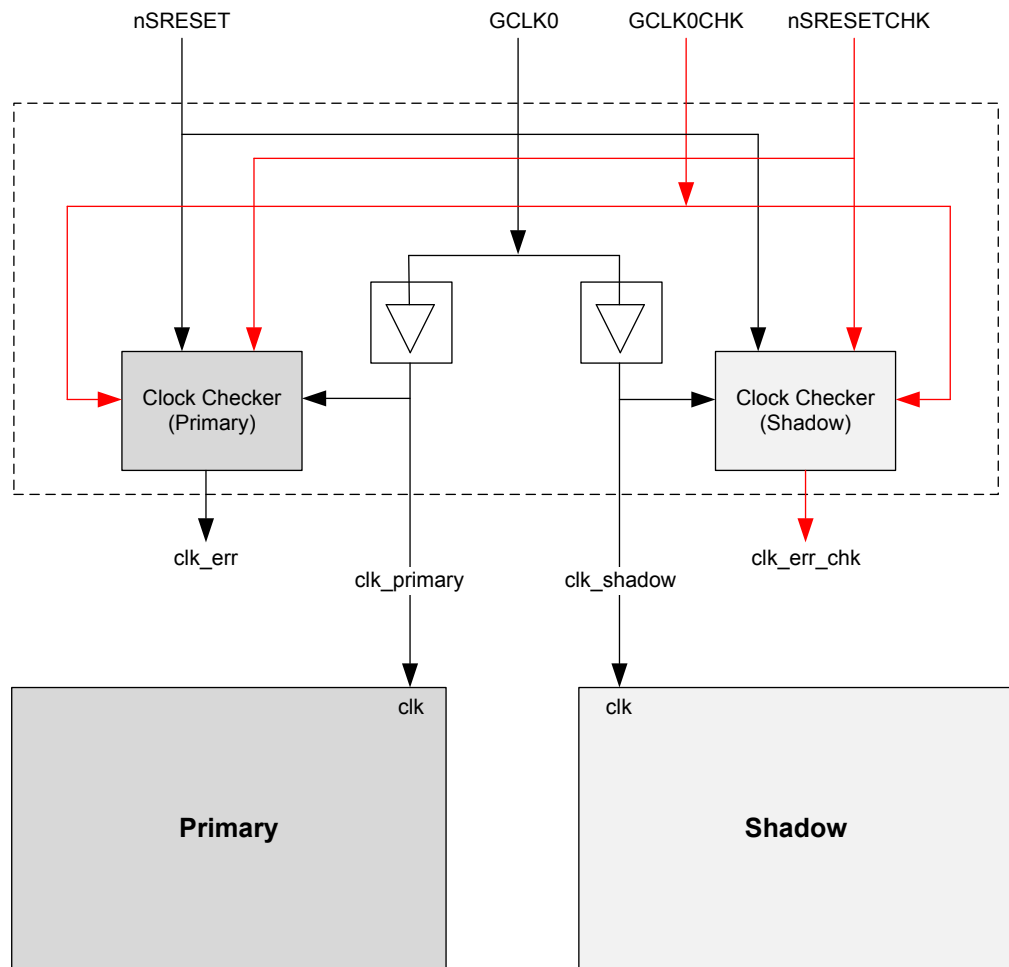


Figure 3-11 Clock protection

— Important —

The reference clock must have the same frequency as the primary clock.

3.8.2 Reset protection

The reset signal is protected by a duplicate signal check.

The reset signal, **nRESET**, is duplicated with the same polarity, **nRESETCHK**. The two reset signals are combined to generate **resetsn_primary** and **resetsn_shadow**, which are the reset signals to the primary and shadow blocks, respectively.

For the functional block reset:

- Assertion is asynchronous. This means that assertion of **resetsn_primary** and **resetsn_shadow** does not depend on the clock.
- Deassertion is synchronous. Additionally, deassertion of **resetsn_shadow** has a delay of two clock cycles after deassertion of **resetsn_primary**. This delay ensures lockstep between primary and shadow blocks coming out of reset.

Reset tree duplication

Primary and shadow logic blocks within a device have their own reset trees.

Transient fault filtering

Reset is asserted to the functional blocks only when **nRESET** and **nRESETCHK** are both asserted. This requirement provides protection from false transition of a reset signal.

Reset is deasserted to the functional blocks when either **nRESET** or **nRESETCHK** is deasserted.

Permanent faults

Stuck-at-0 faults Stuck-at-0 faults are suppressed by the reset generation logic that combines **nRESET** and **nRESETCHK**.

Stuck-at-1 faults Stuck-at-1 fault on reset prevents reset assertion to the functional blocks. A reset checker is implemented to detect this fault and flag FuSa errors.

Reset checker

The reset checker detects stuck-at-1 faults using a timeout mechanism. The reset checker timeout is set to 64 which allows a maximum allowable skew of $(64 - U1)$ clock cycles, where U1 is the uncertainty in the reset synchronizer.

Important

The skew between **nRESET** and **nRESETCHK** during reset deassertion must be less than the maximum allowable skew.

The following figure shows the clock protection mechanism.

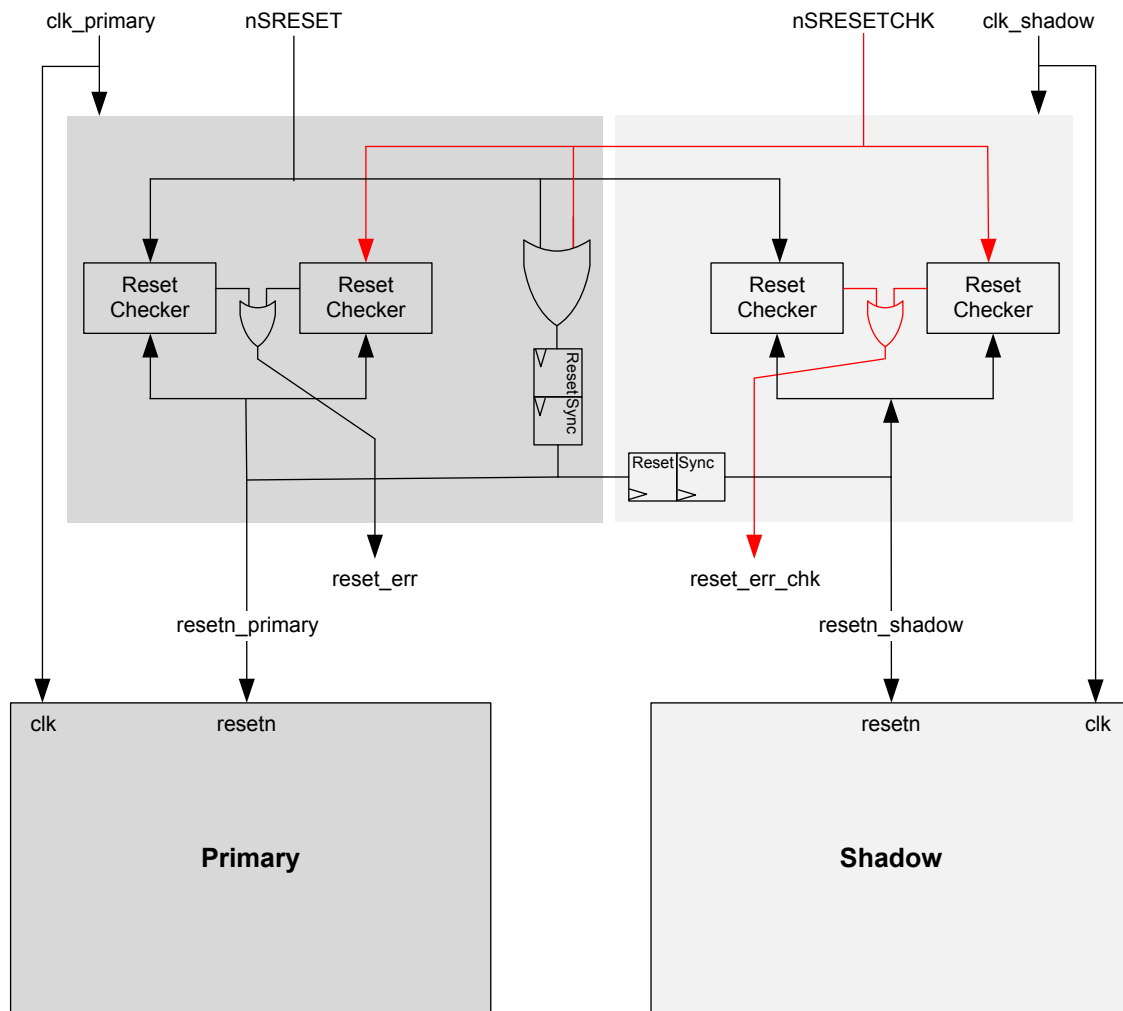


Figure 3-12 Reset protection

The following figure shows the reset timing diagram.

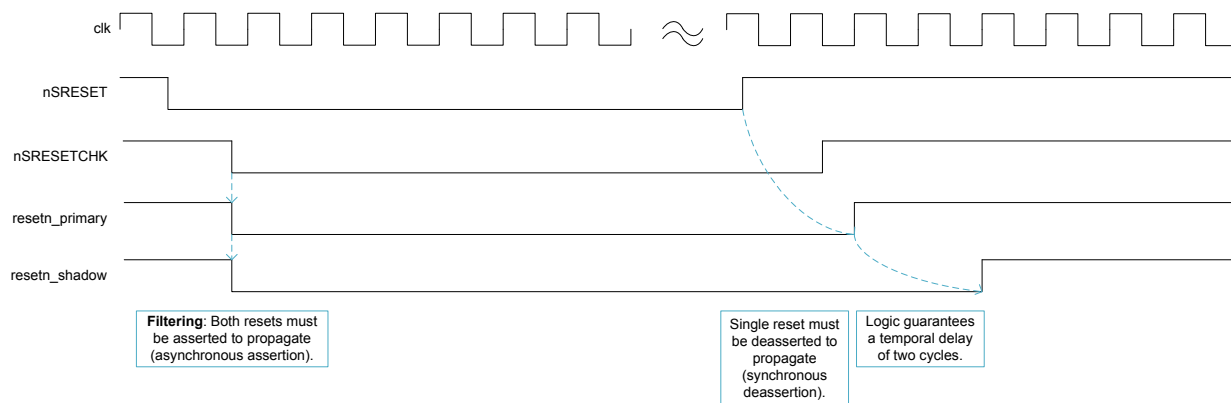


Figure 3-13 Reset timing diagram

3.9 FuSa error reporting

This section describes how FuSa errors are reported.

CMN-600AE FuSa error reporting comprises three steps:

Error aggregation

Each device contains an ERR_AGG module, which performs error aggregation. The ERR_AGG module aggregates errors from all FuSa checker outputs within the device. It classifies the errors into different error types and sends an error vector to the XP to which the device is connected.

Error logging and transmission

Error logging is done by the FDC module located inside the XP. On receiving the error vector from a device, the FDC module records the error status in a set of FDC registers, one set for each device. The error notification is then sent to the FMU on a set of dedicated wires for FuSa interrupt generation. In addition, the FDC module sends a detailed error message containing error source information to the FMU via the utility channel for diagnostic purposes.

FuSa interrupt generation

FuSa interrupts are generated by the FMU located inside the HN-D device. On receiving the error notification from FDC, the FMU signals a FuSa interrupt to the Safety Island. Subsequently, on receiving the error message from the utility channel, the FMU logs the error information in a set of error group status registers (ERRGSR).

The following figure shows the three steps that are involved in CMN-600AE FuSa error reporting.

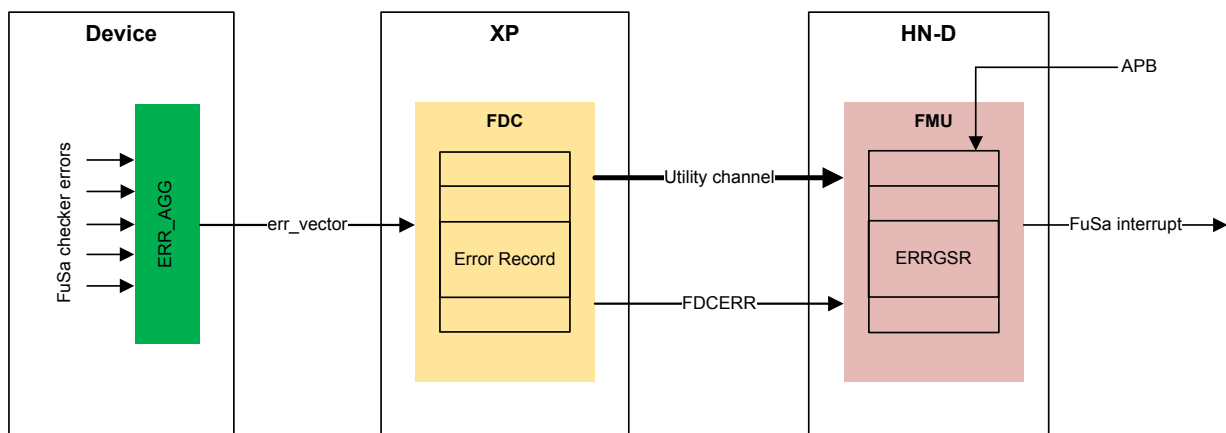


Figure 3-14 CMN-600AE FuSa error reporting

This section contains the following subsections:

- [3.9.1 Error aggregation on page 3-181.](#)
- [3.9.2 Fault Detection and Control on page 3-182.](#)
- [3.9.3 FDC registers on page 3-184.](#)
- [3.9.4 Enabling and disabling a safety mechanism on page 3-185.](#)
- [3.9.5 Clearing the ERRSTATUS on page 3-185.](#)

3.9.1 Error aggregation

The ERR_AGG module aggregates errors from different error sources and classifies them into different error types. It then creates an error vector and sends it out every cycle.

Types of FuSa errors

FuSa errors are classified into the following error types.

CLK	Clock checker error.
RST	Reset checker error.
LSC	Lockstep checker error.
IOC	External interface parity checker error.
ASYNC	Asynchronous signal checker error.
HANG	Hang detector error.
MPU	Memory protection violation error.
ECC_UE	Uncorrected ECC error.
ECC_CE	Corrected ECC error.

Error overflow

When multiple errors of the same type occur, then an overflow is signaled. There is one overflow bit for all error types.

FuSa error vector

The error vector is 10 bits wide and contains one bit for each error type and a single overflow bit. The error type bit indicates occurrence of an error of the corresponding error type. The overflow bit indicates occurrence of multiple errors of the same type. The format of the 10-bit error vector is as follows.

Table 3-2 10-bit error vector format

Bit Position	Error Type
0	CLK
1	RST
2	LSC
3	IOC
4	ASYNC
5	HANG
6	MPU
7	ECC_UE
8	ECC_CE
9	Overflow

Note

All error bits excluding CLK and RST are flopped outputs.

3.9.2 Fault Detection and Control

This section describes how the *Fault Detection and Control* (FDC) module logs and transmits errors.

The FDC module, that is located in the XP to which the device is connected, receives the FuSa error vectors that the devices send. The FDC module is responsible for logging the error status and transmitting error information to the FMU.

FDC module communicates error information to the FMU using the following mechanisms:

- Error notification using a set of dedicated wires.
- Error information transmission using the utility channel.

Error logging

There is a set of FDC registers to log the error information from each device that is connected to the corresponding XP. In addition, there is a set of FDC registers to log error information from the XP FuSa checkers. FuSa error types can be configured as critical or non-critical in the FDC registers.

Error notification

Error notification is sent on the 2-bit FDCERR bus. This method offers a dedicated path for communicating FuSa errors to the FMU.

The FDCERR bus encoding is as follows:

- FDCERR [0] for critical error signaling.
- FDCERR [1] for non-critical error signaling.

The FDCERR bits are wired-OR at each XP and transmitted to the FMU without flop stages. This method ensures that the error notification propagates to the FMU without dependencies on clock or reset.

Error transmission over utility channel

The utility channel offers a way for device-specific error details to be transmitted to the FMU. Error details such as the error source, type, and overflow information are packetized and sent on the utility channel using the mesh transport network.

The following figure illustrates the error propagation from a device to the FMU through the FDC using an example 2×2 mesh topology.

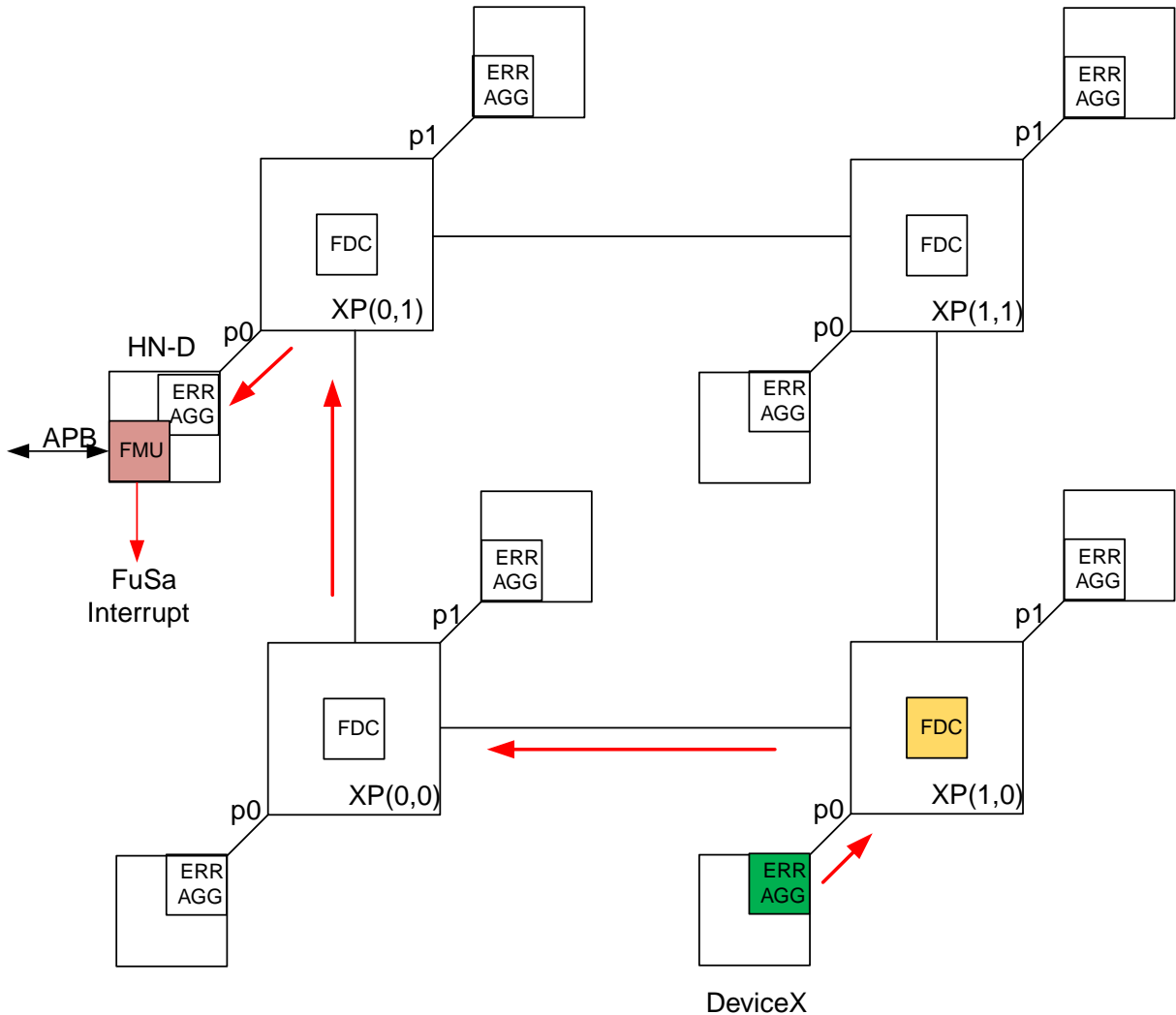


Figure 3-15 CMN-600AE error reporting in an example topology

3.9.3 FDC registers

The FDC registers are based on the RAS error registers described in the *Arm® Reliability, Availability, and Serviceability (RAS) Architecture Specification ARMv8, for the ARMv8-A architecture profile*.

FDC registers provide the following functionality:

- Error reporting control.
- Error status.
- Error injection.

Each XP has a set of dedicated FDC registers, one set for each device connected to the XP and one set for the XP itself.

FDC registers belong to one of the following register types:

- RO** Read-only.
- WO** Write-only.
- RW** Read/write.

W1C Read and write-one-to-clear. Write of zero has no effect. For exceptions, see [3.9.5 Clearing the ERRSTATUS](#) on page 3-185.

The FDC register set comprises the registers that are described in the following table.

Table 3-3 FDC register set

Register Name	Type	Description
ERRFR	RO	Specifies the supported error reporting features.
ERRCTLR	RW	Used to configure the error types as critical vs non-critical.
ERRSTATUS	W1C	Contains the error information status recorded by the FDC.
ERRINJ	WO	Used for error injection. Different types of errors can be injected into the specified interface for software testing purposes.

For more information, see [fdc_register_summary](#) on page 4-231.

3.9.4 Enabling and disabling a safety mechanism

This section describes the enabling and disabling of a safety mechanism.

Safety mechanisms and the corresponding error type reporting are enabled by default.

A safety mechanism is disabled by turning off the corresponding error type reporting in the FDC registers.

3.9.5 Clearing the ERRSTATUS

After reading the ERRSTATUS register, software must clear the valid bits in the register to allow for new errors to be recorded.

Warning

During this period, it is possible for a new error to overwrite the syndrome for the previously read error. If the register is RW, this information is lost.

To prevent this, most bits use a modified version of W1C:

- If the OF bit is set and is not being cleared, writes to the {UE, DE, CE} bits are ignored.
- If any of the {UE, DE, CE} bits are set and are not being cleared, writes to the V bit are ignored.
- If the highest priority error status bit (in priority order: UE, DE, CE) is set and not being cleared, writes to the {AV, MV} valid bits and {ER, PN, UET, IERR, SERR} syndrome fields are ignored.

This is consistent with the ERRSTATUS register definitions specified in the *Arm® Reliability, Availability, and Serviceability (RAS) Architecture Specification ARMv8, for the ARMv8-A architecture profile*.

3.10 Fault Management Unit

This section describes the functions of the *Fault Management Unit* (FMU).

The FMU is a module that is located inside HN-D. It performs the following main functions:

- Generates FuSa interrupts.
- Manages error group status registers.
- Provides APB access for error diagnosis.

This section contains the following subsections:

- [3.10.1 FuSa interrupts on page 3-186.](#)
- [3.10.2 Error Group Status Registers on page 3-186.](#)
- [3.10.3 APB Interface on page 3-187.](#)
- [3.10.4 Example FuSa error handling on page 3-187.](#)

3.10.1 FuSa interrupts

In response to an FDCERR notification, interrupts are signaled on two dedicated pins: FMU_ERI and FMU_FHI.

FMU_ERI interrupt is generated in response to critical errors. FMU_FHI interrupt is generated in response to non-critical errors. Interrupts can be disabled selectively by using the `por_fmu_ctl` configuration register.

3.10.2 Error Group Status Registers

The FMU contains *ERRor Group Status Registers* (ERRGSRs). These registers record the error source information received on the utility channel.

Each device and XP have an ERRGSR. The register mirrors the error status at the corresponding device or XP.

Example 3-1 Error Group Status Register

FMU_ERRGSR_LSC_MXP records the lockstep error status from all XPs.

The bit position corresponds to the logical ID of the XP. If FMU_ERRGSR_LSC_MXP[3] is set, there is a lockstep error status at the XP with a logical ID of 3.

nFMURESET is the dedicated reset for ERRGSRs.

At bootup, **nFMURESET** should be asserted along with the system reset. This assertion ensures that the ERRGSR state is cleared.

During error diagnosis that was prompted by a FuSa error interrupt, **nFMURESET** must remain deasserted. Even if system reset must be asserted to enable error diagnosis, this requirement preserves the ERRGSR state.

Caution

- In the XP, the contents of the FDC registers are cleared when system reset is asserted.
 - Before applying **nSRESET**, `por_fmu_ctl.fmu_errgsr_disable` should be set to 0b1 to avoid any possible data corruption on ERRGSRs.
-

For details about the ERRGSRs, see [4.3.14 FMU register descriptions on page 4-1088](#).

3.10.3 APB Interface

A dedicated APB interface is provided to the SCP to program and monitor MPU, FMU, and FDC functions.

APB can also access all CMN-600AE configuration registers.

Note

Enable RN* access to FMU, FDC, and MPU configuration registers by setting the `apb_access_override` bit in the `por_fmu_ctl` register. When not enabled, RN* writes will be silently dropped and reads return all zeros with no error indication.

A write protect mechanism is implemented to guard against spurious FDC and FMU register writes. All FDC and FMU registers are locked by default. A correct key value must be written into the `FDC_KEY` register to unlock Write-Access into the FDC registers. Likewise, a correct key value must be written into the `FMU_KEY` register to unlock Write-Access into the FMU registers. After a write, the registers are locked again. The key must be provided to unlock each subsequent write.

Note

If the correct key is not provided, writes to a locked register are silently dropped. Reads to a locked register do not require the key to be provided and return the register value normally.

3.10.4 Example FuSa error handling

This example demonstrates the FuSa error handling routine.

The following steps comprise the FuSa error handling routine.

1. Determine the FuSa error criticality. The criticality is determined by whether the error is signaled on the ERI or the FHI pin.
2. Identify the source of the error. The type and location of the error can be identified by reading the Error Global Status Registers (ERRGSR) in the FMU. The ERRGSR gives the ID of the device or XP where the FuSa error originated.

Tip



In some situations, the ERRGSR read can return all zeros. This could be due to the small delay between error interrupt pin asserting and the ERRGSR registers being written. In this case, repeat reading the ERRGSR registers one or more times until it returns a non-zero value.

If repeated reads of the ERRGSR return zeros then it could be because the FuSa error is preventing the propagation of the error status from the FDC registers within the device or XP to the ERRGSR registers in the FMU. In this case, read the FDC registers in each of the devices and the XPs to isolate the error source.

3. Clear the error log. Once the FDC within the faulty device or XP has been identified and read, the error handler should clear the FDC `ERRSTATUS` to allow for logging of new errors. See [3.9.5 Clearing the `ERRSTATUS` on page 3-185](#) for more details. Clearing the FDC error status should cause the interrupt to deassert. If the interrupt does not deassert, then it indicates either a second error occurred in the interim either in the same FDC or in a different FDC. In this case, the error handling process should be repeated for the second error.

Chapter 4

Programmer's model

This chapter describes the memory map and registers, and provides information about programming the device.

It contains the following sections:

- [4.1 About the programmers model on page 4-189.](#)
- [4.2 Register summary on page 4-192.](#)
- [4.3 Register descriptions on page 4-233.](#)
- [4.4 CMN-600AE programming on page 4-1832.](#)
- [4.5 CML programming on page 4-1834.](#)
- [4.6 Support for RN-Fs compliant with CHI Issue A specification on page 4-1845.](#)

4.1 About the programmers model

A CMN-600AE interconnect consists of various components, such as XPs, RN-Is, or DTCs, that are accessed through memory mapped registers for configuration, topology, and status information.

The memory mapped registers are organized in a series of 16KB regions. They are accessed through CHI, AXI, or APB read and write commands. APB accesses to the registers occur through the CMN-600AE HN-D APB interface.

A full description of a CMN-600AE interconnect consists of a list of components, the compile-time configuration options for each component, and the connectivity between the components. Software can determine the full configuration of the CMN-600AE interconnect through a sequence of accesses to the configuration register space.

This section contains the following subsections:

- [4.1.1 Node configuration register address mapping on page 4-189.](#)
- [4.1.2 Global configuration register region on page 4-189.](#)
- [4.1.3 XP configuration register region on page 4-190.](#)
- [4.1.4 Component configuration register region on page 4-190.](#)
- [4.1.5 Requirements of configuration register reads and writes on page 4-190.](#)

4.1.1 Node configuration register address mapping

All CMN-600AE configuration registers are mapped to an address range starting at PERIPHBASE with a maximum size of 64MB for a system with the maximum X and Y dimensions of eight or less.

The **CFGM_PERIPHBASE** input signal controls the reset value of PERIPHBASE. Configuration register accesses through the HN-D APB interface do not include the PERIPHBASE offset and the base for these accesses is zero.

All configuration, information, and status registers in a CMN-600AE interconnect are grouped into 16KB regions each associated with a CMN-600AE component instance. The base address of each region can be determined at compile time, or determined at run time through a software discovery mechanism.

Software discovery consists of three steps:

1. Read information in the 16KB region at ROOTNODEBASE. This information determines the number of XPs in CMN-600AE and the offset from PERIPHBASE for the 16KB region of each XP.
2. Read information in the 16KB region that is associated with each XP. This information determines the components that are associated with that XP, topology information for those components, and the offset from PERIPHBASE for each component 16KB region.
3. Read information in the 16KB region that is associated with the component. This information determines the type of block and the configuration details of the component.

For more information on these steps, see [2.5.4 Discovery tree structure on page 2-62.](#)

With this sequence, software can build a list of all components in the system and the addresses of their respective 16KB configuration regions.

4.1.2 Global configuration register region

The 16KB block at ROOTNODEBASE contains global information and configuration for CMN-600AE, and the first level of discovery information for components in the system.

Each XP Base Address register contains the offset from PERIPHBASE for a 16KB region that contains the information about one XP. The XP Base Address register also contains discovery information for components that are associated with that XP. The XP Base address refers to the relative address of the XP configuration registers. The first level of Discovery points to each `por_mxp_node_info` register of the XPs.

For more register information, see [4.3.1 Configuration master register descriptions on page 4-234.](#)

4.1.3 XP configuration register region

Each XP has a 16KB configuration register region with information about that XP and all associated components.

Refer to [4.3.6 XP register descriptions on page 4-640](#) for more information.

4.1.4 Component configuration register region

Each non-XP component has a 16KB configuration register region. This region has programmable information, status, and configuration options for that component.

The contents are listed in the following table, including the number of 8B registers which fit in the space.

Table 4-1 Configuration register region values

Register sections	Relative offset	Absolute offset	Description
Discovery register section			
NODE INFO (node type, node ID)	0x0	0x0	Up to 16 registers
CHILD INFO (number of children, offset of the first child pointer register = 0x100)	0x80	0x80	Up to 16 registers
CHILD POINTER registers	0x100	0x100	Up to 256 registers
UNIT REGISTER section	0x900	Unit-specific registers	
UNIT INFO	0x0	0x900	Up to 16 registers
UNIT SECURITY	0x80	0x980	Up to 16 registers
UNIT CTRL	0x100	0xA00	Up to 16 registers
UNIT QoS	0x180	0xA80	Up to 32 registers
UNIT DEBUG	0x280	0xB80	Up to 16 registers
UNIT OTHER	0x300	0xC00	Up to 128 registers
UNIT POWER	0x700	0x1000	4KB-aligned space – 512 registers
UNIT PMU	0x1700	0x2000	4KB-aligned space – 512 registers
UNIT RAS (Secure RAS registers)	0x2700	0x3000	4KB-aligned space – 512 registers
UNIT RAS (Non-secure RAS registers)	0x2800	0x3100	4KB-aligned space – 512 registers

4.1.5 Requirements of configuration register reads and writes

Reads and writes to the CMN-600AE configuration registers must meet certain requirements.

If the following requirements are not met, UNPREDICTABLE behavior can occur:

- All accesses must be of device type, either:
 - Device, Strongly Ordered.
 - nGnRE, nGnRnE.
- All accesses must have a data size of 32 bits or 64 bits.
- All accesses must be natively aligned, that is:
 - 32-bit accesses must be aligned to a 32-bit boundary.
 - 64-bit accesses must be aligned to a 64-bit boundary.
- For configuration register writes, all bits, 32 or 64, must be written, that is, all byte lanes must be valid:

- **WRSTB** must indicate that all byte lanes are valid if the write transaction is from an AMBA AXI or ACE-Lite interface.
- **BE** must indicate that all byte lanes are valid if the write transaction is sent from an AMBA 5 CHI interface.
- Secure registers can only be accessed through a Secure access, that is, NS = 0. Non-secure registers can be accessed through either a Secure or Non-secure access.

For more information on error signal handling, see [2.14 Reliability, Availability, and Serviceability](#) on page 2-80.

4.2 Register summary

This section contains summary tables for all registers in CMN-600AE.

This section contains the following subsections:

- [4.2.1 Configuration master register summary on page 4-192.](#)
- [4.2.2 DN register summary on page 4-193.](#)
- [4.2.3 Debug and trace register summary on page 4-196.](#)
- [4.2.4 HN-F register summary on page 4-197.](#)
- [4.2.5 HN-I register summary on page 4-201.](#)
- [4.2.6 XP register summary on page 4-202.](#)
- [4.2.7 RN-D register summary on page 4-205.](#)
- [4.2.8 RN-I register summary on page 4-206.](#)
- [4.2.9 RN SAM register summary on page 4-206.](#)
- [4.2.10 SBSX register summary on page 4-208.](#)
- [4.2.11 CXHA register summary on page 4-209.](#)
- [4.2.12 CXRA register summary on page 4-210.](#)
- [4.2.13 CXLA register summary on page 4-212.](#)
- [4.2.14 FMU register summary on page 4-213.](#)
- [4.2.15 MPU register summary on page 4-216.](#)
- [4.2.16 FDC register summary on page 4-231.](#)

4.2.1 Configuration master register summary

This section lists the configuration master registers used in CMN-600AE.

CFGM register summary

The following table shows the *CFGM* registers in offset order from the base memory address.

Table 4-2 CFGM register summary

Offset	Name	Type	Description
0x0	por_cfgm_node_info	RO	por_cfgm_node_info on page 4-234
0x8	por_cfgm_periph_id_0_periph_id_1	RO	por_cfgm_periph_id_0_periph_id_1 on page 4-235
0x10	por_cfgm_periph_id_2_periph_id_3	RO	por_cfgm_periph_id_2_periph_id_3 on page 4-235
0x18	por_cfgm_periph_id_4_periph_id_5	RO	por_cfgm_periph_id_4_periph_id_5 on page 4-237
0x20	por_cfgm_periph_id_6_periph_id_7	RO	por_cfgm_periph_id_6_periph_id_7 on page 4-238
0x28	por_cfgm_component_id_0_component_id_1	RO	por_cfgm_component_id_0_component_id_1 on page 4-239
0x30	por_cfgm_component_id_2_component_id_3	RO	por_cfgm_component_id_2_component_id_3 on page 4-240
0x80	por_cfgm_child_info	RO	por_cfgm_child_info on page 4-241
0x980	por_cfgm_secure_access	RW	por_cfgm_secure_access on page 4-242
0x3000	por_cfgm_errgsr0	RO	por_cfgm_errgsr0 on page 4-243
0x3008	por_cfgm_errgsr1	RO	por_cfgm_errgsr1 on page 4-244
0x3010	por_cfgm_errgsr2	RO	por_cfgm_errgsr2 on page 4-245

Table 4-2 CFGM register summary (continued)

Offset	Name	Type	Description
0x3018	por_cfgm_errgsr3	RO	por_cfgm_errgsr3 on page 4-245
0x3020	por_cfgm_errgsr4	RO	por_cfgm_errgsr4 on page 4-246
0x3080	por_cfgm_errgsr5	RO	por_cfgm_errgsr5 on page 4-247
0x3088	por_cfgm_errgsr6	RO	por_cfgm_errgsr6 on page 4-248
0x3090	por_cfgm_errgsr7	RO	por_cfgm_errgsr7 on page 4-249
0x3098	por_cfgm_errgsr8	RO	por_cfgm_errgsr8 on page 4-250
0x30A0	por_cfgm_errgsr9	RO	por_cfgm_errgsr9 on page 4-250
0x3100	por_cfgm_errgsr0_NS	RO	por_cfgm_errgsr0_NS on page 4-251
0x3108	por_cfgm_errgsr1_NS	RO	por_cfgm_errgsr1_NS on page 4-252
0x3110	por_cfgm_errgsr2_NS	RO	por_cfgm_errgsr2_NS on page 4-253
0x3118	por_cfgm_errgsr3_NS	RO	por_cfgm_errgsr3_NS on page 4-254
0x3120	por_cfgm_errgsr4_NS	RO	por_cfgm_errgsr4_NS on page 4-255
0x3180	por_cfgm_errgsr5_NS	RO	por_cfgm_errgsr5_NS on page 4-255
0x3188	por_cfgm_errgsr6_NS	RO	por_cfgm_errgsr6_NS on page 4-256
0x3190	por_cfgm_errgsr7_NS	RO	por_cfgm_errgsr7_NS on page 4-257
0x3198	por_cfgm_errgsr8_NS	RO	por_cfgm_errgsr8_NS on page 4-258
0x31A0	por_cfgm_errgsr9_NS	RO	por_cfgm_errgsr9_NS on page 4-259
0x3FA8	por_cfgm_errdevaff	RO	por_cfgm_errdevaff on page 4-260
0x3FB8	por_cfgm_errdevarch	RO	por_cfgm_errdevarch on page 4-260
0x3FC8	por_cfgm_erridr	RO	por_cfgm_erridr on page 4-261
0x3FD0	por_cfgm_errpidr45	RO	por_cfgm_errpidr45 on page 4-262
0x3FD8	por_cfgm_errpidr67	RO	por_cfgm_errpidr67 on page 4-263
0x3FE0	por_cfgm_errpidr01	RO	por_cfgm_errpidr01 on page 4-264
0x3FE8	por_cfgm_errpidr23	RO	por_cfgm_errpidr23 on page 4-265
0x3FF0	por_cfgm_errcidr01	RO	por_cfgm_errcidr01 on page 4-266
0x3FF8	por_cfgm_errcidr23	RO	por_cfgm_errcidr23 on page 4-267
0x900	por_info_global	RO	por_info_global on page 4-268
0x1000	por_ppu_int_enable	RW	por_ppu_int_enable on page 4-270
0x1008	por_ppu_int_status	W1C	por_ppu_int_status on page 4-271
0x1010	por_ppu_qactive_hyst	RW	por_ppu_qactive_hyst on page 4-272
0xCHILD_POINTER_BASE + 8×\$index	por_cfgm_child_pointer_\$index	RO	por_cfgm_child_pointer_\$index on page 4-273

4.2.2 DN register summary

This section lists the DN registers used in CMN-600AE.

DN register summary

The following table shows the *DN* registers in offset order from the base memory address.

Table 4-3 DN register summary

Offset	Name	Type	Description
0x0	por_dn_node_info	RO	por_dn_node_info on page 4-274
0x80	por_dn_child_info	RO	por_dn_child_info on page 4-275
0x900	por_dn_build_info	RO	por_dn_build_info on page 4-275
0x980	por_dn_secure_register_groups_override	RW	por_dn_secure_register_groups_override on page 4-276
0xA00	por_dn_aux_ctl	RW	por_dn_aux_ctl on page 4-277
0xC00	por_dn_vmf0_ctl	RW	por_dn_vmf0_ctl on page 4-278
0xC08	por_dn_vmf0_rnf0	RW	por_dn_vmf0_rnf0 on page 4-280
0xC10	por_dn_vmf0_rnd	RW	por_dn_vmf0_rnd on page 4-280
0xC18	por_dn_vmf0_cxra	RW	por_dn_vmf0_cxra on page 4-281
0xC20	por_dn_vmf1_ctl	RW	por_dn_vmf1_ctl on page 4-282
0xC28	por_dn_vmf1_rnf0	RW	por_dn_vmf1_rnf0 on page 4-283
0xC30	por_dn_vmf1_rnd	RW	por_dn_vmf1_rnd on page 4-284
0xC38	por_dn_vmf1_cxra	RW	por_dn_vmf1_cxra on page 4-285
0xC40	por_dn_vmf2_ctl	RW	por_dn_vmf2_ctl on page 4-286
0xC48	por_dn_vmf2_rnf0	RW	por_dn_vmf2_rnf0 on page 4-287
0xC50	por_dn_vmf2_rnd	RW	por_dn_vmf2_rnd on page 4-288
0xC58	por_dn_vmf2_cxra	RW	por_dn_vmf2_cxra on page 4-289
0xC60	por_dn_vmf3_ctl	RW	por_dn_vmf3_ctl on page 4-290
0xC68	por_dn_vmf3_rnf0	RW	por_dn_vmf3_rnf0 on page 4-291
0xC70	por_dn_vmf3_rnd	RW	por_dn_vmf3_rnd on page 4-292
0xC78	por_dn_vmf3_cxra	RW	por_dn_vmf3_cxra on page 4-293
0xC80	por_dn_vmf4_ctl	RW	por_dn_vmf4_ctl on page 4-294
0xC88	por_dn_vmf4_rnf0	RW	por_dn_vmf4_rnf0 on page 4-295
0xC90	por_dn_vmf4_rnd	RW	por_dn_vmf4_rnd on page 4-296
0xC98	por_dn_vmf4_cxra	RW	por_dn_vmf4_cxra on page 4-297
0xCA0	por_dn_vmf5_ctl	RW	por_dn_vmf5_ctl on page 4-298
0xCA8	por_dn_vmf5_rnf0	RW	por_dn_vmf5_rnf0 on page 4-299
0xCB0	por_dn_vmf5_rnd	RW	por_dn_vmf5_rnd on page 4-300
0xCB8	por_dn_vmf5_cxra	RW	por_dn_vmf5_cxra on page 4-301
0xCC0	por_dn_vmf6_ctl	RW	por_dn_vmf6_ctl on page 4-302
0xCC8	por_dn_vmf6_rnf0	RW	por_dn_vmf6_rnf0 on page 4-303
0xCD0	por_dn_vmf6_rnd	RW	por_dn_vmf6_rnd on page 4-304
0xCD8	por_dn_vmf6_cxra	RW	por_dn_vmf6_cxra on page 4-305

Table 4-3 DN register summary (continued)

Offset	Name	Type	Description
0xCE0	por_dn_vmf7_ctrl	RW	por_dn_vmf7_ctrl on page 4-306
0xCE8	por_dn_vmf7_rnf0	RW	por_dn_vmf7_rnf0 on page 4-307
0xCF0	por_dn_vmf7_rnd	RW	por_dn_vmf7_rnd on page 4-308
0xCF8	por_dn_vmf7_cxra	RW	por_dn_vmf7_cxra on page 4-309
0xD00	por_dn_vmf8_ctrl	RW	por_dn_vmf8_ctrl on page 4-310
0xD08	por_dn_vmf8_rnf0	RW	por_dn_vmf8_rnf0 on page 4-311
0xD10	por_dn_vmf8_rnd	RW	por_dn_vmf8_rnd on page 4-312
0xD18	por_dn_vmf8_cxra	RW	por_dn_vmf8_cxra on page 4-313
0xD20	por_dn_vmf9_ctrl	RW	por_dn_vmf9_ctrl on page 4-314
0xD28	por_dn_vmf9_rnf0	RW	por_dn_vmf9_rnf0 on page 4-315
0xD30	por_dn_vmf9_rnd	RW	por_dn_vmf9_rnd on page 4-316
0xD38	por_dn_vmf9_cxra	RW	por_dn_vmf9_cxra on page 4-317
0xD40	por_dn_vmf10_ctrl	RW	por_dn_vmf10_ctrl on page 4-318
0xD48	por_dn_vmf10_rnf0	RW	por_dn_vmf10_rnf0 on page 4-319
0xD50	por_dn_vmf10_rnd	RW	por_dn_vmf10_rnd on page 4-320
0xD58	por_dn_vmf10_cxra	RW	por_dn_vmf10_cxra on page 4-321
0xD60	por_dn_vmf11_ctrl	RW	por_dn_vmf11_ctrl on page 4-322
0xD68	por_dn_vmf11_rnf0	RW	por_dn_vmf11_rnf0 on page 4-323
0xD70	por_dn_vmf11_rnd	RW	por_dn_vmf11_rnd on page 4-324
0xD78	por_dn_vmf11_cxra	RW	por_dn_vmf11_cxra on page 4-325
0xD80	por_dn_vmf12_ctrl	RW	por_dn_vmf12_ctrl on page 4-326
0xD88	por_dn_vmf12_rnf0	RW	por_dn_vmf12_rnf0 on page 4-327
0xD90	por_dn_vmf12_rnd	RW	por_dn_vmf12_rnd on page 4-328
0xD98	por_dn_vmf12_cxra	RW	por_dn_vmf12_cxra on page 4-329
0xDA0	por_dn_vmf13_ctrl	RW	por_dn_vmf13_ctrl on page 4-330
0xDA8	por_dn_vmf13_rnf0	RW	por_dn_vmf13_rnf0 on page 4-331
0xDB0	por_dn_vmf13_rnd	RW	por_dn_vmf13_rnd on page 4-332
0xDB8	por_dn_vmf13_cxra	RW	por_dn_vmf13_cxra on page 4-333
0xDC0	por_dn_vmf14_ctrl	RW	por_dn_vmf14_ctrl on page 4-334
0xDC8	por_dn_vmf14_rnf0	RW	por_dn_vmf14_rnf0 on page 4-335
0xDD0	por_dn_vmf14_rnd	RW	por_dn_vmf14_rnd on page 4-336
0xDD8	por_dn_vmf14_cxra	RW	por_dn_vmf14_cxra on page 4-337
0xDE0	por_dn_vmf15_ctrl	RW	por_dn_vmf15_ctrl on page 4-338
0xDE8	por_dn_vmf15_rnf0	RW	por_dn_vmf15_rnf0 on page 4-339
0xDF0	por_dn_vmf15_rnd	RW	por_dn_vmf15_rnd on page 4-340

Table 4-3 DN register summary (continued)

Offset	Name	Type	Description
0xDF8	por_dn_vmf15_cxra	RW	por_dn_vmf15_cxra on page 4-341
0x2000	por_dn_pmu_event_sel	RW	por_dn_pmu_event_sel on page 4-342

4.2.3 Debug and trace register summary

This section lists the debug and trace registers used in CMN-600AE.

DT register summary

The following table shows the *DT* registers in offset order from the base memory address.

Table 4-4 DT register summary

Offset	Name	Type	Description
0x0	por_dt_node_info	RO	por_dt_node_info on page 4-345
0x80	por_dt_child_info	RO	por_dt_child_info on page 4-346
0x980	por_dt_secure_access	RW	por_dt_secure_access on page 4-346
0xA00	por_dt_dtc_ctl	RW	por_dt_dtc_ctl on page 4-348
0xA10	por_dt_trigger_status	RO	por_dt_trigger_status on page 4-349
0xA20	por_dt_trigger_status_clr	WO	por_dt_trigger_status_clr on page 4-350
0xA30	por_dt_trace_control	RW	por_dt_trace_control on page 4-351
0xA48	por_dt_traceid	RW	por_dt_traceid on page 4-352
0x2000	por_dt_pmeventAB	RW	por_dt_pmeventAB on page 4-353
0x2010	por_dt_pmeventCD	RW	por_dt_pmeventCD on page 4-354
0x2020	por_dt_pmeventEF	RW	por_dt_pmeventEF on page 4-354
0x2030	por_dt_pmeventGH	RW	por_dt_pmeventGH on page 4-355
0x2040	por_dt_pmcntr	RW	por_dt_pmcntr on page 4-356
0x2050	por_dt_pmeventsAB	RW	por_dt_pmeventsAB on page 4-357
0x2060	por_dt_pmeventsCD	RW	por_dt_pmeventsCD on page 4-358
0x2070	por_dt_pmeventsEF	RW	por_dt_pmeventsEF on page 4-359
0x2080	por_dt_pmeventsGH	RW	por_dt_pmeventsGH on page 4-359
0x2090	por_dt_pmcntrs	RW	por_dt_pmcntrs on page 4-360
0x2100	por_dt_pmcr	RW	por_dt_pmcr on page 4-361
0x2118	por_dt_pmovsr	RO	por_dt_pmovsr on page 4-362
0x2120	por_dt_pmovsr_clr	WO	por_dt_pmovsr_clr on page 4-363
0x2128	por_dt_pmsr	RO	por_dt_pmsr on page 4-364
0x2130	por_dt_pmsr	WO	por_dt_pmsr on page 4-365
0x2DA0	por_dt_claim	RW	por_dt_claim on page 4-366
0x2DA8	por_dt_devaff	RO	por_dt_devaff on page 4-367

Table 4-4 DT register summary (continued)

Offset	Name	Type	Description
0x2DB0	por_dt_lsr	RO	por_dt_lsr on page 4-368
0x2DB8	por_dt_authstatus_devarch	RO	por_dt_authstatus_devarch on page 4-369
0x2DC0	por_dt_devid	RO	por_dt_devid on page 4-370
0x2DC8	por_dt_devtype	RO	por_dt_devtype on page 4-371
0x2DD0	por_dt_pidr45	RO	por_dt_pidr45 on page 4-372
0x2DD8	por_dt_pidr67	RO	por_dt_pidr67 on page 4-373
0x2DE0	por_dt_pidr01	RO	por_dt_pidr01 on page 4-374
0x2DE8	por_dt_pidr23	RO	por_dt_pidr23 on page 4-375
0x2DF0	por_dt_cidr01	RO	por_dt_cidr01 on page 4-376
0x2DF8	por_dt_cidr23	RO	por_dt_cidr23 on page 4-377

4.2.4 HN-F register summary

This section lists the HN-F registers used in CMN-600AE.

HN-F register summary

The following table shows the *HN-F* registers in offset order from the base memory address.

Table 4-5 HN-F register summary

Offset	Name	Type	Description
0x0	por_hnf_node_info	RO	por_hnf_node_info on page 4-379
0x80	por_hnf_child_info	RO	por_hnf_child_info on page 4-380
0x980	por_hnf_secure_register_groups_override	RW	por_hnf_secure_register_groups_override on page 4-380
0x900	por_hnf_unit_info	RO	por_hnf_unit_info on page 4-382
0xA00	por_hnf_cfg_ctl	RW	por_hnf_cfg_ctl on page 4-383
0xA08	por_hnf_aux_ctl	RW	por_hnf_aux_ctl on page 4-385
0xA10	por_hnf_r2_aux_ctl	RW	por_hnf_r2_aux_ctl on page 4-389
0xA18	rdf_hnf_aux_ctl	RW	rdf_hnf_aux_ctl on page 4-390
0x1000	por_hnf_ppu_pwpr	RW	por_hnf_ppu_pwpr on page 4-391
0x1008	por_hnf_ppu_pwsr	RO	por_hnf_ppu_pwsr on page 4-392
0x1014	por_hnf_ppu_misr	RO	por_hnf_ppu_misr on page 4-393
0x1FB0	por_hnf_ppu_idr0	RO	por_hnf_ppu_idr0 on page 4-394
0x1FB4	por_hnf_ppu_idr1	RO	por_hnf_ppu_idr1 on page 4-396
0x1FC8	por_hnf_ppu_iidr	RO	por_hnf_ppu_iidr on page 4-397
0x1FCC	por_hnf_ppu_aidr	RO	por_hnf_ppu_aidr on page 4-398
0x1100	por_hnf_ppu_dyn_ret_threshold	RW	por_hnf_ppu_dyn_ret_threshold on page 4-398
0xA80	por_hnf_qos_band	RO	por_hnf_qos_band on page 4-399

Table 4-5 HN-F register summary (continued)

Offset	Name	Type	Description
0xA88	por_hnf_qos_reservation	RW	por_hnf_qos_reservation on page 4-400
0xA90	por_hnf_rn_starvation	RW	por_hnf_rn_starvation on page 4-402
0x3000	por_hnf_errfr	RO	por_hnf_errfr on page 4-404
0x3008	por_hnf_errctlr	RW	por_hnf_errctlr on page 4-405
0x3010	por_hnf_errstatus	W1C	por_hnf_errstatus on page 4-406
0x3018	por_hnf_erraddr	RW	por_hnf_erraddr on page 4-408
0x3020	por_hnf_errmisc	RW	por_hnf_errmisc on page 4-409
0x3030	por_hnf_err_inj	RW	por_hnf_err_inj on page 4-411
0x3038	por_hnf_byte_par_err_inj	WO	por_hnf_byte_par_err_inj on page 4-412
0x3100	por_hnf_errfr_NS	RO	por_hnf_errfr_NS on page 4-413
0x3108	por_hnf_errctlr_NS	RW	por_hnf_errctlr_NS on page 4-415
0x3110	por_hnf_errstatus_NS	W1C	por_hnf_errstatus_NS on page 4-416
0x3118	por_hnf_erraddr_NS	RW	por_hnf_erraddr_NS on page 4-418
0x3120	por_hnf_errmisc_NS	RW	por_hnf_errmisc_NS on page 4-419
0xC00	por_hnf_slc_lock_ways	RW	por_hnf_slc_lock_ways on page 4-421
0xC08	por_hnf_slc_lock_base0	RW	por_hnf_slc_lock_base0 on page 4-422
0xC10	por_hnf_slc_lock_base1	RW	por_hnf_slc_lock_base1 on page 4-423
0xC18	por_hnf_slc_lock_base2	RW	por_hnf_slc_lock_base2 on page 4-424
0xC20	por_hnf_slc_lock_base3	RW	por_hnf_slc_lock_base3 on page 4-425
0xC30	por_hnf_rni_region_vec	RW	por_hnf_rni_region_vec on page 4-426
0xC38	por_hnf_rnf_region_vec	RW	por_hnf_rnf_region_vec on page 4-427
0xC40	por_hnf_rnd_region_vec	RW	por_hnf_rnd_region_vec on page 4-428
0xC48	por_hnf_slcway_partition0_rnf_vec	RW	por_hnf_slcway_partition0_rnf_vec on page 4-429
0xC50	por_hnf_slcway_partition1_rnf_vec	RW	por_hnf_slcway_partition1_rnf_vec on page 4-430
0xC58	por_hnf_slcway_partition2_rnf_vec	RW	por_hnf_slcway_partition2_rnf_vec on page 4-431
0xC60	por_hnf_slcway_partition3_rnf_vec	RW	por_hnf_slcway_partition3_rnf_vec on page 4-431
0xC28	por_hnf_rnf_region_vec1	RW	por_hnf_rnf_region_vec1 on page 4-432
0xCB0	por_hnf_slcway_partition0_rnf_vec1	RW	por_hnf_slcway_partition0_rnf_vec1 on page 4-433
0xCB8	por_hnf_slcway_partition1_rnf_vec1	RW	por_hnf_slcway_partition1_rnf_vec1 on page 4-434
0xCC0	por_hnf_slcway_partition2_rnf_vec1	RW	por_hnf_slcway_partition2_rnf_vec1 on page 4-435
0xCC8	por_hnf_slcway_partition3_rnf_vec1	RW	por_hnf_slcway_partition3_rnf_vec1 on page 4-436
0xC68	por_hnf_slcway_partition0_rni_vec	RW	por_hnf_slcway_partition0_rni_vec on page 4-437
0xC70	por_hnf_slcway_partition1_rni_vec	RW	por_hnf_slcway_partition1_rni_vec on page 4-438
0xC78	por_hnf_slcway_partition2_rni_vec	RW	por_hnf_slcway_partition2_rni_vec on page 4-438
0xC80	por_hnf_slcway_partition3_rni_vec	RW	por_hnf_slcway_partition3_rni_vec on page 4-439

Table 4-5 HN-F register summary (continued)

Offset	Name	Type	Description
0xC88	por_hnf_slcway_partition0_rnd_vec	RW	por_hnf_slcway_partition0_rnd_vec on page 4-440
0xC90	por_hnf_slcway_partition1_rnd_vec	RW	por_hnf_slcway_partition1_rnd_vec on page 4-441
0xC98	por_hnf_slcway_partition2_rnd_vec	RW	por_hnf_slcway_partition2_rnd_vec on page 4-442
0xCA0	por_hnf_slcway_partition3_rnd_vec	RW	por_hnf_slcway_partition3_rnd_vec on page 4-443
0xCA8	por_hnf_rn_region_lock	RW	por_hnf_rn_region_lock on page 4-444
0xD00	por_hnf_sam_control	RW	por_hnf_sam_control on page 4-445
0xD08	por_hnf_sam_memregion0	RW	por_hnf_sam_memregion0 on page 4-447
0xD10	por_hnf_sam_memregion1	RW	por_hnf_sam_memregion1 on page 4-448
0xD18	por_hnf_sam_sn_properties	RW	por_hnf_sam_sn_properties on page 4-449
0xD20	por_hnf_sam_6sn_nodeid	RW	por_hnf_sam_6sn_nodeid on page 4-452
0xD28	por_hnf_rn_phys_id0	RW	por_hnf_rn_phys_id0 on page 4-453
0xD30	por_hnf_rn_phys_id1	RW	por_hnf_rn_phys_id1 on page 4-456
0xD38	por_hnf_rn_phys_id2	RW	por_hnf_rn_phys_id2 on page 4-458
0xD40	por_hnf_rn_phys_id3	RW	por_hnf_rn_phys_id3 on page 4-460
0xD48	por_hnf_rn_phys_id4	RW	por_hnf_rn_phys_id4 on page 4-462
0xD50	por_hnf_rn_phys_id5	RW	por_hnf_rn_phys_id5 on page 4-464
0xD58	por_hnf_rn_phys_id6	RW	por_hnf_rn_phys_id6 on page 4-466
0xD60	por_hnf_rn_phys_id7	RW	por_hnf_rn_phys_id7 on page 4-468
0xD68	por_hnf_rn_phys_id8	RW	por_hnf_rn_phys_id8 on page 4-470
0xD70	por_hnf_rn_phys_id9	RW	por_hnf_rn_phys_id9 on page 4-472
0xD78	por_hnf_rn_phys_id10	RW	por_hnf_rn_phys_id10 on page 4-474
0xD80	por_hnf_rn_phys_id11	RW	por_hnf_rn_phys_id11 on page 4-476
0xD88	por_hnf_rn_phys_id12	RW	por_hnf_rn_phys_id12 on page 4-478
0xD90	por_hnf_rn_phys_id13	RW	por_hnf_rn_phys_id13 on page 4-480
0xD98	por_hnf_rn_phys_id14	RW	por_hnf_rn_phys_id14 on page 4-482
0xDA0	por_hnf_rn_phys_id15	RW	por_hnf_rn_phys_id15 on page 4-484
0xDA8	por_hnf_rn_phys_id16	RW	por_hnf_rn_phys_id16 on page 4-486
0xDB0	por_hnf_rn_phys_id17	RW	por_hnf_rn_phys_id17 on page 4-488
0xDB8	por_hnf_rn_phys_id18	RW	por_hnf_rn_phys_id18 on page 4-490
0xDC0	por_hnf_rn_phys_id19	RW	por_hnf_rn_phys_id19 on page 4-492
0xDC8	por_hnf_rn_phys_id20	RW	por_hnf_rn_phys_id20 on page 4-494
0xDD0	por_hnf_rn_phys_id21	RW	por_hnf_rn_phys_id21 on page 4-496
0xDD8	por_hnf_rn_phys_id22	RW	por_hnf_rn_phys_id22 on page 4-498
0xDE0	por_hnf_rn_phys_id23	RW	por_hnf_rn_phys_id23 on page 4-500
0xDE8	por_hnf_rn_phys_id24	RW	por_hnf_rn_phys_id24 on page 4-502

Table 4-5 HN-F register summary (continued)

Offset	Name	Type	Description
0xDF0	por_hnf_rn_phys_id25	RW	por_hnf_rn_phys_id25 on page 4-504
0xDF8	por_hnf_rn_phys_id26	RW	por_hnf_rn_phys_id26 on page 4-506
0xE00	por_hnf_rn_phys_id27	RW	por_hnf_rn_phys_id27 on page 4-508
0xE08	por_hnf_rn_phys_id28	RW	por_hnf_rn_phys_id28 on page 4-510
0xE10	por_hnf_rn_phys_id29	RW	por_hnf_rn_phys_id29 on page 4-512
0xE18	por_hnf_rn_phys_id30	RW	por_hnf_rn_phys_id30 on page 4-514
0xE20	por_hnf_rn_phys_id31	RW	por_hnf_rn_phys_id31 on page 4-516
0xF00	por_hnf_sf_cxg_blocked_ways	RW	por_hnf_sf_cxg_blocked_ways on page 4-518
0xF10	por_hnf_cml_port_aggr_grp0_add_mask	RW	por_hnf_cml_port_aggr_grp0_add_mask on page 4-519
0xF18	por_hnf_cml_port_aggr_grp1_add_mask	RW	por_hnf_cml_port_aggr_grp1_add_mask on page 4-520
0xF28	por_hnf_cml_port_aggr_grp0_reg	RW	por_hnf_cml_port_aggr_grp0_reg on page 4-521
0xF30	por_hnf_cml_port_aggr_grp1_reg	RW	por_hnf_cml_port_aggr_grp1_reg on page 4-523
0xF40	hn_sam_hash_addr_mask_reg	RW	hn_sam_hash_addr_mask_reg on page 4-524
0xF48	hn_sam_region_cmp_addr_mask_reg	RW	hn_sam_region_cmp_addr_mask_reg on page 4-525
0xF50	por_hnf_abf_lo_addr	RW	por_hnf_abf_lo_addr on page 4-526
0xF58	por_hnf_abf_hi_addr	RW	por_hnf_abf_hi_addr on page 4-527
0xF60	por_hnf_abf_pr	RW	por_hnf_abf_pr on page 4-528
0xF68	por_hnf_abf_sr	RO	por_hnf_abf_sr on page 4-529
0xE28	por_hnf_rn_phys_id32	RW	por_hnf_rn_phys_id32 on page 4-530
0xE30	por_hnf_rn_phys_id33	RW	por_hnf_rn_phys_id33 on page 4-532
0xE38	por_hnf_rn_phys_id34	RW	por_hnf_rn_phys_id34 on page 4-534
0xE40	por_hnf_rn_phys_id35	RW	por_hnf_rn_phys_id35 on page 4-536
0xE48	por_hnf_rn_phys_id36	RW	por_hnf_rn_phys_id36 on page 4-538
0xE50	por_hnf_rn_phys_id37	RW	por_hnf_rn_phys_id37 on page 4-540
0xE58	por_hnf_rn_phys_id38	RW	por_hnf_rn_phys_id38 on page 4-542
0xE60	por_hnf_rn_phys_id39	RW	por_hnf_rn_phys_id39 on page 4-544
0xE68	por_hnf_rn_phys_id40	RW	por_hnf_rn_phys_id40 on page 4-546
0xE70	por_hnf_rn_phys_id41	RW	por_hnf_rn_phys_id41 on page 4-548
0xE78	por_hnf_rn_phys_id42	RW	por_hnf_rn_phys_id42 on page 4-550
0xE80	por_hnf_rn_phys_id43	RW	por_hnf_rn_phys_id43 on page 4-552
0xE88	por_hnf_rn_phys_id44	RW	por_hnf_rn_phys_id44 on page 4-554
0xE90	por_hnf_rn_phys_id45	RW	por_hnf_rn_phys_id45 on page 4-556
0xE98	por_hnf_rn_phys_id46	RW	por_hnf_rn_phys_id46 on page 4-558
0xEA0	por_hnf_rn_phys_id47	RW	por_hnf_rn_phys_id47 on page 4-560
0xEA8	por_hnf_rn_phys_id48	RW	por_hnf_rn_phys_id48 on page 4-562

Table 4-5 HN-F register summary (continued)

Offset	Name	Type	Description
0xEB0	por_hnf_rn_phys_id49	RW	por_hnf_rn_phys_id49 on page 4-564
0xEB8	por_hnf_rn_phys_id50	RW	por_hnf_rn_phys_id50 on page 4-566
0xEC0	por_hnf_rn_phys_id51	RW	por_hnf_rn_phys_id51 on page 4-568
0xEC8	por_hnf_rn_phys_id52	RW	por_hnf_rn_phys_id52 on page 4-570
0xED0	por_hnf_rn_phys_id53	RW	por_hnf_rn_phys_id53 on page 4-572
0xED8	por_hnf_rn_phys_id54	RW	por_hnf_rn_phys_id54 on page 4-574
0xEE0	por_hnf_rn_phys_id55	RW	por_hnf_rn_phys_id55 on page 4-576
0xEE8	por_hnf_rn_phys_id56	RW	por_hnf_rn_phys_id56 on page 4-578
0xEF0	por_hnf_rn_phys_id57	RW	por_hnf_rn_phys_id57 on page 4-580
0xEF8	por_hnf_rn_phys_id58	RW	por_hnf_rn_phys_id58 on page 4-582
0xF70	por_hnf_rn_phys_id59	RW	por_hnf_rn_phys_id59 on page 4-584
0xF78	por_hnf_rn_phys_id60	RW	por_hnf_rn_phys_id60 on page 4-586
0xF80	por_hnf_rn_phys_id61	RW	por_hnf_rn_phys_id61 on page 4-588
0xF88	por_hnf_rn_phys_id62	RW	por_hnf_rn_phys_id62 on page 4-590
0xF90	por_hnf_rn_phys_id63	RW	por_hnf_rn_phys_id63 on page 4-592
0xF98	por_hnf_ldid_map_table_reg0	RW	por_hnf_ldid_map_table_reg0 on page 4-594
0xFA0	por_hnf_ldid_map_table_reg1	RW	por_hnf_ldid_map_table_reg1 on page 4-596
0xFA8	por_hnf_ldid_map_table_reg2	RW	por_hnf_ldid_map_table_reg2 on page 4-597
0xFB0	por_hnf_ldid_map_table_reg3	RW	por_hnf_ldid_map_table_reg3 on page 4-598
0xB80	por_hnf_cfg_slcsf_dbgrd	WO	por_hnf_cfg_slcsf_dbgrd on page 4-600
0xB88	por_hnf_slc_cache_access_slc_tag	RO	por_hnf_slc_cache_access_slc_tag on page 4-601
0xB90	por_hnf_slc_cache_access_slc_data	RO	por_hnf_slc_cache_access_slc_data on page 4-602
0xB98	por_hnf_slc_cache_access_sf_tag	RO	por_hnf_slc_cache_access_sf_tag on page 4-603
0xBA0	por_hnf_slc_cache_access_sf_tag1	RO	por_hnf_slc_cache_access_sf_tag1 on page 4-604
0xBA8	por_hnf_slc_cache_access_sf_tag2	RO	por_hnf_slc_cache_access_sf_tag2 on page 4-604
0x2000	por_hnf_pmu_event_sel	RW	por_hnf_pmu_event_sel on page 4-605

4.2.5 HN-I register summary

This section lists the HN-I registers used in CMN-600AE.

HN-I register summary

The following table shows the *HN-I* registers in offset order from the base memory address.

Table 4-6 HN-I register summary

Offset	Name	Type	Description
0x0	por_hni_node_info	RO	por_hni_node_info on page 4-610
0x80	por_hni_child_info	RO	por_hni_child_info on page 4-611
0x980	por_hni_secure_register_groups_override	RW	por_hni_secure_register_groups_override on page 4-611
0x900	por_hni_unit_info	RO	por_hni_unit_info on page 4-612
0xC00	por_hni_sam_addrregion0_cfg	RW	por_hni_sam_addrregion0_cfg on page 4-614
0xC08	por_hni_sam_addrregion1_cfg	RW	por_hni_sam_addrregion1_cfg on page 4-615
0xC10	por_hni_sam_addrregion2_cfg	RW	por_hni_sam_addrregion2_cfg on page 4-617
0xC18	por_hni_sam_addrregion3_cfg	RW	por_hni_sam_addrregion3_cfg on page 4-619
0xA00	por_hni_cfg_ctl	RW	por_hni_cfg_ctl on page 4-620
0xA08	por_hni_aux_ctl	RW	por_hni_aux_ctl on page 4-621
0x3000	por_hni_errfr	RO	por_hni_errfr on page 4-622
0x3008	por_hni_errctlr	RW	por_hni_errctlr on page 4-623
0x3010	por_hni_errstatus	W1C	por_hni_errstatus on page 4-625
0x3018	por_hni_erraddr	RW	por_hni_erraddr on page 4-626
0x3020	por_hni_errmisc	RW	por_hni_errmisc on page 4-627
0x3100	por_hni_errfr_NS	RO	por_hni_errfr_NS on page 4-629
0x3108	por_hni_errctlr_NS	RW	por_hni_errctlr_NS on page 4-631
0x3110	por_hni_errstatus_NS	W1C	por_hni_errstatus_NS on page 4-632
0x3118	por_hni_erraddr_NS	RW	por_hni_erraddr_NS on page 4-634
0x3120	por_hni_errmisc_NS	RW	por_hni_errmisc_NS on page 4-635
0x2000	por_hni_pmu_event_sel	RW	por_hni_pmu_event_sel on page 4-637

4.2.6 XP register summary

This section lists the XP registers used in CMN-600AE.

MXP register summary

The following table shows the *MXP* registers in offset order from the base memory address.

Table 4-7 MXP register summary

Offset	Name	Type	Description
0x0	por_mxp_node_info	RO	por_mxp_node_info on page 4-640
0x8	por_mxp_device_port_connect_info_p0	RO	por_mxp_device_port_connect_info_p0 on page 4-641
0x10	por_mxp_device_port_connect_info_p1	RO	por_mxp_device_port_connect_info_p1 on page 4-642
0x18	por_mxp_mesh_port_connect_info_east	RO	por_mxp_mesh_port_connect_info_east on page 4-644
0x20	por_mxp_mesh_port_connect_info_north	RO	por_mxp_mesh_port_connect_info_north on page 4-645
0x80	por_mxp_child_info	RO	por_mxp_child_info on page 4-646
0x100	por_mxp_child_pointer_0	RO	por_mxp_child_pointer_0 on page 4-647

Table 4-7 MXP register summary (continued)

Offset	Name	Type	Description
0x108	por_mxp_child_pointer_1	RO	por_mxp_child_pointer_1 on page 4-648
0x110	por_mxp_child_pointer_2	RO	por_mxp_child_pointer_2 on page 4-649
0x118	por_mxp_child_pointer_3	RO	por_mxp_child_pointer_3 on page 4-650
0x120	por_mxp_child_pointer_4	RO	por_mxp_child_pointer_4 on page 4-651
0x128	por_mxp_child_pointer_5	RO	por_mxp_child_pointer_5 on page 4-652
0x130	por_mxp_child_pointer_6	RO	por_mxp_child_pointer_6 on page 4-653
0x138	por_mxp_child_pointer_7	RO	por_mxp_child_pointer_7 on page 4-654
0x140	por_mxp_child_pointer_8	RO	por_mxp_child_pointer_8 on page 4-655
0x148	por_mxp_child_pointer_9	RO	por_mxp_child_pointer_9 on page 4-656
0x150	por_mxp_child_pointer_10	RO	por_mxp_child_pointer_10 on page 4-657
0x158	por_mxp_child_pointer_11	RO	por_mxp_child_pointer_11 on page 4-658
0x160	por_mxp_child_pointer_12	RO	por_mxp_child_pointer_12 on page 4-659
0x168	por_mxp_child_pointer_13	RO	por_mxp_child_pointer_13 on page 4-660
0x170	por_mxp_child_pointer_14	RO	por_mxp_child_pointer_14 on page 4-661
0x178	por_mxp_child_pointer_15	RO	por_mxp_child_pointer_15 on page 4-662
0x900	por_mxp_p0_info	RO	por_mxp_p0_info on page 4-663
0x908	por_mxp_p1_info	RO	por_mxp_p1_info on page 4-664
0x980	por_mxp_secure_register_groups_override	RW	por_mxp_secure_register_groups_override on page 4-666
0xA00	por_mxp_aux_ctl	RW	por_mxp_aux_ctl on page 4-667
0xA80	por_mxp_p0_qos_control	RW	por_mxp_p0_qos_control on page 4-668
0xA88	por_mxp_p0_qos_lat_tgt	RW	por_mxp_p0_qos_lat_tgt on page 4-669
0xA90	por_mxp_p0_qos_lat_scale	RW	por_mxp_p0_qos_lat_scale on page 4-670
0xA98	por_mxp_p0_qos_lat_range	RW	por_mxp_p0_qos_lat_range on page 4-671
0xAA0	por_mxp_p1_qos_control	RW	por_mxp_p1_qos_control on page 4-672
0xAA8	por_mxp_p1_qos_lat_tgt	RW	por_mxp_p1_qos_lat_tgt on page 4-674
0xAB0	por_mxp_p1_qos_lat_scale	RW	por_mxp_p1_qos_lat_scale on page 4-675
0xAB8	por_mxp_p1_qos_lat_range	RW	por_mxp_p1_qos_lat_range on page 4-676
0x2000	por_mxp_pmu_event_sel	RW	por_mxp_pmu_event_sel on page 4-677
0x3000	por_mxp_errfr	RO	por_mxp_errfr on page 4-679
0x3008	por_mxp_errctlr	RW	por_mxp_errctlr on page 4-680
0x3010	por_mxp_errstatus	WIC	por_mxp_errstatus on page 4-681
0x3028	por_mxp_errmisc	RW	por_mxp_errmisc on page 4-683
0x3030	por_mxp_p0_byte_par_err_inj	WO	por_mxp_p0_byte_par_err_inj on page 4-684
0x3038	por_mxp_p1_byte_par_err_inj	WO	por_mxp_p1_byte_par_err_inj on page 4-685
0x3100	por_mxp_errfr_NS	RO	por_mxp_errfr_NS on page 4-686

Table 4-7 MXP register summary (continued)

Offset	Name	Type	Description
0x3108	por_mxp_errctlr_NS	RW	por_mxp_errctlr_NS on page 4-688
0x3110	por_mxp_errstatus_NS	W1C	por_mxp_errstatus_NS on page 4-689
0x3128	por_mxp_errmisc_NS	RW	por_mxp_errmisc_NS on page 4-691
0x1000	por_mxp_p0_syscoreq_ctl	RW	por_mxp_p0_syscoreq_ctl on page 4-692
0x1008	por_mxp_p1_syscoreq_ctl	RW	por_mxp_p1_syscoreq_ctl on page 4-693
0x1010	por_mxp_p0_syscoack_status	RO	por_mxp_p0_syscoack_status on page 4-695
0x1018	por_mxp_p1_syscoack_status	RO	por_mxp_p1_syscoack_status on page 4-696
0x2100	por_dtm_control	RW	por_dtm_control on page 4-697
0x2118	por_dtm_fifo_entry_ready	W1C	por_dtm_fifo_entry_ready on page 4-698
0x2120	por_dtm_fifo_entry0_0	RO	por_dtm_fifo_entry0_0 on page 4-699
0x2128	por_dtm_fifo_entry0_1	RO	por_dtm_fifo_entry0_1 on page 4-700
0x2130	por_dtm_fifo_entry0_2	RO	por_dtm_fifo_entry0_2 on page 4-701
0x2138	por_dtm_fifo_entry1_0	RO	por_dtm_fifo_entry1_0 on page 4-702
0x2140	por_dtm_fifo_entry1_1	RO	por_dtm_fifo_entry1_1 on page 4-703
0x2148	por_dtm_fifo_entry1_2	RO	por_dtm_fifo_entry1_2 on page 4-703
0x2150	por_dtm_fifo_entry2_0	RO	por_dtm_fifo_entry2_0 on page 4-704
0x2158	por_dtm_fifo_entry2_1	RO	por_dtm_fifo_entry2_1 on page 4-705
0x2160	por_dtm_fifo_entry2_2	RO	por_dtm_fifo_entry2_2 on page 4-706
0x2168	por_dtm_fifo_entry3_0	RO	por_dtm_fifo_entry3_0 on page 4-707
0x2170	por_dtm_fifo_entry3_1	RO	por_dtm_fifo_entry3_1 on page 4-708
0x2178	por_dtm_fifo_entry3_2	RO	por_dtm_fifo_entry3_2 on page 4-708
0x21A0	por_dtm_wp0_config	RW	por_dtm_wp0_config on page 4-709
0x21A8	por_dtm_wp0_val	RW	por_dtm_wp0_val on page 4-711
0x21B0	por_dtm_wp0_mask	RW	por_dtm_wp0_mask on page 4-712
0x21B8	por_dtm_wp1_config	RW	por_dtm_wp1_config on page 4-713
0x21C0	por_dtm_wp1_val	RW	por_dtm_wp1_val on page 4-715
0x21C8	por_dtm_wp1_mask	RW	por_dtm_wp1_mask on page 4-716
0x21D0	por_dtm_wp2_config	RW	por_dtm_wp2_config on page 4-717
0x21D8	por_dtm_wp2_val	RW	por_dtm_wp2_val on page 4-719
0x21E0	por_dtm_wp2_mask	RW	por_dtm_wp2_mask on page 4-719
0x21E8	por_dtm_wp3_config	RW	por_dtm_wp3_config on page 4-720
0x21F0	por_dtm_wp3_val	RW	por_dtm_wp3_val on page 4-722
0x21F8	por_dtm_wp3_mask	RW	por_dtm_wp3_mask on page 4-723
0x2200	por_dtm_pmsicr	RW	por_dtm_pmsicr on page 4-724
0x2208	por_dtm_pmsirr	RW	por_dtm_pmsirr on page 4-725

Table 4-7 MXP register summary (continued)

Offset	Name	Type	Description
0x2210	por_dtm_pmu_config	RW	por_dtm_pmu_config on page 4-726
0x2220	por_dtm_pmevnt	RW	por_dtm_pmevnt on page 4-729
0x2240	por_dtm_pmevntsr	RW	por_dtm_pmevntsr on page 4-730

4.2.7 RN-D register summary

This section lists the RN-D registers used in CMN-600AE.

RN-D register summary

The following table shows the *RND* registers in offset order from the base memory address.

Table 4-8 RN-D register summary

Offset	Name	Type	Description
0x0	por_rnd_node_info	RO	por_rnd_node_info on page 4-732
0x80	por_rnd_child_info	RO	por_rnd_child_info on page 4-733
0x980	por_rnd_secure_register_groups_override	RW	por_rnd_secure_register_groups_override on page 4-733
0x900	por_rnd_unit_info	RO	por_rnd_unit_info on page 4-734
0xA00	por_rnd_cfg_ctl	RW	por_rnd_cfg_ctl on page 4-736
0xA08	por_rnd_aux_ctl	RW	por_rnd_aux_ctl on page 4-738
0xA10	por_rnd_s0_port_control	RW	por_rnd_s0_port_control on page 4-739
0xA18	por_rnd_s1_port_control	RW	por_rnd_s1_port_control on page 4-740
0xA20	por_rnd_s2_port_control	RW	por_rnd_s2_port_control on page 4-741
0xA80	por_rnd_s0_qos_control	RW	por_rnd_s0_qos_control on page 4-742
0xA88	por_rnd_s0_qos_lat_tgt	RW	por_rnd_s0_qos_lat_tgt on page 4-744
0xA90	por_rnd_s0_qos_lat_scale	RW	por_rnd_s0_qos_lat_scale on page 4-745
0xA98	por_rnd_s0_qos_lat_range	RW	por_rnd_s0_qos_lat_range on page 4-747
0xAA0	por_rnd_s1_qos_control	RW	por_rnd_s1_qos_control on page 4-748
0xAA8	por_rnd_s1_qos_lat_tgt	RW	por_rnd_s1_qos_lat_tgt on page 4-750
0xAB0	por_rnd_s1_qos_lat_scale	RW	por_rnd_s1_qos_lat_scale on page 4-751
0xAB8	por_rnd_s1_qos_lat_range	RW	por_rnd_s1_qos_lat_range on page 4-752
0xAC0	por_rnd_s2_qos_control	RW	por_rnd_s2_qos_control on page 4-753
0xAC8	por_rnd_s2_qos_lat_tgt	RW	por_rnd_s2_qos_lat_tgt on page 4-755
0xAD0	por_rnd_s2_qos_lat_scale	RW	por_rnd_s2_qos_lat_scale on page 4-756
0xAD8	por_rnd_s2_qos_lat_range	RW	por_rnd_s2_qos_lat_range on page 4-758
0x2000	por_rnd_pmu_event_sel	RW	por_rnd_pmu_event_sel on page 4-759
0x1000	por_rnd_syscoreq_ctl	RW	por_rnd_syscoreq_ctl on page 4-761
0x1008	por_rnd_syscoack_status	RO	por_rnd_syscoack_status on page 4-762

4.2.8 RN-I register summary

This section lists the RN-I registers used in CMN-600AE.

RN-I register summary

The following table shows the *RNI* registers in offset order from the base memory address.

Table 4-9 RN-I register summary

Offset	Name	Type	Description
0x0	por_rni_node_info	RO	por_rni_node_info on page 4-764
0x80	por_rni_child_info	RO	por_rni_child_info on page 4-765
0x980	por_rni_secure_register_groups_override	RW	por_rni_secure_register_groups_override on page 4-765
0x900	por_rni_unit_info	RO	por_rni_unit_info on page 4-766
0xA00	por_rni_cfg_ctl	RW	por_rni_cfg_ctl on page 4-768
0xA08	por_rni_aux_ctl	RW	por_rni_aux_ctl on page 4-770
0xA10	por_rni_s0_port_control	RW	por_rni_s0_port_control on page 4-771
0xA18	por_rni_s1_port_control	RW	por_rni_s1_port_control on page 4-772
0xA20	por_rni_s2_port_control	RW	por_rni_s2_port_control on page 4-773
0xA80	por_rni_s0_qos_control	RW	por_rni_s0_qos_control on page 4-774
0xA88	por_rni_s0_qos_lat_tgt	RW	por_rni_s0_qos_lat_tgt on page 4-776
0xA90	por_rni_s0_qos_lat_scale	RW	por_rni_s0_qos_lat_scale on page 4-777
0xA98	por_rni_s0_qos_lat_range	RW	por_rni_s0_qos_lat_range on page 4-779
0xAA0	por_rni_s1_qos_control	RW	por_rni_s1_qos_control on page 4-780
0xAA8	por_rni_s1_qos_lat_tgt	RW	por_rni_s1_qos_lat_tgt on page 4-782
0xAB0	por_rni_s1_qos_lat_scale	RW	por_rni_s1_qos_lat_scale on page 4-783
0xAB8	por_rni_s1_qos_lat_range	RW	por_rni_s1_qos_lat_range on page 4-784
0xAC0	por_rni_s2_qos_control	RW	por_rni_s2_qos_control on page 4-785
0xAC8	por_rni_s2_qos_lat_tgt	RW	por_rni_s2_qos_lat_tgt on page 4-787
0xAD0	por_rni_s2_qos_lat_scale	RW	por_rni_s2_qos_lat_scale on page 4-788
0xAD8	por_rni_s2_qos_lat_range	RW	por_rni_s2_qos_lat_range on page 4-790
0x2000	por_rni_pmu_event_sel	RW	por_rni_pmu_event_sel on page 4-791

4.2.9 RN SAM register summary

This section lists the RN SAM registers used in CMN-600AE.

RN SAM register summary

The following table shows the *RNSAM* registers in offset order from the base memory address.

Table 4-10 RN SAM register summary

Offset	Name	Type	Description
0x0	por_rnsam_node_info	RO	por_rnsam_node_info on page 4-794
0x80	por_rnsam_child_info	RO	por_rnsam_child_info on page 4-795
0x980	por_rnsam_secure_register_groups_override	RW	por_rnsam_secure_register_groups_override on page 4-795
0x900	por_rnsam_unit_info	RO	por_rnsam_unit_info on page 4-796
0xC00	rnsam_status	RW	rnsam_status on page 4-797
0xC08	non_hash_mem_region_reg0	RW	non_hash_mem_region_reg0 on page 4-798
0xC10	non_hash_mem_region_reg1	RW	non_hash_mem_region_reg1 on page 4-800
0xC18	non_hash_mem_region_reg2	RW	non_hash_mem_region_reg2 on page 4-802
0xC20	non_hash_mem_region_reg3	RW	non_hash_mem_region_reg3 on page 4-804
0xC30	non_hash_tgt_nodeid0	RW	non_hash_tgt_nodeid0 on page 4-806
0xC38	non_hash_tgt_nodeid1	RW	non_hash_tgt_nodeid1 on page 4-808
0xC40	non_hash_tgt_nodeid2	RW	non_hash_tgt_nodeid2 on page 4-809
0xC48	sys_cache_grp_region0	RW	sys_cache_grp_region0 on page 4-810
0xC50	sys_cache_grp_region1	RW	sys_cache_grp_region1 on page 4-812
0xC58	sys_cache_grp_hn_nodeid_reg0	RW	sys_cache_grp_hn_nodeid_reg0 on page 4-814
0xC60	sys_cache_grp_hn_nodeid_reg1	RW	sys_cache_grp_hn_nodeid_reg1 on page 4-815
0xC68	sys_cache_grp_hn_nodeid_reg2	RW	sys_cache_grp_hn_nodeid_reg2 on page 4-816
0xC70	sys_cache_grp_hn_nodeid_reg3	RW	sys_cache_grp_hn_nodeid_reg3 on page 4-818
0xC78	sys_cache_grp_hn_nodeid_reg4	RW	sys_cache_grp_hn_nodeid_reg4 on page 4-819
0xC80	sys_cache_grp_hn_nodeid_reg5	RW	sys_cache_grp_hn_nodeid_reg5 on page 4-820
0xC88	sys_cache_grp_hn_nodeid_reg6	RW	sys_cache_grp_hn_nodeid_reg6 on page 4-821
0xC90	sys_cache_grp_hn_nodeid_reg7	RW	sys_cache_grp_hn_nodeid_reg7 on page 4-823
0xC98	sys_cache_grp_nonhash_nodeid	RW	sys_cache_grp_nonhash_nodeid on page 4-824
0xD00	sys_cache_group_hn_count	RW	sys_cache_group_hn_count on page 4-825
0xD08	sys_cache_grp_sn_nodeid_reg0	RW	sys_cache_grp_sn_nodeid_reg0 on page 4-826
0xD10	sys_cache_grp_sn_nodeid_reg1	RW	sys_cache_grp_sn_nodeid_reg1 on page 4-828
0xD18	sys_cache_grp_sn_nodeid_reg2	RW	sys_cache_grp_sn_nodeid_reg2 on page 4-829
0xD20	sys_cache_grp_sn_nodeid_reg3	RW	sys_cache_grp_sn_nodeid_reg3 on page 4-830
0xD28	sys_cache_grp_sn_nodeid_reg4	RW	sys_cache_grp_sn_nodeid_reg4 on page 4-831
0xD30	sys_cache_grp_sn_nodeid_reg5	RW	sys_cache_grp_sn_nodeid_reg5 on page 4-833
0xD38	sys_cache_grp_sn_nodeid_reg6	RW	sys_cache_grp_sn_nodeid_reg6 on page 4-834
0xD40	sys_cache_grp_sn_nodeid_reg7	RW	sys_cache_grp_sn_nodeid_reg7 on page 4-835
0xD48	sys_cache_grp_sn_sam_cfg0	RW	sys_cache_grp_sn_sam_cfg0 on page 4-836
0xD50	sys_cache_grp_sn_sam_cfg1	RW	sys_cache_grp_sn_sam_cfg1 on page 4-838
0xD58	gic_mem_region_reg	RW	gic_mem_region_reg on page 4-839

Table 4-10 RN SAM register summary (continued)

Offset	Name	Type	Description
0xD60	sys_cache_grp_sn_attr	RW	sys_cache_grp_sn_attr on page 4-841
0xD68	sys_cache_grp_hn_cpa_en_reg	RW	sys_cache_grp_hn_cpa_en_reg on page 4-843
0xD70	sys_cache_grp_hn_cpa_grp_reg	RW	sys_cache_grp_hn_cpa_grp_reg on page 4-844
0xE00	cml_port_aggr_mode_ctrl_reg	RW	cml_port_aggr_mode_ctrl_reg on page 4-846
0xE08	cml_port_aggr_grp0_add_mask	RW	cml_port_aggr_grp0_add_mask on page 4-849
0xE10	cml_port_aggr_grp1_add_mask	RW	cml_port_aggr_grp1_add_mask on page 4-850
0xE40	cml_port_aggr_grp0_reg	RW	cml_port_aggr_grp0_reg on page 4-851
0xE48	cml_port_aggr_grp1_reg	RW	cml_port_aggr_grp1_reg on page 4-853
0xF00	sys_cache_grp_secondary_reg0	RW	sys_cache_grp_secondary_reg0 on page 4-854
0xF08	sys_cache_grp_secondary_reg1	RW	sys_cache_grp_secondary_reg1 on page 4-856
0xF10	sys_cache_grp_cal_mode_reg	RW	sys_cache_grp_cal_mode_reg on page 4-858
0xF18	rnsam_hash_addr_mask_reg	RW	rnsam_hash_addr_mask_reg on page 4-860
0xF20	rnsam_region_cmp_addr_mask_reg	RW	rnsam_region_cmp_addr_mask_reg on page 4-860
0xF58	sys_cache_grp_hn_nodeid_reg8	RW	sys_cache_grp_hn_nodeid_reg8 on page 4-861
0xF60	sys_cache_grp_hn_nodeid_reg9	RW	sys_cache_grp_hn_nodeid_reg9 on page 4-863
0xF68	sys_cache_grp_hn_nodeid_reg10	RW	sys_cache_grp_hn_nodeid_reg10 on page 4-864
0xF70	sys_cache_grp_hn_nodeid_reg11	RW	sys_cache_grp_hn_nodeid_reg11 on page 4-865
0xF78	sys_cache_grp_hn_nodeid_reg12	RW	sys_cache_grp_hn_nodeid_reg12 on page 4-866
0xF80	sys_cache_grp_hn_nodeid_reg13	RW	sys_cache_grp_hn_nodeid_reg13 on page 4-868
0xF88	sys_cache_grp_hn_nodeid_reg14	RW	sys_cache_grp_hn_nodeid_reg14 on page 4-869
0xF90	sys_cache_grp_hn_nodeid_reg15	RW	sys_cache_grp_hn_nodeid_reg15 on page 4-870
0x1008	sys_cache_grp_sn_nodeid_reg8	RW	sys_cache_grp_sn_nodeid_reg8 on page 4-871
0x1010	sys_cache_grp_sn_nodeid_reg9	RW	sys_cache_grp_sn_nodeid_reg9 on page 4-873
0x1018	sys_cache_grp_sn_nodeid_reg10	RW	sys_cache_grp_sn_nodeid_reg10 on page 4-874
0x1020	sys_cache_grp_sn_nodeid_reg11	RW	sys_cache_grp_sn_nodeid_reg11 on page 4-875
0x1028	sys_cache_grp_sn_nodeid_reg12	RW	sys_cache_grp_sn_nodeid_reg12 on page 4-876
0x1030	sys_cache_grp_sn_nodeid_reg13	RW	sys_cache_grp_sn_nodeid_reg13 on page 4-878
0x1038	sys_cache_grp_sn_nodeid_reg14	RW	sys_cache_grp_sn_nodeid_reg14 on page 4-879
0x1040	sys_cache_grp_sn_nodeid_reg15	RW	sys_cache_grp_sn_nodeid_reg15 on page 4-880

4.2.10 SBSX register summary

This section lists the SBSX registers used in CMN-600AE.

SBSX register summary

The following table shows the SBSX registers in offset order from the base memory address.

Table 4-11 SBSX register summary

Offset	Name	Type	Description
0x0	por_sbsx_node_info	RO	por_sbsx_node_info on page 4-882
0x80	por_sbsx_child_info	RO	por_sbsx_child_info on page 4-883
0x900	por_sbsx_unit_info	RO	por_sbsx_unit_info on page 4-883
0xA08	por_sbsx_aux_ctl	RW	por_sbsx_aux_ctl on page 4-885
0x3000	por_sbsx_errfr	RO	por_sbsx_errfr on page 4-886
0x3008	por_sbsx_errctlr	RW	por_sbsx_errctlr on page 4-887
0x3010	por_sbsx_errstatus	W1C	por_sbsx_errstatus on page 4-888
0x3018	por_sbsx_erraddr	RW	por_sbsx_erraddr on page 4-890
0x3020	por_sbsx_errmisc	RW	por_sbsx_errmisc on page 4-891
0x3100	por_sbsx_errfr_NS	RO	por_sbsx_errfr_NS on page 4-892
0x3108	por_sbsx_errctlr_NS	RW	por_sbsx_errctlr_NS on page 4-894
0x3110	por_sbsx_errstatus_NS	W1C	por_sbsx_errstatus_NS on page 4-895
0x3118	por_sbsx_erraddr_NS	RW	por_sbsx_erraddr_NS on page 4-897
0x3120	por_sbsx_errmisc_NS	RW	por_sbsx_errmisc_NS on page 4-898
0x2000	por_sbsx_pmu_event_sel	RW	por_sbsx_pmu_event_sel on page 4-899

4.2.11 CXHA register summary

This section lists the CXHA registers used in CMN-600AE.

CXHA register summary

The following table shows the *CXG_HA* registers in offset order from the base memory address.

Table 4-12 CXHA register summary

Offset	Name	Type	Description
0x0	por_cxg_ha_node_info	RO	por_cxg_ha_node_info on page 4-902
0x8	por_cxg_ha_id	RW	por_cxg_ha_id on page 4-903
0x80	por_cxg_ha_child_info	RO	por_cxg_ha_child_info on page 4-903
0xA08	por_cxg_ha_aux_ctl	RW	por_cxg_ha_aux_ctl on page 4-904
0x980	por_cxg_ha_secure_register_groups_override	RW	por_cxg_ha_secure_register_groups_override on page 4-906
0x900	por_cxg_ha_unit_info	RO	por_cxg_ha_unit_info on page 4-907
0xC00	por_cxg_ha_rnf_raid_to_ldid_reg0	RW	por_cxg_ha_rnf_raid_to_ldid_reg0 on page 4-908
0xC08	por_cxg_ha_rnf_raid_to_ldid_reg1	RW	por_cxg_ha_rnf_raid_to_ldid_reg1 on page 4-910
0xC10	por_cxg_ha_rnf_raid_to_ldid_reg2	RW	por_cxg_ha_rnf_raid_to_ldid_reg2 on page 4-912
0xC18	por_cxg_ha_rnf_raid_to_ldid_reg3	RW	por_cxg_ha_rnf_raid_to_ldid_reg3 on page 4-914
0xC20	por_cxg_ha_rnf_raid_to_ldid_reg4	RW	por_cxg_ha_rnf_raid_to_ldid_reg4 on page 4-916
0xC28	por_cxg_ha_rnf_raid_to_ldid_reg5	RW	por_cxg_ha_rnf_raid_to_ldid_reg5 on page 4-918
0xC30	por_cxg_ha_rnf_raid_to_ldid_reg6	RW	por_cxg_ha_rnf_raid_to_ldid_reg6 on page 4-920

Table 4-12 CXHA register summary (continued)

Offset	Name	Type	Description
0xC38	por_cxg_ha_rnf_raid_to_ldid_reg7	RW	por_cxg_ha_rnf_raid_to_ldid_reg7 on page 4-922
0xC40	por_cxg_ha_agentid_to_linkid_reg0	RW	por_cxg_ha_agentid_to_linkid_reg0 on page 4-924
0xC48	por_cxg_ha_agentid_to_linkid_reg1	RW	por_cxg_ha_agentid_to_linkid_reg1 on page 4-926
0xC50	por_cxg_ha_agentid_to_linkid_reg2	RW	por_cxg_ha_agentid_to_linkid_reg2 on page 4-928
0xC58	por_cxg_ha_agentid_to_linkid_reg3	RW	por_cxg_ha_agentid_to_linkid_reg3 on page 4-930
0xC60	por_cxg_ha_agentid_to_linkid_reg4	RW	por_cxg_ha_agentid_to_linkid_reg4 on page 4-931
0xC68	por_cxg_ha_agentid_to_linkid_reg5	RW	por_cxg_ha_agentid_to_linkid_reg5 on page 4-933
0xC70	por_cxg_ha_agentid_to_linkid_reg6	RW	por_cxg_ha_agentid_to_linkid_reg6 on page 4-935
0xC78	por_cxg_ha_agentid_to_linkid_reg7	RW	por_cxg_ha_agentid_to_linkid_reg7 on page 4-936
0xD00	por_cxg_ha_agentid_to_linkid_val	RW	por_cxg_ha_agentid_to_linkid_val on page 4-938
0xD08	por_cxg_ha_rnf_raid_to_ldid_val	RW	por_cxg_ha_rnf_raid_to_ldid_val on page 4-939
0x2000	por_cxg_ha_pmu_event_sel	RW	por_cxg_ha_pmu_event_sel on page 4-940
0x1000	por_cxg_ha_cxprtcl_link0_ctl	RW	por_cxg_ha_cxprtcl_link0_ctl on page 4-941
0x1008	por_cxg_ha_cxprtcl_link0_status	RO	por_cxg_ha_cxprtcl_link0_status on page 4-943
0x1010	por_cxg_ha_cxprtcl_link1_ctl	RW	por_cxg_ha_cxprtcl_link1_ctl on page 4-945
0x1018	por_cxg_ha_cxprtcl_link1_status	RO	por_cxg_ha_cxprtcl_link1_status on page 4-946
0x1020	por_cxg_ha_cxprtcl_link2_ctl	RW	por_cxg_ha_cxprtcl_link2_ctl on page 4-948
0x1028	por_cxg_ha_cxprtcl_link2_status	RO	por_cxg_ha_cxprtcl_link2_status on page 4-950
0x3000	por_cxg_ha_errfr	RO	por_cxg_ha_errfr on page 4-951
0x3008	por_cxg_ha_errctlr	RW	por_cxg_ha_errctlr on page 4-953
0x3010	por_cxg_ha_errstatus	W1C	por_cxg_ha_errstatus on page 4-954
0x3018	por_cxg_ha_erraddr	RW	por_cxg_ha_erraddr on page 4-956
0x3020	por_cxg_ha_errmisc	RW	por_cxg_ha_errmisc on page 4-957
0x3100	por_cxg_ha_errfr_NS	RO	por_cxg_ha_errfr_NS on page 4-958
0x3108	por_cxg_ha_errctlr_NS	RW	por_cxg_ha_errctlr_NS on page 4-960
0x3110	por_cxg_ha_errstatus_NS	W1C	por_cxg_ha_errstatus_NS on page 4-961
0x3118	por_cxg_ha_erraddr_NS	RW	por_cxg_ha_erraddr_NS on page 4-963
0x3120	por_cxg_ha_errmisc_NS	RW	por_cxg_ha_errmisc_NS on page 4-964

4.2.12 CXRA register summary

This section lists the CXRA registers used in CMN-600AE.

CXRA register summary

The following table shows the *CXG_RA* registers in offset order from the base memory address.

Table 4-13 CXRA register summary

Offset	Name	Type	Description
0x0	por_cxg_ra_node_info	RO	por_cxg_ra_node_info on page 4-966
0x80	por_cxg_ra_child_info	RO	por_cxg_ra_child_info on page 4-967
0x980	por_cxg_ra_secure_register_groups_override	RW	por_cxg_ra_secure_register_groups_override on page 4-967
0x900	por_cxg_ra_unit_info	RO	por_cxg_ra_unit_info on page 4-968
0xA00	por_cxg_ra_cfg_ctl	RW	por_cxg_ra_cfg_ctl on page 4-970
0xA08	por_cxg_ra_aux_ctl	RW	por_cxg_ra_aux_ctl on page 4-972
0xDA8	por_cxg_ra_sam_addr_region_reg0	RW	por_cxg_ra_sam_addr_region_reg0 on page 4-973
0xDB0	por_cxg_ra_sam_addr_region_reg1	RW	por_cxg_ra_sam_addr_region_reg1 on page 4-975
0xDB8	por_cxg_ra_sam_addr_region_reg2	RW	por_cxg_ra_sam_addr_region_reg2 on page 4-976
0xDC0	por_cxg_ra_sam_addr_region_reg3	RW	por_cxg_ra_sam_addr_region_reg3 on page 4-977
0xDC8	por_cxg_ra_sam_addr_region_reg4	RW	por_cxg_ra_sam_addr_region_reg4 on page 4-978
0xDD0	por_cxg_ra_sam_addr_region_reg5	RW	por_cxg_ra_sam_addr_region_reg5 on page 4-980
0xDD8	por_cxg_ra_sam_addr_region_reg6	RW	por_cxg_ra_sam_addr_region_reg6 on page 4-981
0xDE0	por_cxg_ra_sam_addr_region_reg7	RW	por_cxg_ra_sam_addr_region_reg7 on page 4-982
0xE60	por_cxg_ra_agentid_to_linkid_reg0	RW	por_cxg_ra_agentid_to_linkid_reg0 on page 4-991
0xE68	por_cxg_ra_agentid_to_linkid_reg1	RW	por_cxg_ra_agentid_to_linkid_reg1 on page 4-993
0xE70	por_cxg_ra_agentid_to_linkid_reg2	RW	por_cxg_ra_agentid_to_linkid_reg2 on page 4-995
0xE78	por_cxg_ra_agentid_to_linkid_reg3	RW	por_cxg_ra_agentid_to_linkid_reg3 on page 4-996
0xE80	por_cxg_ra_agentid_to_linkid_reg4	RW	por_cxg_ra_agentid_to_linkid_reg4 on page 4-998
0xE88	por_cxg_ra_agentid_to_linkid_reg5	RW	por_cxg_ra_agentid_to_linkid_reg5 on page 4-1000
0xE90	por_cxg_ra_agentid_to_linkid_reg6	RW	por_cxg_ra_agentid_to_linkid_reg6 on page 4-1001
0xE98	por_cxg_ra_agentid_to_linkid_reg7	RW	por_cxg_ra_agentid_to_linkid_reg7 on page 4-1003
0xEA0	por_cxg_ra_rnf_ldid_to_raid_reg0	RW	por_cxg_ra_rnf_ldid_to_raid_reg0 on page 4-1005
0xEA8	por_cxg_ra_rnf_ldid_to_raid_reg1	RW	por_cxg_ra_rnf_ldid_to_raid_reg1 on page 4-1006
0xEB0	por_cxg_ra_rnf_ldid_to_raid_reg2	RW	por_cxg_ra_rnf_ldid_to_raid_reg2 on page 4-1008
0xEB8	por_cxg_ra_rnf_ldid_to_raid_reg3	RW	por_cxg_ra_rnf_ldid_to_raid_reg3 on page 4-1010
0xEC0	por_cxg_ra_rnf_ldid_to_raid_reg4	RW	por_cxg_ra_rnf_ldid_to_raid_reg4 on page 4-1011
0xEC8	por_cxg_ra_rnf_ldid_to_raid_reg5	RW	por_cxg_ra_rnf_ldid_to_raid_reg5 on page 4-1013
0xED0	por_cxg_ra_rnf_ldid_to_raid_reg6	RW	por_cxg_ra_rnf_ldid_to_raid_reg6 on page 4-1015
0xED8	por_cxg_ra_rnf_ldid_to_raid_reg7	RW	por_cxg_ra_rnf_ldid_to_raid_reg7 on page 4-1016
0xEE0	por_cxg_ra_rni_ldid_to_raid_reg0	RW	por_cxg_ra_rni_ldid_to_raid_reg0 on page 4-1018
0xEE8	por_cxg_ra_rni_ldid_to_raid_reg1	RW	por_cxg_ra_rni_ldid_to_raid_reg1 on page 4-1020
0xEF0	por_cxg_ra_rni_ldid_to_raid_reg2	RW	por_cxg_ra_rni_ldid_to_raid_reg2 on page 4-1021
0xEF8	por_cxg_ra_rni_ldid_to_raid_reg3	RW	por_cxg_ra_rni_ldid_to_raid_reg3 on page 4-1023
0xF00	por_cxg_ra_rnd_ldid_to_raid_reg0	RW	por_cxg_ra_rnd_ldid_to_raid_reg0 on page 4-1025

Table 4-13 CXRA register summary (continued)

Offset	Name	Type	Description
0xF08	por_cxg_ra_rnd_ldid_to_raid_reg1	RW	por_cxg_ra_rnd_ldid_to_raid_reg1 on page 4-1026
0xF10	por_cxg_ra_rnd_ldid_to_raid_reg2	RW	por_cxg_ra_rnd_ldid_to_raid_reg2 on page 4-1028
0xF18	por_cxg_ra_rnd_ldid_to_raid_reg3	RW	por_cxg_ra_rnd_ldid_to_raid_reg3 on page 4-1030
0xF20	por_cxg_ra_agentid_to_linkid_val	RW	por_cxg_ra_agentid_to_linkid_val on page 4-1031
0xF28	por_cxg_ra_rnf_ldid_to_raid_val	RW	por_cxg_ra_rnf_ldid_to_raid_val on page 4-1032
0xF30	por_cxg_ra_rni_ldid_to_raid_val	RW	por_cxg_ra_rni_ldid_to_raid_val on page 4-1033
0xF38	por_cxg_ra_rnd_ldid_to_raid_val	RW	por_cxg_ra_rnd_ldid_to_raid_val on page 4-1034
0x2000	por_cxg_ra_pmu_event_sel	RW	por_cxg_ra_pmu_event_sel on page 4-1035
0x1000	por_cxg_ra_cxprtcl_link0_ctl	RW	por_cxg_ra_cxprtcl_link0_ctl on page 4-1037
0x1008	por_cxg_ra_cxprtcl_link0_status	RO	por_cxg_ra_cxprtcl_link0_status on page 4-1039
0x1010	por_cxg_ra_cxprtcl_link1_ctl	RW	por_cxg_ra_cxprtcl_link1_ctl on page 4-1040
0x1018	por_cxg_ra_cxprtcl_link1_status	RO	por_cxg_ra_cxprtcl_link1_status on page 4-1042
0x1020	por_cxg_ra_cxprtcl_link2_ctl	RW	por_cxg_ra_cxprtcl_link2_ctl on page 4-1043
0x1028	por_cxg_ra_cxprtcl_link2_status	RO	por_cxg_ra_cxprtcl_link2_status on page 4-1045

4.2.13 CXLA register summary

This section lists the CXLA registers used in CMN-600AE.

CXLA register summary

The following table shows the CXLA registers in offset order from the base memory address.

Table 4-14 CXLA register summary

Offset	Name	Type	Description
0x0	por_cxla_node_info	RO	por_cxla_node_info on page 4-1047
0x80	por_cxla_child_info	RO	por_cxla_child_info on page 4-1048
0x980	por_cxla_secure_register_groups_override	RW	por_cxla_secure_register_groups_override on page 4-1048
0x900	por_cxla_unit_info	RO	por_cxla_unit_info on page 4-1049
0xA08	por_cxla_aux_ctl	RW	por_cxla_aux_ctl on page 4-1051
0xC00	por_cxla_ccix_prop_capabilities	RO	por_cxla_ccix_prop_capabilities on page 4-1055
0xC08	por_cxla_ccix_prop_configured	RW	por_cxla_ccix_prop_configured on page 4-1056
0xC10	por_cxla_tx_cxs_attr_capabilities	RO	por_cxla_tx_cxs_attr_capabilities on page 4-1058
0xC18	por_cxla_rx_cxs_attr_capabilities	RO	por_cxla_rx_cxs_attr_capabilities on page 4-1060
0xC30	por_cxla_agentid_to_linkid_reg0	RW	por_cxla_agentid_to_linkid_reg0 on page 4-1062
0xC38	por_cxla_agentid_to_linkid_reg1	RW	por_cxla_agentid_to_linkid_reg1 on page 4-1063
0xC40	por_cxla_agentid_to_linkid_reg2	RW	por_cxla_agentid_to_linkid_reg2 on page 4-1065
0xC48	por_cxla_agentid_to_linkid_reg3	RW	por_cxla_agentid_to_linkid_reg3 on page 4-1067

Table 4-14 CXLA register summary (continued)

Offset	Name	Type	Description
0xC50	por_cxla_agentid_to_linkid_reg4	RW	por_cxla_agentid_to_linkid_reg4 on page 4-1068
0xC58	por_cxla_agentid_to_linkid_reg5	RW	por_cxla_agentid_to_linkid_reg5 on page 4-1070
0xC60	por_cxla_agentid_to_linkid_reg6	RW	por_cxla_agentid_to_linkid_reg6 on page 4-1072
0xC68	por_cxla_agentid_to_linkid_reg7	RW	por_cxla_agentid_to_linkid_reg7 on page 4-1073
0xC70	por_cxla_agentid_to_linkid_val	RW	por_cxla_agentid_to_linkid_val on page 4-1075
0xC78	por_cxla_linkid_to_pcie_bus_num	RW	por_cxla_linkid_to_pcie_bus_num on page 4-1076
0xD00	por_cxla_permmsg_pyld_0_63	RW	por_cxla_permmsg_pyld_0_63 on page 4-1077
0xD08	por_cxla_permmsg_pyld_64_127	RW	por_cxla_permmsg_pyld_64_127 on page 4-1078
0xD10	por_cxla_permmsg_pyld_128_191	RW	por_cxla_permmsg_pyld_128_191 on page 4-1079
0xD18	por_cxla_permmsg_pyld_192_255	RW	por_cxla_permmsg_pyld_192_255 on page 4-1080
0xD20	por_cxla_permmsg_ctl	RW	por_cxla_permmsg_ctl on page 4-1080
0xD28	por_cxla_err_agent_id	RW	por_cxla_err_agent_id on page 4-1082
0x2000	por_cxla_pmu_event_sel	RW	por_cxla_pmu_event_sel on page 4-1082
0x2210	por_cxla_pmu_config	RW	por_cxla_pmu_config on page 4-1084
0x2220	por_cxla_pmevcnt	RW	por_cxla_pmevcnt on page 4-1086
0x2240	por_cxla_pmevcntsr	RW	por_cxla_pmevcntsr on page 4-1087

4.2.14 FMU register summary

This section lists the FMU registers used in CMN-600AE.

FMU register summary

The following table shows the *FMU* registers in offset order from the base memory address.

Table 4-15 FMU register summary

Offset	Name	Type	Description
0x0	por_fmu_node_info	RO	por_fmu_node_info on page 4-1088
0x80	por_fmu_child_info	RO	por_fmu_child_info on page 4-1089
0xC10	por_fmu_ctl	RW	por_fmu_ctl on page 4-1090
0xC18	por_fmu_key	WO	por_fmu_key on page 4-1091
0x3008	por_fmu_errgsr_clk_mxp	RO	por_fmu_errgsr_clk_mxp on page 4-1092
0x3010	por_fmu_errgsr_rst_mxp	RO	por_fmu_errgsr_rst_mxp on page 4-1093
0x3018	por_fmu_errgsr_lsc_mxp	RO	por_fmu_errgsr_lsc_mxp on page 4-1094
0x3020	por_fmu_errgsr_ioc_mxp	RO	por_fmu_errgsr_ioc_mxp on page 4-1095
0x3028	por_fmu_errgsr_async_mxp	RO	por_fmu_errgsr_async_mxp on page 4-1096
0x3030	por_fmu_errgsr_hang_mxp	RO	por_fmu_errgsr_hang_mxp on page 4-1097
0x3038	por_fmu_errgsr_mpu_mxp	RO	por_fmu_errgsr_mpu_mxp on page 4-1097

Table 4-15 FMU register summary (continued)

Offset	Name	Type	Description
0x3040	por_fmu_errgsr_eccue_mxp	RO	<i>por_fmu_errgsr_eccue_mxp</i> on page 4-1098
0x3048	por_fmu_errgsr_eccce_mxp	RO	<i>por_fmu_errgsr_eccce_mxp</i> on page 4-1099
0x3050	por_fmu_errgsr_clk_p0_d0	RO	<i>por_fmu_errgsr_clk_p0_d0</i> on page 4-1100
0x3058	por_fmu_errgsr_rst_p0_d0	RO	<i>por_fmu_errgsr_rst_p0_d0</i> on page 4-1101
0x3060	por_fmu_errgsr_lsc_p0_d0	RO	<i>por_fmu_errgsr_lsc_p0_d0</i> on page 4-1102
0x3068	por_fmu_errgsr_ioc_p0_d0	RO	<i>por_fmu_errgsr_ioc_p0_d0</i> on page 4-1103
0x3070	por_fmu_errgsr_async_p0_d0	RO	<i>por_fmu_errgsr_async_p0_d0</i> on page 4-1103
0x3078	por_fmu_errgsr_hang_p0_d0	RO	<i>por_fmu_errgsr_hang_p0_d0</i> on page 4-1104
0x3080	por_fmu_errgsr_mpu_p0_d0	RO	<i>por_fmu_errgsr_mpu_p0_d0</i> on page 4-1105
0x3088	por_fmu_errgsr_eccue_p0_d0	RO	<i>por_fmu_errgsr_eccue_p0_d0</i> on page 4-1106
0x3090	por_fmu_errgsr_eccce_p0_d0	RO	<i>por_fmu_errgsr_eccce_p0_d0</i> on page 4-1107
0x3098	por_fmu_errgsr_clk_p0_d1	RO	<i>por_fmu_errgsr_clk_p0_d1</i> on page 4-1108
0x30A0	por_fmu_errgsr_rst_p0_d1	RO	<i>por_fmu_errgsr_rst_p0_d1</i> on page 4-1109
0x30A8	por_fmu_errgsr_lsc_p0_d1	RO	<i>por_fmu_errgsr_lsc_p0_d1</i> on page 4-1109
0x30B0	por_fmu_errgsr_ioc_p0_d1	RO	<i>por_fmu_errgsr_ioc_p0_d1</i> on page 4-1110
0x30B8	por_fmu_errgsr_async_p0_d1	RO	<i>por_fmu_errgsr_async_p0_d1</i> on page 4-1111
0x30C0	por_fmu_errgsr_hang_p0_d1	RO	<i>por_fmu_errgsr_hang_p0_d1</i> on page 4-1112
0x30C8	por_fmu_errgsr_mpu_p0_d1	RO	<i>por_fmu_errgsr_mpu_p0_d1</i> on page 4-1113
0x30D0	por_fmu_errgsr_eccue_p0_d1	RO	<i>por_fmu_errgsr_eccue_p0_d1</i> on page 4-1114
0x30D8	por_fmu_errgsr_eccce_p0_d1	RO	<i>por_fmu_errgsr_eccce_p0_d1</i> on page 4-1115
0x30E0	por_fmu_errgsr_clk_p0_d2	RO	<i>por_fmu_errgsr_clk_p0_d2</i> on page 4-1115
0x30E8	por_fmu_errgsr_rst_p0_d2	RO	<i>por_fmu_errgsr_rst_p0_d2</i> on page 4-1116
0x30F0	por_fmu_errgsr_lsc_p0_d2	RO	<i>por_fmu_errgsr_lsc_p0_d2</i> on page 4-1117
0x30F8	por_fmu_errgsr_ioc_p0_d2	RO	<i>por_fmu_errgsr_ioc_p0_d2</i> on page 4-1118
0x3100	por_fmu_errgsr_async_p0_d2	RO	<i>por_fmu_errgsr_async_p0_d2</i> on page 4-1119
0x3108	por_fmu_errgsr_hang_p0_d2	RO	<i>por_fmu_errgsr_hang_p0_d2</i> on page 4-1120
0x3110	por_fmu_errgsr_mpu_p0_d2	RO	<i>por_fmu_errgsr_mpu_p0_d2</i> on page 4-1121
0x3118	por_fmu_errgsr_eccue_p0_d2	RO	<i>por_fmu_errgsr_eccue_p0_d2</i> on page 4-1121
0x3120	por_fmu_errgsr_eccce_p0_d2	RO	<i>por_fmu_errgsr_eccce_p0_d2</i> on page 4-1122
0x3128	por_fmu_errgsr_clk_p0_d3	RO	<i>por_fmu_errgsr_clk_p0_d3</i> on page 4-1123
0x3130	por_fmu_errgsr_rst_p0_d3	RO	<i>por_fmu_errgsr_rst_p0_d3</i> on page 4-1124
0x3138	por_fmu_errgsr_lsc_p0_d3	RO	<i>por_fmu_errgsr_lsc_p0_d3</i> on page 4-1125
0x3140	por_fmu_errgsr_ioc_p0_d3	RO	<i>por_fmu_errgsr_ioc_p0_d3</i> on page 4-1126
0x3148	por_fmu_errgsr_async_p0_d3	RO	<i>por_fmu_errgsr_async_p0_d3</i> on page 4-1127
0x3150	por_fmu_errgsr_hang_p0_d3	RO	<i>por_fmu_errgsr_hang_p0_d3</i> on page 4-1127

Table 4-15 FMU register summary (continued)

Offset	Name	Type	Description
0x3158	por_fmu_errgsr_mpu_p0_d3	RO	por_fmu_errgsr_mpu_p0_d3 on page 4-1128
0x3160	por_fmu_errgsr_eccue_p0_d3	RO	por_fmu_errgsr_eccue_p0_d3 on page 4-1129
0x3168	por_fmu_errgsr_eccce_p0_d3	RO	por_fmu_errgsr_eccce_p0_d3 on page 4-1130
0x3170	por_fmu_errgsr_clk_p1_d0	RO	por_fmu_errgsr_clk_p1_d0 on page 4-1131
0x3178	por_fmu_errgsr_rst_p1_d0	RO	por_fmu_errgsr_rst_p1_d0 on page 4-1132
0x3180	por_fmu_errgsr_lsc_p1_d0	RO	por_fmu_errgsr_lsc_p1_d0 on page 4-1133
0x3188	por_fmu_errgsr_ioc_p1_d0	RO	por_fmu_errgsr_ioc_p1_d0 on page 4-1133
0x3190	por_fmu_errgsr_async_p1_d0	RO	por_fmu_errgsr_async_p1_d0 on page 4-1134
0x3198	por_fmu_errgsr_hang_p1_d0	RO	por_fmu_errgsr_hang_p1_d0 on page 4-1135
0x31A0	por_fmu_errgsr_mpu_p1_d0	RO	por_fmu_errgsr_mpu_p1_d0 on page 4-1136
0x31A8	por_fmu_errgsr_eccue_p1_d0	RO	por_fmu_errgsr_eccue_p1_d0 on page 4-1137
0x31B0	por_fmu_errgsr_eccce_p1_d0	RO	por_fmu_errgsr_eccce_p1_d0 on page 4-1138
0x31B8	por_fmu_errgsr_clk_p1_d1	RO	por_fmu_errgsr_clk_p1_d1 on page 4-1139
0x31C0	por_fmu_errgsr_rst_p1_d1	RO	por_fmu_errgsr_rst_p1_d1 on page 4-1139
0x31C8	por_fmu_errgsr_lsc_p1_d1	RO	por_fmu_errgsr_lsc_p1_d1 on page 4-1140
0x31D0	por_fmu_errgsr_ioc_p1_d1	RO	por_fmu_errgsr_ioc_p1_d1 on page 4-1141
0x31D8	por_fmu_errgsr_async_p1_d1	RO	por_fmu_errgsr_async_p1_d1 on page 4-1142
0x31E0	por_fmu_errgsr_hang_p1_d1	RO	por_fmu_errgsr_hang_p1_d1 on page 4-1143
0x31E8	por_fmu_errgsr_mpu_p1_d1	RO	por_fmu_errgsr_mpu_p1_d1 on page 4-1144
0x31F0	por_fmu_errgsr_eccue_p1_d1	RO	por_fmu_errgsr_eccue_p1_d1 on page 4-1145
0x31F8	por_fmu_errgsr_eccce_p1_d1	RO	por_fmu_errgsr_eccce_p1_d1 on page 4-1145
0x3200	por_fmu_errgsr_clk_p1_d2	RO	por_fmu_errgsr_clk_p1_d2 on page 4-1146
0x3208	por_fmu_errgsr_rst_p1_d2	RO	por_fmu_errgsr_rst_p1_d2 on page 4-1147
0x3210	por_fmu_errgsr_lsc_p1_d2	RO	por_fmu_errgsr_lsc_p1_d2 on page 4-1148
0x3218	por_fmu_errgsr_ioc_p1_d2	RO	por_fmu_errgsr_ioc_p1_d2 on page 4-1149
0x3220	por_fmu_errgsr_async_p1_d2	RO	por_fmu_errgsr_async_p1_d2 on page 4-1150
0x3228	por_fmu_errgsr_hang_p1_d2	RO	por_fmu_errgsr_hang_p1_d2 on page 4-1151
0x3230	por_fmu_errgsr_mpu_p1_d2	RO	por_fmu_errgsr_mpu_p1_d2 on page 4-1151
0x3238	por_fmu_errgsr_eccue_p1_d2	RO	por_fmu_errgsr_eccue_p1_d2 on page 4-1152
0x3240	por_fmu_errgsr_eccce_p1_d2	RO	por_fmu_errgsr_eccce_p1_d2 on page 4-1153
0x3248	por_fmu_errgsr_clk_p1_d3	RO	por_fmu_errgsr_clk_p1_d3 on page 4-1154
0x3250	por_fmu_errgsr_rst_p1_d3	RO	por_fmu_errgsr_rst_p1_d3 on page 4-1155
0x3258	por_fmu_errgsr_lsc_p1_d3	RO	por_fmu_errgsr_lsc_p1_d3 on page 4-1156
0x3260	por_fmu_errgsr_ioc_p1_d3	RO	por_fmu_errgsr_ioc_p1_d3 on page 4-1157
0x3268	por_fmu_errgsr_async_p1_d3	RO	por_fmu_errgsr_async_p1_d3 on page 4-1157

Table 4-15 FMU register summary (continued)

Offset	Name	Type	Description
0x3270	por_fmu_errgsr_hang_p1_d3	RO	por_fmu_errgsr_hang_p1_d3 on page 4-1158
0x3278	por_fmu_errgsr_mpu_p1_d3	RO	por_fmu_errgsr_mpu_p1_d3 on page 4-1159
0x3280	por_fmu_errgsr_eccue_p1_d3	RO	por_fmu_errgsr_eccue_p1_d3 on page 4-1160
0x3288	por_fmu_errgsr_eccce_p1_d3	RO	por_fmu_errgsr_eccce_p1_d3 on page 4-1161

4.2.15 MPU register summary

This section lists the MPU registers used in CMN-600AE.

MPU register summary

The following table shows the *MPU* registers in offset order from the base memory address.

Table 4-16 MPU register summary

Offset	Name	Type	Description
0x0	por_mpu_node_info	RO	por_mpu_node_info on page 4-1162
0x80	por_mpu_child_info	RO	por_mpu_child_info on page 4-1163
0x900	por_mpu_unit_info	RO	por_mpu_unit_info on page 4-1164
0x1000	por_mpu_m0_ctl	RW	por_mpu_m0_ctl on page 4-1166
0x1010	por_mpu_m0_prbar0	RW	por_mpu_m0_prbar0 on page 4-1167
0x1018	por_mpu_m0_prlar0	RW	por_mpu_m0_prlar0 on page 4-1168
0x1020	por_mpu_m0_prbar1	RW	por_mpu_m0_prbar1 on page 4-1169
0x1028	por_mpu_m0_prlar1	RW	por_mpu_m0_prlar1 on page 4-1170
0x1030	por_mpu_m0_prbar2	RW	por_mpu_m0_prbar2 on page 4-1171
0x1038	por_mpu_m0_prlar2	RW	por_mpu_m0_prlar2 on page 4-1173
0x1040	por_mpu_m0_prbar3	RW	por_mpu_m0_prbar3 on page 4-1174
0x1048	por_mpu_m0_prlar3	RW	por_mpu_m0_prlar3 on page 4-1175
0x1050	por_mpu_m0_prbar4	RW	por_mpu_m0_prbar4 on page 4-1176
0x1058	por_mpu_m0_prlar4	RW	por_mpu_m0_prlar4 on page 4-1177
0x1060	por_mpu_m0_prbar5	RW	por_mpu_m0_prbar5 on page 4-1178
0x1068	por_mpu_m0_prlar5	RW	por_mpu_m0_prlar5 on page 4-1180
0x1070	por_mpu_m0_prbar6	RW	por_mpu_m0_prbar6 on page 4-1181
0x1078	por_mpu_m0_prlar6	RW	por_mpu_m0_prlar6 on page 4-1182
0x1080	por_mpu_m0_prbar7	RW	por_mpu_m0_prbar7 on page 4-1183
0x1088	por_mpu_m0_prlar7	RW	por_mpu_m0_prlar7 on page 4-1184
0x1090	por_mpu_m0_prbar8	RW	por_mpu_m0_prbar8 on page 4-1185
0x1098	por_mpu_m0_prlar8	RW	por_mpu_m0_prlar8 on page 4-1187
0x10A0	por_mpu_m0_prbar9	RW	por_mpu_m0_prbar9 on page 4-1188

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x10A8	por_mpu_m0_prlar9	RW	por_mpu_m0_prlar9 on page 4-1189
0x10B0	por_mpu_m0_prbar10	RW	por_mpu_m0_prbar10 on page 4-1190
0x10B8	por_mpu_m0_prlar10	RW	por_mpu_m0_prlar10 on page 4-1191
0x10C0	por_mpu_m0_prbar11	RW	por_mpu_m0_prbar11 on page 4-1192
0x10C8	por_mpu_m0_prlar11	RW	por_mpu_m0_prlar11 on page 4-1194
0x10D0	por_mpu_m0_prbar12	RW	por_mpu_m0_prbar12 on page 4-1195
0x10D8	por_mpu_m0_prlar12	RW	por_mpu_m0_prlar12 on page 4-1196
0x10E0	por_mpu_m0_prbar13	RW	por_mpu_m0_prbar13 on page 4-1197
0x10E8	por_mpu_m0_prlar13	RW	por_mpu_m0_prlar13 on page 4-1198
0x10F0	por_mpu_m0_prbar14	RW	por_mpu_m0_prbar14 on page 4-1199
0x10F8	por_mpu_m0_prlar14	RW	por_mpu_m0_prlar14 on page 4-1201
0x1100	por_mpu_m0_prbar15	RW	por_mpu_m0_prbar15 on page 4-1202
0x1108	por_mpu_m0_prlar15	RW	por_mpu_m0_prlar15 on page 4-1203
0x1110	por_mpu_m0_prbar16	RW	por_mpu_m0_prbar16 on page 4-1204
0x1118	por_mpu_m0_prlar16	RW	por_mpu_m0_prlar16 on page 4-1205
0x1120	por_mpu_m0_prbar17	RW	por_mpu_m0_prbar17 on page 4-1206
0x1128	por_mpu_m0_prlar17	RW	por_mpu_m0_prlar17 on page 4-1208
0x1130	por_mpu_m0_prbar18	RW	por_mpu_m0_prbar18 on page 4-1209
0x1138	por_mpu_m0_prlar18	RW	por_mpu_m0_prlar18 on page 4-1210
0x1140	por_mpu_m0_prbar19	RW	por_mpu_m0_prbar19 on page 4-1211
0x1148	por_mpu_m0_prlar19	RW	por_mpu_m0_prlar19 on page 4-1212
0x1150	por_mpu_m0_prbar20	RW	por_mpu_m0_prbar20 on page 4-1213
0x1158	por_mpu_m0_prlar20	RW	por_mpu_m0_prlar20 on page 4-1215
0x1160	por_mpu_m0_prbar21	RW	por_mpu_m0_prbar21 on page 4-1216
0x1168	por_mpu_m0_prlar21	RW	por_mpu_m0_prlar21 on page 4-1217
0x1170	por_mpu_m0_prbar22	RW	por_mpu_m0_prbar22 on page 4-1218
0x1178	por_mpu_m0_prlar22	RW	por_mpu_m0_prlar22 on page 4-1219
0x1180	por_mpu_m0_prbar23	RW	por_mpu_m0_prbar23 on page 4-1220
0x1188	por_mpu_m0_prlar23	RW	por_mpu_m0_prlar23 on page 4-1222
0x1190	por_mpu_m0_prbar24	RW	por_mpu_m0_prbar24 on page 4-1223
0x1198	por_mpu_m0_prlar24	RW	por_mpu_m0_prlar24 on page 4-1224
0x11A0	por_mpu_m0_prbar25	RW	por_mpu_m0_prbar25 on page 4-1225
0x11A8	por_mpu_m0_prlar25	RW	por_mpu_m0_prlar25 on page 4-1226
0x11B0	por_mpu_m0_prbar26	RW	por_mpu_m0_prbar26 on page 4-1227
0x11B8	por_mpu_m0_prlar26	RW	por_mpu_m0_prlar26 on page 4-1229

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x11C0	por_mpu_m0_prbar27	RW	por_mpu_m0_prbar27 on page 4-1230
0x11C8	por_mpu_m0_prlar27	RW	por_mpu_m0_prlar27 on page 4-1231
0x11D0	por_mpu_m0_prbar28	RW	por_mpu_m0_prbar28 on page 4-1232
0x11D8	por_mpu_m0_prlar28	RW	por_mpu_m0_prlar28 on page 4-1233
0x11E0	por_mpu_m0_prbar29	RW	por_mpu_m0_prbar29 on page 4-1234
0x11E8	por_mpu_m0_prlar29	RW	por_mpu_m0_prlar29 on page 4-1236
0x11F0	por_mpu_m0_prbar30	RW	por_mpu_m0_prbar30 on page 4-1237
0x11F8	por_mpu_m0_prlar30	RW	por_mpu_m0_prlar30 on page 4-1238
0x1200	por_mpu_m0_prbar31	RW	por_mpu_m0_prbar31 on page 4-1239
0x1208	por_mpu_m0_prlar31	RW	por_mpu_m0_prlar31 on page 4-1240
0x1400	por_mpu_m1_ctl	RW	por_mpu_m1_ctl on page 4-1241
0x1410	por_mpu_m1_prbar0	RW	por_mpu_m1_prbar0 on page 4-1242
0x1418	por_mpu_m1_prlar0	RW	por_mpu_m1_prlar0 on page 4-1244
0x1420	por_mpu_m1_prbar1	RW	por_mpu_m1_prbar1 on page 4-1245
0x1428	por_mpu_m1_prlar1	RW	por_mpu_m1_prlar1 on page 4-1246
0x1430	por_mpu_m1_prbar2	RW	por_mpu_m1_prbar2 on page 4-1247
0x1438	por_mpu_m1_prlar2	RW	por_mpu_m1_prlar2 on page 4-1248
0x1440	por_mpu_m1_prbar3	RW	por_mpu_m1_prbar3 on page 4-1249
0x1448	por_mpu_m1_prlar3	RW	por_mpu_m1_prlar3 on page 4-1251
0x1450	por_mpu_m1_prbar4	RW	por_mpu_m1_prbar4 on page 4-1252
0x1458	por_mpu_m1_prlar4	RW	por_mpu_m1_prlar4 on page 4-1253
0x1460	por_mpu_m1_prbar5	RW	por_mpu_m1_prbar5 on page 4-1254
0x1468	por_mpu_m1_prlar5	RW	por_mpu_m1_prlar5 on page 4-1255
0x1470	por_mpu_m1_prbar6	RW	por_mpu_m1_prbar6 on page 4-1256
0x1478	por_mpu_m1_prlar6	RW	por_mpu_m1_prlar6 on page 4-1258
0x1480	por_mpu_m1_prbar7	RW	por_mpu_m1_prbar7 on page 4-1259
0x1488	por_mpu_m1_prlar7	RW	por_mpu_m1_prlar7 on page 4-1260
0x1490	por_mpu_m1_prbar8	RW	por_mpu_m1_prbar8 on page 4-1261
0x1498	por_mpu_m1_prlar8	RW	por_mpu_m1_prlar8 on page 4-1262
0x14A0	por_mpu_m1_prbar9	RW	por_mpu_m1_prbar9 on page 4-1263
0x14A8	por_mpu_m1_prlar9	RW	por_mpu_m1_prlar9 on page 4-1265
0x14B0	por_mpu_m1_prbar10	RW	por_mpu_m1_prbar10 on page 4-1266
0x14B8	por_mpu_m1_prlar10	RW	por_mpu_m1_prlar10 on page 4-1267
0x14C0	por_mpu_m1_prbar11	RW	por_mpu_m1_prbar11 on page 4-1268
0x14C8	por_mpu_m1_prlar11	RW	por_mpu_m1_prlar11 on page 4-1269

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x14D0	por_mpu_m1_prbar12	RW	por_mpu_m1_prbar12 on page 4-1270
0x14D8	por_mpu_m1_prlar12	RW	por_mpu_m1_prlar12 on page 4-1272
0x14E0	por_mpu_m1_prbar13	RW	por_mpu_m1_prbar13 on page 4-1273
0x14E8	por_mpu_m1_prlar13	RW	por_mpu_m1_prlar13 on page 4-1274
0x14F0	por_mpu_m1_prbar14	RW	por_mpu_m1_prbar14 on page 4-1275
0x14F8	por_mpu_m1_prlar14	RW	por_mpu_m1_prlar14 on page 4-1276
0x1500	por_mpu_m1_prbar15	RW	por_mpu_m1_prbar15 on page 4-1277
0x1508	por_mpu_m1_prlar15	RW	por_mpu_m1_prlar15 on page 4-1279
0x1510	por_mpu_m1_prbar16	RW	por_mpu_m1_prbar16 on page 4-1280
0x1518	por_mpu_m1_prlar16	RW	por_mpu_m1_prlar16 on page 4-1281
0x1520	por_mpu_m1_prbar17	RW	por_mpu_m1_prbar17 on page 4-1282
0x1528	por_mpu_m1_prlar17	RW	por_mpu_m1_prlar17 on page 4-1283
0x1530	por_mpu_m1_prbar18	RW	por_mpu_m1_prbar18 on page 4-1284
0x1538	por_mpu_m1_prlar18	RW	por_mpu_m1_prlar18 on page 4-1286
0x1540	por_mpu_m1_prbar19	RW	por_mpu_m1_prbar19 on page 4-1287
0x1548	por_mpu_m1_prlar19	RW	por_mpu_m1_prlar19 on page 4-1288
0x1550	por_mpu_m1_prbar20	RW	por_mpu_m1_prbar20 on page 4-1289
0x1558	por_mpu_m1_prlar20	RW	por_mpu_m1_prlar20 on page 4-1290
0x1560	por_mpu_m1_prbar21	RW	por_mpu_m1_prbar21 on page 4-1291
0x1568	por_mpu_m1_prlar21	RW	por_mpu_m1_prlar21 on page 4-1293
0x1570	por_mpu_m1_prbar22	RW	por_mpu_m1_prbar22 on page 4-1294
0x1578	por_mpu_m1_prlar22	RW	por_mpu_m1_prlar22 on page 4-1295
0x1580	por_mpu_m1_prbar23	RW	por_mpu_m1_prbar23 on page 4-1296
0x1588	por_mpu_m1_prlar23	RW	por_mpu_m1_prlar23 on page 4-1297
0x1590	por_mpu_m1_prbar24	RW	por_mpu_m1_prbar24 on page 4-1298
0x1598	por_mpu_m1_prlar24	RW	por_mpu_m1_prlar24 on page 4-1300
0x15A0	por_mpu_m1_prbar25	RW	por_mpu_m1_prbar25 on page 4-1301
0x15A8	por_mpu_m1_prlar25	RW	por_mpu_m1_prlar25 on page 4-1302
0x15B0	por_mpu_m1_prbar26	RW	por_mpu_m1_prbar26 on page 4-1303
0x15B8	por_mpu_m1_prlar26	RW	por_mpu_m1_prlar26 on page 4-1304
0x15C0	por_mpu_m1_prbar27	RW	por_mpu_m1_prbar27 on page 4-1305
0x15C8	por_mpu_m1_prlar27	RW	por_mpu_m1_prlar27 on page 4-1307
0x15D0	por_mpu_m1_prbar28	RW	por_mpu_m1_prbar28 on page 4-1308
0x15D8	por_mpu_m1_prlar28	RW	por_mpu_m1_prlar28 on page 4-1309
0x15E0	por_mpu_m1_prbar29	RW	por_mpu_m1_prbar29 on page 4-1310

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x15E8	por_mpu_m1_prlar29	RW	por_mpu_m1_prlar29 on page 4-1311
0x15F0	por_mpu_m1_prbar30	RW	por_mpu_m1_prbar30 on page 4-1312
0x15F8	por_mpu_m1_prlar30	RW	por_mpu_m1_prlar30 on page 4-1314
0x1600	por_mpu_m1_prbar31	RW	por_mpu_m1_prbar31 on page 4-1315
0x1608	por_mpu_m1_prlar31	RW	por_mpu_m1_prlar31 on page 4-1316
0x1800	por_mpu_m2_ctl	RW	por_mpu_m2_ctl on page 4-1317
0x1810	por_mpu_m2_prbar0	RW	por_mpu_m2_prbar0 on page 4-1318
0x1818	por_mpu_m2_prlar0	RW	por_mpu_m2_prlar0 on page 4-1319
0x1820	por_mpu_m2_prbar1	RW	por_mpu_m2_prbar1 on page 4-1320
0x1828	por_mpu_m2_prlar1	RW	por_mpu_m2_prlar1 on page 4-1322
0x1830	por_mpu_m2_prbar2	RW	por_mpu_m2_prbar2 on page 4-1323
0x1838	por_mpu_m2_prlar2	RW	por_mpu_m2_prlar2 on page 4-1324
0x1840	por_mpu_m2_prbar3	RW	por_mpu_m2_prbar3 on page 4-1325
0x1848	por_mpu_m2_prlar3	RW	por_mpu_m2_prlar3 on page 4-1327
0x1850	por_mpu_m2_prbar4	RW	por_mpu_m2_prbar4 on page 4-1328
0x1858	por_mpu_m2_prlar4	RW	por_mpu_m2_prlar4 on page 4-1329
0x1860	por_mpu_m2_prbar5	RW	por_mpu_m2_prbar5 on page 4-1330
0x1868	por_mpu_m2_prlar5	RW	por_mpu_m2_prlar5 on page 4-1331
0x1870	por_mpu_m2_prbar6	RW	por_mpu_m2_prbar6 on page 4-1332
0x1878	por_mpu_m2_prlar6	RW	por_mpu_m2_prlar6 on page 4-1334
0x1880	por_mpu_m2_prbar7	RW	por_mpu_m2_prbar7 on page 4-1335
0x1888	por_mpu_m2_prlar7	RW	por_mpu_m2_prlar7 on page 4-1336
0x1890	por_mpu_m2_prbar8	RW	por_mpu_m2_prbar8 on page 4-1337
0x1898	por_mpu_m2_prlar8	RW	por_mpu_m2_prlar8 on page 4-1338
0x18A0	por_mpu_m2_prbar9	RW	por_mpu_m2_prbar9 on page 4-1339
0x18A8	por_mpu_m2_prlar9	RW	por_mpu_m2_prlar9 on page 4-1341
0x18B0	por_mpu_m2_prbar10	RW	por_mpu_m2_prbar10 on page 4-1342
0x18B8	por_mpu_m2_prlar10	RW	por_mpu_m2_prlar10 on page 4-1343
0x18C0	por_mpu_m2_prbar11	RW	por_mpu_m2_prbar11 on page 4-1344
0x18C8	por_mpu_m2_prlar11	RW	por_mpu_m2_prlar11 on page 4-1345
0x18D0	por_mpu_m2_prbar12	RW	por_mpu_m2_prbar12 on page 4-1346
0x18D8	por_mpu_m2_prlar12	RW	por_mpu_m2_prlar12 on page 4-1348
0x18E0	por_mpu_m2_prbar13	RW	por_mpu_m2_prbar13 on page 4-1349
0x18E8	por_mpu_m2_prlar13	RW	por_mpu_m2_prlar13 on page 4-1350
0x18F0	por_mpu_m2_prbar14	RW	por_mpu_m2_prbar14 on page 4-1351

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x18F8	por_mpu_m2_prlar14	RW	por_mpu_m2_prlar14 on page 4-1352
0x1900	por_mpu_m2_prbar15	RW	por_mpu_m2_prbar15 on page 4-1353
0x1908	por_mpu_m2_prlar15	RW	por_mpu_m2_prlar15 on page 4-1355
0x1910	por_mpu_m2_prbar16	RW	por_mpu_m2_prbar16 on page 4-1356
0x1918	por_mpu_m2_prlar16	RW	por_mpu_m2_prlar16 on page 4-1357
0x1920	por_mpu_m2_prbar17	RW	por_mpu_m2_prbar17 on page 4-1358
0x1928	por_mpu_m2_prlar17	RW	por_mpu_m2_prlar17 on page 4-1359
0x1930	por_mpu_m2_prbar18	RW	por_mpu_m2_prbar18 on page 4-1360
0x1938	por_mpu_m2_prlar18	RW	por_mpu_m2_prlar18 on page 4-1362
0x1940	por_mpu_m2_prbar19	RW	por_mpu_m2_prbar19 on page 4-1363
0x1948	por_mpu_m2_prlar19	RW	por_mpu_m2_prlar19 on page 4-1364
0x1950	por_mpu_m2_prbar20	RW	por_mpu_m2_prbar20 on page 4-1365
0x1958	por_mpu_m2_prlar20	RW	por_mpu_m2_prlar20 on page 4-1366
0x1960	por_mpu_m2_prbar21	RW	por_mpu_m2_prbar21 on page 4-1367
0x1968	por_mpu_m2_prlar21	RW	por_mpu_m2_prlar21 on page 4-1369
0x1970	por_mpu_m2_prbar22	RW	por_mpu_m2_prbar22 on page 4-1370
0x1978	por_mpu_m2_prlar22	RW	por_mpu_m2_prlar22 on page 4-1371
0x1980	por_mpu_m2_prbar23	RW	por_mpu_m2_prbar23 on page 4-1372
0x1988	por_mpu_m2_prlar23	RW	por_mpu_m2_prlar23 on page 4-1373
0x1990	por_mpu_m2_prbar24	RW	por_mpu_m2_prbar24 on page 4-1374
0x1998	por_mpu_m2_prlar24	RW	por_mpu_m2_prlar24 on page 4-1376
0x19A0	por_mpu_m2_prbar25	RW	por_mpu_m2_prbar25 on page 4-1377
0x19A8	por_mpu_m2_prlar25	RW	por_mpu_m2_prlar25 on page 4-1378
0x19B0	por_mpu_m2_prbar26	RW	por_mpu_m2_prbar26 on page 4-1379
0x19B8	por_mpu_m2_prlar26	RW	por_mpu_m2_prlar26 on page 4-1380
0x19C0	por_mpu_m2_prbar27	RW	por_mpu_m2_prbar27 on page 4-1381
0x19C8	por_mpu_m2_prlar27	RW	por_mpu_m2_prlar27 on page 4-1383
0x19D0	por_mpu_m2_prbar28	RW	por_mpu_m2_prbar28 on page 4-1384
0x19D8	por_mpu_m2_prlar28	RW	por_mpu_m2_prlar28 on page 4-1385
0x19E0	por_mpu_m2_prbar29	RW	por_mpu_m2_prbar29 on page 4-1386
0x19E8	por_mpu_m2_prlar29	RW	por_mpu_m2_prlar29 on page 4-1387
0x19F0	por_mpu_m2_prbar30	RW	por_mpu_m2_prbar30 on page 4-1388
0x19F8	por_mpu_m2_prlar30	RW	por_mpu_m2_prlar30 on page 4-1390
0x1A00	por_mpu_m2_prbar31	RW	por_mpu_m2_prbar31 on page 4-1391
0x1A08	por_mpu_m2_prlar31	RW	por_mpu_m2_prlar31 on page 4-1392

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x1C00	por_mpu_m3_ctl	RW	por_mpu_m3_ctl on page 4-1393
0x1C10	por_mpu_m3_prbar0	RW	por_mpu_m3_prbar0 on page 4-1394
0x1C18	por_mpu_m3_prlar0	RW	por_mpu_m3_prlar0 on page 4-1395
0x1C20	por_mpu_m3_prbar1	RW	por_mpu_m3_prbar1 on page 4-1396
0x1C28	por_mpu_m3_prlar1	RW	por_mpu_m3_prlar1 on page 4-1398
0x1C30	por_mpu_m3_prbar2	RW	por_mpu_m3_prbar2 on page 4-1399
0x1C38	por_mpu_m3_prlar2	RW	por_mpu_m3_prlar2 on page 4-1400
0x1C40	por_mpu_m3_prbar3	RW	por_mpu_m3_prbar3 on page 4-1401
0x1C48	por_mpu_m3_prlar3	RW	por_mpu_m3_prlar3 on page 4-1403
0x1C50	por_mpu_m3_prbar4	RW	por_mpu_m3_prbar4 on page 4-1404
0x1C58	por_mpu_m3_prlar4	RW	por_mpu_m3_prlar4 on page 4-1405
0x1C60	por_mpu_m3_prbar5	RW	por_mpu_m3_prbar5 on page 4-1406
0x1C68	por_mpu_m3_prlar5	RW	por_mpu_m3_prlar5 on page 4-1407
0x1C70	por_mpu_m3_prbar6	RW	por_mpu_m3_prbar6 on page 4-1408
0x1C78	por_mpu_m3_prlar6	RW	por_mpu_m3_prlar6 on page 4-1410
0x1C80	por_mpu_m3_prbar7	RW	por_mpu_m3_prbar7 on page 4-1411
0x1C88	por_mpu_m3_prlar7	RW	por_mpu_m3_prlar7 on page 4-1412
0x1C90	por_mpu_m3_prbar8	RW	por_mpu_m3_prbar8 on page 4-1413
0x1C98	por_mpu_m3_prlar8	RW	por_mpu_m3_prlar8 on page 4-1414
0x1CA0	por_mpu_m3_prbar9	RW	por_mpu_m3_prbar9 on page 4-1415
0x1CA8	por_mpu_m3_prlar9	RW	por_mpu_m3_prlar9 on page 4-1417
0x1CB0	por_mpu_m3_prbar10	RW	por_mpu_m3_prbar10 on page 4-1418
0x1CB8	por_mpu_m3_prlar10	RW	por_mpu_m3_prlar10 on page 4-1419
0x1CC0	por_mpu_m3_prbar11	RW	por_mpu_m3_prbar11 on page 4-1420
0x1CC8	por_mpu_m3_prlar11	RW	por_mpu_m3_prlar11 on page 4-1421
0x1CD0	por_mpu_m3_prbar12	RW	por_mpu_m3_prbar12 on page 4-1422
0x1CD8	por_mpu_m3_prlar12	RW	por_mpu_m3_prlar12 on page 4-1424
0x1CE0	por_mpu_m3_prbar13	RW	por_mpu_m3_prbar13 on page 4-1425
0x1CE8	por_mpu_m3_prlar13	RW	por_mpu_m3_prlar13 on page 4-1426
0x1CF0	por_mpu_m3_prbar14	RW	por_mpu_m3_prbar14 on page 4-1427
0x1CF8	por_mpu_m3_prlar14	RW	por_mpu_m3_prlar14 on page 4-1428
0x1D00	por_mpu_m3_prbar15	RW	por_mpu_m3_prbar15 on page 4-1429
0x1D08	por_mpu_m3_prlar15	RW	por_mpu_m3_prlar15 on page 4-1431
0x1D10	por_mpu_m3_prbar16	RW	por_mpu_m3_prbar16 on page 4-1432
0x1D18	por_mpu_m3_prlar16	RW	por_mpu_m3_prlar16 on page 4-1433

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x1D20	por_mpu_m3_prbar17	RW	por_mpu_m3_prbar17 on page 4-1434
0x1D28	por_mpu_m3_prlar17	RW	por_mpu_m3_prlar17 on page 4-1435
0x1D30	por_mpu_m3_prbar18	RW	por_mpu_m3_prbar18 on page 4-1436
0x1D38	por_mpu_m3_prlar18	RW	por_mpu_m3_prlar18 on page 4-1438
0x1D40	por_mpu_m3_prbar19	RW	por_mpu_m3_prbar19 on page 4-1439
0x1D48	por_mpu_m3_prlar19	RW	por_mpu_m3_prlar19 on page 4-1440
0x1D50	por_mpu_m3_prbar20	RW	por_mpu_m3_prbar20 on page 4-1441
0x1D58	por_mpu_m3_prlar20	RW	por_mpu_m3_prlar20 on page 4-1442
0x1D60	por_mpu_m3_prbar21	RW	por_mpu_m3_prbar21 on page 4-1443
0x1D68	por_mpu_m3_prlar21	RW	por_mpu_m3_prlar21 on page 4-1445
0x1D70	por_mpu_m3_prbar22	RW	por_mpu_m3_prbar22 on page 4-1446
0x1D78	por_mpu_m3_prlar22	RW	por_mpu_m3_prlar22 on page 4-1447
0x1D80	por_mpu_m3_prbar23	RW	por_mpu_m3_prbar23 on page 4-1448
0x1D88	por_mpu_m3_prlar23	RW	por_mpu_m3_prlar23 on page 4-1449
0x1D90	por_mpu_m3_prbar24	RW	por_mpu_m3_prbar24 on page 4-1450
0x1D98	por_mpu_m3_prlar24	RW	por_mpu_m3_prlar24 on page 4-1452
0x1DA0	por_mpu_m3_prbar25	RW	por_mpu_m3_prbar25 on page 4-1453
0x1DA8	por_mpu_m3_prlar25	RW	por_mpu_m3_prlar25 on page 4-1454
0x1DB0	por_mpu_m3_prbar26	RW	por_mpu_m3_prbar26 on page 4-1455
0x1DB8	por_mpu_m3_prlar26	RW	por_mpu_m3_prlar26 on page 4-1456
0x1DC0	por_mpu_m3_prbar27	RW	por_mpu_m3_prbar27 on page 4-1457
0x1DC8	por_mpu_m3_prlar27	RW	por_mpu_m3_prlar27 on page 4-1459
0x1DD0	por_mpu_m3_prbar28	RW	por_mpu_m3_prbar28 on page 4-1460
0x1DD8	por_mpu_m3_prlar28	RW	por_mpu_m3_prlar28 on page 4-1461
0x1DE0	por_mpu_m3_prbar29	RW	por_mpu_m3_prbar29 on page 4-1462
0x1DE8	por_mpu_m3_prlar29	RW	por_mpu_m3_prlar29 on page 4-1463
0x1DF0	por_mpu_m3_prbar30	RW	por_mpu_m3_prbar30 on page 4-1464
0x1DF8	por_mpu_m3_prlar30	RW	por_mpu_m3_prlar30 on page 4-1466
0x1E00	por_mpu_m3_prbar31	RW	por_mpu_m3_prbar31 on page 4-1467
0x1E08	por_mpu_m3_prlar31	RW	por_mpu_m3_prlar31 on page 4-1468
0x2000	por_mpu_m4_ctl	RW	por_mpu_m4_ctl on page 4-1469
0x2010	por_mpu_m4_prbar0	RW	por_mpu_m4_prbar0 on page 4-1470
0x2018	por_mpu_m4_prlar0	RW	por_mpu_m4_prlar0 on page 4-1471
0x2020	por_mpu_m4_prbar1	RW	por_mpu_m4_prbar1 on page 4-1472
0x2028	por_mpu_m4_prlar1	RW	por_mpu_m4_prlar1 on page 4-1474

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x2030	por_mpu_m4_prbar2	RW	por_mpu_m4_prbar2 on page 4-1475
0x2038	por_mpu_m4_prlar2	RW	por_mpu_m4_prlar2 on page 4-1476
0x2040	por_mpu_m4_prbar3	RW	por_mpu_m4_prbar3 on page 4-1477
0x2048	por_mpu_m4_prlar3	RW	por_mpu_m4_prlar3 on page 4-1479
0x2050	por_mpu_m4_prbar4	RW	por_mpu_m4_prbar4 on page 4-1480
0x2058	por_mpu_m4_prlar4	RW	por_mpu_m4_prlar4 on page 4-1481
0x2060	por_mpu_m4_prbar5	RW	por_mpu_m4_prbar5 on page 4-1482
0x2068	por_mpu_m4_prlar5	RW	por_mpu_m4_prlar5 on page 4-1483
0x2070	por_mpu_m4_prbar6	RW	por_mpu_m4_prbar6 on page 4-1484
0x2078	por_mpu_m4_prlar6	RW	por_mpu_m4_prlar6 on page 4-1486
0x2080	por_mpu_m4_prbar7	RW	por_mpu_m4_prbar7 on page 4-1487
0x2088	por_mpu_m4_prlar7	RW	por_mpu_m4_prlar7 on page 4-1488
0x2090	por_mpu_m4_prbar8	RW	por_mpu_m4_prbar8 on page 4-1489
0x2098	por_mpu_m4_prlar8	RW	por_mpu_m4_prlar8 on page 4-1490
0x20A0	por_mpu_m4_prbar9	RW	por_mpu_m4_prbar9 on page 4-1491
0x20A8	por_mpu_m4_prlar9	RW	por_mpu_m4_prlar9 on page 4-1493
0x20B0	por_mpu_m4_prbar10	RW	por_mpu_m4_prbar10 on page 4-1494
0x20B8	por_mpu_m4_prlar10	RW	por_mpu_m4_prlar10 on page 4-1495
0x20C0	por_mpu_m4_prbar11	RW	por_mpu_m4_prbar11 on page 4-1496
0x20C8	por_mpu_m4_prlar11	RW	por_mpu_m4_prlar11 on page 4-1497
0x20D0	por_mpu_m4_prbar12	RW	por_mpu_m4_prbar12 on page 4-1498
0x20D8	por_mpu_m4_prlar12	RW	por_mpu_m4_prlar12 on page 4-1500
0x20E0	por_mpu_m4_prbar13	RW	por_mpu_m4_prbar13 on page 4-1501
0x20E8	por_mpu_m4_prlar13	RW	por_mpu_m4_prlar13 on page 4-1502
0x20F0	por_mpu_m4_prbar14	RW	por_mpu_m4_prbar14 on page 4-1503
0x20F8	por_mpu_m4_prlar14	RW	por_mpu_m4_prlar14 on page 4-1504
0x2100	por_mpu_m4_prbar15	RW	por_mpu_m4_prbar15 on page 4-1505
0x2108	por_mpu_m4_prlar15	RW	por_mpu_m4_prlar15 on page 4-1507
0x2110	por_mpu_m4_prbar16	RW	por_mpu_m4_prbar16 on page 4-1508
0x2118	por_mpu_m4_prlar16	RW	por_mpu_m4_prlar16 on page 4-1509
0x2120	por_mpu_m4_prbar17	RW	por_mpu_m4_prbar17 on page 4-1510
0x2128	por_mpu_m4_prlar17	RW	por_mpu_m4_prlar17 on page 4-1511
0x2130	por_mpu_m4_prbar18	RW	por_mpu_m4_prbar18 on page 4-1512
0x2138	por_mpu_m4_prlar18	RW	por_mpu_m4_prlar18 on page 4-1514
0x2140	por_mpu_m4_prbar19	RW	por_mpu_m4_prbar19 on page 4-1515

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x2148	por_mpu_m4_prlar19	RW	por_mpu_m4_prlar19 on page 4-1516
0x2150	por_mpu_m4_prbar20	RW	por_mpu_m4_prbar20 on page 4-1517
0x2158	por_mpu_m4_prlar20	RW	por_mpu_m4_prlar20 on page 4-1518
0x2160	por_mpu_m4_prbar21	RW	por_mpu_m4_prbar21 on page 4-1519
0x2168	por_mpu_m4_prlar21	RW	por_mpu_m4_prlar21 on page 4-1521
0x2170	por_mpu_m4_prbar22	RW	por_mpu_m4_prbar22 on page 4-1522
0x2178	por_mpu_m4_prlar22	RW	por_mpu_m4_prlar22 on page 4-1523
0x2180	por_mpu_m4_prbar23	RW	por_mpu_m4_prbar23 on page 4-1524
0x2188	por_mpu_m4_prlar23	RW	por_mpu_m4_prlar23 on page 4-1525
0x2190	por_mpu_m4_prbar24	RW	por_mpu_m4_prbar24 on page 4-1526
0x2198	por_mpu_m4_prlar24	RW	por_mpu_m4_prlar24 on page 4-1528
0x21A0	por_mpu_m4_prbar25	RW	por_mpu_m4_prbar25 on page 4-1529
0x21A8	por_mpu_m4_prlar25	RW	por_mpu_m4_prlar25 on page 4-1530
0x21B0	por_mpu_m4_prbar26	RW	por_mpu_m4_prbar26 on page 4-1531
0x21B8	por_mpu_m4_prlar26	RW	por_mpu_m4_prlar26 on page 4-1532
0x21C0	por_mpu_m4_prbar27	RW	por_mpu_m4_prbar27 on page 4-1533
0x21C8	por_mpu_m4_prlar27	RW	por_mpu_m4_prlar27 on page 4-1535
0x21D0	por_mpu_m4_prbar28	RW	por_mpu_m4_prbar28 on page 4-1536
0x21D8	por_mpu_m4_prlar28	RW	por_mpu_m4_prlar28 on page 4-1537
0x21E0	por_mpu_m4_prbar29	RW	por_mpu_m4_prbar29 on page 4-1538
0x21E8	por_mpu_m4_prlar29	RW	por_mpu_m4_prlar29 on page 4-1539
0x21F0	por_mpu_m4_prbar30	RW	por_mpu_m4_prbar30 on page 4-1540
0x21F8	por_mpu_m4_prlar30	RW	por_mpu_m4_prlar30 on page 4-1542
0x2200	por_mpu_m4_prbar31	RW	por_mpu_m4_prbar31 on page 4-1543
0x2208	por_mpu_m4_prlar31	RW	por_mpu_m4_prlar31 on page 4-1544
0x2400	por_mpu_m5_ctl	RW	por_mpu_m5_ctl on page 4-1545
0x2410	por_mpu_m5_prbar0	RW	por_mpu_m5_prbar0 on page 4-1546
0x2418	por_mpu_m5_prlar0	RW	por_mpu_m5_prlar0 on page 4-1547
0x2420	por_mpu_m5_prbar1	RW	por_mpu_m5_prbar1 on page 4-1548
0x2428	por_mpu_m5_prlar1	RW	por_mpu_m5_prlar1 on page 4-1550
0x2430	por_mpu_m5_prbar2	RW	por_mpu_m5_prbar2 on page 4-1551
0x2438	por_mpu_m5_prlar2	RW	por_mpu_m5_prlar2 on page 4-1552
0x2440	por_mpu_m5_prbar3	RW	por_mpu_m5_prbar3 on page 4-1553
0x2448	por_mpu_m5_prlar3	RW	por_mpu_m5_prlar3 on page 4-1555
0x2450	por_mpu_m5_prbar4	RW	por_mpu_m5_prbar4 on page 4-1556

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x2458	por_mpu_m5_prlar4	RW	por_mpu_m5_prlar4 on page 4-1557
0x2460	por_mpu_m5_prbar5	RW	por_mpu_m5_prbar5 on page 4-1558
0x2468	por_mpu_m5_prlar5	RW	por_mpu_m5_prlar5 on page 4-1559
0x2470	por_mpu_m5_prbar6	RW	por_mpu_m5_prbar6 on page 4-1560
0x2478	por_mpu_m5_prlar6	RW	por_mpu_m5_prlar6 on page 4-1562
0x2480	por_mpu_m5_prbar7	RW	por_mpu_m5_prbar7 on page 4-1563
0x2488	por_mpu_m5_prlar7	RW	por_mpu_m5_prlar7 on page 4-1564
0x2490	por_mpu_m5_prbar8	RW	por_mpu_m5_prbar8 on page 4-1565
0x2498	por_mpu_m5_prlar8	RW	por_mpu_m5_prlar8 on page 4-1566
0x24A0	por_mpu_m5_prbar9	RW	por_mpu_m5_prbar9 on page 4-1567
0x24A8	por_mpu_m5_prlar9	RW	por_mpu_m5_prlar9 on page 4-1569
0x24B0	por_mpu_m5_prbar10	RW	por_mpu_m5_prbar10 on page 4-1570
0x24B8	por_mpu_m5_prlar10	RW	por_mpu_m5_prlar10 on page 4-1571
0x24C0	por_mpu_m5_prbar11	RW	por_mpu_m5_prbar11 on page 4-1572
0x24C8	por_mpu_m5_prlar11	RW	por_mpu_m5_prlar11 on page 4-1573
0x24D0	por_mpu_m5_prbar12	RW	por_mpu_m5_prbar12 on page 4-1574
0x24D8	por_mpu_m5_prlar12	RW	por_mpu_m5_prlar12 on page 4-1576
0x24E0	por_mpu_m5_prbar13	RW	por_mpu_m5_prbar13 on page 4-1577
0x24E8	por_mpu_m5_prlar13	RW	por_mpu_m5_prlar13 on page 4-1578
0x24F0	por_mpu_m5_prbar14	RW	por_mpu_m5_prbar14 on page 4-1579
0x24F8	por_mpu_m5_prlar14	RW	por_mpu_m5_prlar14 on page 4-1580
0x2500	por_mpu_m5_prbar15	RW	por_mpu_m5_prbar15 on page 4-1581
0x2508	por_mpu_m5_prlar15	RW	por_mpu_m5_prlar15 on page 4-1583
0x2510	por_mpu_m5_prbar16	RW	por_mpu_m5_prbar16 on page 4-1584
0x2518	por_mpu_m5_prlar16	RW	por_mpu_m5_prlar16 on page 4-1585
0x2520	por_mpu_m5_prbar17	RW	por_mpu_m5_prbar17 on page 4-1586
0x2528	por_mpu_m5_prlar17	RW	por_mpu_m5_prlar17 on page 4-1587
0x2530	por_mpu_m5_prbar18	RW	por_mpu_m5_prbar18 on page 4-1588
0x2538	por_mpu_m5_prlar18	RW	por_mpu_m5_prlar18 on page 4-1590
0x2540	por_mpu_m5_prbar19	RW	por_mpu_m5_prbar19 on page 4-1591
0x2548	por_mpu_m5_prlar19	RW	por_mpu_m5_prlar19 on page 4-1592
0x2550	por_mpu_m5_prbar20	RW	por_mpu_m5_prbar20 on page 4-1593
0x2558	por_mpu_m5_prlar20	RW	por_mpu_m5_prlar20 on page 4-1594
0x2560	por_mpu_m5_prbar21	RW	por_mpu_m5_prbar21 on page 4-1595
0x2568	por_mpu_m5_prlar21	RW	por_mpu_m5_prlar21 on page 4-1597

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x2570	por_mpu_m5_prbar22	RW	por_mpu_m5_prbar22 on page 4-1598
0x2578	por_mpu_m5_prlar22	RW	por_mpu_m5_prlar22 on page 4-1599
0x2580	por_mpu_m5_prbar23	RW	por_mpu_m5_prbar23 on page 4-1600
0x2588	por_mpu_m5_prlar23	RW	por_mpu_m5_prlar23 on page 4-1601
0x2590	por_mpu_m5_prbar24	RW	por_mpu_m5_prbar24 on page 4-1602
0x2598	por_mpu_m5_prlar24	RW	por_mpu_m5_prlar24 on page 4-1604
0x25A0	por_mpu_m5_prbar25	RW	por_mpu_m5_prbar25 on page 4-1605
0x25A8	por_mpu_m5_prlar25	RW	por_mpu_m5_prlar25 on page 4-1606
0x25B0	por_mpu_m5_prbar26	RW	por_mpu_m5_prbar26 on page 4-1607
0x25B8	por_mpu_m5_prlar26	RW	por_mpu_m5_prlar26 on page 4-1608
0x25C0	por_mpu_m5_prbar27	RW	por_mpu_m5_prbar27 on page 4-1609
0x25C8	por_mpu_m5_prlar27	RW	por_mpu_m5_prlar27 on page 4-1611
0x25D0	por_mpu_m5_prbar28	RW	por_mpu_m5_prbar28 on page 4-1612
0x25D8	por_mpu_m5_prlar28	RW	por_mpu_m5_prlar28 on page 4-1613
0x25E0	por_mpu_m5_prbar29	RW	por_mpu_m5_prbar29 on page 4-1614
0x25E8	por_mpu_m5_prlar29	RW	por_mpu_m5_prlar29 on page 4-1615
0x25F0	por_mpu_m5_prbar30	RW	por_mpu_m5_prbar30 on page 4-1616
0x25F8	por_mpu_m5_prlar30	RW	por_mpu_m5_prlar30 on page 4-1618
0x2600	por_mpu_m5_prbar31	RW	por_mpu_m5_prbar31 on page 4-1619
0x2608	por_mpu_m5_prlar31	RW	por_mpu_m5_prlar31 on page 4-1620
0x2800	por_mpu_m6_ctl	RW	por_mpu_m6_ctl on page 4-1621
0x2810	por_mpu_m6_prbar0	RW	por_mpu_m6_prbar0 on page 4-1622
0x2818	por_mpu_m6_prlar0	RW	por_mpu_m6_prlar0 on page 4-1623
0x2820	por_mpu_m6_prbar1	RW	por_mpu_m6_prbar1 on page 4-1624
0x2828	por_mpu_m6_prlar1	RW	por_mpu_m6_prlar1 on page 4-1626
0x2830	por_mpu_m6_prbar2	RW	por_mpu_m6_prbar2 on page 4-1627
0x2838	por_mpu_m6_prlar2	RW	por_mpu_m6_prlar2 on page 4-1628
0x2840	por_mpu_m6_prbar3	RW	por_mpu_m6_prbar3 on page 4-1629
0x2848	por_mpu_m6_prlar3	RW	por_mpu_m6_prlar3 on page 4-1631
0x2850	por_mpu_m6_prbar4	RW	por_mpu_m6_prbar4 on page 4-1632
0x2858	por_mpu_m6_prlar4	RW	por_mpu_m6_prlar4 on page 4-1633
0x2860	por_mpu_m6_prbar5	RW	por_mpu_m6_prbar5 on page 4-1634
0x2868	por_mpu_m6_prlar5	RW	por_mpu_m6_prlar5 on page 4-1635
0x2870	por_mpu_m6_prbar6	RW	por_mpu_m6_prbar6 on page 4-1636
0x2878	por_mpu_m6_prlar6	RW	por_mpu_m6_prlar6 on page 4-1638

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x2880	por_mpu_m6_prbar7	RW	por_mpu_m6_prbar7 on page 4-1639
0x2888	por_mpu_m6_prlar7	RW	por_mpu_m6_prlar7 on page 4-1640
0x2890	por_mpu_m6_prbar8	RW	por_mpu_m6_prbar8 on page 4-1641
0x2898	por_mpu_m6_prlar8	RW	por_mpu_m6_prlar8 on page 4-1642
0x28A0	por_mpu_m6_prbar9	RW	por_mpu_m6_prbar9 on page 4-1643
0x28A8	por_mpu_m6_prlar9	RW	por_mpu_m6_prlar9 on page 4-1645
0x28B0	por_mpu_m6_prbar10	RW	por_mpu_m6_prbar10 on page 4-1646
0x28B8	por_mpu_m6_prlar10	RW	por_mpu_m6_prlar10 on page 4-1647
0x28C0	por_mpu_m6_prbar11	RW	por_mpu_m6_prbar11 on page 4-1648
0x28C8	por_mpu_m6_prlar11	RW	por_mpu_m6_prlar11 on page 4-1649
0x28D0	por_mpu_m6_prbar12	RW	por_mpu_m6_prbar12 on page 4-1650
0x28D8	por_mpu_m6_prlar12	RW	por_mpu_m6_prlar12 on page 4-1652
0x28E0	por_mpu_m6_prbar13	RW	por_mpu_m6_prbar13 on page 4-1653
0x28E8	por_mpu_m6_prlar13	RW	por_mpu_m6_prlar13 on page 4-1654
0x28F0	por_mpu_m6_prbar14	RW	por_mpu_m6_prbar14 on page 4-1655
0x28F8	por_mpu_m6_prlar14	RW	por_mpu_m6_prlar14 on page 4-1656
0x2900	por_mpu_m6_prbar15	RW	por_mpu_m6_prbar15 on page 4-1657
0x2908	por_mpu_m6_prlar15	RW	por_mpu_m6_prlar15 on page 4-1659
0x2910	por_mpu_m6_prbar16	RW	por_mpu_m6_prbar16 on page 4-1660
0x2918	por_mpu_m6_prlar16	RW	por_mpu_m6_prlar16 on page 4-1661
0x2920	por_mpu_m6_prbar17	RW	por_mpu_m6_prbar17 on page 4-1662
0x2928	por_mpu_m6_prlar17	RW	por_mpu_m6_prlar17 on page 4-1663
0x2930	por_mpu_m6_prbar18	RW	por_mpu_m6_prbar18 on page 4-1664
0x2938	por_mpu_m6_prlar18	RW	por_mpu_m6_prlar18 on page 4-1666
0x2940	por_mpu_m6_prbar19	RW	por_mpu_m6_prbar19 on page 4-1667
0x2948	por_mpu_m6_prlar19	RW	por_mpu_m6_prlar19 on page 4-1668
0x2950	por_mpu_m6_prbar20	RW	por_mpu_m6_prbar20 on page 4-1669
0x2958	por_mpu_m6_prlar20	RW	por_mpu_m6_prlar20 on page 4-1670
0x2960	por_mpu_m6_prbar21	RW	por_mpu_m6_prbar21 on page 4-1671
0x2968	por_mpu_m6_prlar21	RW	por_mpu_m6_prlar21 on page 4-1673
0x2970	por_mpu_m6_prbar22	RW	por_mpu_m6_prbar22 on page 4-1674
0x2978	por_mpu_m6_prlar22	RW	por_mpu_m6_prlar22 on page 4-1675
0x2980	por_mpu_m6_prbar23	RW	por_mpu_m6_prbar23 on page 4-1676
0x2988	por_mpu_m6_prlar23	RW	por_mpu_m6_prlar23 on page 4-1677
0x2990	por_mpu_m6_prbar24	RW	por_mpu_m6_prbar24 on page 4-1678

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x2998	por_mpu_m6_prlar24	RW	por_mpu_m6_prlar24 on page 4-1680
0x29A0	por_mpu_m6_prbar25	RW	por_mpu_m6_prbar25 on page 4-1681
0x29A8	por_mpu_m6_prlar25	RW	por_mpu_m6_prlar25 on page 4-1682
0x29B0	por_mpu_m6_prbar26	RW	por_mpu_m6_prbar26 on page 4-1683
0x29B8	por_mpu_m6_prlar26	RW	por_mpu_m6_prlar26 on page 4-1684
0x29C0	por_mpu_m6_prbar27	RW	por_mpu_m6_prbar27 on page 4-1685
0x29C8	por_mpu_m6_prlar27	RW	por_mpu_m6_prlar27 on page 4-1687
0x29D0	por_mpu_m6_prbar28	RW	por_mpu_m6_prbar28 on page 4-1688
0x29D8	por_mpu_m6_prlar28	RW	por_mpu_m6_prlar28 on page 4-1689
0x29E0	por_mpu_m6_prbar29	RW	por_mpu_m6_prbar29 on page 4-1690
0x29E8	por_mpu_m6_prlar29	RW	por_mpu_m6_prlar29 on page 4-1691
0x29F0	por_mpu_m6_prbar30	RW	por_mpu_m6_prbar30 on page 4-1692
0x29F8	por_mpu_m6_prlar30	RW	por_mpu_m6_prlar30 on page 4-1694
0x2A00	por_mpu_m6_prbar31	RW	por_mpu_m6_prbar31 on page 4-1695
0x2A08	por_mpu_m6_prlar31	RW	por_mpu_m6_prlar31 on page 4-1696
0x2C00	por_mpu_m7_ctl	RW	por_mpu_m7_ctl on page 4-1697
0x2C10	por_mpu_m7_prbar0	RW	por_mpu_m7_prbar0 on page 4-1698
0x2C18	por_mpu_m7_prlar0	RW	por_mpu_m7_prlar0 on page 4-1699
0x2C20	por_mpu_m7_prbar1	RW	por_mpu_m7_prbar1 on page 4-1700
0x2C28	por_mpu_m7_prlar1	RW	por_mpu_m7_prlar1 on page 4-1702
0x2C30	por_mpu_m7_prbar2	RW	por_mpu_m7_prbar2 on page 4-1703
0x2C38	por_mpu_m7_prlar2	RW	por_mpu_m7_prlar2 on page 4-1704
0x2C40	por_mpu_m7_prbar3	RW	por_mpu_m7_prbar3 on page 4-1705
0x2C48	por_mpu_m7_prlar3	RW	por_mpu_m7_prlar3 on page 4-1707
0x2C50	por_mpu_m7_prbar4	RW	por_mpu_m7_prbar4 on page 4-1708
0x2C58	por_mpu_m7_prlar4	RW	por_mpu_m7_prlar4 on page 4-1709
0x2C60	por_mpu_m7_prbar5	RW	por_mpu_m7_prbar5 on page 4-1710
0x2C68	por_mpu_m7_prlar5	RW	por_mpu_m7_prlar5 on page 4-1711
0x2C70	por_mpu_m7_prbar6	RW	por_mpu_m7_prbar6 on page 4-1712
0x2C78	por_mpu_m7_prlar6	RW	por_mpu_m7_prlar6 on page 4-1714
0x2C80	por_mpu_m7_prbar7	RW	por_mpu_m7_prbar7 on page 4-1715
0x2C88	por_mpu_m7_prlar7	RW	por_mpu_m7_prlar7 on page 4-1716
0x2C90	por_mpu_m7_prbar8	RW	por_mpu_m7_prbar8 on page 4-1717
0x2C98	por_mpu_m7_prlar8	RW	por_mpu_m7_prlar8 on page 4-1718
0x2CA0	por_mpu_m7_prbar9	RW	por_mpu_m7_prbar9 on page 4-1719

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x2CA8	por_mpu_m7_prlar9	RW	por_mpu_m7_prlar9 on page 4-1721
0x2CB0	por_mpu_m7_prbar10	RW	por_mpu_m7_prbar10 on page 4-1722
0x2CB8	por_mpu_m7_prlar10	RW	por_mpu_m7_prlar10 on page 4-1723
0x2CC0	por_mpu_m7_prbar11	RW	por_mpu_m7_prbar11 on page 4-1724
0x2CC8	por_mpu_m7_prlar11	RW	por_mpu_m7_prlar11 on page 4-1725
0x2CD0	por_mpu_m7_prbar12	RW	por_mpu_m7_prbar12 on page 4-1726
0x2CD8	por_mpu_m7_prlar12	RW	por_mpu_m7_prlar12 on page 4-1728
0x2CE0	por_mpu_m7_prbar13	RW	por_mpu_m7_prbar13 on page 4-1729
0x2CE8	por_mpu_m7_prlar13	RW	por_mpu_m7_prlar13 on page 4-1730
0x2CF0	por_mpu_m7_prbar14	RW	por_mpu_m7_prbar14 on page 4-1731
0x2CF8	por_mpu_m7_prlar14	RW	por_mpu_m7_prlar14 on page 4-1732
0x2D00	por_mpu_m7_prbar15	RW	por_mpu_m7_prbar15 on page 4-1733
0x2D08	por_mpu_m7_prlar15	RW	por_mpu_m7_prlar15 on page 4-1735
0x2D10	por_mpu_m7_prbar16	RW	por_mpu_m7_prbar16 on page 4-1736
0x2D18	por_mpu_m7_prlar16	RW	por_mpu_m7_prlar16 on page 4-1737
0x2D20	por_mpu_m7_prbar17	RW	por_mpu_m7_prbar17 on page 4-1738
0x2D28	por_mpu_m7_prlar17	RW	por_mpu_m7_prlar17 on page 4-1739
0x2D30	por_mpu_m7_prbar18	RW	por_mpu_m7_prbar18 on page 4-1740
0x2D38	por_mpu_m7_prlar18	RW	por_mpu_m7_prlar18 on page 4-1742
0x2D40	por_mpu_m7_prbar19	RW	por_mpu_m7_prbar19 on page 4-1743
0x2D48	por_mpu_m7_prlar19	RW	por_mpu_m7_prlar19 on page 4-1744
0x2D50	por_mpu_m7_prbar20	RW	por_mpu_m7_prbar20 on page 4-1745
0x2D58	por_mpu_m7_prlar20	RW	por_mpu_m7_prlar20 on page 4-1746
0x2D60	por_mpu_m7_prbar21	RW	por_mpu_m7_prbar21 on page 4-1747
0x2D68	por_mpu_m7_prlar21	RW	por_mpu_m7_prlar21 on page 4-1749
0x2D70	por_mpu_m7_prbar22	RW	por_mpu_m7_prbar22 on page 4-1750
0x2D78	por_mpu_m7_prlar22	RW	por_mpu_m7_prlar22 on page 4-1751
0x2D80	por_mpu_m7_prbar23	RW	por_mpu_m7_prbar23 on page 4-1752
0x2D88	por_mpu_m7_prlar23	RW	por_mpu_m7_prlar23 on page 4-1753
0x2D90	por_mpu_m7_prbar24	RW	por_mpu_m7_prbar24 on page 4-1754
0x2D98	por_mpu_m7_prlar24	RW	por_mpu_m7_prlar24 on page 4-1756
0x2DA0	por_mpu_m7_prbar25	RW	por_mpu_m7_prbar25 on page 4-1757
0x2DA8	por_mpu_m7_prlar25	RW	por_mpu_m7_prlar25 on page 4-1758
0x2DB0	por_mpu_m7_prbar26	RW	por_mpu_m7_prbar26 on page 4-1759
0x2DB8	por_mpu_m7_prlar26	RW	por_mpu_m7_prlar26 on page 4-1760

Table 4-16 MPU register summary (continued)

Offset	Name	Type	Description
0x2DC0	por_mpu_m7_prbar27	RW	por_mpu_m7_prbar27 on page 4-1761
0x2DC8	por_mpu_m7_prlar27	RW	por_mpu_m7_prlar27 on page 4-1763
0x2DD0	por_mpu_m7_prbar28	RW	por_mpu_m7_prbar28 on page 4-1764
0x2DD8	por_mpu_m7_prlar28	RW	por_mpu_m7_prlar28 on page 4-1765
0x2DE0	por_mpu_m7_prbar29	RW	por_mpu_m7_prbar29 on page 4-1766
0x2DE8	por_mpu_m7_prlar29	RW	por_mpu_m7_prlar29 on page 4-1767
0x2DF0	por_mpu_m7_prbar30	RW	por_mpu_m7_prbar30 on page 4-1768
0x2DF8	por_mpu_m7_prlar30	RW	por_mpu_m7_prlar30 on page 4-1770
0x2E00	por_mpu_m7_prbar31	RW	por_mpu_m7_prbar31 on page 4-1771
0x2E08	por_mpu_m7_prlar31	RW	por_mpu_m7_prlar31 on page 4-1772

4.2.16 FDC register summary

This section lists the FDC registers used in CMN-600AE.

FDC register summary

The following table shows the *FDC* registers in offset order from the base memory address.

Table 4-17 FDC register summary

Offset	Name	Type	Description
0x0	por_fdc_node_info	RO	por_fdc_node_info on page 4-1774
0x80	por_fdc_child_info	RO	por_fdc_child_info on page 4-1775
0x3300	por_errinject	WO	por_errinject on page 4-1775
0x3308	por_fdc_key	WO	por_fdc_key on page 4-1777
0x3000	por_errfr_mxp	RO	por_errfr_mxp on page 4-1778
0x3008	por_errctlr_mxp	RW	por_errctlr_mxp on page 4-1779
0x3010	por_errstatus_mxp	W1C	por_errstatus_mxp on page 4-1781
0x3018	por_fdc_aux_ctl_mxp	RW	por_fdc_aux_ctl_mxp on page 4-1783
0x3040	por_errfr_p0_d0	RO	por_errfr_p0_d0 on page 4-1783
0x3048	por_errctlr_p0_d0	RW	por_errctlr_p0_d0 on page 4-1784
0x3050	por_errstatus_p0_d0	W1C	por_errstatus_p0_d0 on page 4-1786
0x3058	por_fdc_aux_ctl_p0_d0	RW	por_fdc_aux_ctl_p0_d0 on page 4-1788
0x3080	por_errfr_p0_d1	RO	por_errfr_p0_d1 on page 4-1790
0x3088	por_errctlr_p0_d1	RW	por_errctlr_p0_d1 on page 4-1791
0x3090	por_errstatus_p0_d1	W1C	por_errstatus_p0_d1 on page 4-1792
0x3098	por_fdc_aux_ctl_p0_d1	RW	por_fdc_aux_ctl_p0_d1 on page 4-1794
0x30C0	por_errfr_p0_d2	RO	por_errfr_p0_d2 on page 4-1796

Table 4-17 FDC register summary (continued)

Offset	Name	Type	Description
0x30C8	por_errctlr_p0_d2	RW	por_errctlr_p0_d2 on page 4-1797
0x30D0	por_errstatus_p0_d2	W1C	por_errstatus_p0_d2 on page 4-1798
0x30D8	por_fdc_aux_ctl_p0_d2	RW	por_fdc_aux_ctl_p0_d2 on page 4-1800
0x3100	por_errfr_p0_d3	RO	por_errfr_p0_d3 on page 4-1802
0x3108	por_errctlr_p0_d3	RW	por_errctlr_p0_d3 on page 4-1803
0x3110	por_errstatus_p0_d3	W1C	por_errstatus_p0_d3 on page 4-1804
0x3118	por_fdc_aux_ctl_p0_d3	RW	por_fdc_aux_ctl_p0_d3 on page 4-1806
0x3140	por_errfr_p1_d0	RO	por_errfr_p1_d0 on page 4-1808
0x3148	por_errctlr_p1_d0	RW	por_errctlr_p1_d0 on page 4-1809
0x3150	por_errstatus_p1_d0	W1C	por_errstatus_p1_d0 on page 4-1810
0x3158	por_fdc_aux_ctl_p1_d0	RW	por_fdc_aux_ctl_p1_d0 on page 4-1812
0x3180	por_errfr_p1_d1	RO	por_errfr_p1_d1 on page 4-1814
0x3188	por_errctlr_p1_d1	RW	por_errctlr_p1_d1 on page 4-1815
0x3190	por_errstatus_p1_d1	W1C	por_errstatus_p1_d1 on page 4-1816
0x3198	por_fdc_aux_ctl_p1_d1	RW	por_fdc_aux_ctl_p1_d1 on page 4-1818
0x31C0	por_errfr_p1_d2	RO	por_errfr_p1_d2 on page 4-1820
0x31C8	por_errctlr_p1_d2	RW	por_errctlr_p1_d2 on page 4-1821
0x31D0	por_errstatus_p1_d2	W1C	por_errstatus_p1_d2 on page 4-1822
0x31D8	por_fdc_aux_ctl_p1_d2	RW	por_fdc_aux_ctl_p1_d2 on page 4-1824
0x3200	por_errfr_p1_d3	RO	por_errfr_p1_d3 on page 4-1826
0x3208	por_errctlr_p1_d3	RW	por_errctlr_p1_d3 on page 4-1827
0x3210	por_errstatus_p1_d3	W1C	por_errstatus_p1_d3 on page 4-1828
0x3218	por_fdc_aux_ctl_p1_d3	RW	por_fdc_aux_ctl_p1_d3 on page 4-1830

4.3 Register descriptions

This section contains register descriptions.

This section contains the following subsections:

- [4.3.1 Configuration master register descriptions on page 4-234.](#)
- [4.3.2 DN register descriptions on page 4-274.](#)
- [4.3.3 Debug and trace register descriptions on page 4-345.](#)
- [4.3.4 HN-F register descriptions on page 4-379.](#)
- [4.3.5 HN-I register descriptions on page 4-610.](#)
- [4.3.6 XP register descriptions on page 4-640.](#)
- [4.3.7 RN-D register descriptions on page 4-732.](#)
- [4.3.8 RN-I register descriptions on page 4-764.](#)
- [4.3.9 RN SAM register descriptions on page 4-794.](#)
- [4.3.10 SBSX register descriptions on page 4-882.](#)
- [4.3.11 CXHA configuration registers on page 4-902.](#)
- [4.3.12 CXRA configuration registers on page 4-966.](#)
- [4.3.13 CXLA configuration registers on page 4-1047.](#)
- [4.3.14 FMU register descriptions on page 4-1088.](#)
- [4.3.15 MPU register descriptions on page 4-1162.](#)
- [4.3.16 FDC configuration registers on page 4-1774.](#)

4.3.1 Configuration master register descriptions

This section lists the configuration registers.

por_cfgm_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

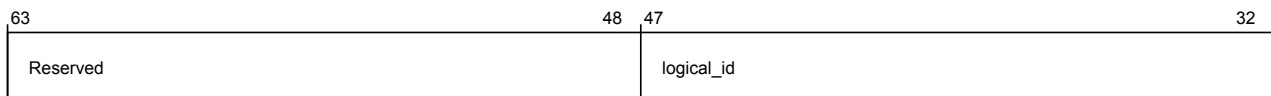


Figure 4-1 por_cfgm_por_cfgm_node_info (high)

The following table shows the por_cfgm_node_info higher register bit assignments.

Table 4-18 por_cfgm_por_cfgm_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

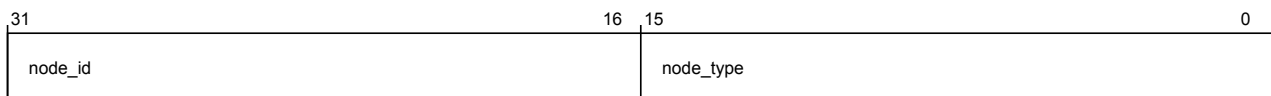


Figure 4-2 por_cfgm_por_cfgm_node_info (low)

The following table shows the por_cfgm_node_info lower register bit assignments.

Table 4-19 por_cfgm_por_cfgm_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0002

por_cfgm_periph_id_0_periph_id_1

Functions as the peripheral ID 0 and peripheral ID 1 register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h8
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

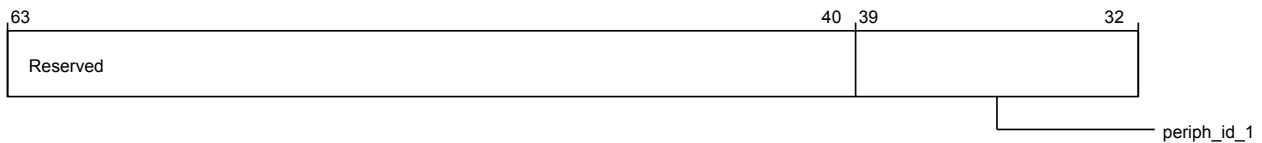


Figure 4-3 por_cfgm_periph_id_0_periph_id_1 (high)

The following table shows the por_cfgm_periph_id_0_periph_id_1 higher register bit assignments.

Table 4-20 por_cfgm_periph_id_0_periph_id_1 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_1	Peripheral ID 1	RO	8'b10110100

The following image shows the lower register bit assignments.

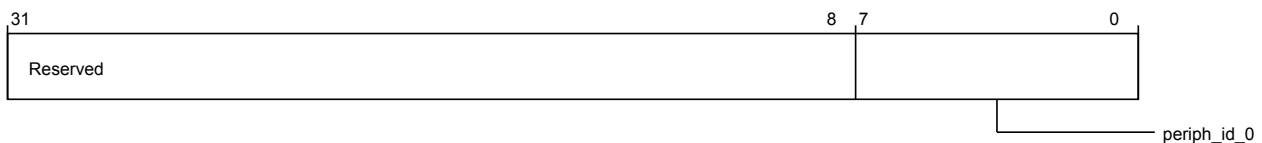


Figure 4-4 por_cfgm_periph_id_0_periph_id_1 (low)

The following table shows the por_cfgm_periph_id_0_periph_id_1 lower register bit assignments.

Table 4-21 por_cfgm_periph_id_0_periph_id_1 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_0	Peripheral ID 0	RO	Configuration dependent

por_cfgm_periph_id_2_periph_id_3

Functions as the peripheral ID 2 and peripheral ID 3 register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h10
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

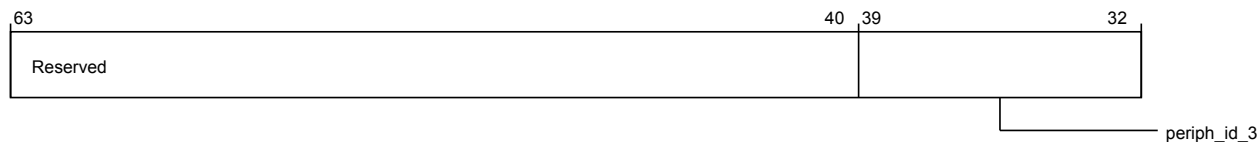


Figure 4-5 por_cfgm_por_cfgm_periph_id_2_periph_id_3 (high)

The following table shows the por_cfgm_periph_id_2_periph_id_3 higher register bit assignments.

Table 4-22 por_cfgm_por_cfgm_periph_id_2_periph_id_3 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_3	Peripheral ID 3	RO	8'b0

The following image shows the lower register bit assignments.

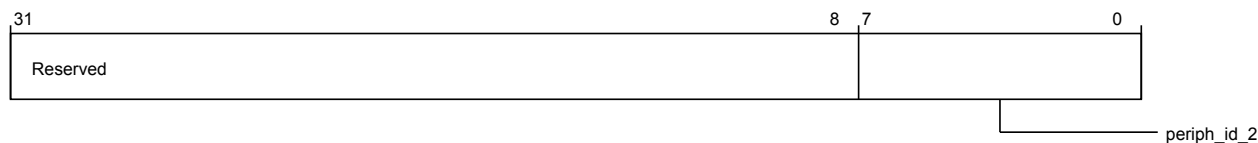


Figure 4-6 por_cfgm_por_cfgm_periph_id_2_periph_id_3 (low)

The following table shows the por_cfgm_periph_id_2_periph_id_3 lower register bit assignments.

Table 4-23 por_cfgm_por_cfgm_periph_id_2_periph_id_3 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_2	Peripheral ID 2 [7:4] indicates revision: 0x0 r1p0 0x1 r1p1 0x2 r1p2 0x3 r1p3 0x4 r2p0 [3] JEDEC JEP106 identity code, 1'b1 [2:0] JEP106 identity code [6:4], 0'b011	RO	Configuration dependent

por_cfgm_periph_id_4_periph_id_5

Functions as the peripheral ID 4 and peripheral ID 5 register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h18
Register reset	64'b011000100
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

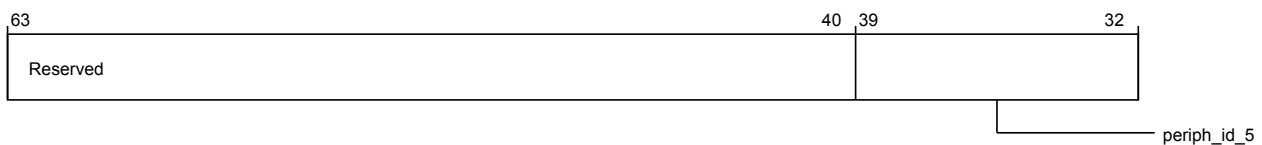


Figure 4-7 por_cfgm_por_cfgm_periph_id_4_periph_id_5 (high)

The following table shows the por_cfgm_periph_id_4_periph_id_5 higher register bit assignments.

Table 4-24 por_cfgm_por_cfgm_periph_id_4_periph_id_5 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_5	Peripheral ID 5	RO	8'b0

The following image shows the lower register bit assignments.

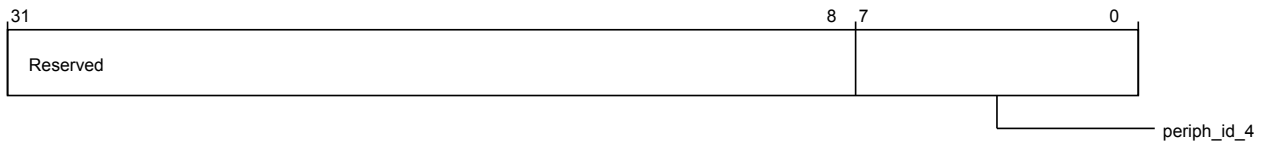


Figure 4-8 por_cfgm_periph_id_4_periph_id_5 (low)

The following table shows the por_cfgm_periph_id_4_periph_id_5 lower register bit assignments.

Table 4-25 por_cfgm_periph_id_4_periph_id_5 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_4	Peripheral ID 4	RO	8'b11000100

por_cfgm_periph_id_6_periph_id_7

Functions as the peripheral ID 6 and peripheral ID 7 register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h20
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

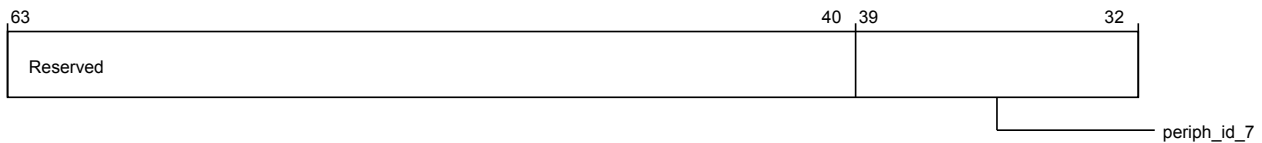


Figure 4-9 por_cfgm_periph_id_6_periph_id_7 (high)

The following table shows the por_cfgm_periph_id_6_periph_id_7 higher register bit assignments.

Table 4-26 por_cfgm_periph_id_6_periph_id_7 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_7	Peripheral ID 7	RO	8'b0

The following image shows the lower register bit assignments.

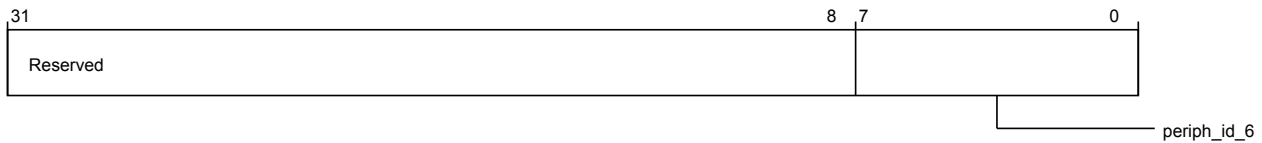


Figure 4-10 por_cfgm_por_cfgm_periph_id_6_periph_id_7 (low)

The following table shows the por_cfgm_periph_id_6_periph_id_7 lower register bit assignments.

Table 4-27 por_cfgm_por_cfgm_periph_id_6_periph_id_7 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_6	Peripheral ID 6	RO	8'b0

por_cfgm_component_id_0_component_id_1

Functions as the component ID 0 and component ID 1 register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h28
Register reset	64'b1111000000001101
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

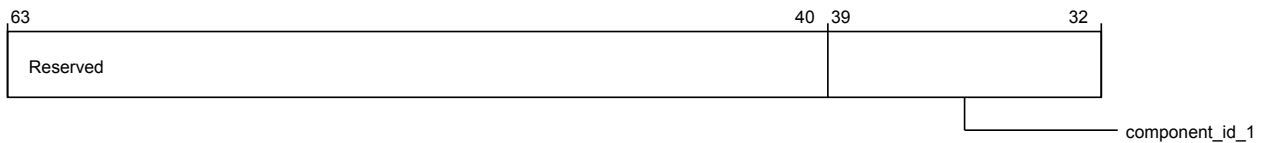


Figure 4-11 por_cfgm_por_cfgm_component_id_0_component_id_1 (high)

The following table shows the por_cfgm_component_id_0_component_id_1 higher register bit assignments.

Table 4-28 por_cfgm_por_cfgm_component_id_0_component_id_1 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	component_id_1	Component ID 1	RO	8'b11110000

The following image shows the lower register bit assignments.

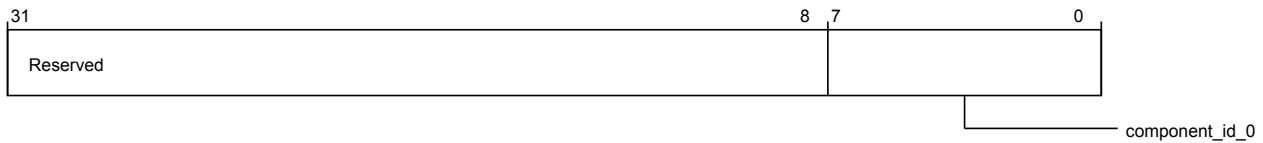


Figure 4-12 por_cfgm_por_cfgm_component_id_0_component_id_1 (low)

The following table shows the por_cfgm_component_id_0_component_id_1 lower register bit assignments.

Table 4-29 por_cfgm_por_cfgm_component_id_0_component_id_1 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	component_id_0	Component ID 0	RO	8'b00001101

por_cfgm_component_id_2_component_id_3

Functions as the component ID 2 and component ID 3 register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h30
Register reset	64'b1011000100000101
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

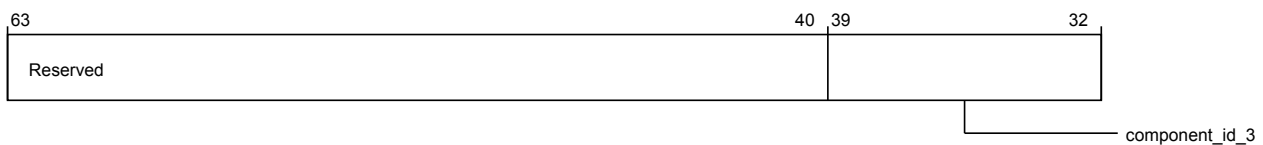


Figure 4-13 por_cfgm_por_cfgm_component_id_2_component_id_3 (high)

The following table shows the por_cfgm_component_id_2_component_id_3 higher register bit assignments.

Table 4-30 por_cfgm_por_cfgm_component_id_2_component_id_3 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	component_id_3	Component ID 3	RO	8'b10110001

The following image shows the lower register bit assignments.

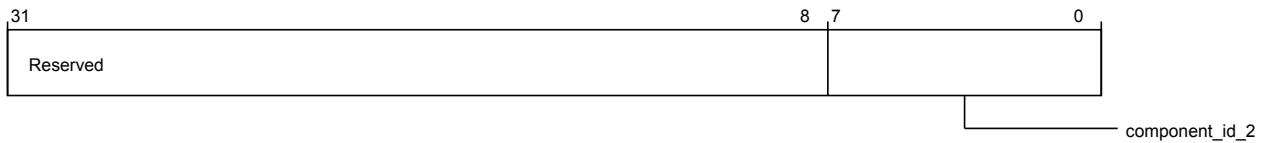


Figure 4-14 por_cfgm_por_cfgm_component_id_2_component_id_3 (low)

The following table shows the por_cfgm_component_id_2_component_id_3 lower register bit assignments.

Table 4-31 por_cfgm_por_cfgm_component_id_2_component_id_3 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	component_id_2	Component ID 2	RO	8'b00000101

por_cfgm_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

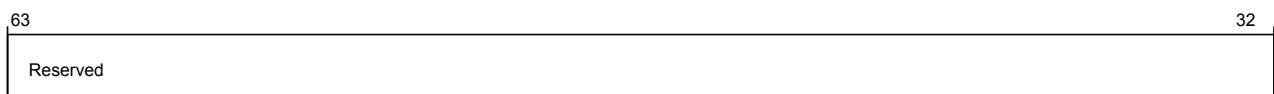


Figure 4-15 por_cfgm_por_cfgm_child_info (high)

The following table shows the por_cfgm_child_info higher register bit assignments.

Table 4-32 por_cfgm_por_cfgm_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

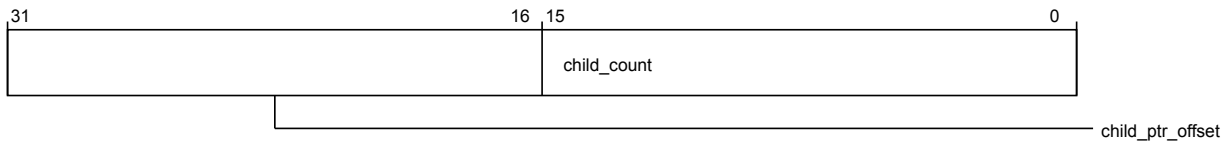


Figure 4-16 por_cfgm_por_cfgm_child_info (low)

The following table shows the por_cfgm_child_info lower register bit assignments.

Table 4-33 por_cfgm_por_cfgm_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h100
15:0	child_count	Number of child nodes; used in discovery process	RO	Configuration dependent

por_cfgm_secure_access

Functions as the secure access control register. This register must be set up at boot time. Before initiating a write to this register, software must ensure that no other configuration accesses are in flight. Once this write is initiated, no other configuration accesses are initiated until complete.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h980
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

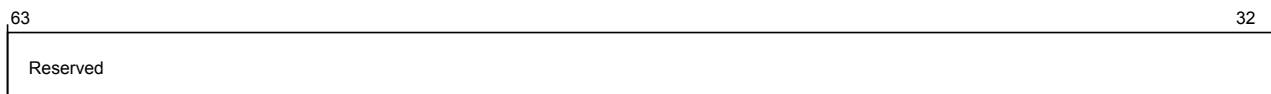


Figure 4-17 por_cfgm_por_cfgm_secure_access (high)

The following table shows the por_cfgm_secure_access higher register bit assignments.

Table 4-34 por_cfgm_por_cfgm_secure_access (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

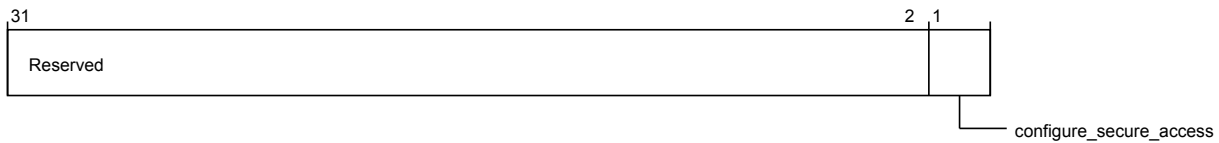


Figure 4-18 `por_cfgm_por_cfgm_secure_access` (low)

The following table shows the `por_cfgm_secure_access` lower register bit assignments.

Table 4-35 `por_cfgm_por_cfgm_secure_access` (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1:0	<code>configure_secure_access</code>	Secure access mode 2'b00: Default operation 2'b01: Allows non-secure access to secure registers 2'b10: Allows secure access only to any configuration register regardless of its security status 2'b11: Undefined behavior	RW	2'b0

`por_cfgm_errgsr0`

Provides the XP <n> secure error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3000

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

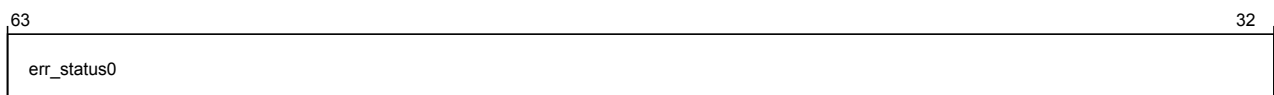


Figure 4-19 `por_cfgm_por_cfgm_errgsr0` (high)

The following table shows the `por_cfgm_errgsr0` higher register bit assignments.

Table 4-36 `por_cfgm_por_cfgm_errgsr0` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status0</code>	Read-only copy of <code>por_mxp_err<n>status</code>	RO	64'h0

The following image shows the lower register bit assignments.

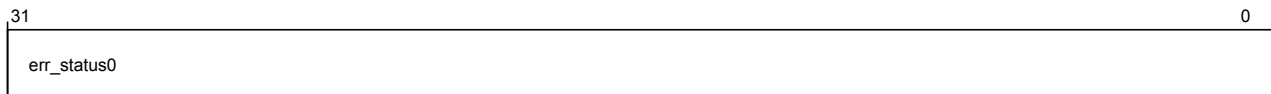


Figure 4-20 por_cfgm_por_cfgm_errgsr0 (low)

The following table shows the por_cfgm_errgsr0 lower register bit assignments.

Table 4-37 por_cfgm_por_cfgm_errgsr0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status0	Read-only copy of por_mxp_err<n>status	RO	64'h0

por_cfgm_errgsr1

Provides the HN-I <n> secure error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3008
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

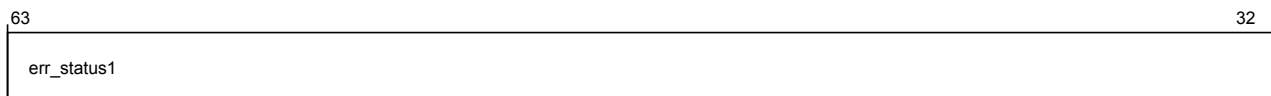


Figure 4-21 por_cfgm_por_cfgm_errgsr1 (high)

The following table shows the por_cfgm_errgsr1 higher register bit assignments.

Table 4-38 por_cfgm_por_cfgm_errgsr1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status1	Read-only copy of por_hni_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

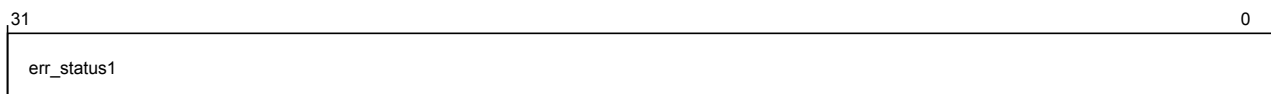


Figure 4-22 por_cfgm_por_cfgm_errgsr1 (low)

The following table shows the por_cfgm_errgsr1 lower register bit assignments.

Table 4-39 por_cfgm_por_cfgm_errgsr1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status1	Read-only copy of por_hni_err<n>status	RO	64'h0

por_cfgm_errgsr2

Provides the HN-F <n> secure error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3010

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

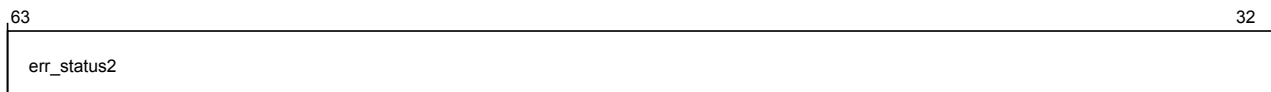


Figure 4-23 por_cfgm_por_cfgm_errgsr2 (high)

The following table shows the por_cfgm_errgsr2 higher register bit assignments.

Table 4-40 por_cfgm_por_cfgm_errgsr2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status2	Read-only copy of por_hnf_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

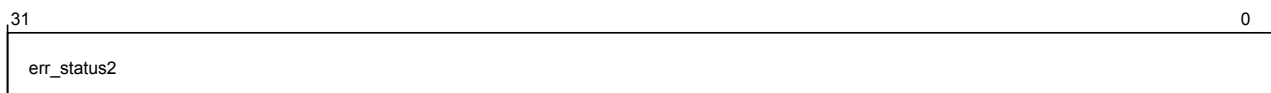


Figure 4-24 por_cfgm_por_cfgm_errgsr2 (low)

The following table shows the por_cfgm_errgsr2 lower register bit assignments.

Table 4-41 por_cfgm_por_cfgm_errgsr2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status2	Read-only copy of por_hnf_err<n>status	RO	64'h0

por_cfgm_errgsr3

Provides the SBSX <n> secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3018
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-25 por_cfgm_por_cfgm_errgsr3 (high)

The following table shows the por_cfgm_errgsr3 higher register bit assignments.

Table 4-42 por_cfgm_por_cfgm_errgsr3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status3	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

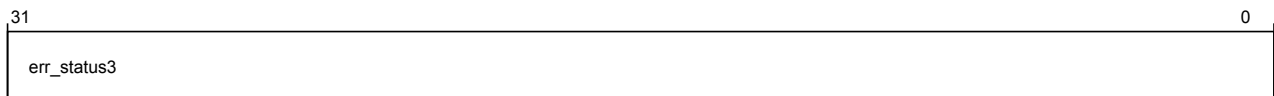


Figure 4-26 por_cfgm_por_cfgm_errgsr3 (low)

The following table shows the por_cfgm_errgsr3 lower register bit assignments.

Table 4-43 por_cfgm_por_cfgm_errgsr3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status3	Read-only copy of por_sbsx_err<n>status	RO	64'h0

por_cfgm_errgsr4

Provides the CXG <n> secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3020
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

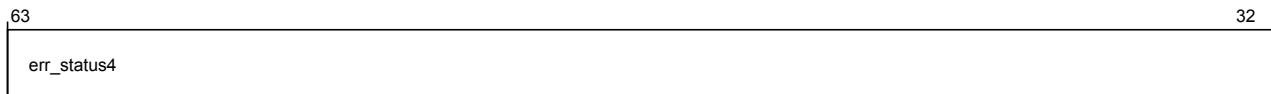


Figure 4-27 por_cfgm_por_cfgm_errgsr4 (high)

The following table shows the por_cfgm_errgsr4 higher register bit assignments.

Table 4-44 por_cfgm_por_cfgm_errgsr4 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status4	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

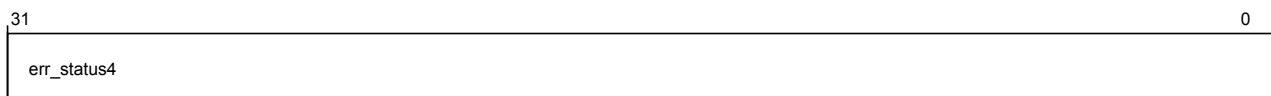


Figure 4-28 por_cfgm_por_cfgm_errgsr4 (low)

The following table shows the por_cfgm_errgsr4 lower register bit assignments.

Table 4-45 por_cfgm_por_cfgm_errgsr4 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status4	Read-only copy of por_cxg_err<n>status	RO	64'h0

por_cfgm_errgsr5

Provides the XP <n> secure fault status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3080

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

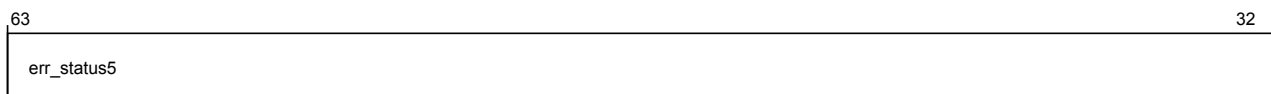


Figure 4-29 por_cfgm_por_cfgm_errgsr5 (high)

The following table shows the por_cfgm_errgsr5 higher register bit assignments.

Table 4-46 por_cfgm_por_cfgm_errgsr5 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status5	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-30 por_cfgm_por_cfgm_errgsr5 (low)

The following table shows the por_cfgm_errgsr5 lower register bit assignments.

Table 4-47 por_cfgm_por_cfgm_errgsr5 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status5	Read-only copy of por_mxp_err<n>status	RO	64'h0

por_cfgm_errgsr6

Provides the HN-I <n> secure fault status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3088

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

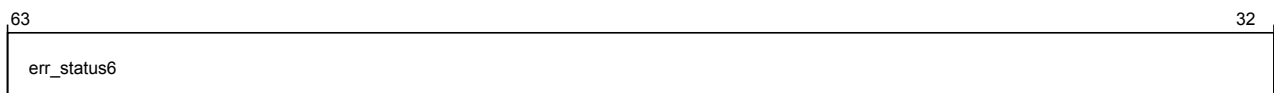


Figure 4-31 por_cfgm_por_cfgm_errgsr6 (high)

The following table shows the por_cfgm_errgsr6 higher register bit assignments.

Table 4-48 por_cfgm_por_cfgm_errgsr6 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status6	Read-only copy of por_hni_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

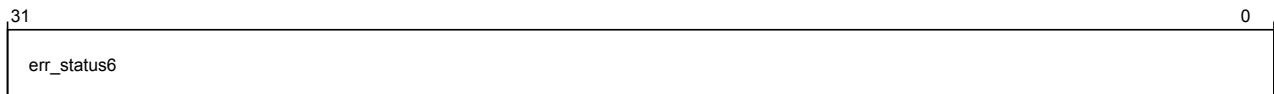


Figure 4-32 por_cfgm_por_cfgm_errgsr6 (low)

The following table shows the por_cfgm_errgsr6 lower register bit assignments.

Table 4-49 por_cfgm_por_cfgm_errgsr6 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status6	Read-only copy of por_hni_err<n>status	RO	64'h0

por_cfgm_errgsr7

Provides the HN-F <n> secure fault status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3090
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

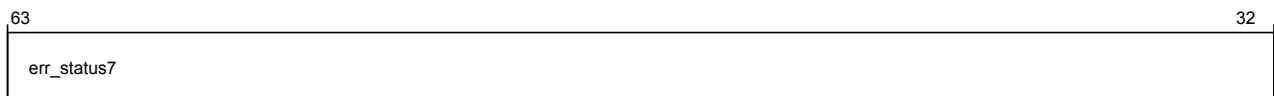


Figure 4-33 por_cfgm_por_cfgm_errgsr7 (high)

The following table shows the por_cfgm_errgsr7 higher register bit assignments.

Table 4-50 por_cfgm_por_cfgm_errgsr7 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status7	Read-only copy of por_hnf_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

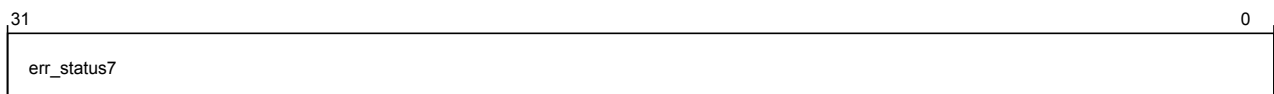


Figure 4-34 por_cfgm_por_cfgm_errgsr7 (low)

The following table shows the por_cfgm_errgsr7 lower register bit assignments.

Table 4-51 por_cfgm_por_cfgm_errgsr7 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status7	Read-only copy of por_hnf_err<n>status	RO	64'h0

por_cfgm_errgsr8

Provides the SBSX <n> secure fault status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3098

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

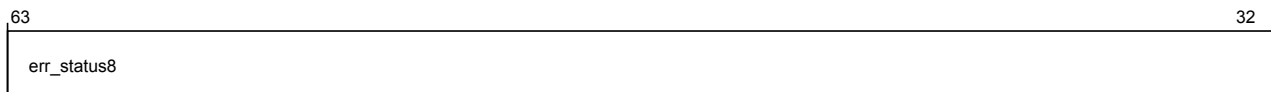


Figure 4-35 por_cfgm_por_cfgm_errgsr8 (high)

The following table shows the por_cfgm_errgsr8 higher register bit assignments.

Table 4-52 por_cfgm_por_cfgm_errgsr8 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status8	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

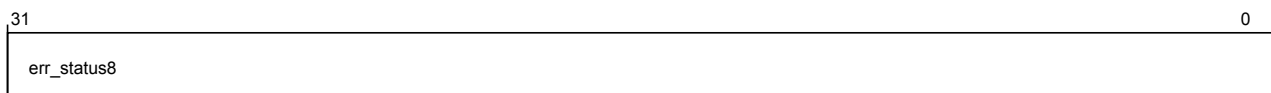


Figure 4-36 por_cfgm_por_cfgm_errgsr8 (low)

The following table shows the por_cfgm_errgsr8 lower register bit assignments.

Table 4-53 por_cfgm_por_cfgm_errgsr8 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status8	Read-only copy of por_sbsx_err<n>status	RO	64'h0

por_cfgm_errgsr9

Provides the CXG <n> secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h30A0
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

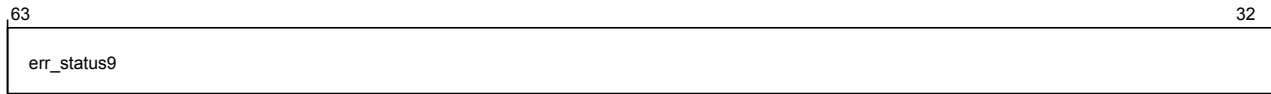


Figure 4-37 por_cfgm_por_cfgm_errgsr9 (high)

The following table shows the por_cfgm_errgsr9 higher register bit assignments.

Table 4-54 por_cfgm_por_cfgm_errgsr9 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status9	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-38 por_cfgm_por_cfgm_errgsr9 (low)

The following table shows the por_cfgm_errgsr9 lower register bit assignments.

Table 4-55 por_cfgm_por_cfgm_errgsr9 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status9	Read-only copy of por_cxg_err<n>status	RO	64'h0

por_cfgm_errgsr0_NS

Provides the XP <n> non-secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3100
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

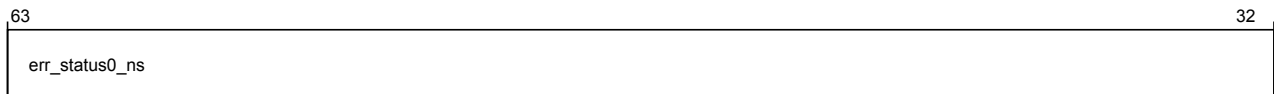


Figure 4-39 por_cfgm_por_cfgm_errgsr0_ns (high)

The following table shows the por_cfgm_errgsr0_NS higher register bit assignments.

Table 4-56 por_cfgm_por_cfgm_errgsr0_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status0_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

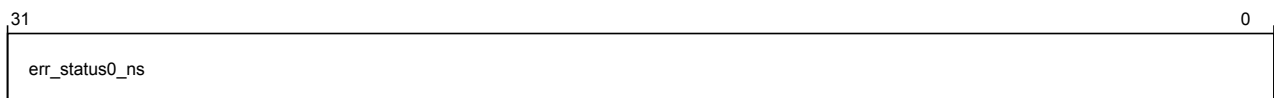


Figure 4-40 por_cfgm_por_cfgm_errgsr0_ns (low)

The following table shows the por_cfgm_errgsr0_NS lower register bit assignments.

Table 4-57 por_cfgm_por_cfgm_errgsr0_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status0_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

por_cfgm_errgsr1_NS

Provides the HN-I <n> non-secure error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3108
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

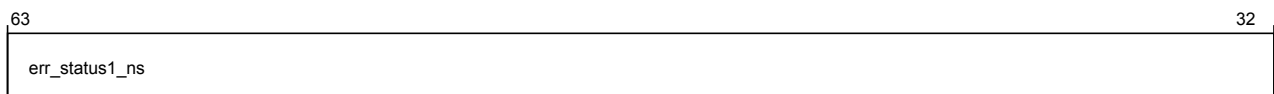


Figure 4-41 por_cfgm_por_cfgm_errgsr1_ns (high)

The following table shows the por_cfgm_errgsr1_NS higher register bit assignments.

Table 4-58 por_cfgm_por_cfgm_errgsr1_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status1_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-42 por_cfgm_por_cfgm_errgsr1_ns (low)

The following table shows the por_cfgm_errgsr1_NS lower register bit assignments.

Table 4-59 por_cfgm_por_cfgm_errgsr1_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status1_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

por_cfgm_errgsr2_NS

Provides the HN-F <n> non-secure error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3110
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

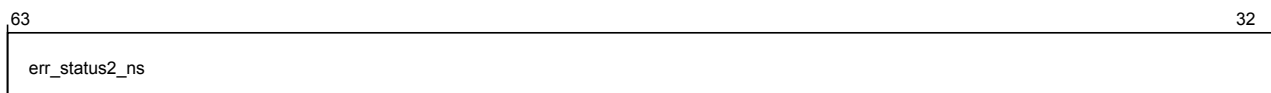


Figure 4-43 por_cfgm_por_cfgm_errgsr2_ns (high)

The following table shows the por_cfgm_errgsr2_NS higher register bit assignments.

Table 4-60 por_cfgm_por_cfgm_errgsr2_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status2_ns	Read-only copy of por_hnf_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

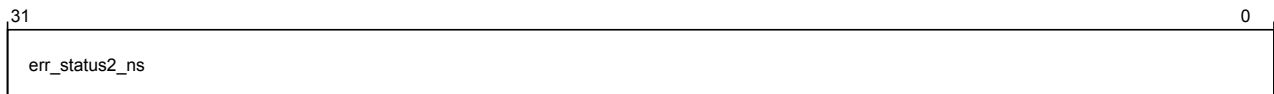


Figure 4-44 por_cfgm_por_cfgm_errgsr2_ns (low)

The following table shows the por_cfgm_errgsr2_NS lower register bit assignments.

Table 4-61 por_cfgm_por_cfgm_errgsr2_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status2_ns	Read-only copy of por_hnf_err<n>status	RO	64'h0

por_cfgm_errgsr3_NS

Provides the SBSX <n> non-secure error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3118
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

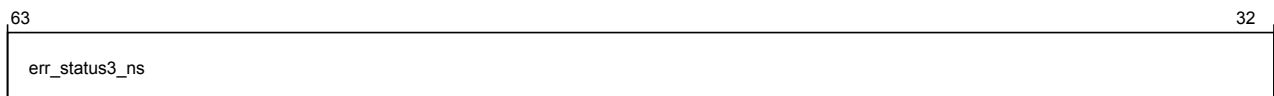


Figure 4-45 por_cfgm_por_cfgm_errgsr3_ns (high)

The following table shows the por_cfgm_errgsr3_NS higher register bit assignments.

Table 4-62 por_cfgm_por_cfgm_errgsr3_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status3_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

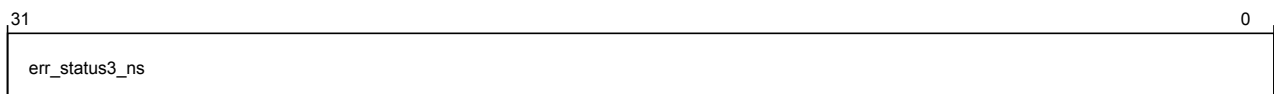


Figure 4-46 por_cfgm_por_cfgm_errgsr3_ns (low)

The following table shows the por_cfgm_errgsr3_NS lower register bit assignments.

Table 4-63 por_cfgm_por_cfgm_errgsr3_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status3_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

por_cfgm_errgsr4_NS

Provides the CXG <n> secure error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3120

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

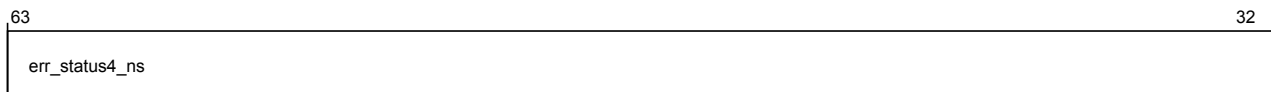


Figure 4-47 por_cfgm_por_cfgm_errgsr4_ns (high)

The following table shows the por_cfgm_errgsr4_NS higher register bit assignments.

Table 4-64 por_cfgm_por_cfgm_errgsr4_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status4_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

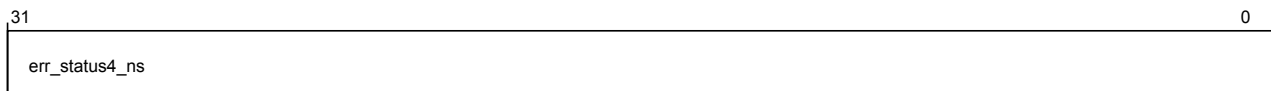


Figure 4-48 por_cfgm_por_cfgm_errgsr4_ns (low)

The following table shows the por_cfgm_errgsr4_NS lower register bit assignments.

Table 4-65 por_cfgm_por_cfgm_errgsr4_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status4_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

por_cfgm_errgsr5_NS

Provides the XP <n> non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3180
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

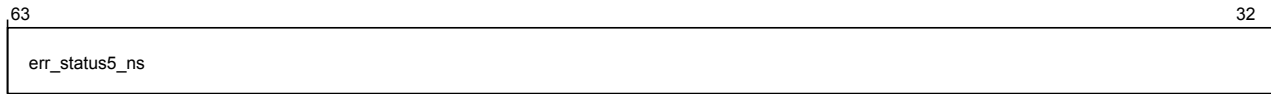


Figure 4-49 por_cfgm_por_cfgm_errgsr5_ns (high)

The following table shows the por_cfgm_errgsr5_NS higher register bit assignments.

Table 4-66 por_cfgm_por_cfgm_errgsr5_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status5_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

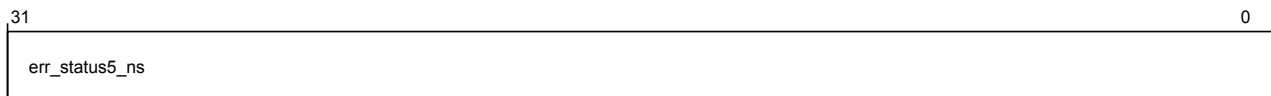


Figure 4-50 por_cfgm_por_cfgm_errgsr5_ns (low)

The following table shows the por_cfgm_errgsr5_NS lower register bit assignments.

Table 4-67 por_cfgm_por_cfgm_errgsr5_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status5_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

por_cfgm_errgsr6_NS

Provides the HN-I <n> non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3188
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

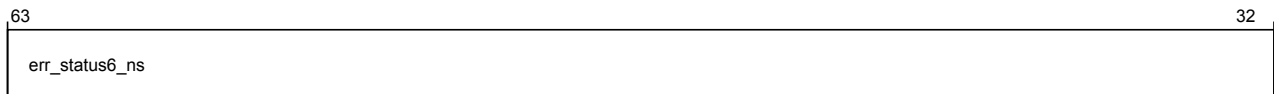


Figure 4-51 por_cfgm_por_cfgm_errgsr6_ns (high)

The following table shows the por_cfgm_errgsr6_NS higher register bit assignments.

Table 4-68 por_cfgm_por_cfgm_errgsr6_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status6_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

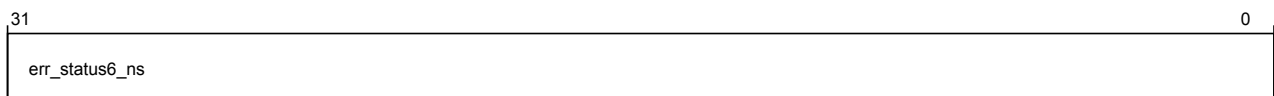


Figure 4-52 por_cfgm_por_cfgm_errgsr6_ns (low)

The following table shows the por_cfgm_errgsr6_NS lower register bit assignments.

Table 4-69 por_cfgm_por_cfgm_errgsr6_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status6_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

por_cfgm_errgsr7_NS

Provides the HN-F <n> non-secure fault status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3190
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

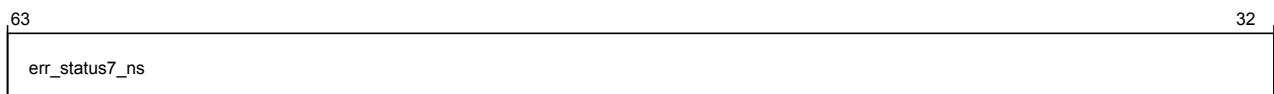


Figure 4-53 por_cfgm_por_cfgm_errgsr7_ns (high)

The following table shows the por_cfgm_errgsr7_NS higher register bit assignments.

Table 4-70 `por_cfgm_por_cfgm_errgsr7_ns` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status7_ns</code>	Read-only copy of <code>por_hnf_err<n>status</code>	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-54 `por_cfgm_por_cfgm_errgsr7_ns` (low)

The following table shows the `por_cfgm_errgsr7_NS` lower register bit assignments.

Table 4-71 `por_cfgm_por_cfgm_errgsr7_ns` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>err_status7_ns</code>	Read-only copy of <code>por_hnf_err<n>status</code>	RO	64'h0

`por_cfgm_errgsr8_NS`

Provides the SBSX <n> non-secure fault status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3198
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

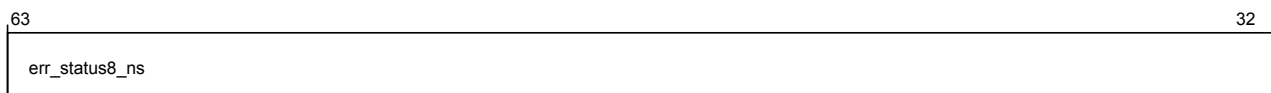


Figure 4-55 `por_cfgm_por_cfgm_errgsr8_ns` (high)

The following table shows the `por_cfgm_errgsr8_NS` higher register bit assignments.

Table 4-72 `por_cfgm_por_cfgm_errgsr8_ns` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status8_ns</code>	Read-only copy of <code>por_sbsx_err<n>status</code>	RO	64'h0

The following image shows the lower register bit assignments.

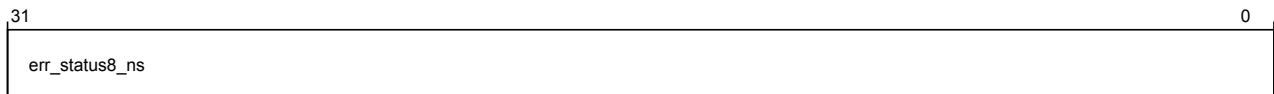


Figure 4-56 por_cfgm_por_cfgm_errgsr8_ns (low)

The following table shows the por_cfgm_errgsr8_NS lower register bit assignments.

Table 4-73 por_cfgm_por_cfgm_errgsr8_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status8_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

por_cfgm_errgsr9_NS

Provides the CXG <n> secure error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h31A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

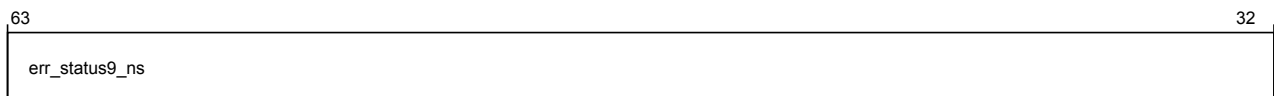


Figure 4-57 por_cfgm_por_cfgm_errgsr9_ns (high)

The following table shows the por_cfgm_errgsr9_NS higher register bit assignments.

Table 4-74 por_cfgm_por_cfgm_errgsr9_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status9_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

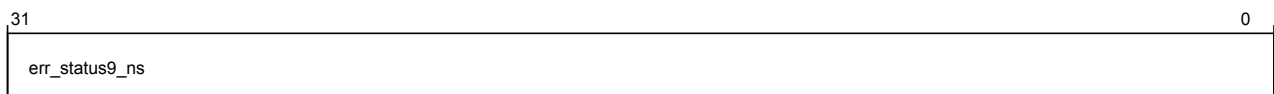


Figure 4-58 por_cfgm_por_cfgm_errgsr9_ns (low)

The following table shows the por_cfgm_errgsr9_NS lower register bit assignments.

Table 4-75 por_cfgm_por_cfgm_errgrs9_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status9_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

por_cfgm_errdevaff

Functions as the device affinity register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3FA8
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

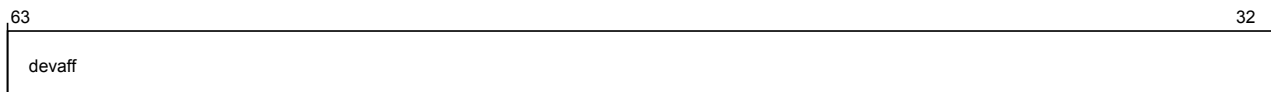


Figure 4-59 por_cfgm_por_cfgm_errdevaff (high)

The following table shows the por_cfgm_errdevaff higher register bit assignments.

Table 4-76 por_cfgm_por_cfgm_errdevaff (high)

Bits	Field name	Description	Type	Reset
63:32	devaff	Device affinity register	RO	64'b0

The following image shows the lower register bit assignments.

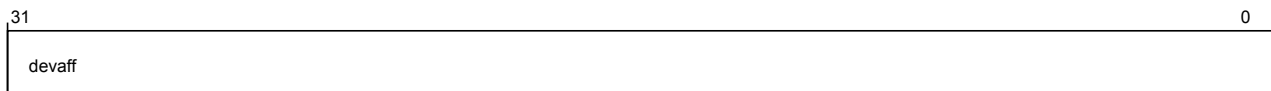


Figure 4-60 por_cfgm_por_cfgm_errdevaff (low)

The following table shows the por_cfgm_errdevaff lower register bit assignments.

Table 4-77 por_cfgm_por_cfgm_errdevaff (low)

Bits	Field name	Description	Type	Reset
31:0	devaff	Device affinity register	RO	64'b0

por_cfgm_errdevarch

Functions as the device architecture register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3FB8
Register reset 64'b0001011101110000000000101000
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

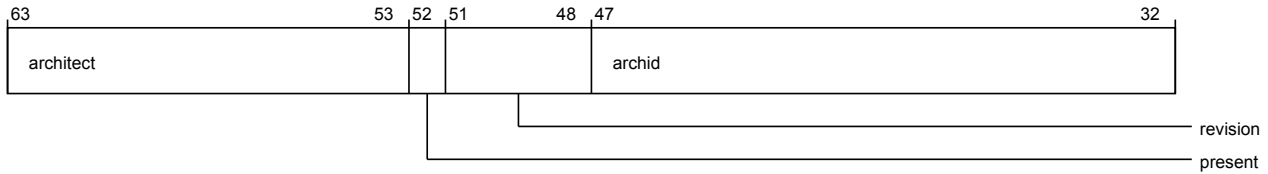


Figure 4-61 por_cfgm_por_cfgm_errdevarch (high)

The following table shows the por_cfgm_errdevarch higher register bit assignments.

Table 4-78 por_cfgm_por_cfgm_errdevarch (high)

Bits	Field name	Description	Type	Reset
63:53	architect	Architect	RO	11'h23B
52	present	Present	RO	1'b1
51:48	revision	Architecture revision	RO	4'b0
47:32	archid	Architecture ID	RO	16'h0A00

The following image shows the lower register bit assignments.

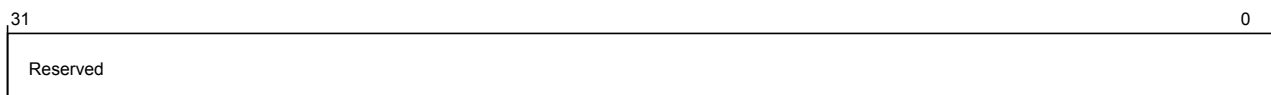


Figure 4-62 por_cfgm_por_cfgm_errdevarch (low)

The following table shows the por_cfgm_errdevarch lower register bit assignments.

Table 4-79 por_cfgm_por_cfgm_errdevarch (low)

Bits	Field name	Description	Type	Reset
31:0	Reserved	Reserved	RO	-

por_cfgm_erridr

Contains the number of error records.

Its characteristics are:

Type RO

Register width (Bits) 64
Address offset 14'h3FC8
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

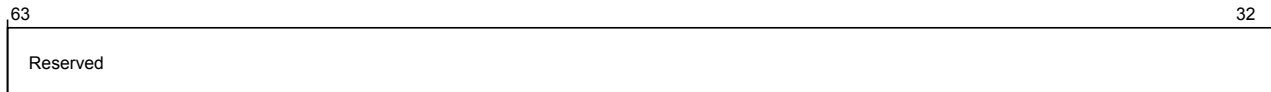


Figure 4-63 por_cfgm_erridr (high)

The following table shows the por_cfgm_erridr higher register bit assignments.

Table 4-80 por_cfgm_erridr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

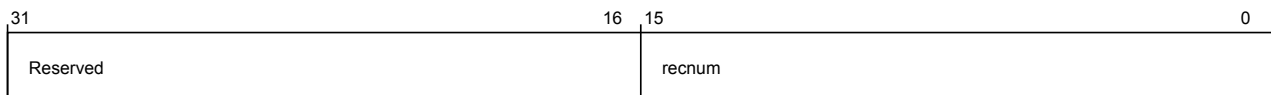


Figure 4-64 por_cfgm_erridr (low)

The following table shows the por_cfgm_erridr lower register bit assignments.

Table 4-81 por_cfgm_erridr (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	recnum	Number of error records; equal to 2*(number of logical devices)	RO	Configuration dependent

por_cfgm_errpidr45

Functions as the identification register for peripheral ID 4 and peripheral ID 5.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3FD0
Register reset 64'b000000100
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

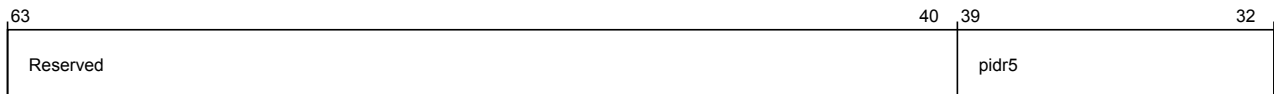


Figure 4-65 por_cfgm_errpidr45 (high)

The following table shows the por_cfgm_errpidr45 higher register bit assignments.

Table 4-82 por_cfgm_errpidr45 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr5	Peripheral ID 5	RO	8'b0

The following image shows the lower register bit assignments.

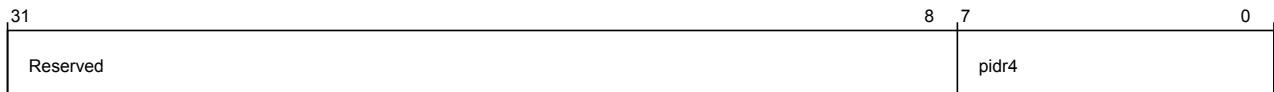


Figure 4-66 por_cfgm_errpidr45 (low)

The following table shows the por_cfgm_errpidr45 lower register bit assignments.

Table 4-83 por_cfgm_errpidr45 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr4	Peripheral ID 4	RO	8'h4

por_cfgm_errpidr67

Functions as the identification register for peripheral ID 6 and peripheral ID 7.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3FD8
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

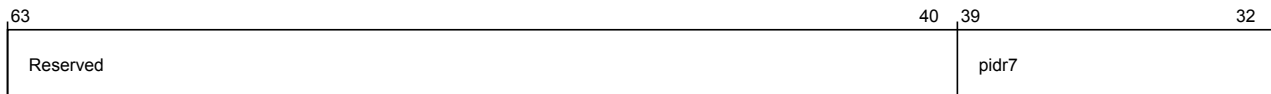


Figure 4-67 por_cfgm_errpidr67 (high)

The following table shows the por_cfgm_errpidr67 higher register bit assignments.

Table 4-84 por_cfgm_errpidr67 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr7	Peripheral ID 7	RO	8'b0

The following image shows the lower register bit assignments.

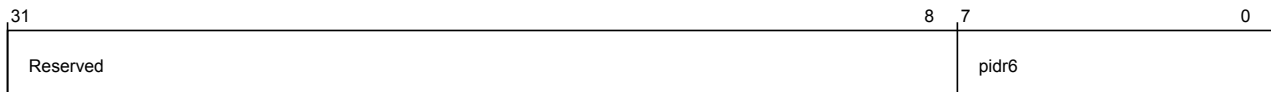


Figure 4-68 por_cfgm_errpidr67 (low)

The following table shows the por_cfgm_errpidr67 lower register bit assignments.

Table 4-85 por_cfgm_errpidr67 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr6	Peripheral ID 6	RO	8'b0

por_cfgm_errpidr01

Functions as the identification register for peripheral ID 0 and peripheral ID 1.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3FE0
Register reset	64'b0101110000011100
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

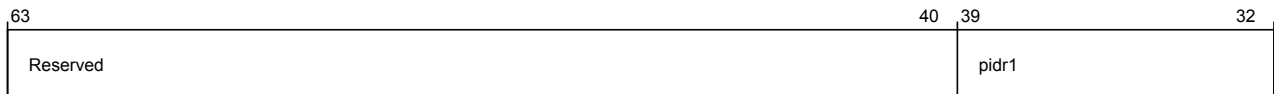


Figure 4-69 por_cfgm_errpidr01 (high)

The following table shows the por_cfgm_errpidr01 higher register bit assignments.

Table 4-86 por_cfgm_errpidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr1	Peripheral ID 1	RO	8'hb4

The following image shows the lower register bit assignments.

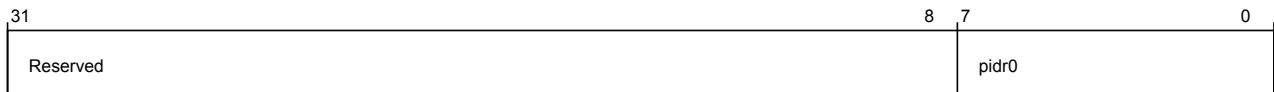


Figure 4-70 por_cfgm_errpidr01 (low)

The following table shows the por_cfgm_errpidr01 lower register bit assignments.

Table 4-87 por_cfgm_errpidr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr0	Peripheral ID 0	RO	8'h34

por_cfgm_errpidr23

Functions as the identification register for peripheral ID 2 and peripheral ID 3.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3FE8
Register reset	64'b000000111
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

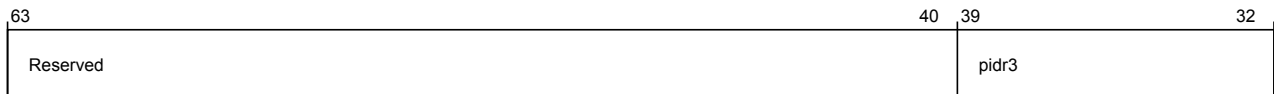


Figure 4-71 por_cfgm_errpidr23 (high)

The following table shows the por_cfgm_errpidr23 higher register bit assignments.

Table 4-88 por_cfgm_errpidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr3	Peripheral ID 3	RO	8'b0

The following image shows the lower register bit assignments.

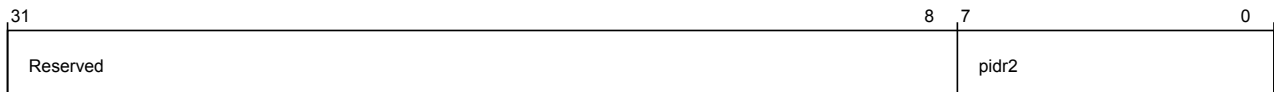


Figure 4-72 por_cfgm_errpidr23 (low)

The following table shows the por_cfgm_errpidr23 lower register bit assignments.

Table 4-89 por_cfgm_errpidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr2	Peripheral ID 2	RO	8'h7

por_cfgm_errcidr01

Functions as the identification register for component ID 0 and component ID 1.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3FF0
Register reset	64'b1111111100001101
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

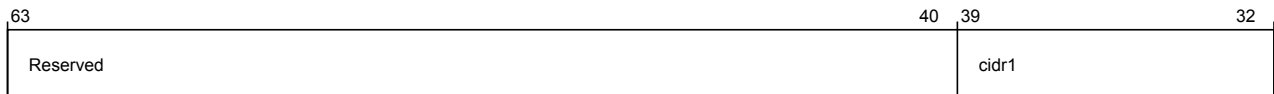


Figure 4-73 por_cfgm_errcldr01 (high)

The following table shows the por_cfgm_errcldr01 higher register bit assignments.

Table 4-90 por_cfgm_errcldr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	cidr1	Component ID 1	RO	8'hff

The following image shows the lower register bit assignments.

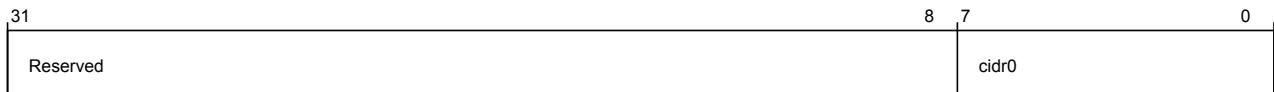


Figure 4-74 por_cfgm_errcldr01 (low)

The following table shows the por_cfgm_errcldr01 lower register bit assignments.

Table 4-91 por_cfgm_errcldr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr0	Component ID 0	RO	8'hd

por_cfgm_errcldr23

Functions as the identification register for component ID 2 and component ID 3.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3FF8
Register reset	64'b0001011100000101
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

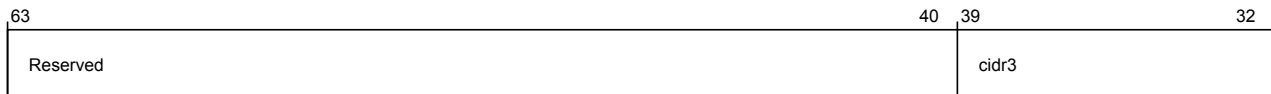


Figure 4-75 por_cfgm_errcidr23 (high)

The following table shows the por_cfgm_errcidr23 higher register bit assignments.

Table 4-92 por_cfgm_errcidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	cidr3	Component ID 3	RO	8'hb1

The following image shows the lower register bit assignments.

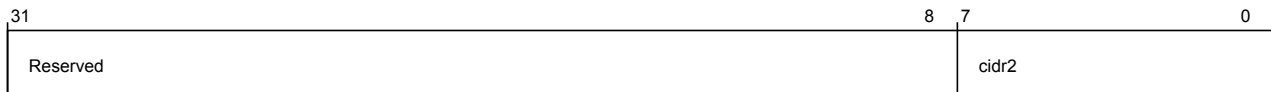


Figure 4-76 por_cfgm_errcidr23 (low)

The following table shows the por_cfgm_errcidr23 lower register bit assignments.

Table 4-93 por_cfgm_errcidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr2	Component ID 2	RO	8'h5

por_info_global

Contains user-specified values of build-time global configuration parameters.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h900
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

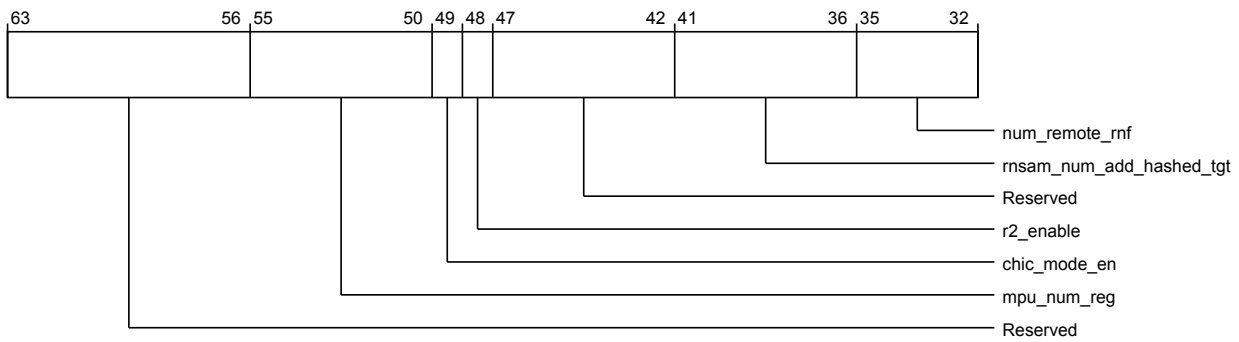


Figure 4-77 por_cfgm_por_info_global (high)

The following table shows the por_info_global higher register bit assignments.

Table 4-94 por_cfgm_por_info_global (high)

Bits	Field name	Description	Type	Reset
63:56	Reserved	Reserved	RO	-
55:50	mpu_num_reg	Number of MPU programmable regions	RO	Configuration dependent
49	chic_mode_en	CHI-C mode enable	RO	Configuration dependent
48	r2_enable	CMN R2 feature enable	RO	Configuration dependent
47:42	Reserved	Reserved	RO	-
41:36	rnsam_num_add_hashed_tgt	Number of additional hashed target ID's supported by the RN SAM, beyond the local HNF count	RO	Configuration dependent
35:32	num_remote_rnf	Number of remote RN-F devices in the system when the CML feature is enabled	RO	Configuration dependent

The following image shows the lower register bit assignments.

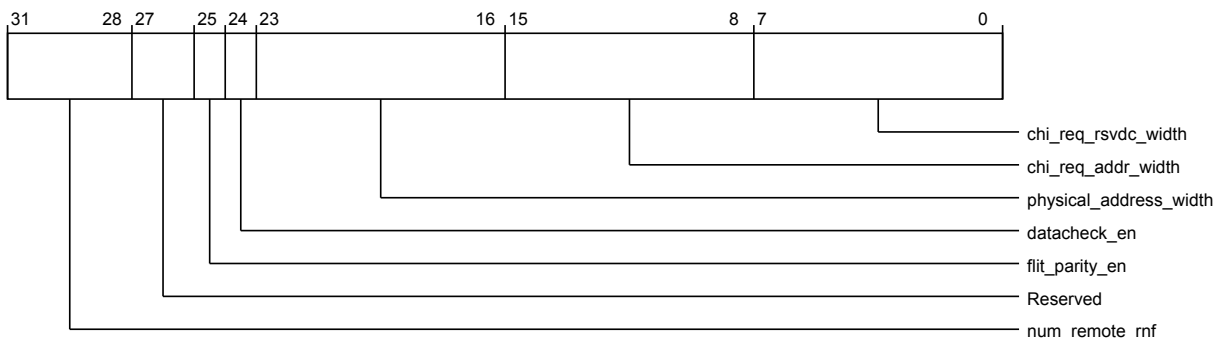


Figure 4-78 por_cfgm_por_info_global (low)

The following table shows the por_info_global lower register bit assignments.

Table 4-95 por_cfgm_por_info_global (low)

Bits	Field name	Description	Type	Reset
31:28	num_remote_rnf	Number of remote RN-F devices in the system when the CML feature is enabled	RO	Configuration dependent
27:26	Reserved	Reserved	RO	-
25	flit_parity_en	Indicates whether parity checking is enabled in the transport layer on all flits sent on the interconnect	RO	Configuration dependent
24	datacheck_en	Indicates whether datacheck feature is enabled for CHI DAT flit	RO	Configuration dependent
23:16	physical_address_width	Physical address width	RO	Configuration dependent
15:8	chi_req_addr_width	REQ address width	RO	Configuration dependent
7:0	chi_req_rsvdc_width	RSVDC field width in CHI REQ flit (internal)	RO	Configuration dependent

por_ppu_int_enable

Configures the HN-F PPU event interrupt. Contains the interrupt mask.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1000

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

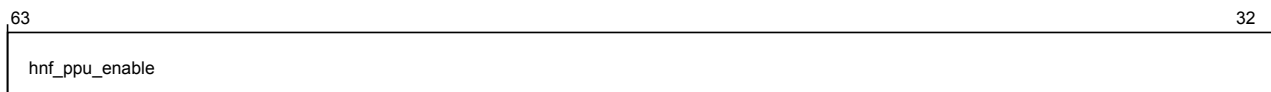


Figure 4-79 por_cfgm_por_ppu_int_enable (high)

The following table shows the por_ppu_int_enable higher register bit assignments.

Table 4-96 por_cfgm_por_ppu_int_enable (high)

Bits	Field name	Description	Type	Reset
63:32	hnf_ppu_enable	Interrupt mask	RW	64'b0

The following image shows the lower register bit assignments.

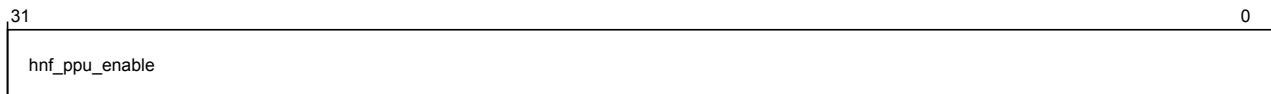


Figure 4-80 por_cfgm_por_ppu_int_enable (low)

The following table shows the por_ppu_int_enable lower register bit assignments.

Table 4-97 por_cfgm_por_ppu_int_enable (low)

Bits	Field name	Description	Type	Reset
31:0	hnf_ppu_enable	Interrupt mask	RW	64'b0

por_ppu_int_status

Provides HN-F PPU event interrupt status.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h1008
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

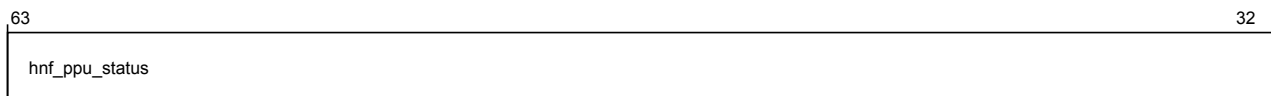


Figure 4-81 por_cfgm_por_ppu_int_status (high)

The following table shows the por_ppu_int_status higher register bit assignments.

Table 4-98 por_cfgm_por_ppu_int_status (high)

Bits	Field name	Description	Type	Reset
63:32	hnf_ppu_status	Interrupt status	W1C	64'b0

The following image shows the lower register bit assignments.

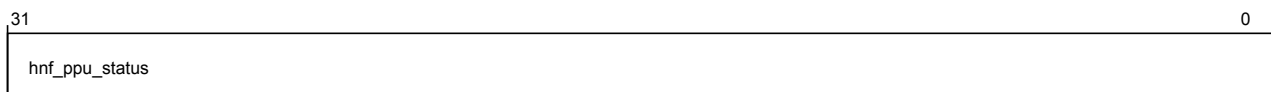


Figure 4-82 por_cfgm_por_ppu_int_status (low)

The following table shows the por_ppu_int_status lower register bit assignments.

Table 4-99 por_cfgm_por_ppu_int_status (low)

Bits	Field name	Description	Type	Reset
31:0	hnf_ppu_status	Interrupt status	W1C	64'b0

por_ppu_qactive_hyst

Number of hysteresis clock cycles to retain QACTIVE assertion

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1010

Register reset 64'b00000000000000010

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

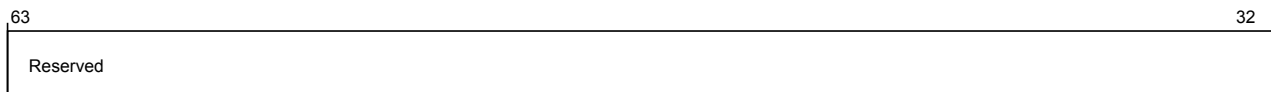


Figure 4-83 por_cfgm_por_ppu_qactive_hyst (high)

The following table shows the por_ppu_qactive_hyst higher register bit assignments.

Table 4-100 por_cfgm_por_ppu_qactive_hyst (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

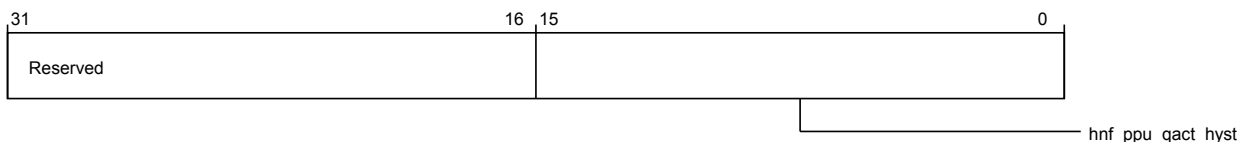


Figure 4-84 por_cfgm_por_ppu_qactive_hyst (low)

The following table shows the por_ppu_qactive_hyst lower register bit assignments.

Table 4-101 por_cfgm_por_ppu_qactive_hyst (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	hnf_ppu_qact_hyst	QACTIVE hysteresis	RW	16'h10

por_cfgm_child_pointer_\$index

Contains base address of child configuration node. NOTE: There will be as many child pointer registers in the Global Config Unit as the number of XPs on the chip. Each successive child pointer register will be at the next 8 byte address boundary. Each successive child pointer register will be named with the suffix corresponding to the register number, for example, por_cfgm_child_pointer_<0:255>.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	CHILD_POINTER_BASE + 8 × \$index
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

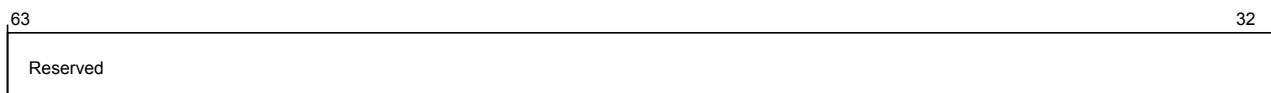


Figure 4-85 por_cfgm_por_cfgm_child_pointer_\$index (high)

The following table shows the por_cfgm_child_pointer_\$index higher register bit assignments.

Table 4-102 por_cfgm_por_cfgm_child_pointer_\$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

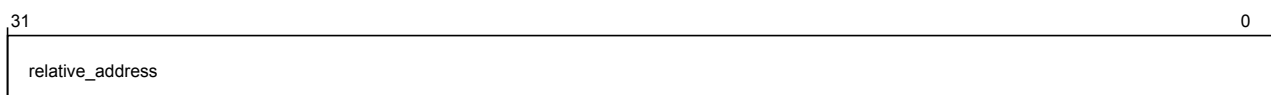


Figure 4-86 por_cfgm_por_cfgm_child_pointer_\$index (low)

The following table shows the por_cfgm_child_pointer_\$index lower register bit assignments.

Table 4-103 por_cfgm_por_cfgm_child_pointer_\$index (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address	Bit 31: External or internal child node 1'b1: Indicates child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPBASE	RO	32'b0

4.3.2 DN register descriptions

This section lists the DN registers.

por_dn_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

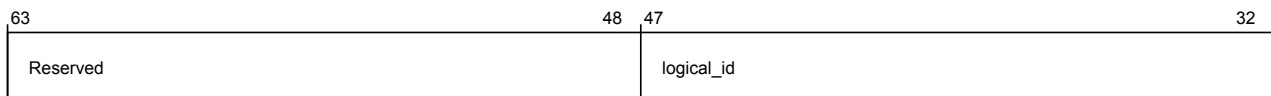


Figure 4-87 por_dn_node_info (high)

The following table shows the por_dn_node_info higher register bit assignments.

Table 4-104 por_dn_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

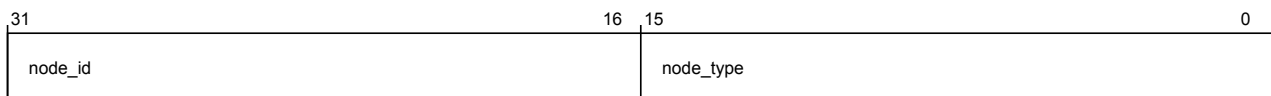


Figure 4-88 por_dn_node_info (low)

The following table shows the por_dn_node_info lower register bit assignments.

Table 4-105 por_dn_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0001

por_dn_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-89 por_dn_por_dn_child_info (high)

The following table shows the por_dn_child_info higher register bit assignments.

Table 4-106 por_dn_por_dn_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

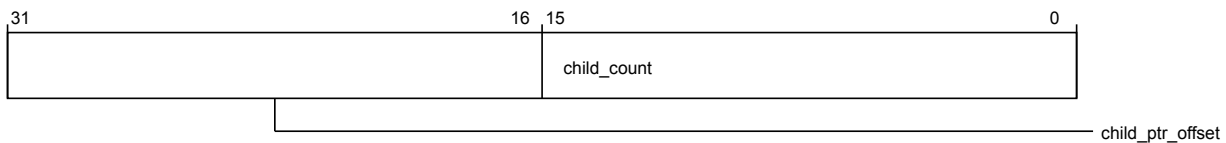


Figure 4-90 por_dn_por_dn_child_info (low)

The following table shows the por_dn_child_info lower register bit assignments.

Table 4-107 por_dn_por_dn_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

por_dn_build_info

Contains the configuration parameter values. Indicates the specific DN configuration.

Its characteristics are:

Type	RO
Register width (Bits)	64

Address offset 14'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

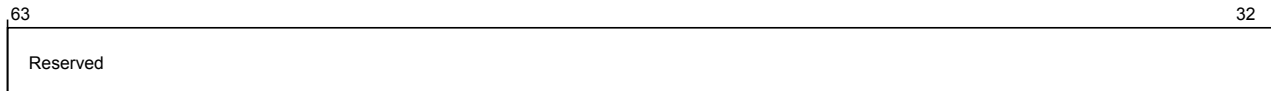


Figure 4-91 por_dn_por_dn_build_info (high)

The following table shows the por_dn_build_info higher register bit assignments.

Table 4-108 por_dn_por_dn_build_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

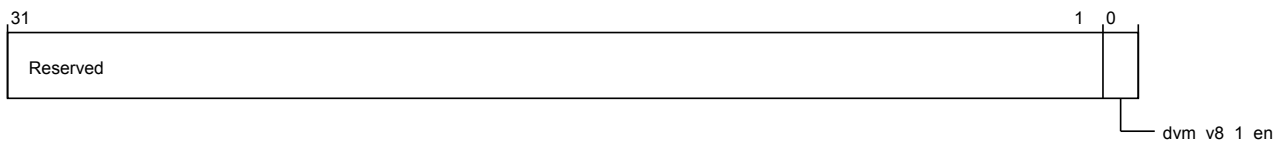


Figure 4-92 por_dn_por_dn_build_info (low)

The following table shows the por_dn_build_info lower register bit assignments.

Table 4-109 por_dn_por_dn_build_info (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	dvm_v8_1_en	Determines whether all nodes receiving DVM snoops support DVM v8.1 operations; must be set to 0 if not supported by all nodes, therefore allowing the node to perform demotion before sending out the DVM snoop	RO	Configuration dependent

por_dn_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h980
Register reset 64'b0
Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.



Figure 4-93 `por_dn_secure_register_groups_override` (high)

The following table shows the `por_dn_secure_register_groups_override` higher register bit assignments.

Table 4-110 `por_dn_secure_register_groups_override` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

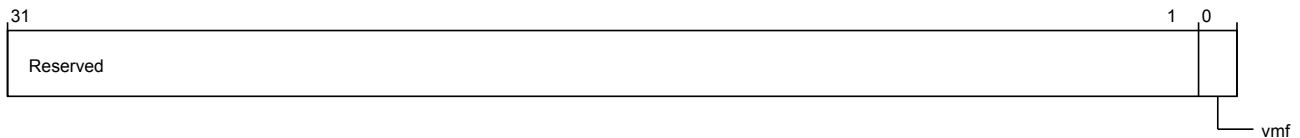


Figure 4-94 `por_dn_secure_register_groups_override` (low)

The following table shows the `por_dn_secure_register_groups_override` lower register bit assignments.

Table 4-111 `por_dn_secure_register_groups_override` (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	vmf	Allows non-secure access to secure VMF registers	RW	1'b0

`por_dn_aux_ctl`

Functions as the auxiliary control register for DN.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA00

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

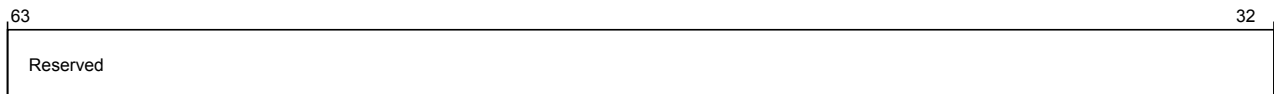


Figure 4-95 por_dn_por_dn_aux_ctl (high)

The following table shows the por_dn_aux_ctl higher register bit assignments.

Table 4-112 por_dn_por_dn_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

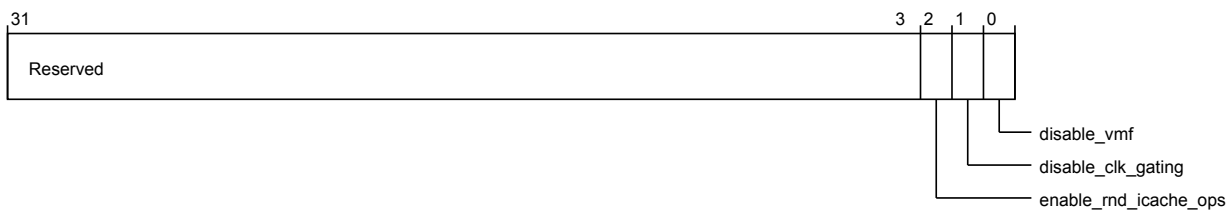


Figure 4-96 por_dn_por_dn_aux_ctl (low)

The following table shows the por_dn_aux_ctl lower register bit assignments.

Table 4-113 por_dn_por_dn_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	enable_rnd_icache_ops	Filters out BPI and VICI/PICI Snps to RNDs when set	RW	Configuration dependent
1	disable_clk_gating	Disables autonomous clock gating when set	RW	1'b0
0	disable_vmf	This bit is currently not supported. Software must not program this bit.	RW	Configuration dependent

por_dn_vmf0_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC00
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

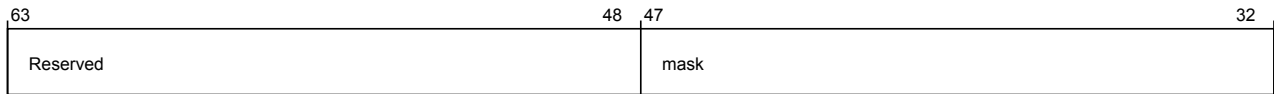


Figure 4-97 por_dn_por_dn_vmf0_ctrl (high)

The following table shows the por_dn_vmf0_ctrl higher register bit assignments.

Table 4-114 por_dn_por_dn_vmf0_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf0_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

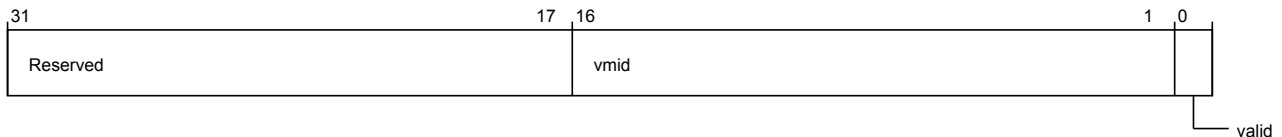


Figure 4-98 por_dn_por_dn_vmf0_ctrl (low)

The following table shows the por_dn_vmf0_ctrl lower register bit assignments.

Table 4-115 por_dn_por_dn_vmf0_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf0_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC08
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

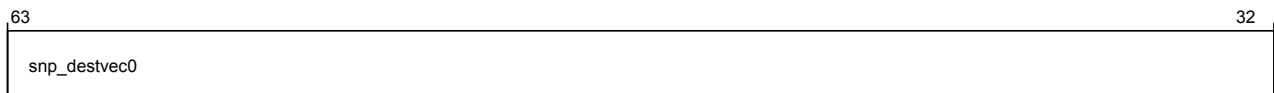


Figure 4-99 por_dn_vmf0_rnf0 (high)

The following table shows the por_dn_vmf0_rnf0 higher register bit assignments.

Table 4-116 por_dn_vmf0_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

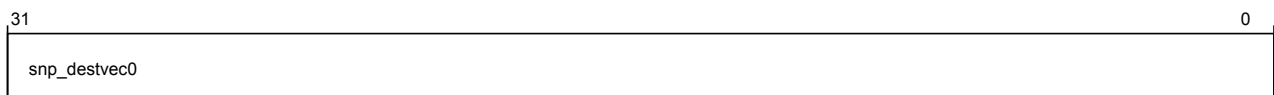


Figure 4-100 por_dn_vmf0_rnf0 (low)

The following table shows the por_dn_vmf0_rnf0 lower register bit assignments.

Table 4-117 por_dn_vmf0_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

por_dn_vmf0_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
-------------	----

Register width (Bits) 64
Address offset 14'hC10
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.



Figure 4-101 por_dn_por_dn_vmf0_rnd (high)

The following table shows the por_dn_vmf0_rnd higher register bit assignments.

Table 4-118 por_dn_por_dn_vmf0_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

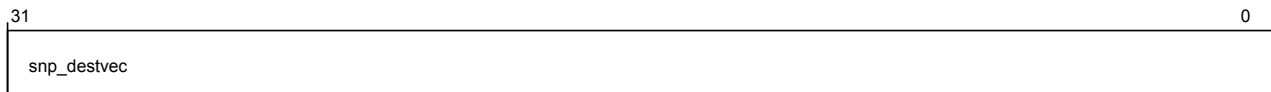


Figure 4-102 por_dn_por_dn_vmf0_rnd (low)

The following table shows the por_dn_vmf0_rnd lower register bit assignments.

Table 4-119 por_dn_por_dn_vmf0_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

por_dn_vmf0_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC18
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

Secure group `por_dn_secure_register_groups_override.vmf`
override

The following image shows the higher register bit assignments.



Figure 4-103 `por_dn_por_dn_vmf0_cxra` (high)

The following table shows the `por_dn_vmf0_cxra` higher register bit assignments.

Table 4-120 `por_dn_por_dn_vmf0_cxra` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>snp_destvec</code>	CXRA bit vector 63:0 corresponding to <code>por_dn_vmf0_ctrl.vmid</code>	RW	64'b0

The following image shows the lower register bit assignments.

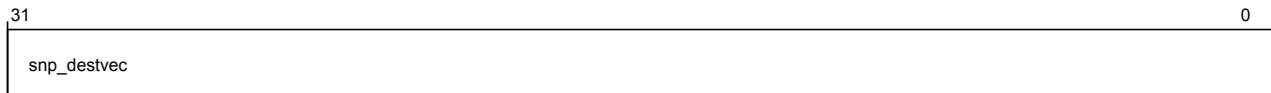


Figure 4-104 `por_dn_por_dn_vmf0_cxra` (low)

The following table shows the `por_dn_vmf0_cxra` lower register bit assignments.

Table 4-121 `por_dn_por_dn_vmf0_cxra` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>snp_destvec</code>	CXRA bit vector 63:0 corresponding to <code>por_dn_vmf0_ctrl.vmid</code>	RW	64'b0

`por_dn_vmf1_ctrl`

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when `por_dn_aux_ctl.disable_vmf` is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC20
Register reset 64'b11111111111111110000000000000000
Usage constraints Only accessible by secure accesses.
Secure group `por_dn_secure_register_groups_override.vmf`
override

The following image shows the higher register bit assignments.

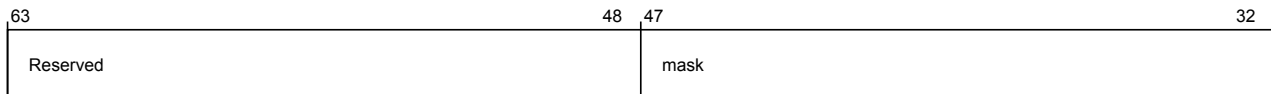


Figure 4-105 por_dn_por_dn_vmf1_ctrl (high)

The following table shows the por_dn_vmf1_ctrl higher register bit assignments.

Table 4-122 por_dn_por_dn_vmf1_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf1_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

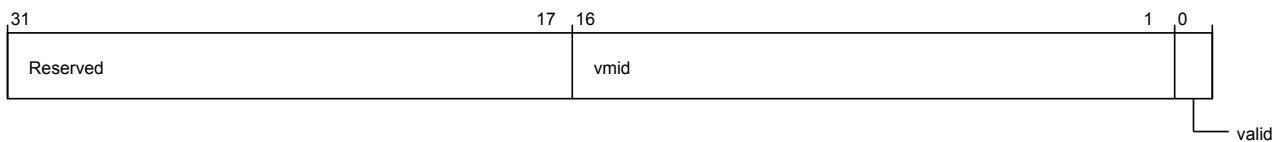


Figure 4-106 por_dn_por_dn_vmf1_ctrl (low)

The following table shows the por_dn_vmf1_ctrl lower register bit assignments.

Table 4-123 por_dn_por_dn_vmf1_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf1_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC28
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

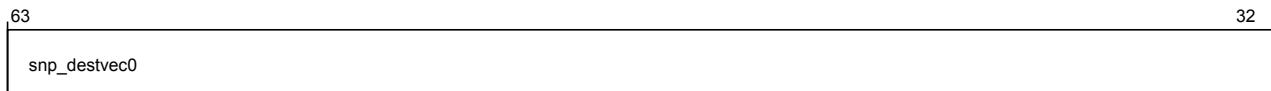


Figure 4-107 por_dn_por_dn_vmf1_rnf0 (high)

The following table shows the por_dn_vmf1_rnf0 higher register bit assignments.

Table 4-124 por_dn_por_dn_vmf1_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

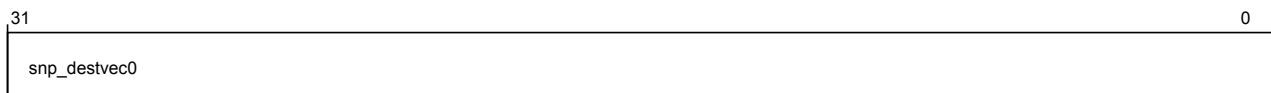


Figure 4-108 por_dn_por_dn_vmf1_rnf0 (low)

The following table shows the por_dn_vmf1_rnf0 lower register bit assignments.

Table 4-125 por_dn_por_dn_vmf1_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

por_dn_vmf1_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC30
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

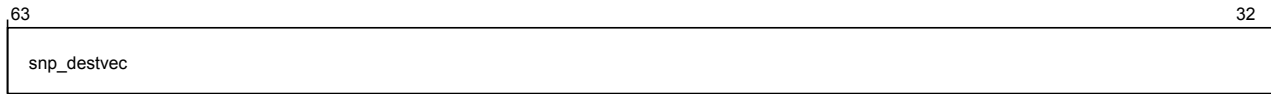


Figure 4-109 por_dn_por_dn_vmf1_rnd (high)

The following table shows the por_dn_vmf1_rnd higher register bit assignments.

Table 4-126 por_dn_por_dn_vmf1_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

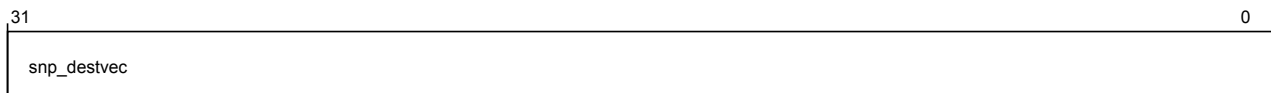


Figure 4-110 por_dn_por_dn_vmf1_rnd (low)

The following table shows the por_dn_vmf1_rnd lower register bit assignments.

Table 4-127 por_dn_por_dn_vmf1_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

por_dn_vmf1_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

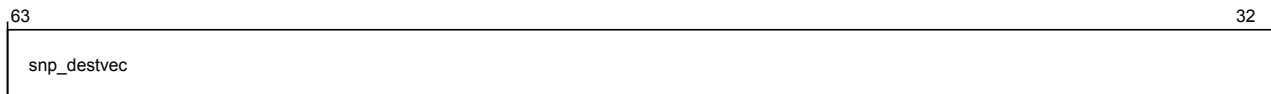


Figure 4-111 por_dn_por_dn_vmf1_cxra (high)

The following table shows the por_dn_vmf1_cxra higher register bit assignments.

Table 4-128 por_dn_por_dn_vmf1_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

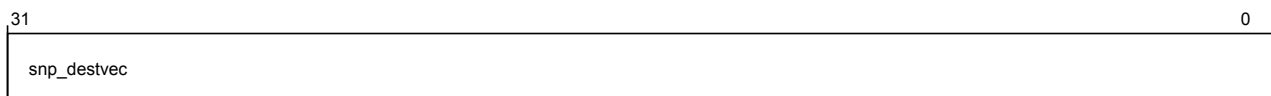


Figure 4-112 por_dn_por_dn_vmf1_cxra (low)

The following table shows the por_dn_vmf1_cxra lower register bit assignments.

Table 4-129 por_dn_por_dn_vmf1_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

por_dn_vmf2_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC40
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

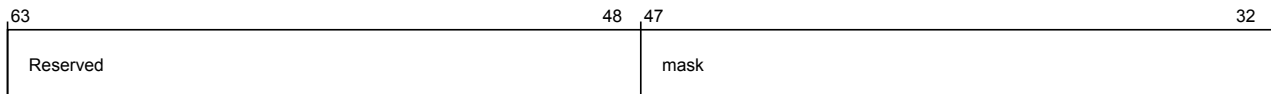


Figure 4-113 por_dn_por_dn_vmf2_ctrl (high)

The following table shows the por_dn_vmf2_ctrl higher register bit assignments.

Table 4-130 por_dn_por_dn_vmf2_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf2_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

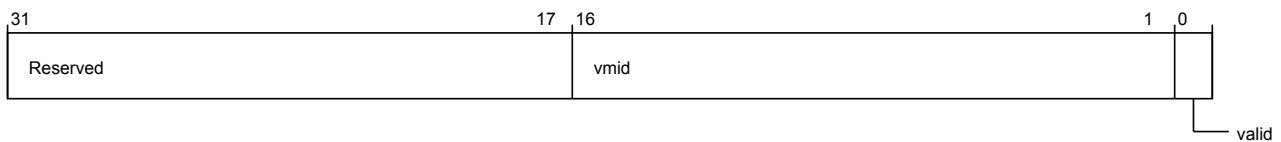


Figure 4-114 por_dn_por_dn_vmf2_ctrl (low)

The following table shows the por_dn_vmf2_ctrl lower register bit assignments.

Table 4-131 por_dn_por_dn_vmf2_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf2_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC48
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

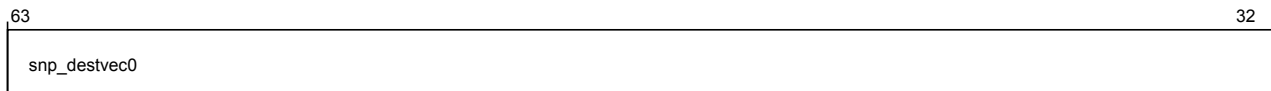


Figure 4-115 por_dn_vmf2_rnf0 (high)

The following table shows the por_dn_vmf2_rnf0 higher register bit assignments.

Table 4-132 por_dn_vmf2_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

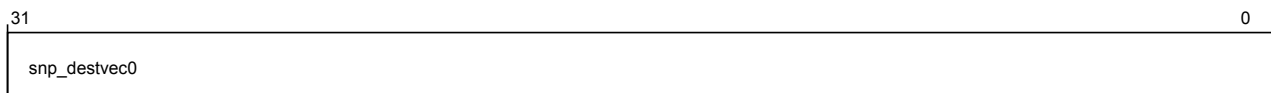


Figure 4-116 por_dn_vmf2_rnf0 (low)

The following table shows the por_dn_vmf2_rnf0 lower register bit assignments.

Table 4-133 por_dn_vmf2_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

por_dn_vmf2_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC50
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

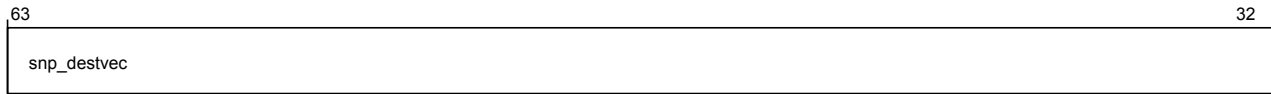


Figure 4-117 por_dn_por_dn_vmf2_rnd (high)

The following table shows the por_dn_vmf2_rnd higher register bit assignments.

Table 4-134 por_dn_por_dn_vmf2_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

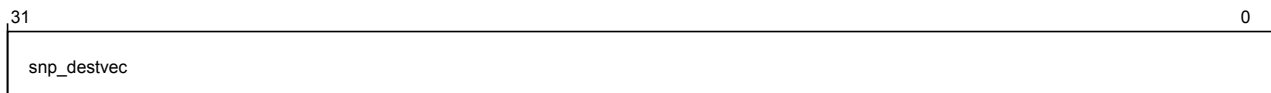


Figure 4-118 por_dn_por_dn_vmf2_rnd (low)

The following table shows the por_dn_vmf2_rnd lower register bit assignments.

Table 4-135 por_dn_por_dn_vmf2_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

por_dn_vmf2_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC58

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

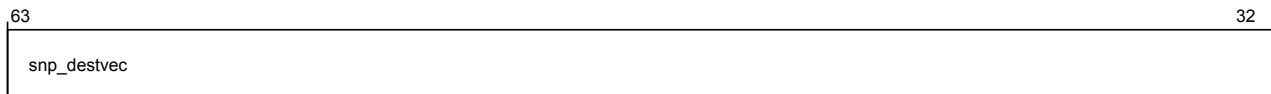


Figure 4-119 por_dn_por_dn_vmf2_cxra (high)

The following table shows the por_dn_vmf2_cxra higher register bit assignments.

Table 4-136 por_dn_por_dn_vmf2_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

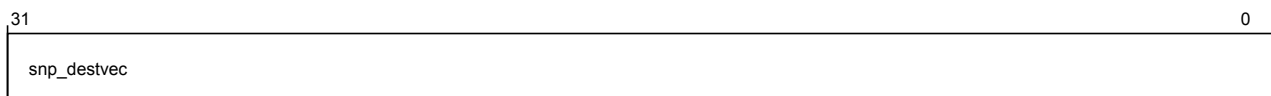


Figure 4-120 por_dn_por_dn_vmf2_cxra (low)

The following table shows the por_dn_vmf2_cxra lower register bit assignments.

Table 4-137 por_dn_por_dn_vmf2_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

por_dn_vmf3_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC60
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

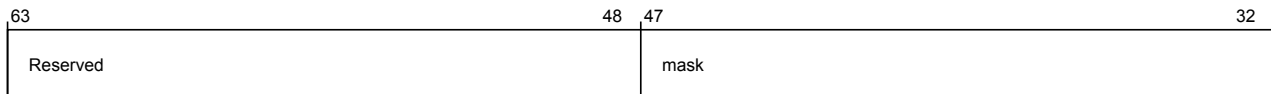


Figure 4-121 por_dn_por_dn_vmf3_ctrl (high)

The following table shows the por_dn_vmf3_ctrl higher register bit assignments.

Table 4-138 por_dn_por_dn_vmf3_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf3_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

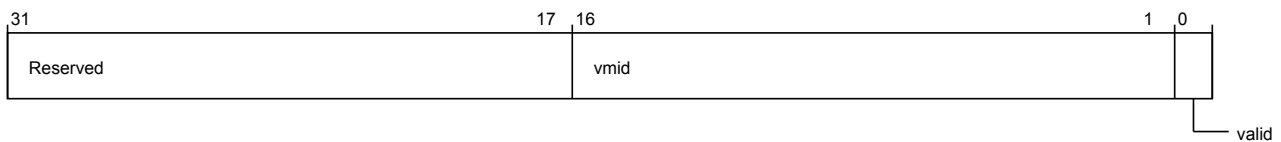


Figure 4-122 por_dn_por_dn_vmf3_ctrl (low)

The following table shows the por_dn_vmf3_ctrl lower register bit assignments.

Table 4-139 por_dn_por_dn_vmf3_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf3_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC68
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

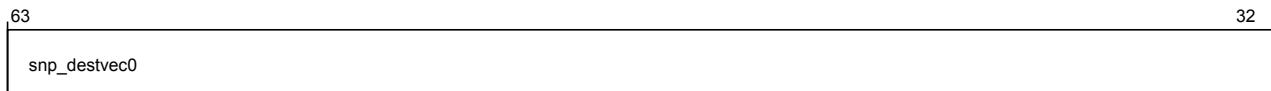


Figure 4-123 por_dn_por_dn_vmf3_rnf0 (high)

The following table shows the por_dn_vmf3_rnf0 higher register bit assignments.

Table 4-140 por_dn_por_dn_vmf3_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

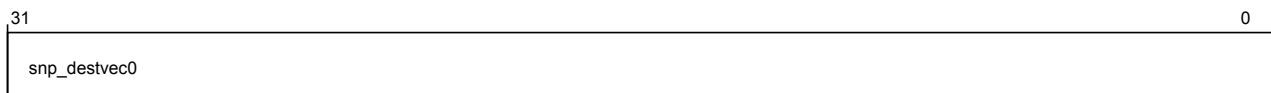


Figure 4-124 por_dn_por_dn_vmf3_rnf0 (low)

The following table shows the por_dn_vmf3_rnf0 lower register bit assignments.

Table 4-141 por_dn_por_dn_vmf3_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

por_dn_vmf3_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC70
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

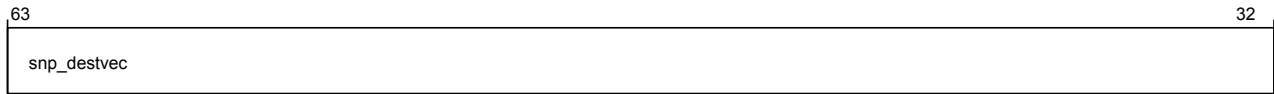


Figure 4-125 por_dn_por_dn_vmf3_rnd (high)

The following table shows the por_dn_vmf3_rnd higher register bit assignments.

Table 4-142 por_dn_por_dn_vmf3_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

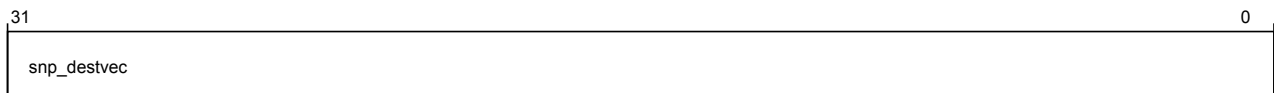


Figure 4-126 por_dn_por_dn_vmf3_rnd (low)

The following table shows the por_dn_vmf3_rnd lower register bit assignments.

Table 4-143 por_dn_por_dn_vmf3_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

por_dn_vmf3_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

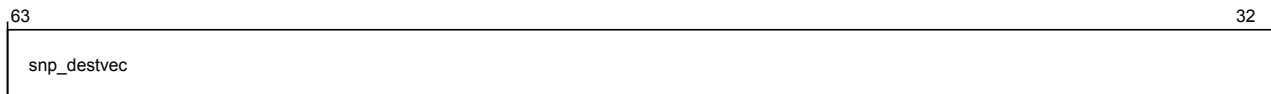


Figure 4-127 por_dn_por_dn_vmf3_cxra (high)

The following table shows the por_dn_vmf3_cxra higher register bit assignments.

Table 4-144 por_dn_por_dn_vmf3_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

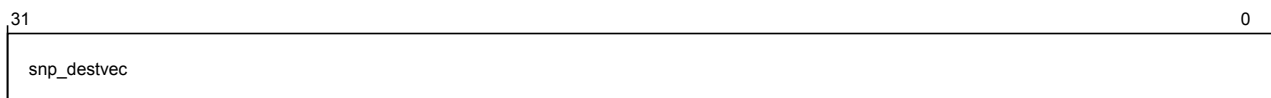


Figure 4-128 por_dn_por_dn_vmf3_cxra (low)

The following table shows the por_dn_vmf3_cxra lower register bit assignments.

Table 4-145 por_dn_por_dn_vmf3_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

por_dn_vmf4_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC80
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

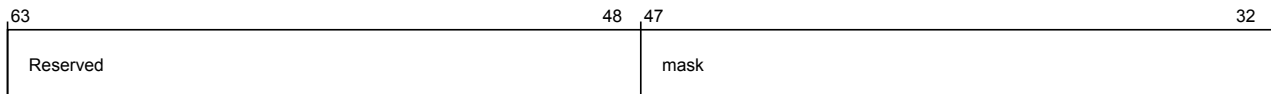


Figure 4-129 por_dn_por_dn_vmf4_ctrl (high)

The following table shows the por_dn_vmf4_ctrl higher register bit assignments.

Table 4-146 por_dn_por_dn_vmf4_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf4_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

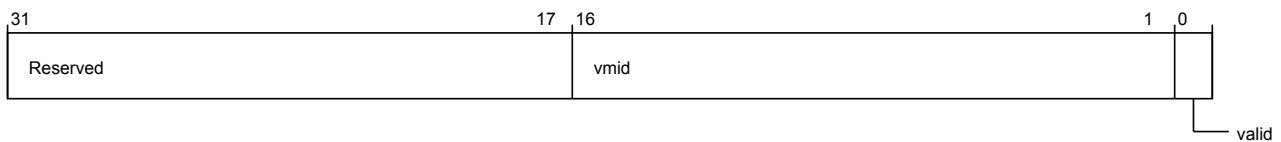


Figure 4-130 por_dn_por_dn_vmf4_ctrl (low)

The following table shows the por_dn_vmf4_ctrl lower register bit assignments.

Table 4-147 por_dn_por_dn_vmf4_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf4_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC88
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

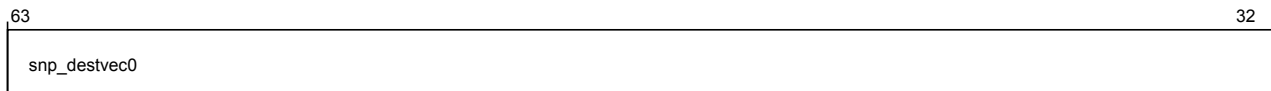


Figure 4-131 por_dn_por_dn_vmf4_rnf0 (high)

The following table shows the por_dn_vmf4_rnf0 higher register bit assignments.

Table 4-148 por_dn_por_dn_vmf4_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

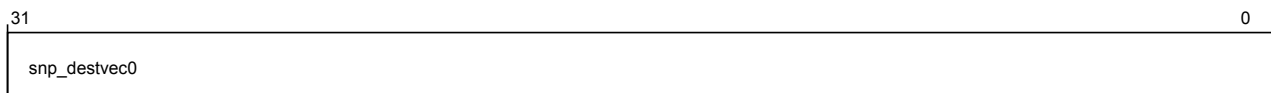


Figure 4-132 por_dn_por_dn_vmf4_rnf0 (low)

The following table shows the por_dn_vmf4_rnf0 lower register bit assignments.

Table 4-149 por_dn_por_dn_vmf4_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

por_dn_vmf4_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC90
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

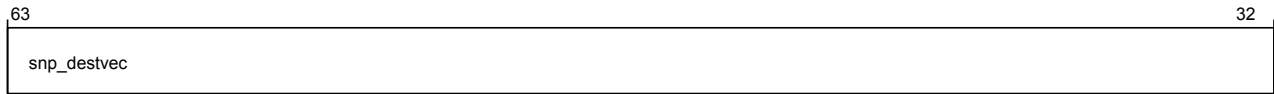


Figure 4-133 por_dn_por_dn_vmf4_rnd (high)

The following table shows the por_dn_vmf4_rnd higher register bit assignments.

Table 4-150 por_dn_por_dn_vmf4_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

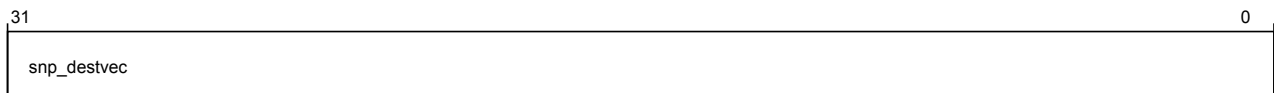


Figure 4-134 por_dn_por_dn_vmf4_rnd (low)

The following table shows the por_dn_vmf4_rnd lower register bit assignments.

Table 4-151 por_dn_por_dn_vmf4_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

por_dn_vmf4_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC98

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

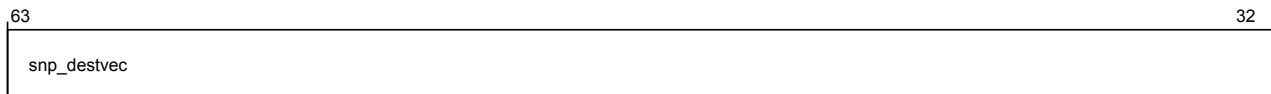


Figure 4-135 por_dn_vmf4_cxra (high)

The following table shows the por_dn_vmf4_cxra higher register bit assignments.

Table 4-152 por_dn_vmf4_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

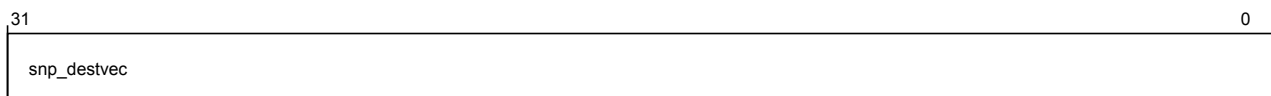


Figure 4-136 por_dn_vmf4_cxra (low)

The following table shows the por_dn_vmf4_cxra lower register bit assignments.

Table 4-153 por_dn_vmf4_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

por_dn_vmf5_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCA0
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

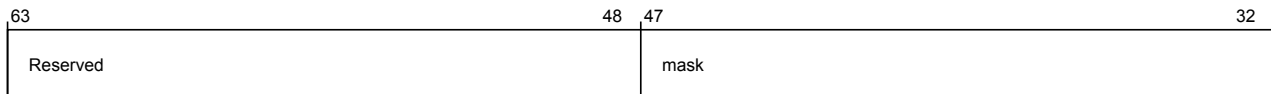


Figure 4-137 por_dn_por_dn_vmf5_ctrl (high)

The following table shows the por_dn_vmf5_ctrl higher register bit assignments.

Table 4-154 por_dn_por_dn_vmf5_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf5_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

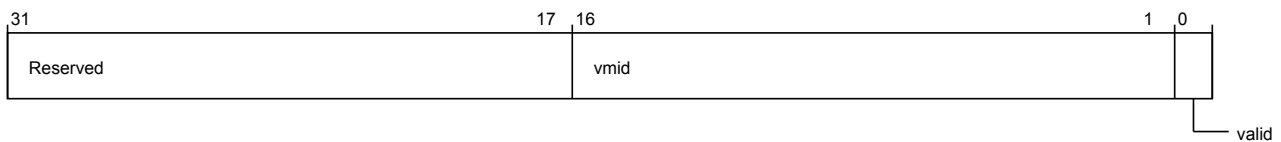


Figure 4-138 por_dn_por_dn_vmf5_ctrl (low)

The following table shows the por_dn_vmf5_ctrl lower register bit assignments.

Table 4-155 por_dn_por_dn_vmf5_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf5_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCA8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

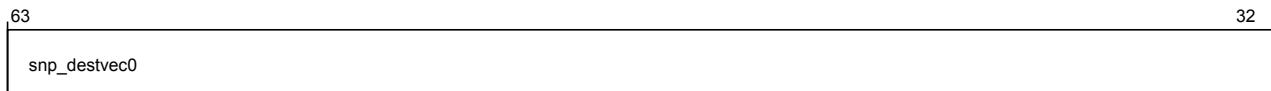


Figure 4-139 por_dn_por_dn_vmf5_rnf0 (high)

The following table shows the por_dn_vmf5_rnf0 higher register bit assignments.

Table 4-156 por_dn_por_dn_vmf5_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

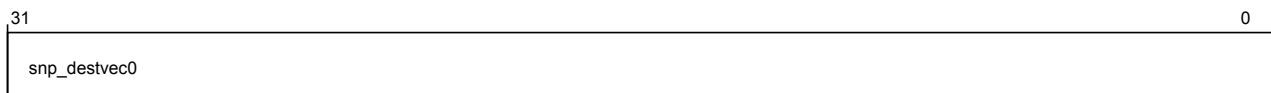


Figure 4-140 por_dn_por_dn_vmf5_rnf0 (low)

The following table shows the por_dn_vmf5_rnf0 lower register bit assignments.

Table 4-157 por_dn_por_dn_vmf5_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

por_dn_vmf5_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCB0
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

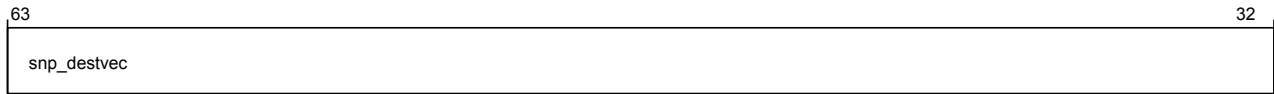


Figure 4-141 por_dn_por_dn_vmf5_rnd (high)

The following table shows the por_dn_vmf5_rnd higher register bit assignments.

Table 4-158 por_dn_por_dn_vmf5_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

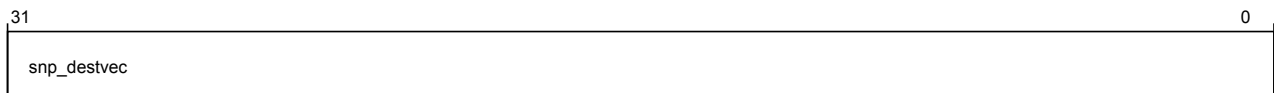


Figure 4-142 por_dn_por_dn_vmf5_rnd (low)

The following table shows the por_dn_vmf5_rnd lower register bit assignments.

Table 4-159 por_dn_por_dn_vmf5_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

por_dn_vmf5_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

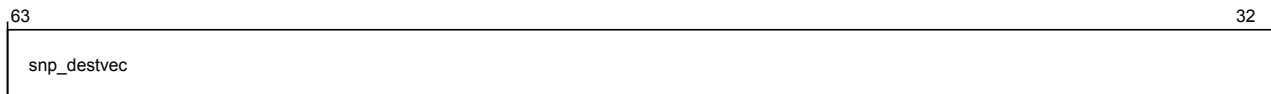


Figure 4-143 por_dn_vmf5_cxra (high)

The following table shows the por_dn_vmf5_cxra higher register bit assignments.

Table 4-160 por_dn_vmf5_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

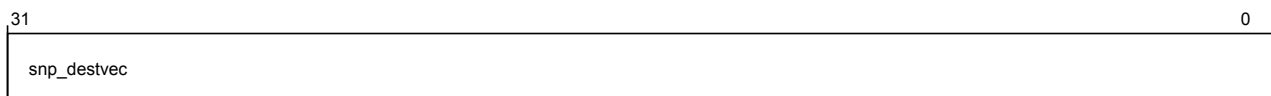


Figure 4-144 por_dn_vmf5_cxra (low)

The following table shows the por_dn_vmf5_cxra lower register bit assignments.

Table 4-161 por_dn_vmf5_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

por_dn_vmf6_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCC0
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

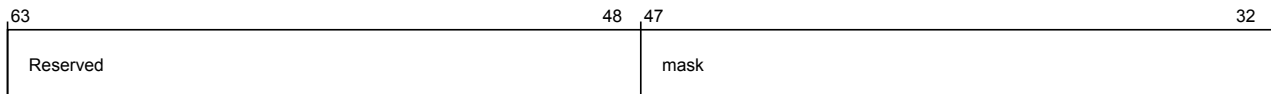


Figure 4-145 por_dn_por_dn_vmf6_ctrl (high)

The following table shows the por_dn_vmf6_ctrl higher register bit assignments.

Table 4-162 por_dn_por_dn_vmf6_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf6_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

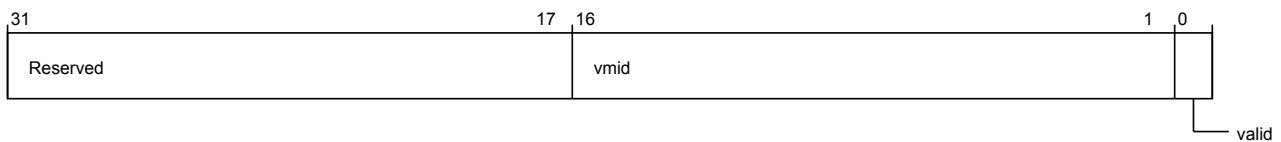


Figure 4-146 por_dn_por_dn_vmf6_ctrl (low)

The following table shows the por_dn_vmf6_ctrl lower register bit assignments.

Table 4-163 por_dn_por_dn_vmf6_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf6_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCC8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

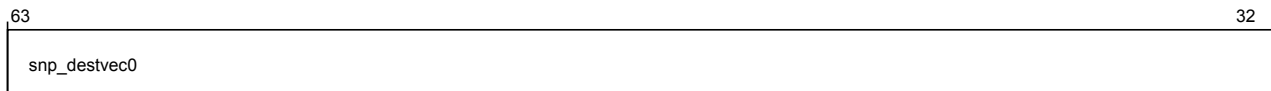


Figure 4-147 por_dn_por_dn_vmf6_rnf0 (high)

The following table shows the por_dn_vmf6_rnf0 higher register bit assignments.

Table 4-164 por_dn_por_dn_vmf6_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

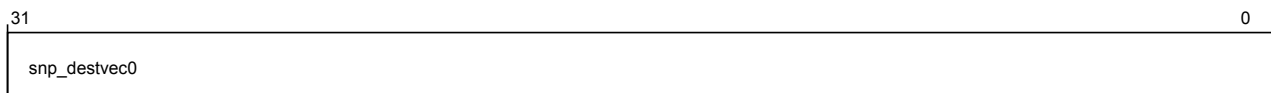


Figure 4-148 por_dn_por_dn_vmf6_rnf0 (low)

The following table shows the por_dn_vmf6_rnf0 lower register bit assignments.

Table 4-165 por_dn_por_dn_vmf6_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

por_dn_vmf6_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCD0
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.



Figure 4-149 por_dn_por_dn_vmf6_rnd (high)

The following table shows the por_dn_vmf6_rnd higher register bit assignments.

Table 4-166 por_dn_por_dn_vmf6_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

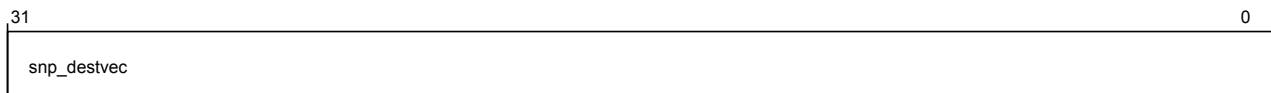


Figure 4-150 por_dn_por_dn_vmf6_rnd (low)

The following table shows the por_dn_vmf6_rnd lower register bit assignments.

Table 4-167 por_dn_por_dn_vmf6_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

por_dn_vmf6_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

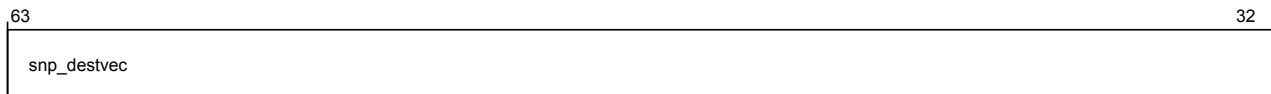


Figure 4-151 por_dn_por_dn_vmf6_cxra (high)

The following table shows the por_dn_vmf6_cxra higher register bit assignments.

Table 4-168 por_dn_por_dn_vmf6_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

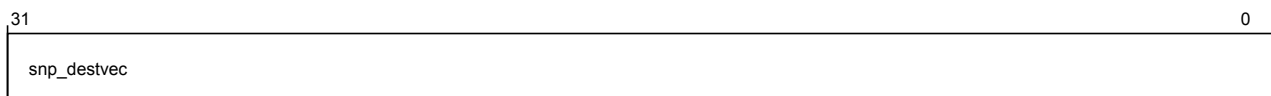


Figure 4-152 por_dn_por_dn_vmf6_cxra (low)

The following table shows the por_dn_vmf6_cxra lower register bit assignments.

Table 4-169 por_dn_por_dn_vmf6_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

por_dn_vmf7_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCE0
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

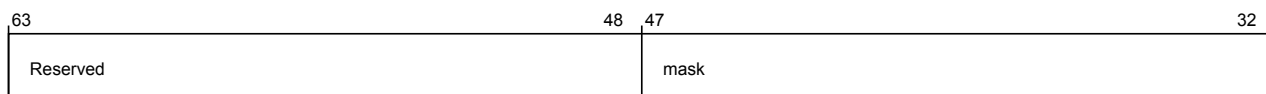


Figure 4-153 por_dn_por_dn_vmf7_ctrl (high)

The following table shows the por_dn_vmf7_ctrl higher register bit assignments.

Table 4-170 por_dn_por_dn_vmf7_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf7_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

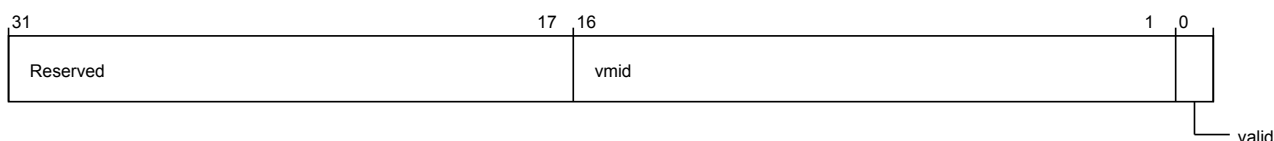


Figure 4-154 por_dn_por_dn_vmf7_ctrl (low)

The following table shows the por_dn_vmf7_ctrl lower register bit assignments.

Table 4-171 por_dn_por_dn_vmf7_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf7_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCE8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

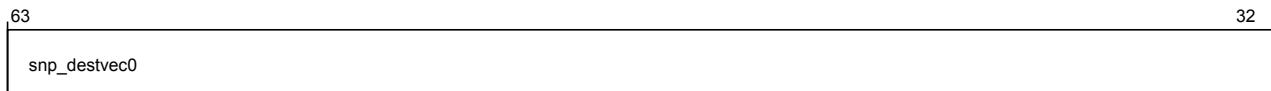


Figure 4-155 por_dn_por_dn_vmf7_rnf0 (high)

The following table shows the por_dn_vmf7_rnf0 higher register bit assignments.

Table 4-172 por_dn_por_dn_vmf7_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

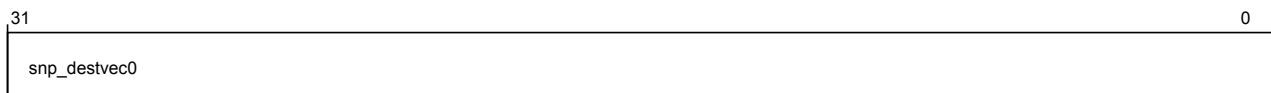


Figure 4-156 por_dn_por_dn_vmf7_rnf0 (low)

The following table shows the por_dn_vmf7_rnf0 lower register bit assignments.

Table 4-173 por_dn_por_dn_vmf7_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

por_dn_vmf7_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCF0
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

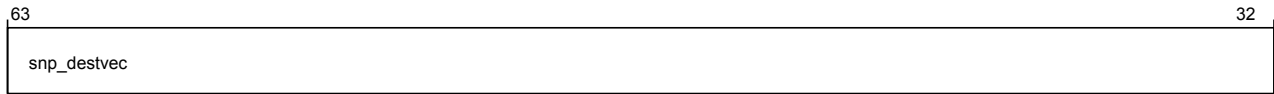


Figure 4-157 por_dn_por_dn_vmf7_rnd (high)

The following table shows the por_dn_vmf7_rnd higher register bit assignments.

Table 4-174 por_dn_por_dn_vmf7_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

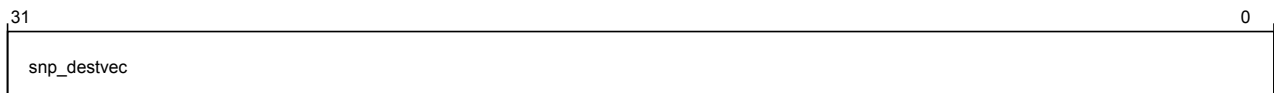


Figure 4-158 por_dn_por_dn_vmf7_rnd (low)

The following table shows the por_dn_vmf7_rnd lower register bit assignments.

Table 4-175 por_dn_por_dn_vmf7_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

por_dn_vmf7_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

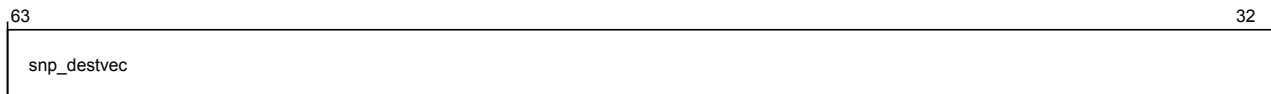


Figure 4-159 por_dn_por_dn_vmf7_cxra (high)

The following table shows the por_dn_vmf7_cxra higher register bit assignments.

Table 4-176 por_dn_por_dn_vmf7_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

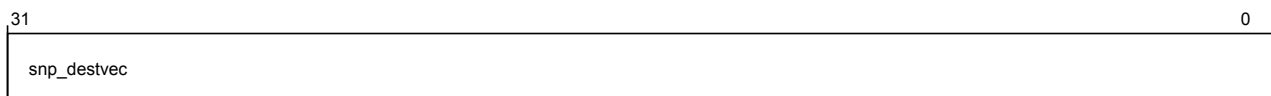


Figure 4-160 por_dn_por_dn_vmf7_cxra (low)

The following table shows the por_dn_vmf7_cxra lower register bit assignments.

Table 4-177 por_dn_por_dn_vmf7_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

por_dn_vmf8_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD00
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

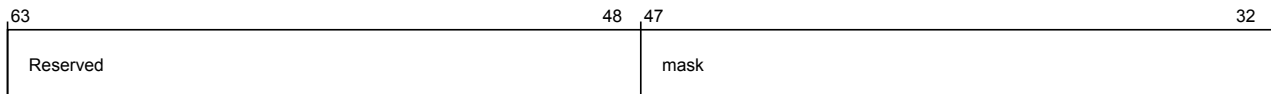


Figure 4-161 por_dn_por_dn_vmf8_ctrl (high)

The following table shows the por_dn_vmf8_ctrl higher register bit assignments.

Table 4-178 por_dn_por_dn_vmf8_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf8_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

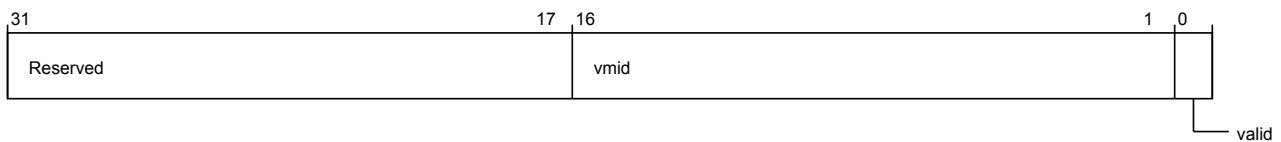


Figure 4-162 por_dn_por_dn_vmf8_ctrl (low)

The following table shows the por_dn_vmf8_ctrl lower register bit assignments.

Table 4-179 por_dn_por_dn_vmf8_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf8_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD08
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

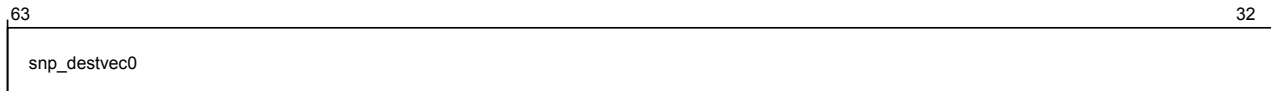


Figure 4-163 por_dn_por_dn_vmf8_rnf0 (high)

The following table shows the por_dn_vmf8_rnf0 higher register bit assignments.

Table 4-180 por_dn_por_dn_vmf8_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.



Figure 4-164 por_dn_por_dn_vmf8_rnf0 (low)

The following table shows the por_dn_vmf8_rnf0 lower register bit assignments.

Table 4-181 por_dn_por_dn_vmf8_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

por_dn_vmf8_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD10
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

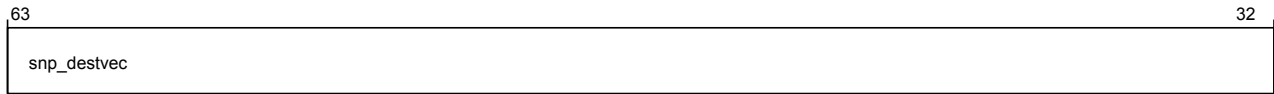


Figure 4-165 por_dn_por_dn_vmf8_rnd (high)

The following table shows the por_dn_vmf8_rnd higher register bit assignments.

Table 4-182 por_dn_por_dn_vmf8_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

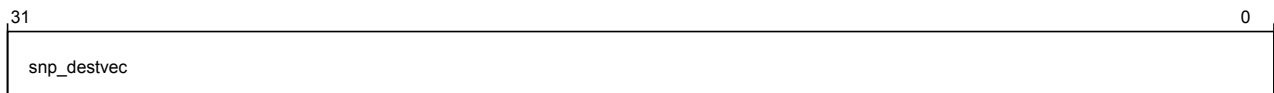


Figure 4-166 por_dn_por_dn_vmf8_rnd (low)

The following table shows the por_dn_vmf8_rnd lower register bit assignments.

Table 4-183 por_dn_por_dn_vmf8_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

por_dn_vmf8_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD18

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

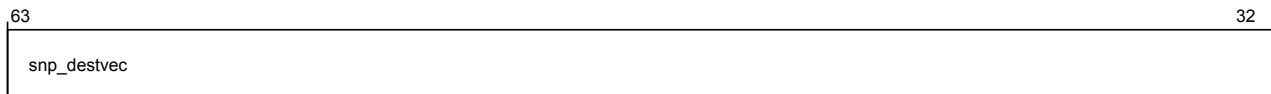


Figure 4-167 por_dn_vmf8_cxra (high)

The following table shows the por_dn_vmf8_cxra higher register bit assignments.

Table 4-184 por_dn_vmf8_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

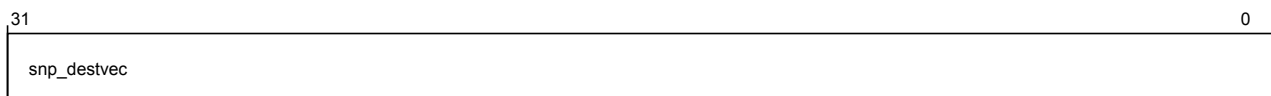


Figure 4-168 por_dn_vmf8_cxra (low)

The following table shows the por_dn_vmf8_cxra lower register bit assignments.

Table 4-185 por_dn_vmf8_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

por_dn_vmf9_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD20
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

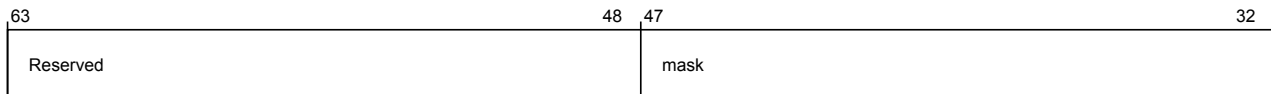


Figure 4-169 por_dn_por_dn_vmf9_ctrl (high)

The following table shows the por_dn_vmf9_ctrl higher register bit assignments.

Table 4-186 por_dn_por_dn_vmf9_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf9_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

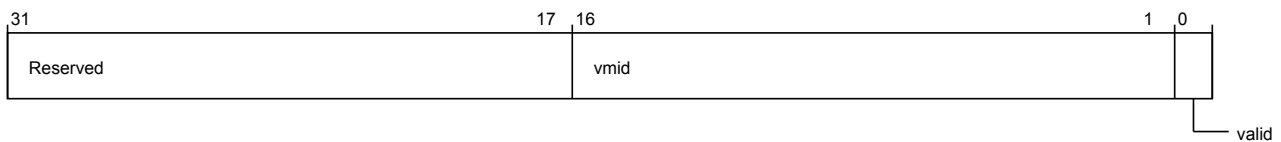


Figure 4-170 por_dn_por_dn_vmf9_ctrl (low)

The following table shows the por_dn_vmf9_ctrl lower register bit assignments.

Table 4-187 por_dn_por_dn_vmf9_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf9_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD28
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

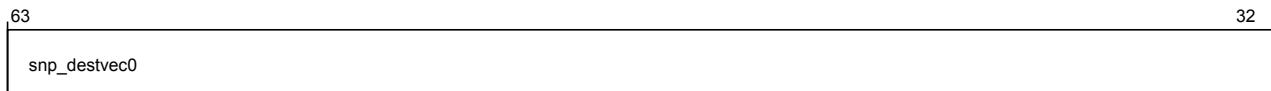


Figure 4-171 por_dn_por_dn_vmf9_rnf0 (high)

The following table shows the por_dn_vmf9_rnf0 higher register bit assignments.

Table 4-188 por_dn_por_dn_vmf9_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

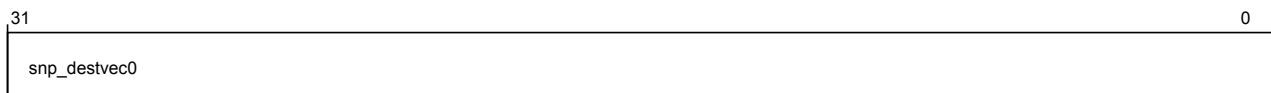


Figure 4-172 por_dn_por_dn_vmf9_rnf0 (low)

The following table shows the por_dn_vmf9_rnf0 lower register bit assignments.

Table 4-189 por_dn_por_dn_vmf9_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

por_dn_vmf9_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD30
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

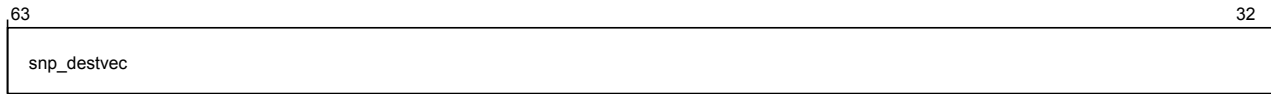


Figure 4-173 por_dn_por_dn_vmf9_rnd (high)

The following table shows the por_dn_vmf9_rnd higher register bit assignments.

Table 4-190 por_dn_por_dn_vmf9_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

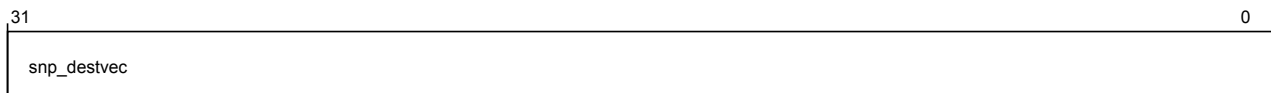


Figure 4-174 por_dn_por_dn_vmf9_rnd (low)

The following table shows the por_dn_vmf9_rnd lower register bit assignments.

Table 4-191 por_dn_por_dn_vmf9_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

por_dn_vmf9_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

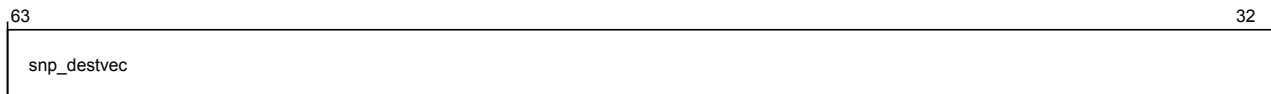


Figure 4-175 por_dn_por_dn_vmf9_cxra (high)

The following table shows the por_dn_vmf9_cxra higher register bit assignments.

Table 4-192 por_dn_por_dn_vmf9_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

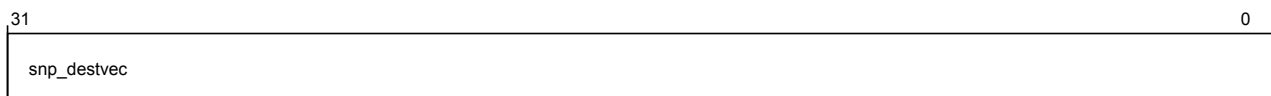


Figure 4-176 por_dn_por_dn_vmf9_cxra (low)

The following table shows the por_dn_vmf9_cxra lower register bit assignments.

Table 4-193 por_dn_por_dn_vmf9_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

por_dn_vmf10_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD40
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

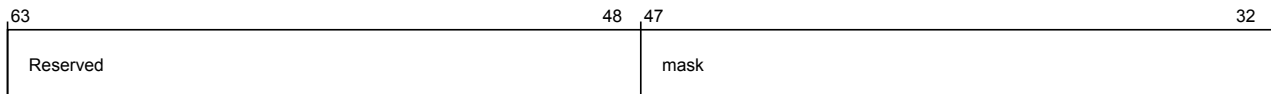


Figure 4-177 por_dn_por_dn_vmf10_ctrl (high)

The following table shows the por_dn_vmf10_ctrl higher register bit assignments.

Table 4-194 por_dn_por_dn_vmf10_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf10_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

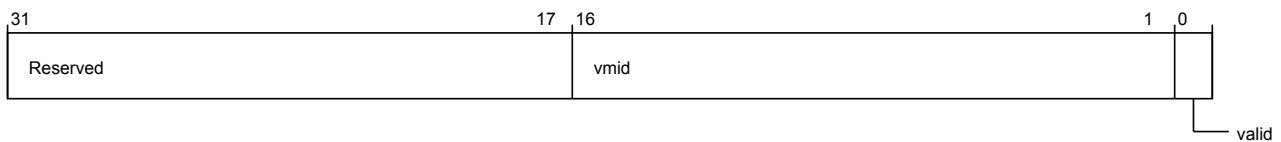


Figure 4-178 por_dn_por_dn_vmf10_ctrl (low)

The following table shows the por_dn_vmf10_ctrl lower register bit assignments.

Table 4-195 por_dn_por_dn_vmf10_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf10_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD48
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

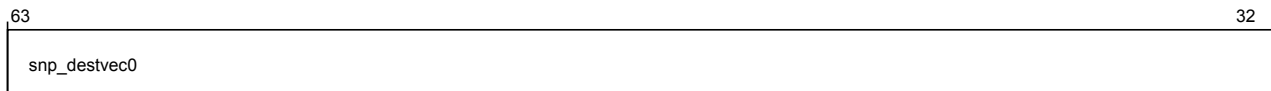


Figure 4-179 por_dn_por_dn_vmf10_rnf0 (high)

The following table shows the por_dn_vmf10_rnf0 higher register bit assignments.

Table 4-196 por_dn_por_dn_vmf10_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

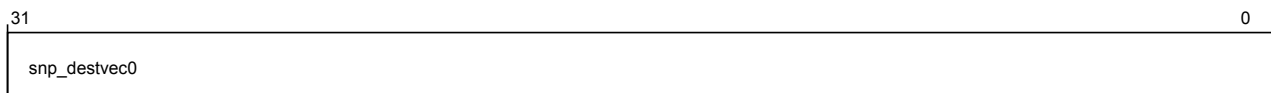


Figure 4-180 por_dn_por_dn_vmf10_rnf0 (low)

The following table shows the por_dn_vmf10_rnf0 lower register bit assignments.

Table 4-197 por_dn_por_dn_vmf10_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

por_dn_vmf10_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD50
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

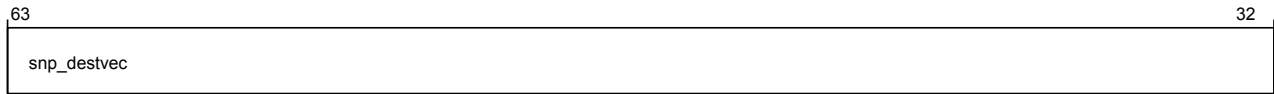


Figure 4-181 por_dn_por_dn_vmf10_rnd (high)

The following table shows the por_dn_vmf10_rnd higher register bit assignments.

Table 4-198 por_dn_por_dn_vmf10_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

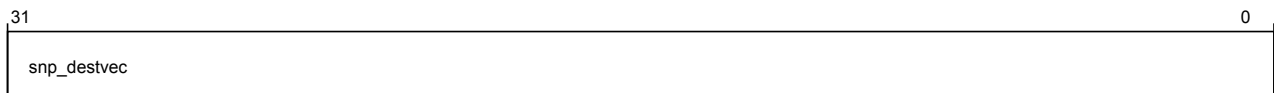


Figure 4-182 por_dn_por_dn_vmf10_rnd (low)

The following table shows the por_dn_vmf10_rnd lower register bit assignments.

Table 4-199 por_dn_por_dn_vmf10_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

por_dn_vmf10_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD58

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

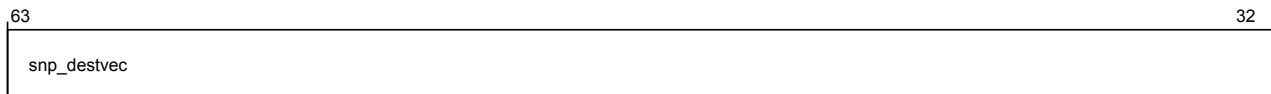


Figure 4-183 por_dn_por_dn_vmf10_cxra (high)

The following table shows the por_dn_vmf10_cxra higher register bit assignments.

Table 4-200 por_dn_por_dn_vmf10_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.



Figure 4-184 por_dn_por_dn_vmf10_cxra (low)

The following table shows the por_dn_vmf10_cxra lower register bit assignments.

Table 4-201 por_dn_por_dn_vmf10_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

por_dn_vmf11_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD60
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

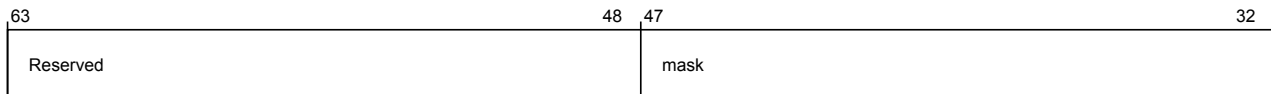


Figure 4-185 por_dn_por_dn_vmf11_ctrl (high)

The following table shows the por_dn_vmf11_ctrl higher register bit assignments.

Table 4-202 por_dn_por_dn_vmf11_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf11_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

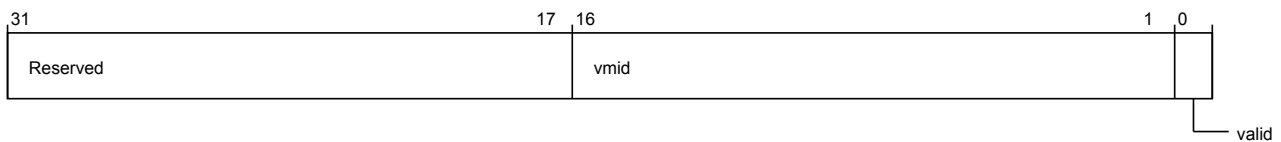


Figure 4-186 por_dn_por_dn_vmf11_ctrl (low)

The following table shows the por_dn_vmf11_ctrl lower register bit assignments.

Table 4-203 por_dn_por_dn_vmf11_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf11_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD68
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

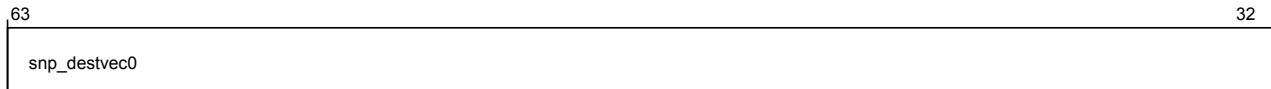


Figure 4-187 `por_dn_por_dn_vmf11_rnf0` (high)

The following table shows the `por_dn_vmf11_rnf0` higher register bit assignments.

Table 4-204 `por_dn_por_dn_vmf11_rnf0` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>snp_destvec0</code>	RN-F bit vector 63:0 corresponding to <code>por_dn_vmf11_ctrl.vmid</code>	RW	64'b0

The following image shows the lower register bit assignments.

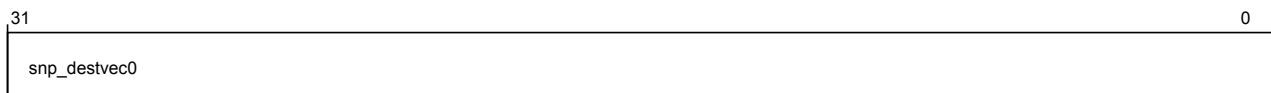


Figure 4-188 `por_dn_por_dn_vmf11_rnf0` (low)

The following table shows the `por_dn_vmf11_rnf0` lower register bit assignments.

Table 4-205 `por_dn_por_dn_vmf11_rnf0` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>snp_destvec0</code>	RN-F bit vector 63:0 corresponding to <code>por_dn_vmf11_ctrl.vmid</code>	RW	64'b0

`por_dn_vmf11_rnd`

Contains the logical RN-D bit vector 63:0 corresponding to `por_dn_vmf11_ctrl.vmid`. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD70
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

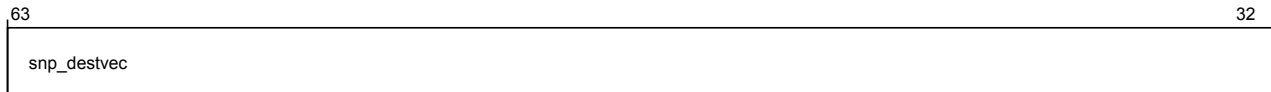


Figure 4-189 por_dn_por_dn_vmf11_rnd (high)

The following table shows the por_dn_vmf11_rnd higher register bit assignments.

Table 4-206 por_dn_por_dn_vmf11_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

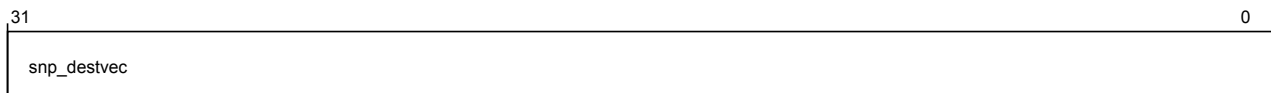


Figure 4-190 por_dn_por_dn_vmf11_rnd (low)

The following table shows the por_dn_vmf11_rnd lower register bit assignments.

Table 4-207 por_dn_por_dn_vmf11_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

por_dn_vmf11_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

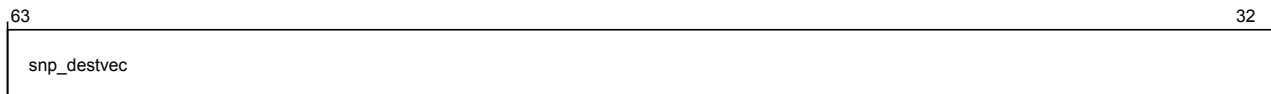


Figure 4-191 por_dn_por_dn_vmf11_cxra (high)

The following table shows the por_dn_vmf11_cxra higher register bit assignments.

Table 4-208 por_dn_por_dn_vmf11_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

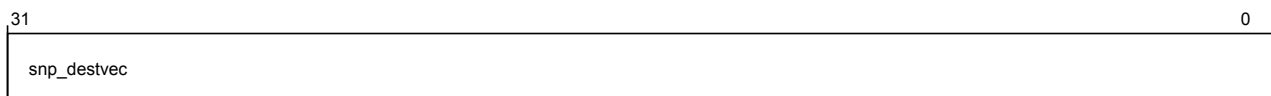


Figure 4-192 por_dn_por_dn_vmf11_cxra (low)

The following table shows the por_dn_vmf11_cxra lower register bit assignments.

Table 4-209 por_dn_por_dn_vmf11_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

por_dn_vmf12_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD80
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

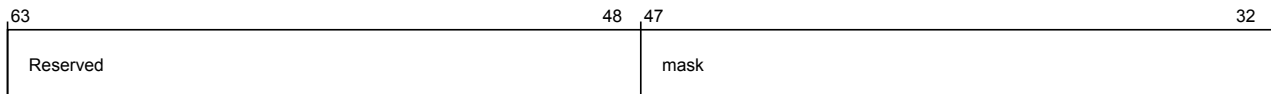


Figure 4-193 por_dn_por_dn_vmf12_ctrl (high)

The following table shows the por_dn_vmf12_ctrl higher register bit assignments.

Table 4-210 por_dn_por_dn_vmf12_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf12_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

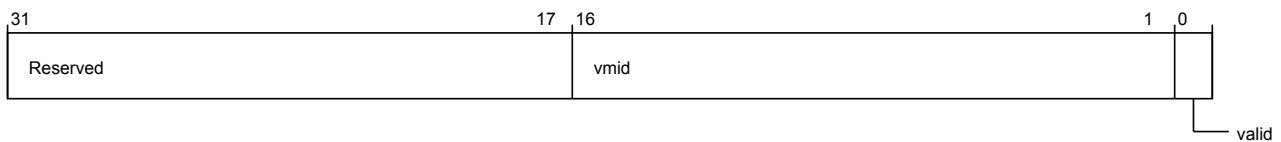


Figure 4-194 por_dn_por_dn_vmf12_ctrl (low)

The following table shows the por_dn_vmf12_ctrl lower register bit assignments.

Table 4-211 por_dn_por_dn_vmf12_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf12_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD88
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

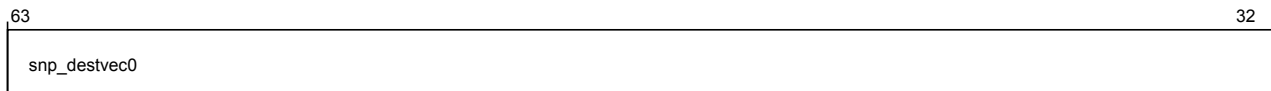


Figure 4-195 por_dn_por_dn_vmf12_rnf0 (high)

The following table shows the por_dn_vmf12_rnf0 higher register bit assignments.

Table 4-212 por_dn_por_dn_vmf12_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

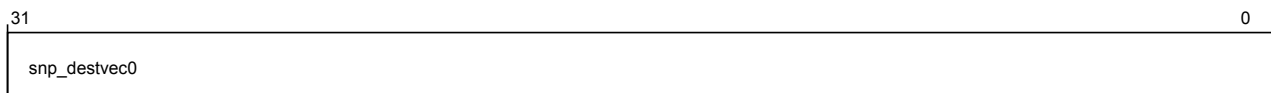


Figure 4-196 por_dn_por_dn_vmf12_rnf0 (low)

The following table shows the por_dn_vmf12_rnf0 lower register bit assignments.

Table 4-213 por_dn_por_dn_vmf12_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

por_dn_vmf12_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD90
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

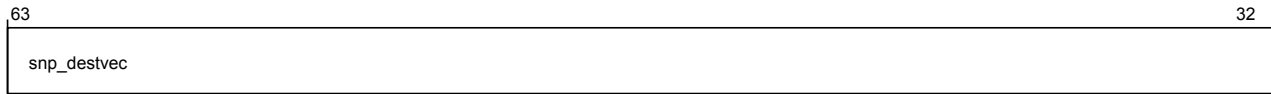


Figure 4-197 por_dn_por_dn_vmf12_rnd (high)

The following table shows the por_dn_vmf12_rnd higher register bit assignments.

Table 4-214 por_dn_por_dn_vmf12_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

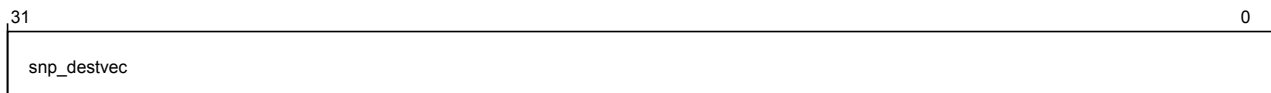


Figure 4-198 por_dn_por_dn_vmf12_rnd (low)

The following table shows the por_dn_vmf12_rnd lower register bit assignments.

Table 4-215 por_dn_por_dn_vmf12_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

por_dn_vmf12_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD98

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

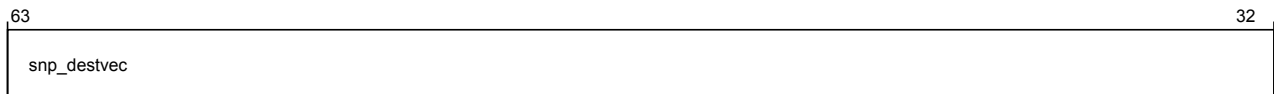


Figure 4-199 `por_dn_por_dn_vmf12_cxra` (high)

The following table shows the `por_dn_vmf12_cxra` higher register bit assignments.

Table 4-216 `por_dn_por_dn_vmf12_cxra` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>snp_destvec</code>	CXRA bit vector 63:0 corresponding to <code>por_dn_vmf12_ctrl.vmid</code>	RW	64'b0

The following image shows the lower register bit assignments.

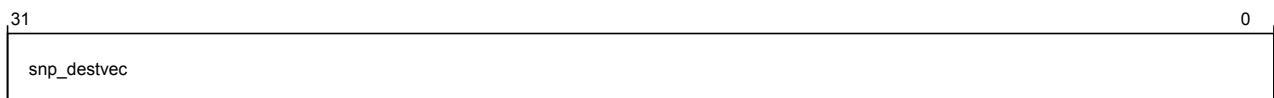


Figure 4-200 `por_dn_por_dn_vmf12_cxra` (low)

The following table shows the `por_dn_vmf12_cxra` lower register bit assignments.

Table 4-217 `por_dn_por_dn_vmf12_cxra` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>snp_destvec</code>	CXRA bit vector 63:0 corresponding to <code>por_dn_vmf12_ctrl.vmid</code>	RW	64'b0

`por_dn_vmf13_ctrl`

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when `por_dn_aux_ctl.disable_vmf` is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDA0
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_dn_secure_register_groups_override.vmf</code>

The following image shows the higher register bit assignments.

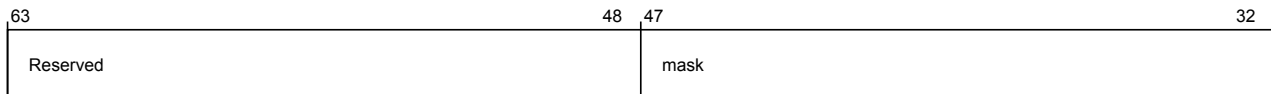


Figure 4-201 por_dn_por_dn_vmf13_ctrl (high)

The following table shows the por_dn_vmf13_ctrl higher register bit assignments.

Table 4-218 por_dn_por_dn_vmf13_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf13_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

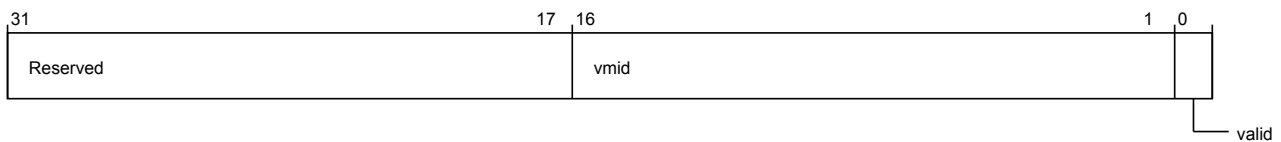


Figure 4-202 por_dn_por_dn_vmf13_ctrl (low)

The following table shows the por_dn_vmf13_ctrl lower register bit assignments.

Table 4-219 por_dn_por_dn_vmf13_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf13_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDA8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

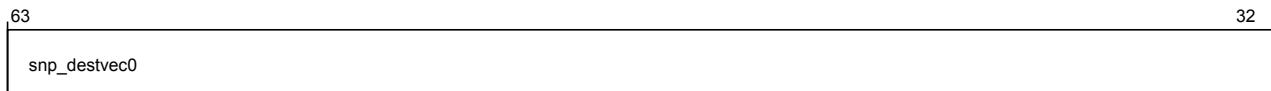


Figure 4-203 `por_dn_por_dn_vmf13_rnf0` (high)

The following table shows the `por_dn_vmf13_rnf0` higher register bit assignments.

Table 4-220 `por_dn_por_dn_vmf13_rnf0` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>snp_destvec0</code>	RN-F bit vector 63:0 corresponding to <code>por_dn_vmf13_ctrl.vmid</code>	RW	64'b0

The following image shows the lower register bit assignments.

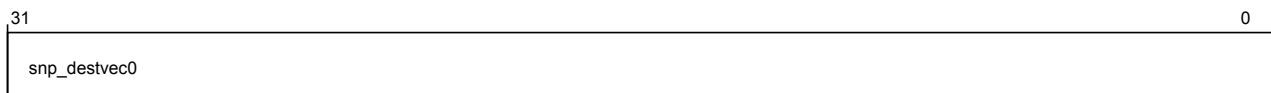


Figure 4-204 `por_dn_por_dn_vmf13_rnf0` (low)

The following table shows the `por_dn_vmf13_rnf0` lower register bit assignments.

Table 4-221 `por_dn_por_dn_vmf13_rnf0` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>snp_destvec0</code>	RN-F bit vector 63:0 corresponding to <code>por_dn_vmf13_ctrl.vmid</code>	RW	64'b0

`por_dn_vmf13_rnd`

Contains the logical RN-D bit vector 63:0 corresponding to `por_dn_vmf13_ctrl.vmid`. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDB0
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.



Figure 4-205 por_dn_por_dn_vmf13_rnd (high)

The following table shows the por_dn_vmf13_rnd higher register bit assignments.

Table 4-222 por_dn_por_dn_vmf13_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

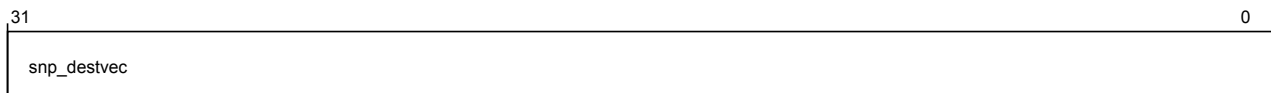


Figure 4-206 por_dn_por_dn_vmf13_rnd (low)

The following table shows the por_dn_vmf13_rnd lower register bit assignments.

Table 4-223 por_dn_por_dn_vmf13_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

por_dn_vmf13_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

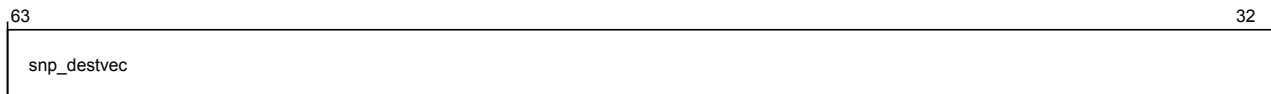


Figure 4-207 por_dn_por_dn_vmf13_cxra (high)

The following table shows the por_dn_vmf13_cxra higher register bit assignments.

Table 4-224 por_dn_por_dn_vmf13_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

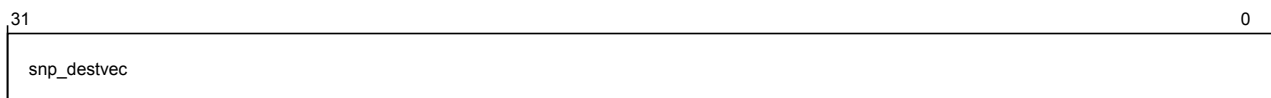


Figure 4-208 por_dn_por_dn_vmf13_cxra (low)

The following table shows the por_dn_vmf13_cxra lower register bit assignments.

Table 4-225 por_dn_por_dn_vmf13_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

por_dn_vmf14_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDC0
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

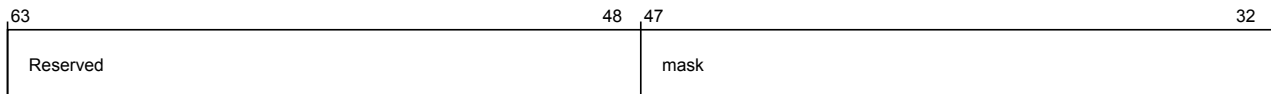


Figure 4-209 por_dn_por_dn_vmf14_ctrl (high)

The following table shows the por_dn_vmf14_ctrl higher register bit assignments.

Table 4-226 por_dn_por_dn_vmf14_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf14_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

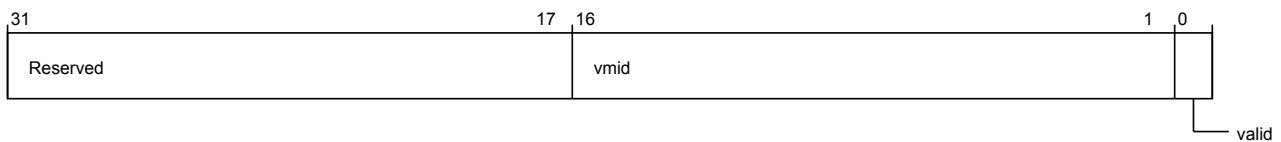


Figure 4-210 por_dn_por_dn_vmf14_ctrl (low)

The following table shows the por_dn_vmf14_ctrl lower register bit assignments.

Table 4-227 por_dn_por_dn_vmf14_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf14_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDC8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

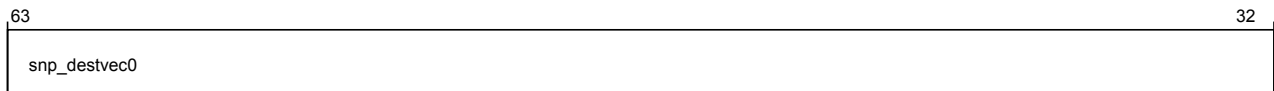


Figure 4-211 por_dn_por_dn_vmf14_rnf0 (high)

The following table shows the por_dn_vmf14_rnf0 higher register bit assignments.

Table 4-228 por_dn_por_dn_vmf14_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

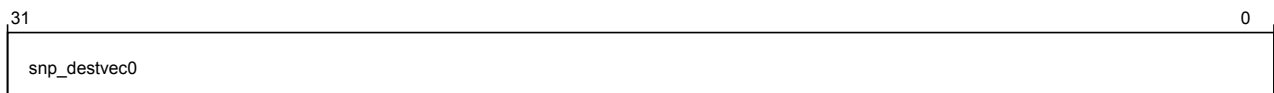


Figure 4-212 por_dn_por_dn_vmf14_rnf0 (low)

The following table shows the por_dn_vmf14_rnf0 lower register bit assignments.

Table 4-229 por_dn_por_dn_vmf14_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

por_dn_vmf14_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDD0
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

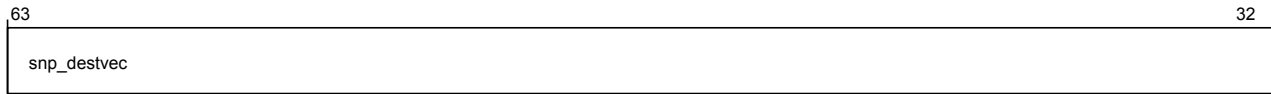


Figure 4-213 por_dn_por_dn_vmf14_rnd (high)

The following table shows the por_dn_vmf14_rnd higher register bit assignments.

Table 4-230 por_dn_por_dn_vmf14_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

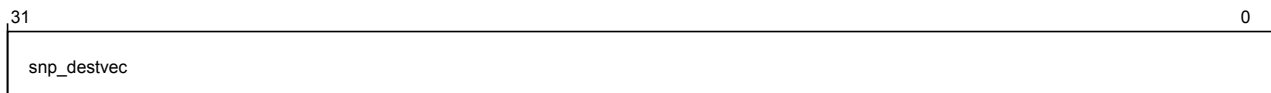


Figure 4-214 por_dn_por_dn_vmf14_rnd (low)

The following table shows the por_dn_vmf14_rnd lower register bit assignments.

Table 4-231 por_dn_por_dn_vmf14_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

por_dn_vmf14_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

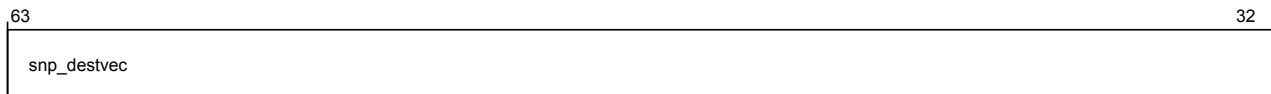


Figure 4-215 por_dn_por_dn_vmf14_cxra (high)

The following table shows the por_dn_vmf14_cxra higher register bit assignments.

Table 4-232 por_dn_por_dn_vmf14_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

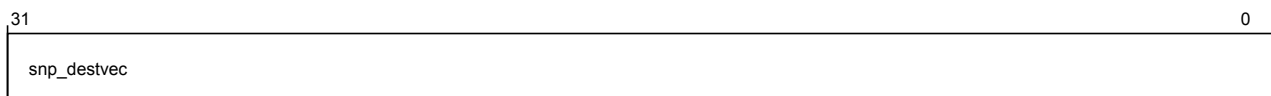


Figure 4-216 por_dn_por_dn_vmf14_cxra (low)

The following table shows the por_dn_vmf14_cxra lower register bit assignments.

Table 4-233 por_dn_por_dn_vmf14_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

por_dn_vmf15_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDE0
Register reset	64'b11111111111111110000000000000000
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

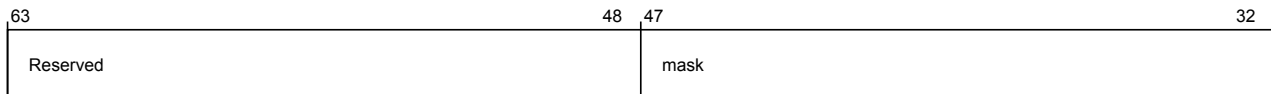


Figure 4-217 por_dn_por_dn_vmf15_ctrl (high)

The following table shows the por_dn_vmf15_ctrl higher register bit assignments.

Table 4-234 por_dn_por_dn_vmf15_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf15_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

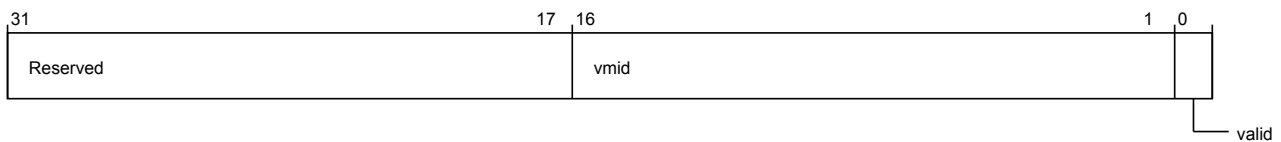


Figure 4-218 por_dn_por_dn_vmf15_ctrl (low)

The following table shows the por_dn_vmf15_ctrl lower register bit assignments.

Table 4-235 por_dn_por_dn_vmf15_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf15_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDE8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

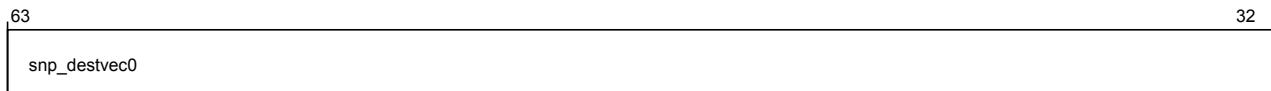


Figure 4-219 por_dn_por_dn_vmf15_rnf0 (high)

The following table shows the por_dn_vmf15_rnf0 higher register bit assignments.

Table 4-236 por_dn_por_dn_vmf15_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

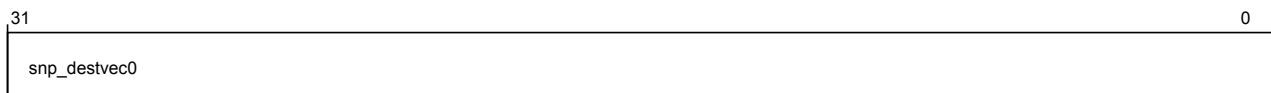


Figure 4-220 por_dn_por_dn_vmf15_rnf0 (low)

The following table shows the por_dn_vmf15_rnf0 lower register bit assignments.

Table 4-237 por_dn_por_dn_vmf15_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

por_dn_vmf15_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDF0
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.



Figure 4-221 por_dn_por_dn_vmf15_rnd (high)

The following table shows the por_dn_vmf15_rnd higher register bit assignments.

Table 4-238 por_dn_por_dn_vmf15_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

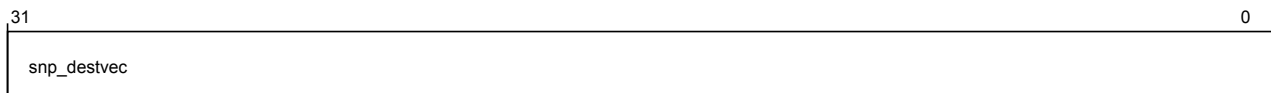


Figure 4-222 por_dn_por_dn_vmf15_rnd (low)

The following table shows the por_dn_vmf15_rnd lower register bit assignments.

Table 4-239 por_dn_por_dn_vmf15_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

por_dn_vmf15_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600AE system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

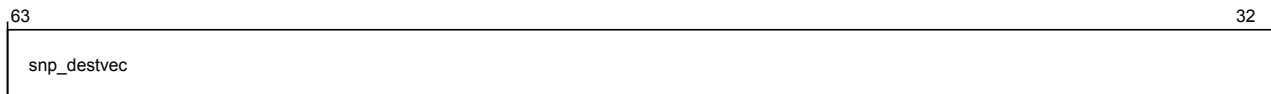


Figure 4-223 `por_dn_por_dn_vmf15_cxra` (high)

The following table shows the `por_dn_vmf15_cxra` higher register bit assignments.

Table 4-240 `por_dn_por_dn_vmf15_cxra` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>snp_destvec</code>	CXRA bit vector 63:0 corresponding to <code>por_dn_vmf15_ctrl.vmid</code>	RW	64'b0

The following image shows the lower register bit assignments.

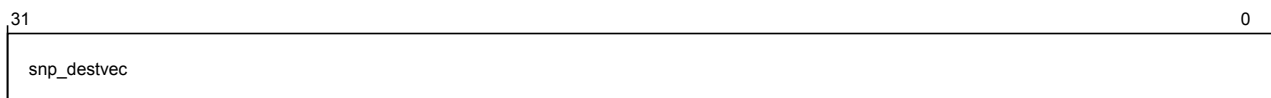


Figure 4-224 `por_dn_por_dn_vmf15_cxra` (low)

The following table shows the `por_dn_vmf15_cxra` lower register bit assignments.

Table 4-241 `por_dn_por_dn_vmf15_cxra` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>snp_destvec</code>	CXRA bit vector 63:0 corresponding to <code>por_dn_vmf15_ctrl.vmid</code>	RW	64'b0

`por_dn_pmu_event_sel`

Specifies the PMU event to be counted.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2000
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

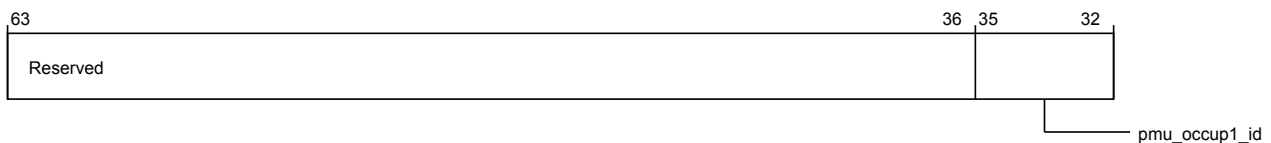


Figure 4-225 `por_dn_por_dn_pmu_event_sel` (high)

The following table shows the `por_dn_pmu_event_sel` higher register bit assignments.

Table 4-242 por_dn_por_dn_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:36	Reserved	Reserved	RO	-
35:32	pmu_occup1_id	PMU occupancy event selector ID 4'b0000: All 4'b0001: DVM ops 4'b0010: DVM syncs	RW	4'b0

The following image shows the lower register bit assignments.

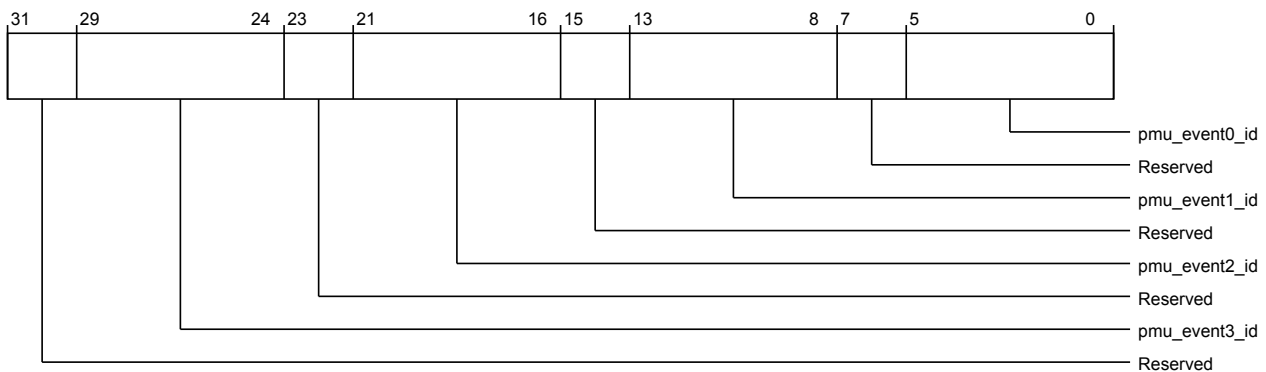


Figure 4-226 por_dn_por_dn_pmu_event_sel (low)

The following table shows the por_dn_pmu_event_sel lower register bit assignments.

Table 4-243 por_dn_por_dn_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	PMU Event 3 ID; see pmu_event0_id for encodings	RW	5'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	PMU Event 2 ID; see pmu_event0_id for encodings	RW	5'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	PMU Event 1 ID; see pmu_event0_id for encodings	RW	5'b0

Table 4-243 `por_dn_por_dn_pmu_event_sel` (low) (continued)

Bits	Field name	Description	Type	Reset
7:6	Reserved	Reserved	RO	-
5:0	<code>pmu_event0_id</code>	PMU Event 0 ID 6'h00: No event 6'h01: Number of TLBI DVM op requests 6'h02: Number of BPI DVM op requests 6'h03: Number of PICI DVM op requests 6'h04: Number of VICI DVM op requests 6'h05: Number of DVM sync requests 6'h06: Number of DVM op requests that were filtered using VMID filtering 6'h07: Number of DVM op requests to RNDs, BPI or PICI/VICI, that were filtered 6'h08: Number of retried REQ 6'h09: Number of SNPs sent to RNs 6'h0a: Number of SNPs stalled to RNs due to lack of Crds 6'h0b: DVM tracker full counter 6'h0c: DVM tracker occupancy counter	RW	5'b0

4.3.3 Debug and trace register descriptions

This section lists the debug and trace registers.

por_dt_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

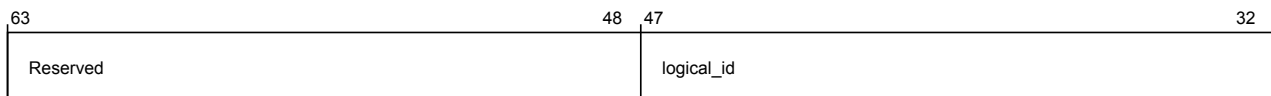


Figure 4-227 por_dt_por_dt_node_info (high)

The following table shows the por_dt_node_info higher register bit assignments.

Table 4-244 por_dt_por_dt_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

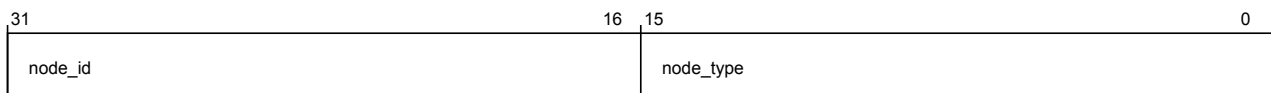


Figure 4-228 por_dt_por_dt_node_info (low)

The following table shows the por_dt_node_info lower register bit assignments.

Table 4-245 por_dt_por_dt_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h3

por_dt_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

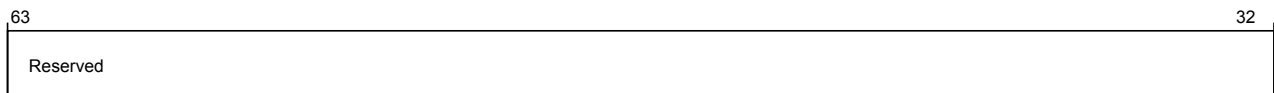


Figure 4-229 por_dt_por_dt_child_info (high)

The following table shows the por_dt_child_info higher register bit assignments.

Table 4-246 por_dt_por_dt_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

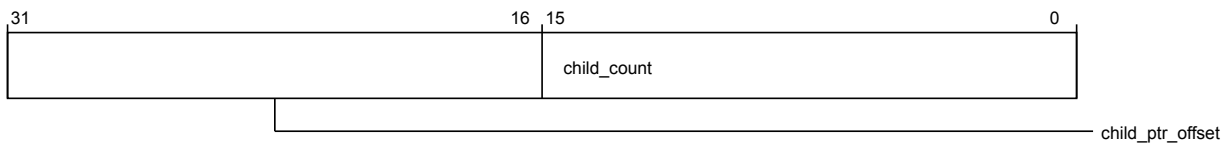


Figure 4-230 por_dt_por_dt_child_info (low)

The following table shows the por_dt_child_info lower register bit assignments.

Table 4-247 por_dt_por_dt_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0000
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_dt_secure_access

Functions as the secure access control register.

Its characteristics are:

Type	RW
Register width (Bits)	64

Address offset 14'h980
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-231 por_dt_secure_access (high)

The following table shows the por_dt_secure_access higher register bit assignments.

Table 4-248 por_dt_secure_access (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

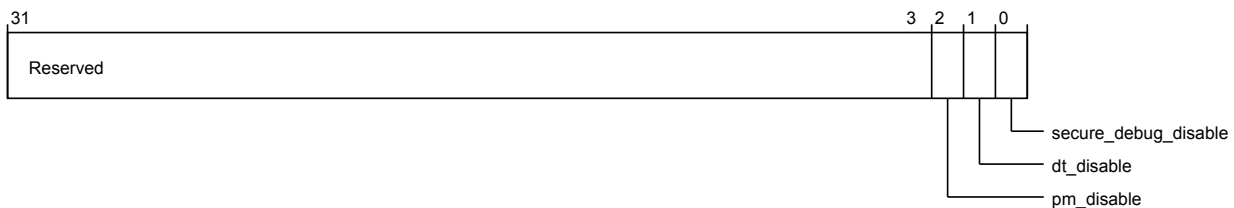


Figure 4-232 por_dt_secure_access (low)

The following table shows the por_dt_secure_access lower register bit assignments.

Table 4-249 por_dt_secure_access (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	pm_disable	PMU disable 1'b0: PMU function is not affected 1'b1: PMU function is disabled.	RW	1'b0
1	dt_disable	Debug disable 1'b0: DT function is not affected 1'b1: DT function is disabled.	RW	1'b0
0	secure_debug_disable	Secure debug disable 1'b0: Secure events are monitored by the PMU 1'b1: Secure events are only monitored by the PMU if SPNIDEN is set to 1	RW	1'b0

por_dt_dtc_ctl

Functions as the debug trace control register.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA00
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

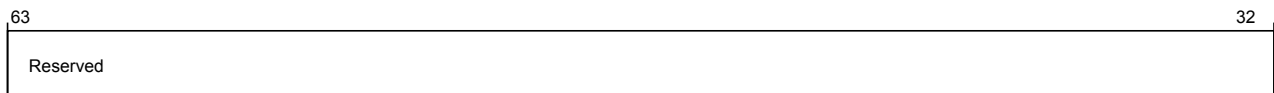


Figure 4-233 por_dt_por_dt_dtc_ctl (high)

The following table shows the por_dt_dtc_ctl higher register bit assignments.

Table 4-250 por_dt_por_dt_dtc_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

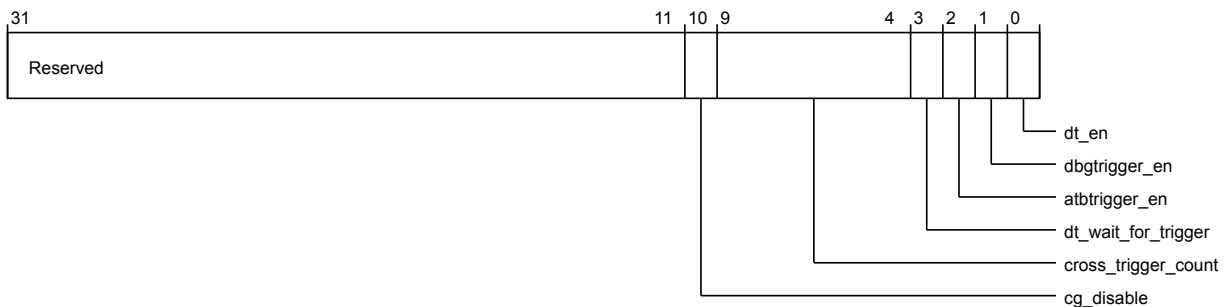


Figure 4-234 por_dt_por_dt_dtc_ctl (low)

The following table shows the por_dt_dtc_ctl lower register bit assignments.

Table 4-251 por_dt_por_dt_dtc_ctl (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10	cg_disable	Disables DT architectural clock gates	RW	1'b0
9:4	cross_trigger_count	Number of cross triggers received before trace enable NOTE: Only applicable if dt_wait_for_trigger is set to 1.	RW	6'b0

Table 4-251 por_dt_por_dt_dtc_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
3	dt_wait_for_trigger	Enables waiting for cross trigger before trace enable	RW	1'b0
2	atbtrigger_en	ATB trigger enable	RW	1'b0
1	dbgtrigger_en	DBGWATCHTRIG enable	RW	1'b0
0	dt_en	Enables debug, trace, and PMU features	RW	1'b0

por_dt_trigger_status

Provides the trigger status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'hA10
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

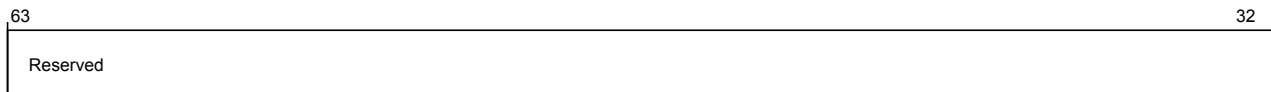


Figure 4-235 por_dt_por_dt_trigger_status (high)

The following table shows the por_dt_trigger_status higher register bit assignments.

Table 4-252 por_dt_por_dt_trigger_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

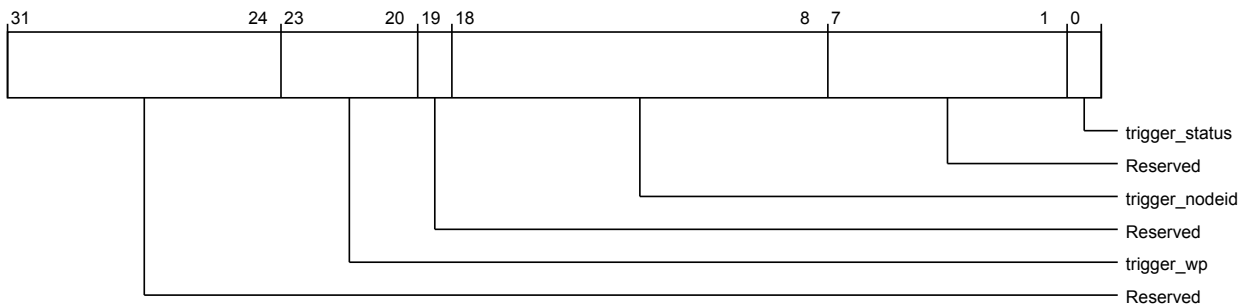


Figure 4-236 por_dt_por_dt_trigger_status (low)

The following table shows the por_dt_trigger_status lower register bit assignments.

Table 4-253 por_dt_por_dt_trigger_status (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	trigger_wp	DBGWATCHTRIGREQ assertion and/or ATB trigger are caused by watchpoint	RO	1'h0
19	Reserved	Reserved	RO	-
18:8	trigger_nodeid	DBGWATCHTRIGREQ assertion and/or ATB trigger are caused by node ID	RO	11'h0
7:1	Reserved	Reserved	RO	-
0	trigger_status	Indicates DBGWATCHTRIGREQ assertion and/or ATB trigger	RO	1'h0

por_dt_trigger_status_clr

Clears the trigger status.

Its characteristics are:

Type WO

Register width (Bits) 64

Address offset 14'hA20

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

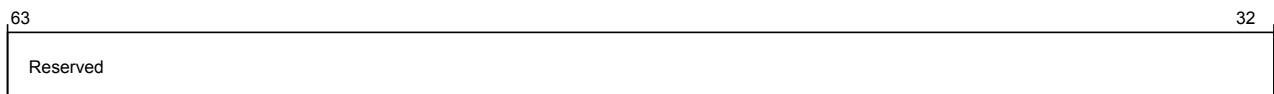


Figure 4-237 por_dt_por_dt_trigger_status_clr (high)

The following table shows the por_dt_trigger_status_clr higher register bit assignments.

Table 4-254 por_dt_por_dt_trigger_status_clr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

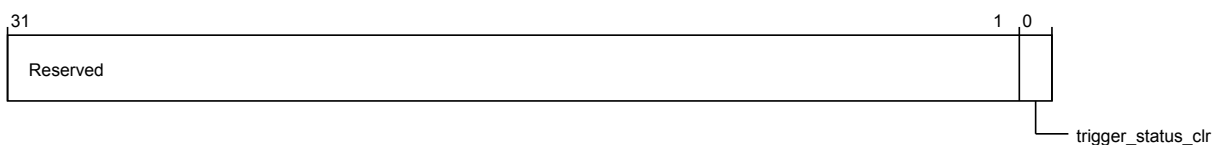


Figure 4-238 por_dt_por_dt_trigger_status_clr (low)

The following table shows the por_dt_trigger_status_clr lower register bit assignments.

Table 4-255 por_dt_por_dt_trigger_status_clr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	trigger_status_clr	Write a 1 to clear por_dt_trigger_status.trigger_status	WO	1'b0

por_dt_trace_control

Functions as the trace control register.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA30
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

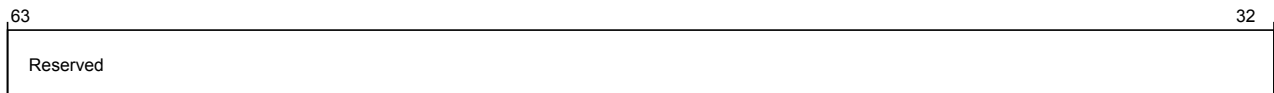


Figure 4-239 por_dt_por_dt_trace_control (high)

The following table shows the por_dt_trace_control higher register bit assignments.

Table 4-256 por_dt_por_dt_trace_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

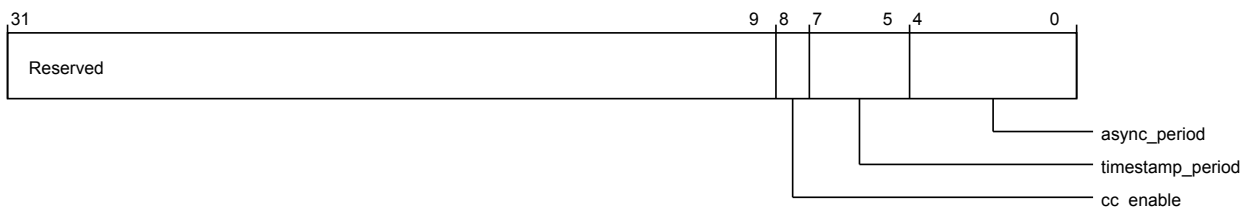


Figure 4-240 por_dt_por_dt_trace_control (low)

The following table shows the por_dt_trace_control lower register bit assignments.

Table 4-257 por_dt_por_dt_trace_control (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	cc_enable	Cycle count enable	RW	1'b0
7:5	timestamp_period	Time stamp packet insertion period 3'b000: Time stamp disabled 3'b011: Time stamp every 8K clock cycles 3'b100: Time stamp every 16K clock cycles 3'b101: Time stamp every 32K clock cycles 3'b110: Time stamp every 64K clock cycles	RW	3'b0
4:0	async_period	Alignment sync packet insertion period 5'h00: Alignment sync disabled 5'h08: Alignment sync inserted after 256B of trace 5'h09: Alignment sync inserted after 512B of trace 5'h14: Alignment sync inserted after 1048576B of trace NOTE: All other values are reserved.	RW	5'b0

por_dt_traceid

Contains the ATB ID.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA48
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

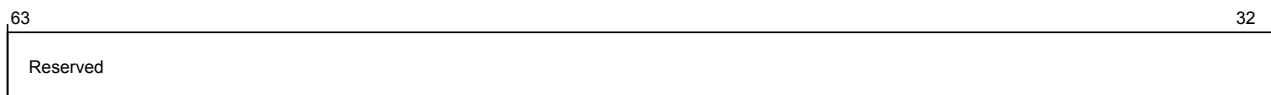


Figure 4-241 por_dt_por_dt_traceid (high)

The following table shows the por_dt_traceid higher register bit assignments.

Table 4-258 por_dt_por_dt_traceid (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

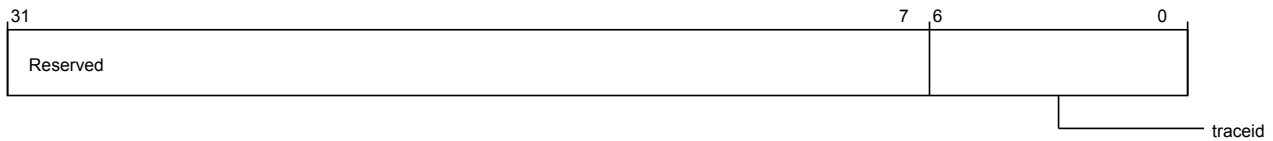


Figure 4-242 por_dt_por_dt_traceid (low)

The following table shows the por_dt_traceid lower register bit assignments.

Table 4-259 por_dt_por_dt_traceid (low)

Bits	Field name	Description	Type	Reset
31:7	Reserved	Reserved	RO	-
6:0	traceid	ATB ID	RW	7'h0

por_dt_pmevcntAB

Contains the PMU event counters A and B.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2000
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

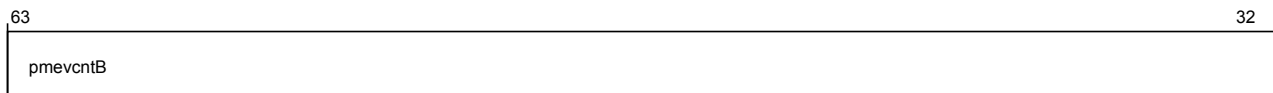


Figure 4-243 por_dt_por_dt_pmevcntab (high)

The following table shows the por_dt_pmevcntAB higher register bit assignments.

Table 4-260 por_dt_por_dt_pmevcntab (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntB	PMU counter B	RW	32'h0000

The following image shows the lower register bit assignments.

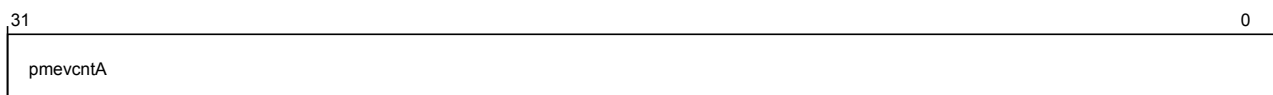


Figure 4-244 por_dt_por_dt_pmevcntab (low)

The following table shows the por_dt_pmevntAB lower register bit assignments.

Table 4-261 por_dt_por_dt_pmevntab (low)

Bits	Field name	Description	Type	Reset
31:0	pmevntA	PMU counter A	RW	32'h0000

por_dt_pmevntCD

Contains the PMU event counters C and D.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2010
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

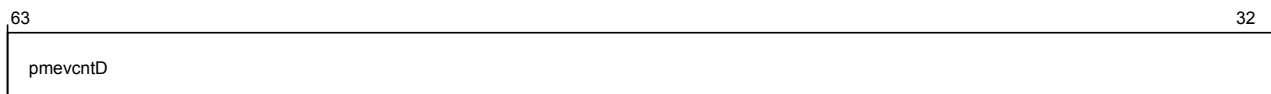


Figure 4-245 por_dt_por_dt_pmevntcd (high)

The following table shows the por_dt_pmevntCD higher register bit assignments.

Table 4-262 por_dt_por_dt_pmevntcd (high)

Bits	Field name	Description	Type	Reset
63:32	pmevntD	PMU counter D	RW	32'h0000

The following image shows the lower register bit assignments.

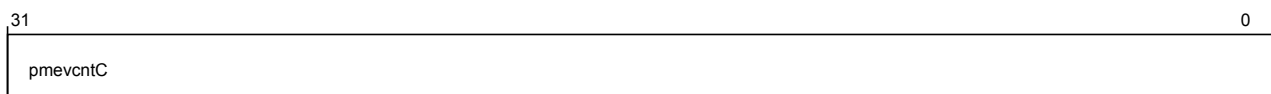


Figure 4-246 por_dt_por_dt_pmevntcd (low)

The following table shows the por_dt_pmevntCD lower register bit assignments.

Table 4-263 por_dt_por_dt_pmevntcd (low)

Bits	Field name	Description	Type	Reset
31:0	pmevntC	PMU counter C	RW	32'h0000

por_dt_pmevntEF

Contains the PMU event counters E and F.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2020
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

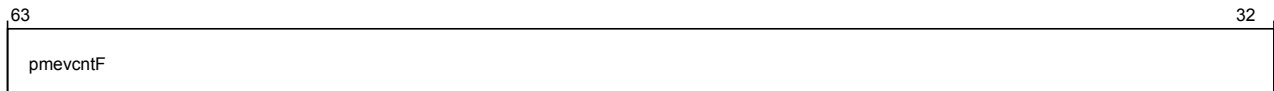


Figure 4-247 por_dt_por_dt_pmevcntef (high)

The following table shows the por_dt_pmevcntEF higher register bit assignments.

Table 4-264 por_dt_por_dt_pmevcntef (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntF	PMU counter F	RW	32'h0000

The following image shows the lower register bit assignments.

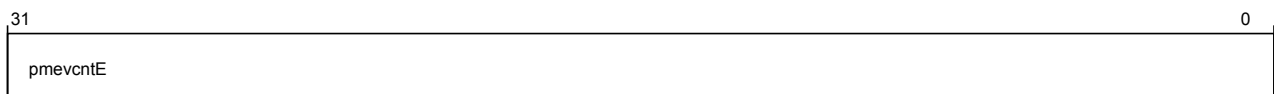


Figure 4-248 por_dt_por_dt_pmevcntef (low)

The following table shows the por_dt_pmevcntEF lower register bit assignments.

Table 4-265 por_dt_por_dt_pmevcntef (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntE	PMU counter E	RW	32'h0000

por_dt_pmevcntGH

Contains the PMU event counters G and H.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2030
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

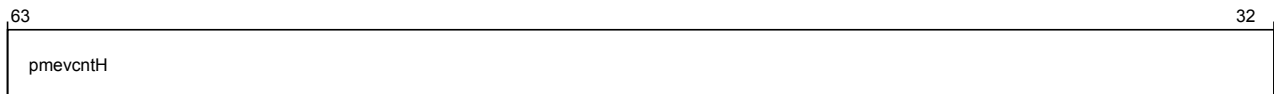


Figure 4-249 `por_dt_por_dt_pmevcntgh` (high)

The following table shows the `por_dt_pmevcntGH` higher register bit assignments.

Table 4-266 `por_dt_por_dt_pmevcntgh` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>pmecntH</code>	PMU counter H	RW	32'h0000

The following image shows the lower register bit assignments.



Figure 4-250 `por_dt_por_dt_pmevcntgh` (low)

The following table shows the `por_dt_pmevcntGH` lower register bit assignments.

Table 4-267 `por_dt_por_dt_pmevcntgh` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>pmecntG</code>	PMU counter G	RW	32'h0000

`por_dt_pmccntr`

Contains the PMU cycle counter.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2040
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

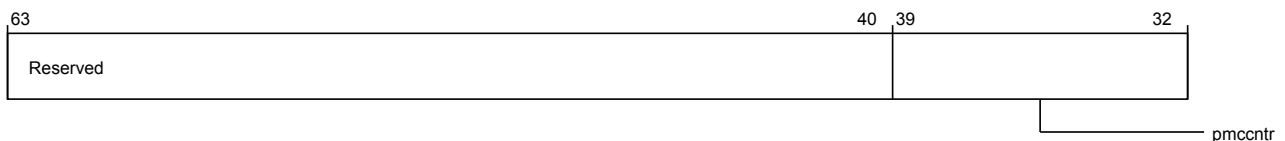


Figure 4-251 `por_dt_por_dt_pmccntr` (high)

The following table shows the `por_dt_pmccntr` higher register bit assignments.

Table 4-268 `por_dt_por_dt_pmcctr` (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	<code>pmcctr</code>	PMU cycle counter	RW	40'h0

The following image shows the lower register bit assignments.

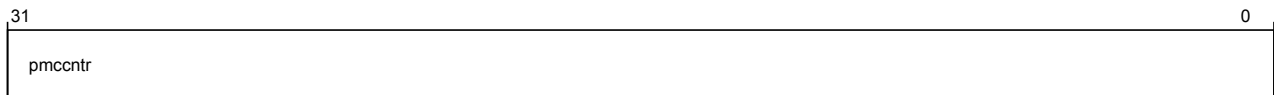


Figure 4-252 `por_dt_por_dt_pmcctr` (low)

The following table shows the `por_dt_pmcctr` lower register bit assignments.

Table 4-269 `por_dt_por_dt_pmcctr` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>pmcctr</code>	PMU cycle counter	RW	40'h0

`por_dt_pmevntsrAB`

Contains the PMU event counter shadow registers A and B.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2050
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

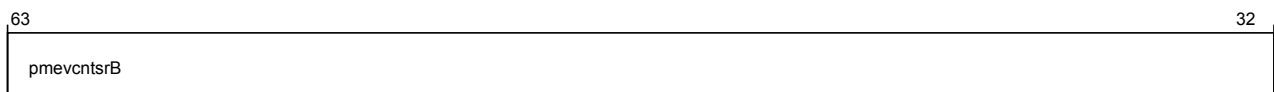


Figure 4-253 `por_dt_por_dt_pmevntsrab` (high)

The following table shows the `por_dt_pmevntsrAB` higher register bit assignments.

Table 4-270 `por_dt_por_dt_pmevntsrab` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>pmevntsrB</code>	PMU counter B shadow register	RW	32'h0000

The following image shows the lower register bit assignments.

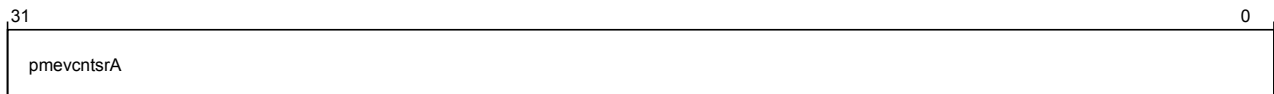


Figure 4-254 por_dt_por_dt_pmevcntsrab (low)

The following table shows the por_dt_pmevcntsrAB lower register bit assignments.

Table 4-271 por_dt_por_dt_pmevcntsrab (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntsrA	PMU counter A shadow register	RW	32'h0000

por_dt_pmevcntsrCD

Contains the PMU event counter shadow registers C and D.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2060
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

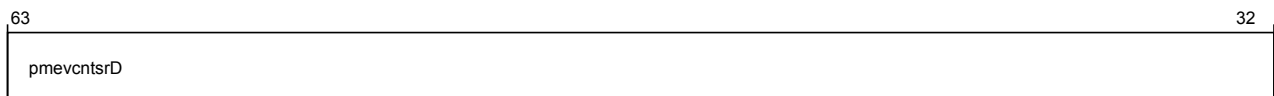


Figure 4-255 por_dt_por_dt_pmevcntsracd (high)

The following table shows the por_dt_pmevcntsrCD higher register bit assignments.

Table 4-272 por_dt_por_dt_pmevcntsracd (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntsrD	PMU counter D shadow register	RW	32'h0000

The following image shows the lower register bit assignments.

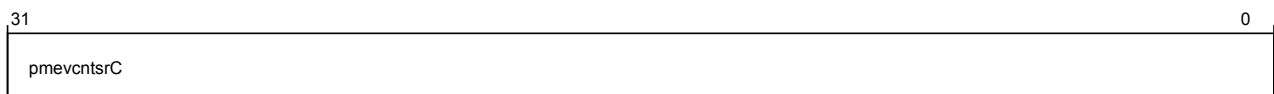


Figure 4-256 por_dt_por_dt_pmevcntsracd (low)

The following table shows the por_dt_pmevcntsrCD lower register bit assignments.

Table 4-273 por_dt_por_dt_pmevntsrC (low)

Bits	Field name	Description	Type	Reset
31:0	pmevntsrC	PMU counter C shadow register	RW	32'h0000

por_dt_pmevntsrEF

Contains the PMU event counter shadow registers E and F.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2070
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

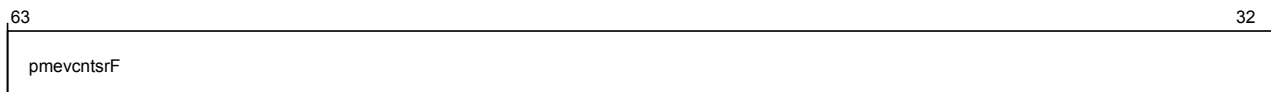


Figure 4-257 por_dt_por_dt_pmevntsrEF (high)

The following table shows the por_dt_pmevntsrEF higher register bit assignments.

Table 4-274 por_dt_por_dt_pmevntsrF (high)

Bits	Field name	Description	Type	Reset
63:32	pmevntsrF	PMU counter F shadow register	RW	32'h0000

The following image shows the lower register bit assignments.

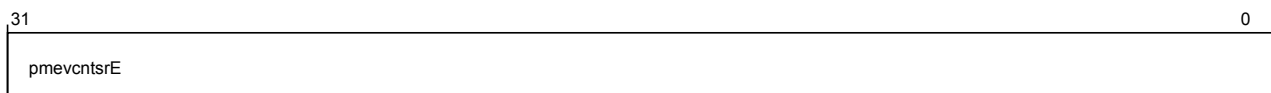


Figure 4-258 por_dt_por_dt_pmevntsrEF (low)

The following table shows the por_dt_pmevntsrEF lower register bit assignments.

Table 4-275 por_dt_por_dt_pmevntsrE (low)

Bits	Field name	Description	Type	Reset
31:0	pmevntsrE	PMU counter E shadow register	RW	32'h0000

por_dt_pmevntsrGH

Contains the PMU event counter shadow registers G and H.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2080
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-259 por_dt_por_dt_pmevcntrgh (high)

The following table shows the por_dt_pmevcntrGH higher register bit assignments.

Table 4-276 por_dt_por_dt_pmevcntrgh (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntrH	PMU counter H shadow register	RW	32'h0000

The following image shows the lower register bit assignments.



Figure 4-260 por_dt_por_dt_pmevcntrgh (low)

The following table shows the por_dt_pmevcntrGH lower register bit assignments.

Table 4-277 por_dt_por_dt_pmevcntrgh (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntrG	PMU counter G shadow register	RW	32'h0000

por_dt_pmccntrsr

Contains the PMU cycle counter shadow register.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2090
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

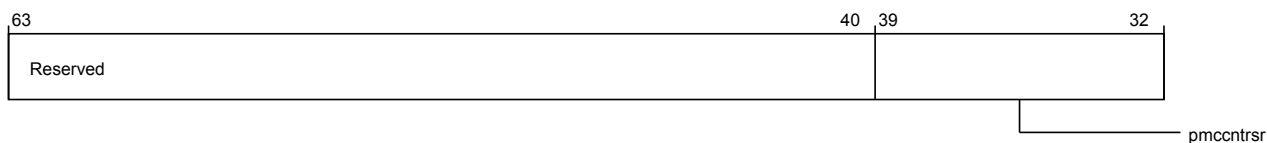


Figure 4-261 por_dt_por_dt_pmccntrsr (high)

The following table shows the por_dt_pmccntrsr higher register bit assignments.

Table 4-278 por_dt_por_dt_pmccntrsr (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pmccntrsr	PMU cycle counter shadow register	RW	40'h0

The following image shows the lower register bit assignments.

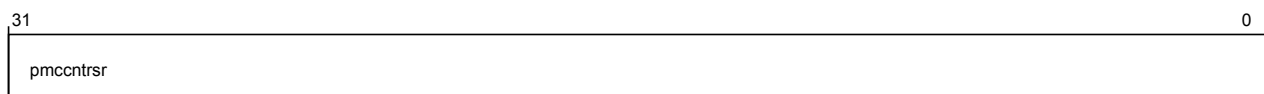


Figure 4-262 por_dt_por_dt_pmccntrsr (low)

The following table shows the por_dt_pmccntrsr lower register bit assignments.

Table 4-279 por_dt_por_dt_pmccntrsr (low)

Bits	Field name	Description	Type	Reset
31:0	pmccntrsr	PMU cycle counter shadow register	RW	40'h0

por_dt_pmcr

Functions as the PMU control register.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2100
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

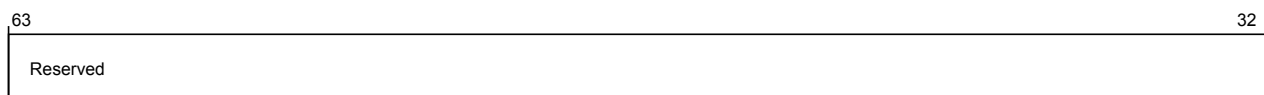


Figure 4-263 por_dt_por_dt_pmcr (high)

The following table shows the por_dt_pmc_r higher register bit assignments.

Table 4-280 por_dt_por_dt_pmc_r (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

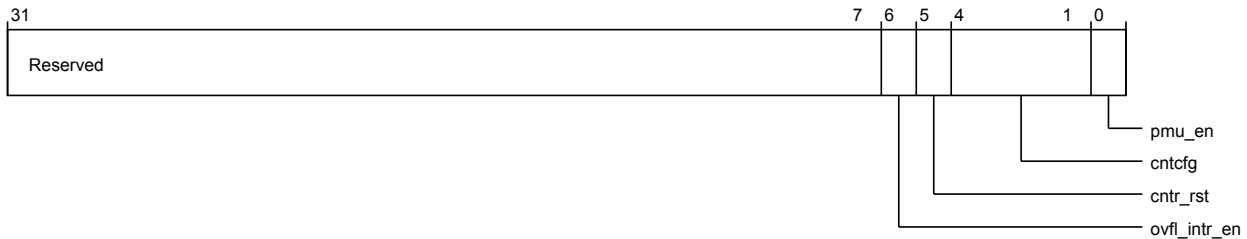


Figure 4-264 por_dt_por_dt_pmc_r (low)

The following table shows the por_dt_pmc_r lower register bit assignments.

Table 4-281 por_dt_por_dt_pmc_r (low)

Bits	Field name	Description	Type	Reset
31:7	Reserved	Reserved	RO	-
6	ovfl_intr_en	Enables INTREQPMU assertion on PMU counter overflow	RW	1'h0
5	cntr_rst	Enables clearing of live counters upon assertion of por_dt_pmsrr.ss_req or PMUSNAPSHOTREQ	RW	1'h0
4:1	cntcfg	Groups adjacent 32-bit registers into a 64-bit register	RW	4'h0
0	pmu_en	Enables PMU features	RW	1'b0

por_dt_pmovsr

Provides the PMU overflow status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2118
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

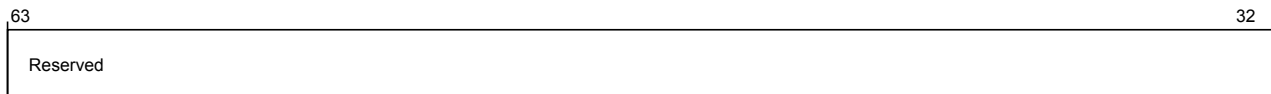


Figure 4-265 por_dt_por_dt_pmovsr (high)

The following table shows the por_dt_pmovsr higher register bit assignments.

Table 4-282 por_dt_por_dt_pmovsr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

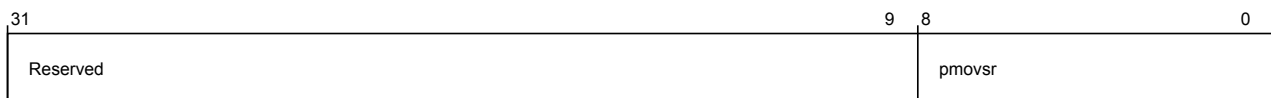


Figure 4-266 por_dt_por_dt_pmovsr (low)

The following table shows the por_dt_pmovsr lower register bit assignments.

Table 4-283 por_dt_por_dt_pmovsr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8:0	pmovsr	PMU overflow status Bit 8: Indicates overflow from cycle counter Bits [7:0]: Indicates overflow from counters 7 to 0	RO	9'h0

por_dt_pmovsr_clr

Clears the PMU overflow status.

Its characteristics are:

Type WO

Register width (Bits) 64

Address offset 14'h2120

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

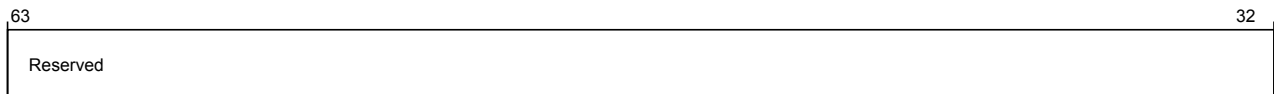


Figure 4-267 por_dt_por_dt_pmovsr_clr (high)

The following table shows the por_dt_pmovsr_clr higher register bit assignments.

Table 4-284 por_dt_por_dt_pmovsr_clr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

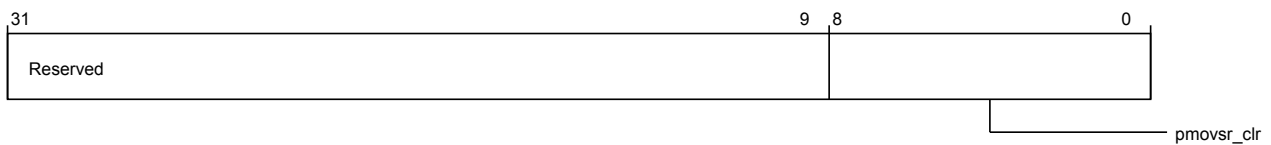


Figure 4-268 por_dt_por_dt_pmovsr_clr (low)

The following table shows the por_dt_pmovsr_clr lower register bit assignments.

Table 4-285 por_dt_por_dt_pmovsr_clr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8:0	pmovsr_clr	Write a 1 to clear the corresponding bit in por_dt_pmovsr.pmovsr	WO	9'b0

por_dt_pmssr

Provides the PMU snapshot status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2128
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

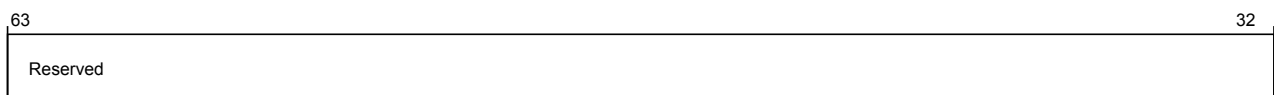


Figure 4-269 por_dt_por_dt_pmssr (high)

The following table shows the por_dt_pmsrr higher register bit assignments.

Table 4-286 por_dt_por_dt_pmsrr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

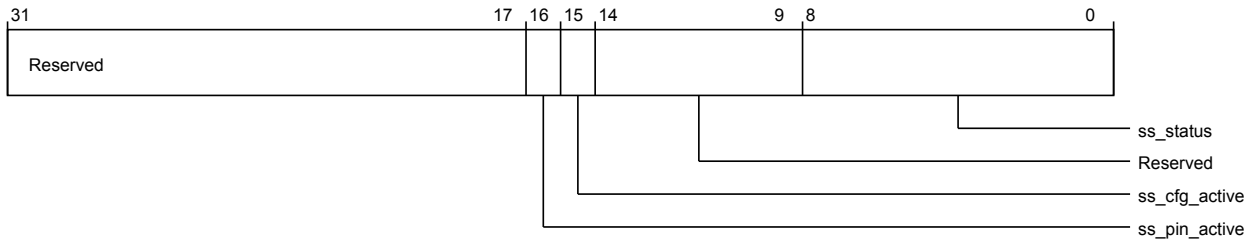


Figure 4-270 por_dt_por_dt_pmsrr (low)

The following table shows the por_dt_pmsrr lower register bit assignments.

Table 4-287 por_dt_por_dt_pmsrr (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	ss_pin_active	Activates PMU snapshot from PMUSNAPSHOTREQ	RO	1'b0
15	ss_cfg_active	PMU snapshot activated from configuration write	RO	1'b0
14:9	Reserved	Reserved	RO	-
8:0	ss_status	PMU snapshot status Bit 8: Indicates snapshot status for cycle counter Bits [7:0]: Indicates snapshot status for counters 7 to 0	RO	9'b0

por_dt_pmsrr

Sends PMU snapshot requests.

Its characteristics are:

Type	WO
Register width (Bits)	64
Address offset	14'h2130
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

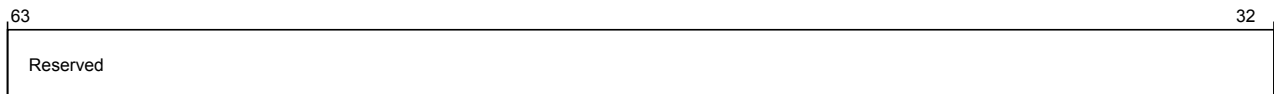


Figure 4-271 por_dt_por_dt_pmsrr (high)

The following table shows the por_dt_pmsrr higher register bit assignments.

Table 4-288 por_dt_por_dt_pmsrr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

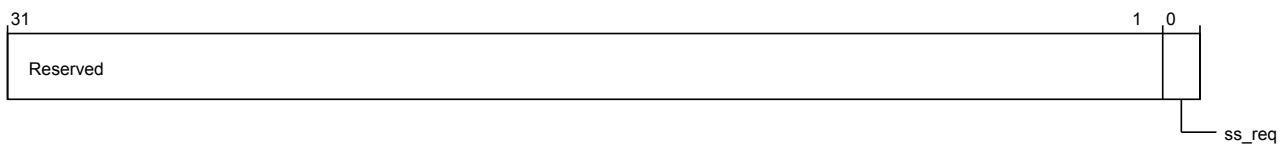


Figure 4-272 por_dt_por_dt_pmsrr (low)

The following table shows the por_dt_pmsrr lower register bit assignments.

Table 4-289 por_dt_por_dt_pmsrr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	ss_req	Write a 1 to request PMU snapshot	WO	1'b0

por_dt_claim

Functions as the claim tag set register.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2DA0
Register reset	64'b01111111111111111111111111111111
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

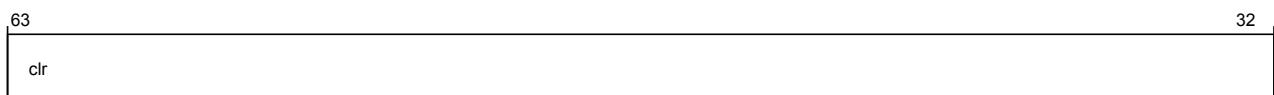


Figure 4-273 por_dt_por_dt_claim (high)

The following table shows the por_dt_claim higher register bit assignments.

Table 4-290 por_dt_por_dt_claim (high)

Bits	Field name	Description	Type	Reset
63:32	clr	Upper half of the claim tag value; enables individual bits to be cleared (write) and returns the current claim tag value (read)	RW	32'b0

The following image shows the lower register bit assignments.

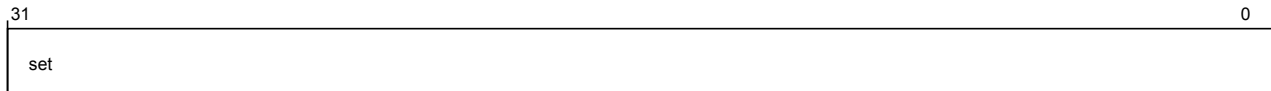


Figure 4-274 por_dt_por_dt_claim (low)

The following table shows the por_dt_claim lower register bit assignments.

Table 4-291 por_dt_por_dt_claim (low)

Bits	Field name	Description	Type	Reset
31:0	set	Lower half of the claim tag value; allows individual bits to be set (write) and returns the number of bits that can be set (read)	RW	32'hfffffff

por_dt_devaff

Functions as the device affinity register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DA8
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

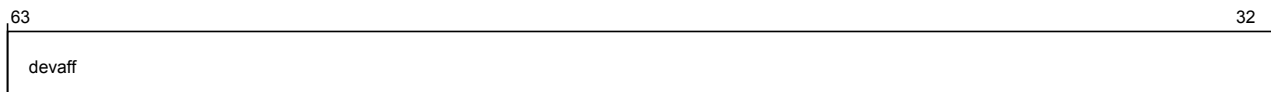


Figure 4-275 por_dt_por_dt_devaff (high)

The following table shows the por_dt_devaff higher register bit assignments.

Table 4-292 por_dt_por_dt_devaff (high)

Bits	Field name	Description	Type	Reset
63:32	devaff	Device affinity register	RO	64'b0

The following image shows the lower register bit assignments.



Figure 4-276 por_dt_por_dt_devaff (low)

The following table shows the por_dt_devaff lower register bit assignments.

Table 4-293 por_dt_por_dt_devaff (low)

Bits	Field name	Description	Type	Reset
31:0	devaff	Device affinity register	RO	64'b0

por_dt_lsr

Functions as the lock status register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DB0
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

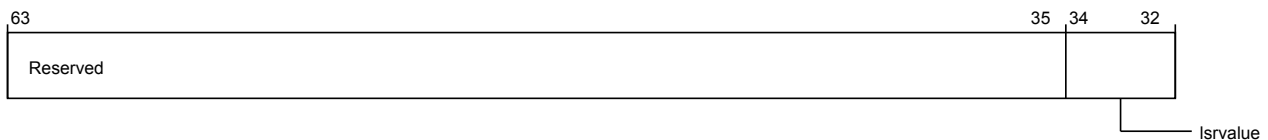


Figure 4-277 por_dt_por_dt_lsr (high)

The following table shows the por_dt_lsr higher register bit assignments.

Table 4-294 por_dt_por_dt_lsr (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	lsrvalue	Lock status value	RO	3'b0

The following image shows the lower register bit assignments.

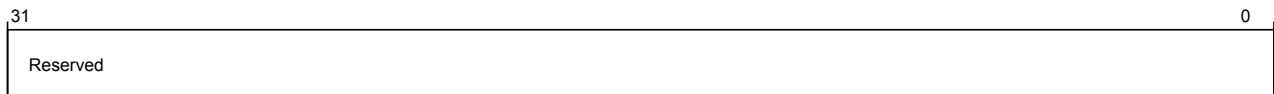


Figure 4-278 por_dt_por_dt_lsr (low)

The following table shows the por_dt_lsr lower register bit assignments.

Table 4-295 por_dt_por_dt_lsr (low)

Bits	Field name	Description	Type	Reset
31:0	Reserved	Reserved	RO	-

por_dt_authstatus_devarch

Functions as the authentication status register and the device architecture register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DB8
Register reset	64'b01001010
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

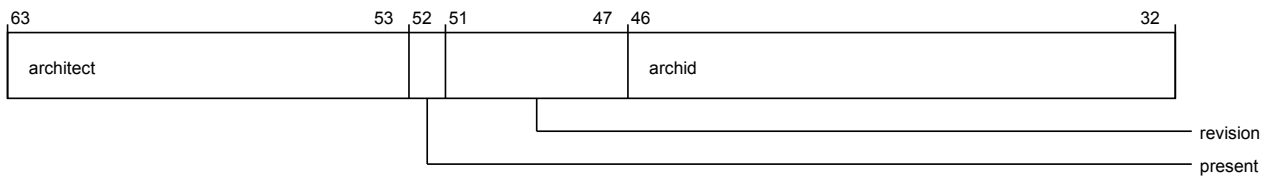


Figure 4-279 por_dt_por_dt_authstatus_devarch (high)

The following table shows the por_dt_authstatus_devarch higher register bit assignments.

Table 4-296 por_dt_por_dt_authstatus_devarch (high)

Bits	Field name	Description	Type	Reset
63:53	architect	Architect	RO	11'b0
52	present	Present	RO	1'b1
51:47	revision	Architecture revision	RO	6'b0
46:32	archid	Architecture ID	RO	16'b0

The following image shows the lower register bit assignments.

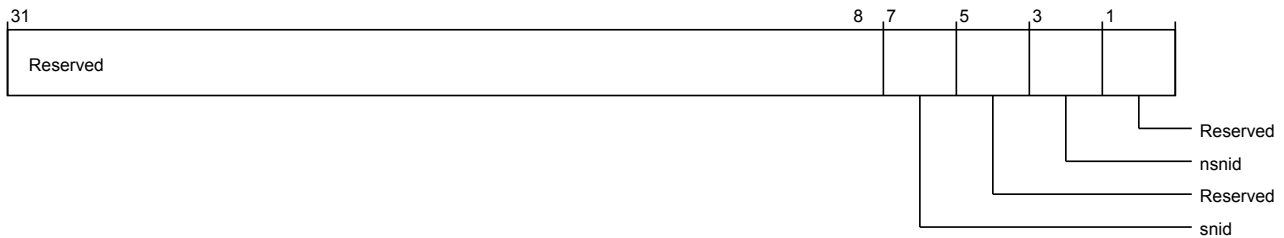


Figure 4-280 por_dt_por_dt_authstatus_devarch (low)

The following table shows the por_dt_authstatus_devarch lower register bit assignments.

Table 4-297 por_dt_por_dt_authstatus_devarch (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	snid	Secure non-invasive debug	RO	2'b10
5:4	Reserved	Reserved	RO	-
3:2	nsnid	Non-secure non-invasive debug	RO	2'b10
1:0	Reserved	Reserved	RO	-

por_dt_devid

Functions as the device configuration register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DC0
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

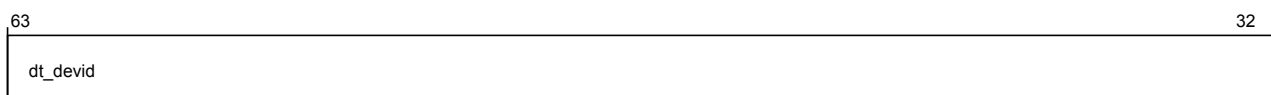


Figure 4-281 por_dt_por_dt_devid (high)

The following table shows the por_dt_devid higher register bit assignments.

Table 4-298 por_dt_por_dt_devid (high)

Bits	Field name	Description	Type	Reset
63:32	dt_devid	Device ID	RO	64'b0

The following image shows the lower register bit assignments.



Figure 4-282 por_dt_por_dt_devid (low)

The following table shows the por_dt_devid lower register bit assignments.

Table 4-299 por_dt_por_dt_devid (low)

Bits	Field name	Description	Type	Reset
31:0	dt_devid	Device ID	RO	64'b0

por_dt_devtype

Functions as the device type identifier register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DC8
Register reset	64'b01000011
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

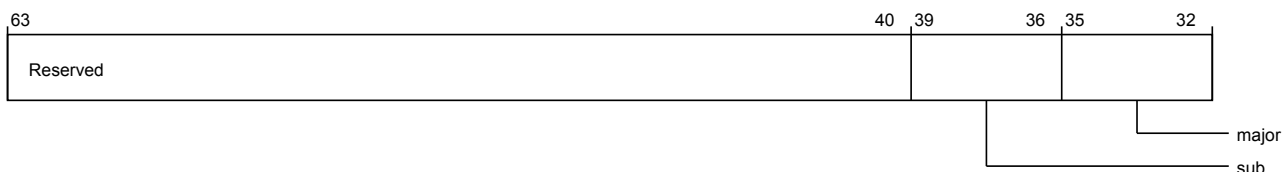


Figure 4-283 por_dt_por_dt_devtype (high)

The following table shows the por_dt_devtype higher register bit assignments.

Table 4-300 por_dt_por_dt_devtype (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:36	sub	Sub type	RO	4'h4
35:32	major	Major type	RO	4'h3

The following image shows the lower register bit assignments.

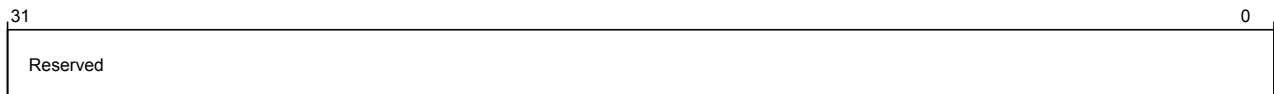


Figure 4-284 por_dt_por_dt_devtype (low)

The following table shows the por_dt_devtype lower register bit assignments.

Table 4-301 por_dt_por_dt_devtype (low)

Bits	Field name	Description	Type	Reset
31:0	Reserved	Reserved	RO	-

por_dt_pidr45

Functions as the identification register for peripheral ID 4 and peripheral ID 5.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DD0
Register reset	64'b000000100
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

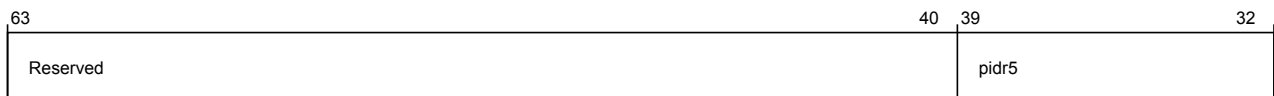


Figure 4-285 por_dt_por_dt_pidr45 (high)

The following table shows the por_dt_pidr45 higher register bit assignments.

Table 4-302 por_dt_por_dt_pidr45 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr5	Peripheral ID 5	RO	8'b0

The following image shows the lower register bit assignments.

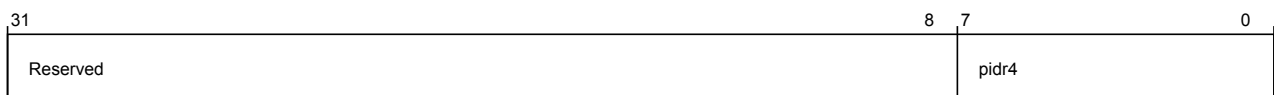


Figure 4-286 por_dt_por_dt_pidr45 (low)

The following table shows the por_dt_pidr45 lower register bit assignments.

Table 4-303 por_dt_por_dt_pidr45 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr4	Peripheral ID 4	RO	8'h4

por_dt_pidr67

Functions as the identification register for peripheral ID 6 and peripheral ID 7.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DD8
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

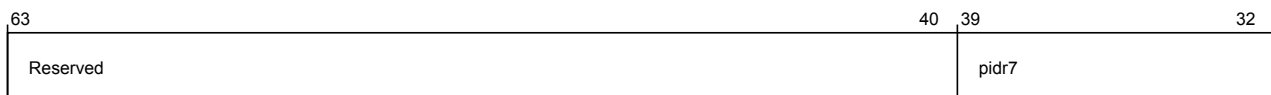


Figure 4-287 por_dt_por_dt_pidr67 (high)

The following table shows the por_dt_pidr67 higher register bit assignments.

Table 4-304 por_dt_por_dt_pidr67 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr7	Peripheral ID 7	RO	8'b0

The following image shows the lower register bit assignments.

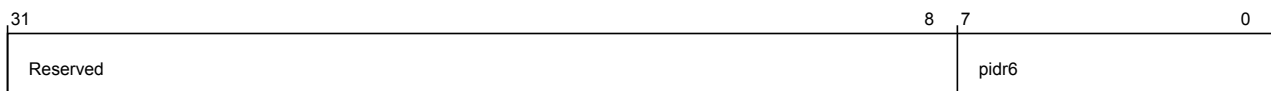


Figure 4-288 por_dt_por_dt_pidr67 (low)

The following table shows the por_dt_pidr67 lower register bit assignments.

Table 4-305 por_dt_por_dt_pidr67 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr6	Peripheral ID 6	RO	8'b0

por_dt_pidr01

Functions as the identification register for peripheral ID 0 and peripheral ID 1.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DE0
Register reset	64'b0101110000011100
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-289 por_dt_por_dt_pidr01 (high)

The following table shows the por_dt_pidr01 higher register bit assignments.

Table 4-306 por_dt_por_dt_pidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr1	Peripheral ID 1	RO	8'hb4

The following image shows the lower register bit assignments.

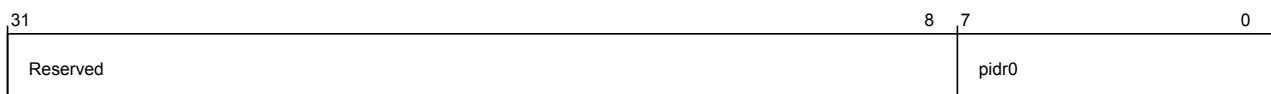


Figure 4-290 por_dt_por_dt_pidr01 (low)

The following table shows the por_dt_pidr01 lower register bit assignments.

Table 4-307 por_dt_por_dt_pidr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr0	Peripheral ID 0	RO	8'h34

por_dt_pidr23

Functions as the identification register for peripheral ID 2 and peripheral ID 3.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DE8
Register reset	64'b000000111
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-291 por_dt_por_dt_pidr23 (high)

The following table shows the por_dt_pidr23 higher register bit assignments.

Table 4-308 por_dt_por_dt_pidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr3	Peripheral ID 3	RO	8'b0

The following image shows the lower register bit assignments.

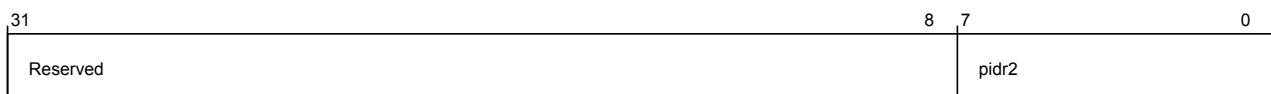


Figure 4-292 por_dt_por_dt_pidr23 (low)

The following table shows the por_dt_pidr23 lower register bit assignments.

Table 4-309 por_dt_por_dt_pidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr2	Peripheral ID 2	RO	8'h7

por_dt_cidr01

Functions as the identification register for component ID 0 and component ID 1.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DF0
Register reset	64'b1001111100001101
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

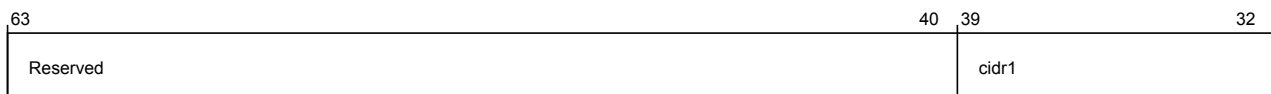


Figure 4-293 por_dt_por_dt_cidr01 (high)

The following table shows the por_dt_cidr01 higher register bit assignments.

Table 4-310 por_dt_por_dt_cidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	cidr1	Component ID 1	RO	8'h9f

The following image shows the lower register bit assignments.

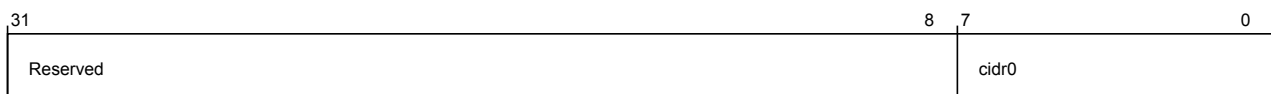


Figure 4-294 por_dt_por_dt_cidr01 (low)

The following table shows the por_dt_cidr01 lower register bit assignments.

Table 4-311 `por_dt_por_dt_cidr01` (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	<code>cidr0</code>	Component ID 0	RO	8'hd

`por_dt_cidr23`

Functions as the identification register for component ID 2 and component ID 3.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2DF8
Register reset	64'b0001011100000101
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

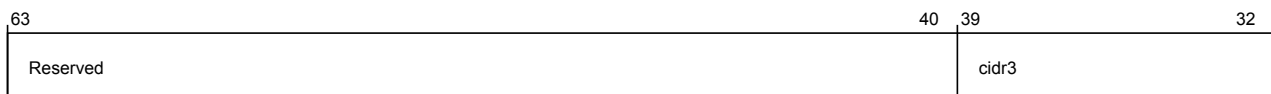


Figure 4-295 `por_dt_por_dt_cidr23` (high)

The following table shows the `por_dt_cidr23` higher register bit assignments.

Table 4-312 `por_dt_por_dt_cidr23` (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	<code>cidr3</code>	Component ID 3	RO	8'hb1

The following image shows the lower register bit assignments.

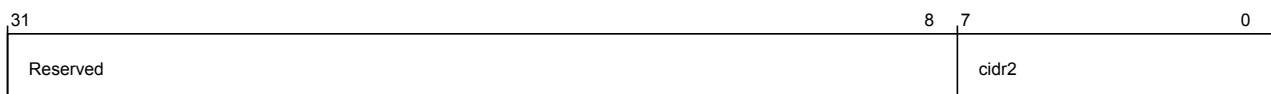


Figure 4-296 `por_dt_por_dt_cidr23` (low)

The following table shows the `por_dt_cidr23` lower register bit assignments.

Table 4-313 por_dt_por_dt_cidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr2	Component ID 2	RO	8'h5

4.3.4 HN-F register descriptions

Lists the HN-F registers.

por_hnf_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

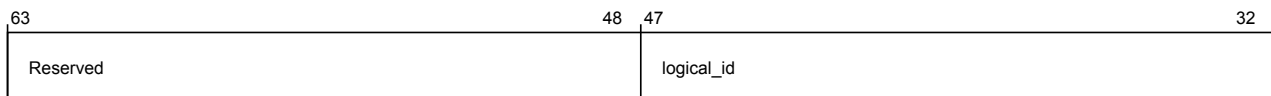


Figure 4-297 por_hnf_por_hnf_node_info (high)

The following table shows the por_hnf_node_info higher register bit assignments.

Table 4-314 por_hnf_por_hnf_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

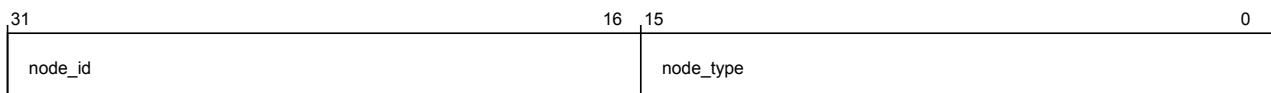


Figure 4-298 por_hnf_por_hnf_node_info (low)

The following table shows the por_hnf_node_info lower register bit assignments.

Table 4-315 por_hnf_por_hnf_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0005

por_hnf_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

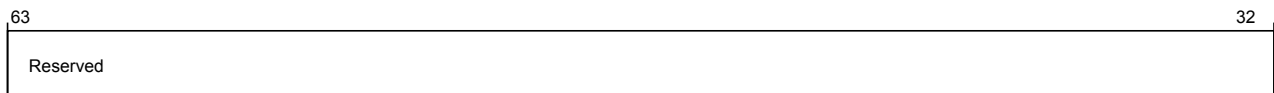


Figure 4-299 por_hnf_por_hnf_child_info (high)

The following table shows the por_hnf_child_info higher register bit assignments.

Table 4-316 por_hnf_por_hnf_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

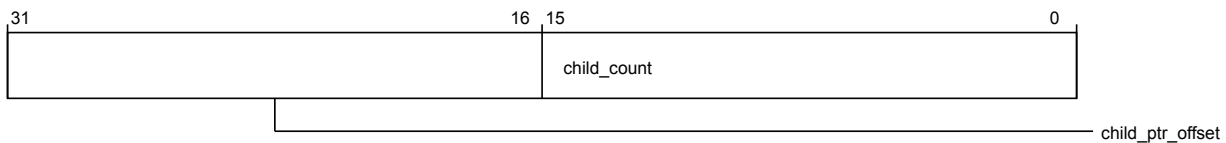


Figure 4-300 por_hnf_por_hnf_child_info (low)

The following table shows the por_hnf_child_info lower register bit assignments.

Table 4-317 por_hnf_por_hnf_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_hnf_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type	RW
Register width (Bits)	64

Address offset	14'h980
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

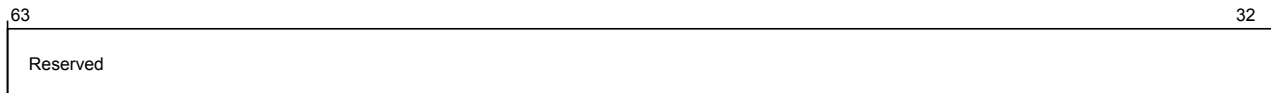


Figure 4-301 por_hnf_por_hnf_secure_register_groups_override (high)

The following table shows the por_hnf_secure_register_groups_override higher register bit assignments.

Table 4-318 por_hnf_por_hnf_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

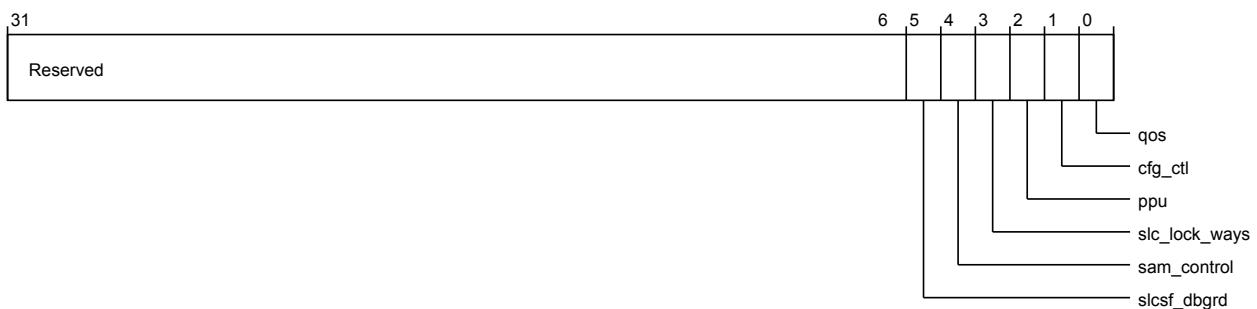


Figure 4-302 por_hnf_por_hnf_secure_register_groups_override (low)

The following table shows the por_hnf_secure_register_groups_override lower register bit assignments.

Table 4-319 por_hnf_por_hnf_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5	slcsf_dbgdr	Allows non-secure access to secure SLC/SF debug read registers	RW	1'b0
4	sam_control	Allows non-secure access to secure HN-F SAM control registers	RW	1'b0
3	slc_lock_ways	Allows non-secure access to secure cache way locking registers	RW	1'b0
2	ppu	Allows non-secure access to secure power policy registers	RW	1'b0
1	cfg_ctl	Allows non-secure access to secure configuration control register (por_hnf_cfg_ctl)	RW	1'b0
0	qos	Allows non-secure access to secure QoS registers	RW	1'b0

por_hnf_unit_info

Provides component identification information for HN-F.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h900
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

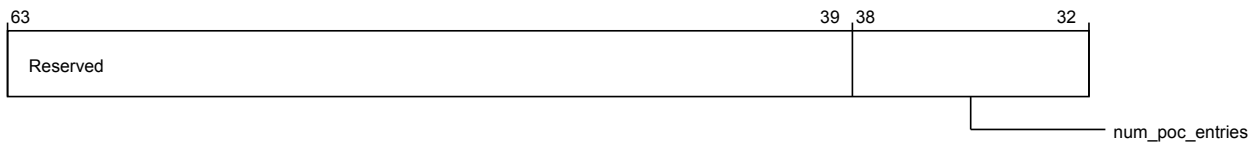


Figure 4-303 por_hnf_por_hnf_unit_info (high)

The following table shows the por_hnf_unit_info higher register bit assignments.

Table 4-320 por_hnf_por_hnf_unit_info (high)

Bits	Field name	Description	Type	Reset
63:39	Reserved	Reserved	RO	-
38:32	num_poc_entries	Number of POCQ entries	RO	Configuration dependent

The following image shows the lower register bit assignments.

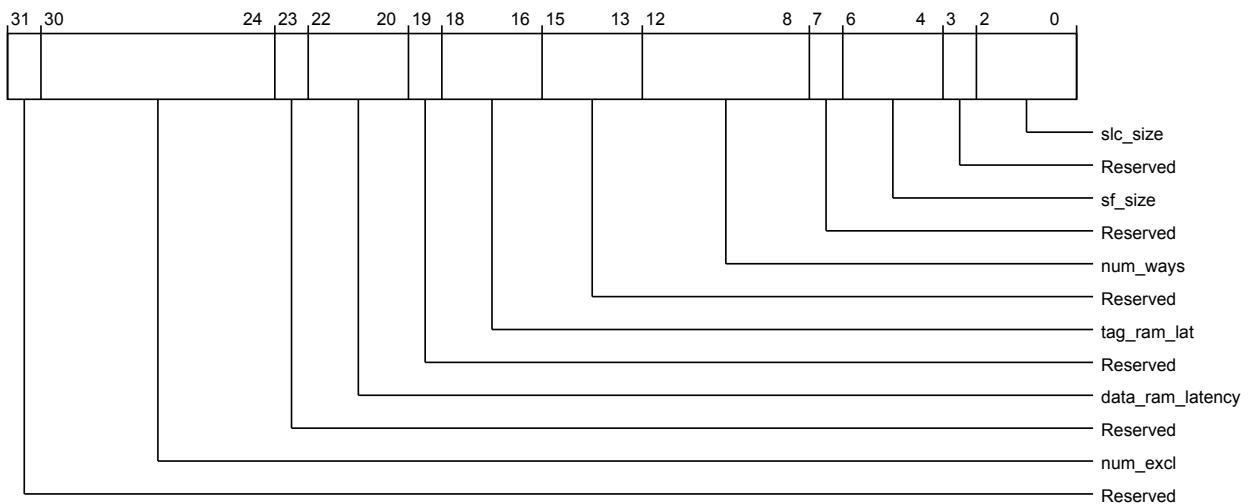


Figure 4-304 por_hnf_por_hnf_unit_info (low)

The following table shows the por_hnf_unit_info lower register bit assignments.

Table 4-321 por_hnf_por_hnf_unit_info (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:24	num_excl	Number of exclusive monitors	RO	-
23	Reserved	Reserved	RO	-
22:20	data_ram_latency	SLC data RAM latency (in cycles)	RO	-
19	Reserved	Reserved	RO	-
18:16	tag_ram_lat	SLC tag RAM latency (in cycles)	RO	-
15:13	Reserved	Reserved	RO	-
12:8	num_ways	Number of cache ways in the SLC	RO	-
7	Reserved	Reserved	RO	-
6:4	sf_size	SF size 3'b000: 512KB 3'b001: 1MB 3'b010: 2MB 3'b011: 4MB 3'b100: 8MB	RO	-
3	Reserved	Reserved	RO	-
2:0	slc_size	SLC size 3'b000: No SLC 3'b001: 128KB 3'b010: 256KB 3'b011: 512KB 3'b100: 1MB 3'b101: 2MB 3'b110: 3MB 3'b111: 4MB	RO	-

por_hnf_cfg_ctl

Functions as the configuration control register for HN-F.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA00
Register reset	Configuration dependent

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.cfg_ctl

The following image shows the higher register bit assignments.

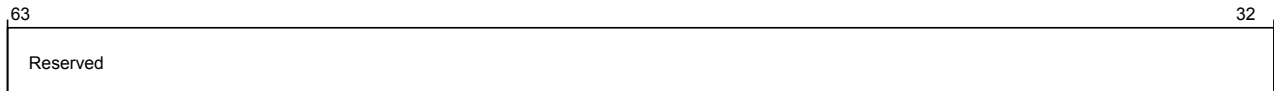


Figure 4-305 por_hnf_por_hnf_cfg_ctl (high)

The following table shows the por_hnf_cfg_ctl higher register bit assignments.

Table 4-322 por_hnf_por_hnf_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

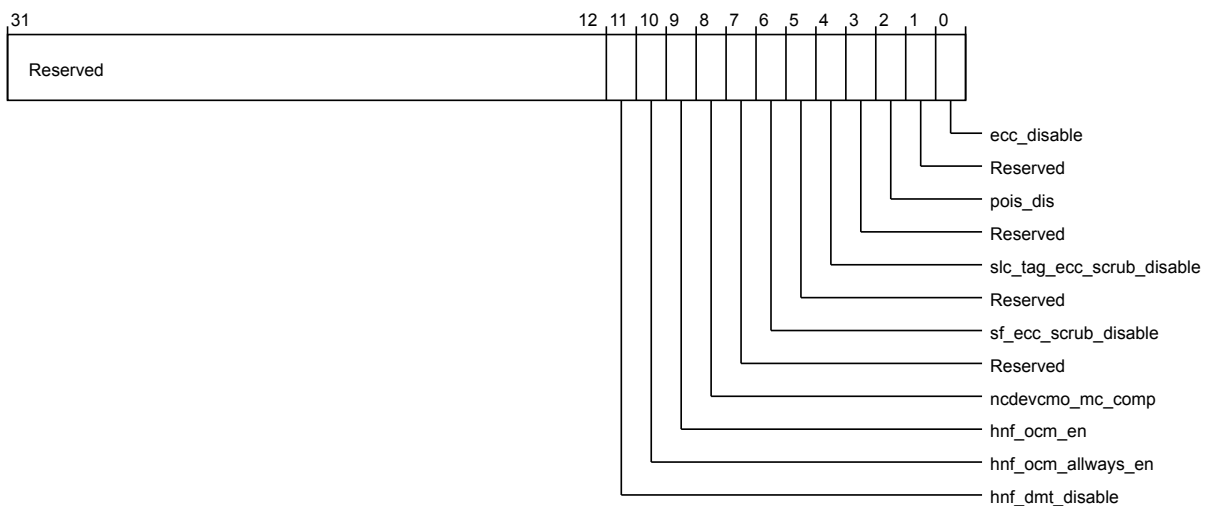


Figure 4-306 por_hnf_por_hnf_cfg_ctl (low)

The following table shows the por_hnf_cfg_ctl lower register bit assignments.

Table 4-323 por_hnf_por_hnf_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11	hnf_dmt_disable	Disables DMT when set	RW	1'b0
10	hnf_ocm_allways_en	Enables all SLC ways with OCM	RW	1'b0
9	hnf_ocm_en	Enables region locking with OCM support	RW	1'b0

Table 4-323 por_hnf_por_hnf_cfg_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
8	ncdevcmo_mc_comp	Disables HN-F completion when set NOTE: When set, HN-F sends completion for the following transactions received after completion from SN: 1. Non-cacheable WriteNoSnp 2. Device WriteNoSnp 3. CMO (cache maintenance operations) CONSTRAINT: When this bit is set, por_rni_cfg_ctl.dis_ncwr_stream and por_rnd_cfg_ctl.dis_ncwr_stream must also be set.	RW	1'b0
7	Reserved	Reserved	RO	-
6	sf_ecc_scrub_disable	Disables SF tag single-bit ECC error scrubbing when set	RW	Configuration dependent
5	Reserved	Reserved	RO	-
4	slc_tag_ecc_scrub_disable	Disables SLC tag single-bit ECC error scrubbing when set	RW	Configuration dependent
3	Reserved	Reserved	RO	-
2	pois_dis	Disables parity error data poison when set	RW	1'b0
1	Reserved	Reserved	RO	-
0	ecc_disable	Disables SLC and SF ECC generation/detection when set	RW	1'b0

por_hnf_aux_ctl

Functions as the auxiliary control register for HN-F.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

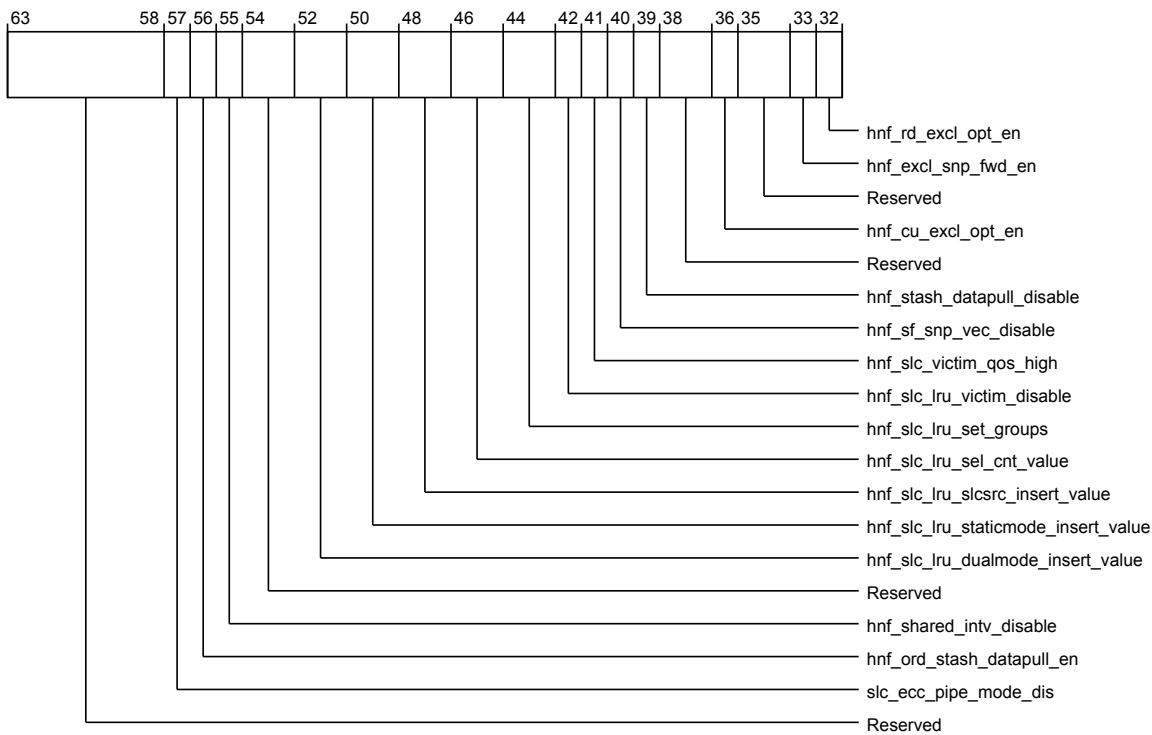


Figure 4-307 por_hnf_por_hnf_aux_ctl (high)

The following table shows the por_hnf_aux_ctl higher register bit assignments.

Table 4-324 por_hnf_por_hnf_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57	slc_ecc_pipe_mode_dis	Disables inline ECC pipe mode in SLC. CONSTRAINT: Must be programmed at boot time.	RW	1'b0
56	hnf_ord_stash_datapull_en	Enables stash datapull for ordered write stash requests	RW	Configuration dependent
55	hnf_shared_intv_disable	Disables snoop requests to CHIB RN-F with shared copy	RW	Configuration dependent
54:53	Reserved	Reserved	RO	-
52:51	hnf_slc_lru_dualmode_insert_value	Insertion value for Dual mode eLRU NOTE: Default is 2'b11.	RW	2'b11
50:49	hnf_slc_lru_staticmode_insert_value	Insertion value for Static mode eLRU NOTE: Default is 2'b10.	RW	2'b10
48:47	hnf_slc_lru_slcsrc_insert_value	Insertion value if SLC source bit is set NOTE: Default is 2'b00.	RW	2'b00

Table 4-324 por_hnf_por_hnf_aux_ctl (high) (continued)

Bits	Field name	Description	Type	Reset
46:45	hnf_slc_lru_sel_cnt_value	Selection counter value for eLRU to determine which group policy is more effective 2'b00: Sel counter is like an 8-bit range; upper limit is 255; middle point is 128 2'b01: Sel counter is like a 9-bit range; upper limit is 511; middle point is 256 2'b10: Sel counter is like a 10-bit range; upper limit is 1023; middle point is 512 2'b11: Sel counter is like an 11-bit range; upper limit is 2047; middle point is 1024 NOTE: Default is 10-bit with counter reset to a value of 512.	RW	2'b10
44:43	hnf_slc_lru_set_groups	Number of sets in monitor group for enhance LRU 2'b00: 16 2'b01: 32 2'b10: 64 2'b11: 128 NOTE: Default is 32 sets per monitor group. If cache size is small (128KB or less), there would be only one set per group.	RW	2'b01
42	hnf_slc_lru_victim_disable	Disable enhanced LRU based victim selection for SLC 1'b0: SLC victim selection is based on eLRU. 1'b1: SLC victim selection is based on LFSR. NOTE: Victim selection for SF is always LFSR-based.	RW	1'b1
41	hnf_slc_victim_qos_high	SLC victim QoS behavior for SN write request 1'b0: Each victim inherits the QoS value of the request which caused it 1'b1: All victims use high QoS class (14)	RW	1'b0
40	hnf_sf_snp_vec_disable	Disables SF snoop vector when set	RW	1'b0
39	hnf_stash_datapull_disable	Disables HN-F stash data pull support when set	RW	Configuration dependent
38:37	Reserved	Reserved	RO	-
36	hnf_cu_excl_opt_en	CleanUnique exclusive optimization enable	RW	Configuration dependent
35:34	Reserved	Reserved	RO	-
33	hnf_excl_snp_fwd_en	This bit is currently not supported. Software must not program this bit.	RW	1'b0
32	hnf_rd_excl_opt_en	ReadNotSharedDirty exclusive optimization enable	RW	1'b0

The following image shows the lower register bit assignments.

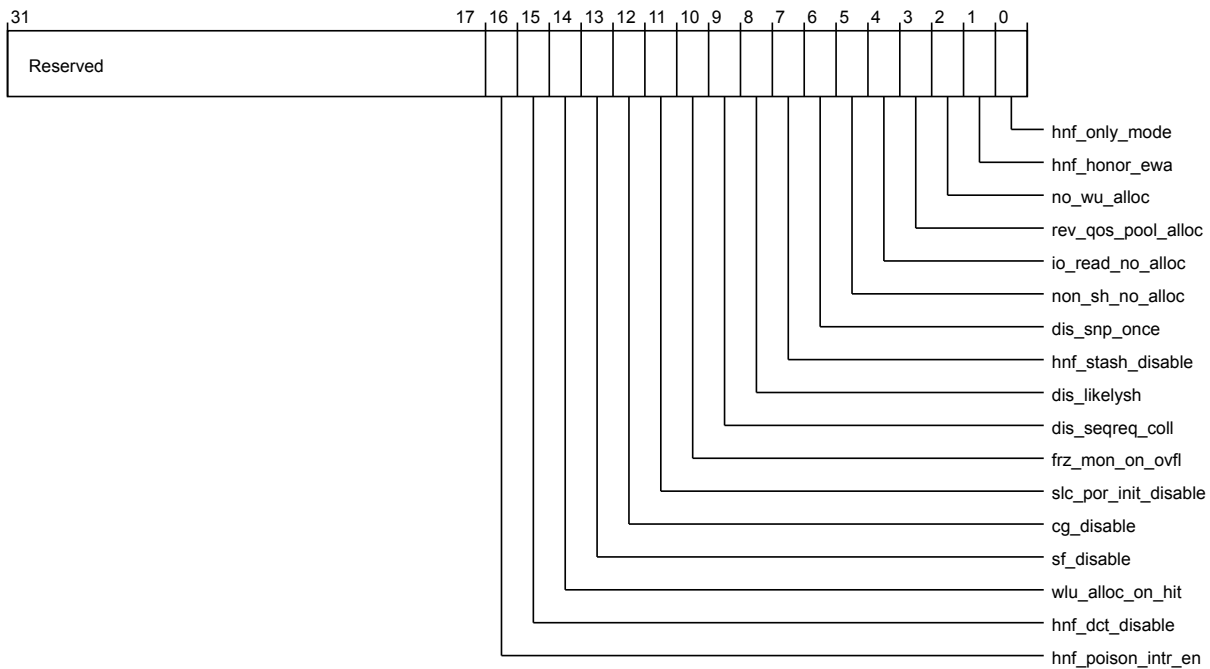


Figure 4-308 `por_hnf_por_hnf_aux_ctl (low)`

The following table shows the `por_hnf_aux_ctl` lower register bit assignments.

Table 4-325 `por_hnf_por_hnf_aux_ctl (low)`

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	<code>hnf_poison_intr_en</code>	Enables reporting an interrupt by HN-F when poison is detected at SLC	RW	Configuration dependent
15	<code>hnf_dct_disable</code>	Disables DCT when set	RW	Configuration dependent
14	<code>wlu_alloc_on_hit</code>	Forces WLU requests to allocate if the line hit in SLC	RW	1'b0
13	<code>sf_disable</code>	Disables SF	RW	1'b0
12	<code>cg_disable</code>	Disables HN-F architectural clock gates	RW	1'b0
11	<code>slc_por_init_disable</code>	Disables SLC and SF initialization on Reset	RW	1'b0
10	<code>frz_mon_on_ovfl</code>	Freezes the exclusive monitors	RW	1'b0
9	<code>dis_seqreq_coll</code>		RW	1'b0
8	<code>dis_likelysh</code>	Disables Likely Shared based allocations	RW	1'b0
7	<code>hnf_stash_disable</code>	Disables HN-F stash support	RW	Configuration dependent
6	<code>dis_snp_once</code>	When set, disables SnpOnce and converts to SnpShared	RW	Configuration dependent

Table 4-325 por_hnf_por_hnf_aux_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
5	non_sh_no_alloc	Disables SLC allocation for non-shareable cacheable transactions when set	RW	1'b0
4	io_read_no_alloc	When set, disables ReadOnce and ReadNoSnp allocation in SLC from RN-Is	RW	1'b0
3	rev_qos_pool_alloc	Reverses QoS pool allocation algorithm	RW	1'b0
2	no_wu_alloc	Disables WriteUnique/WriteLineUnique allocations in SLC when set	RW	1'b0
1	hnf_honor_ewa	When set, postpones completion for writes where EWA=0 in the request until HN-F receives completion from MC or SBSX	RW	1'b1
0	hnf_only_mode	Enables HN-F only mode; disables SLC and SF when set	RW	1'b0

por_hnf_r2_aux_ctl

Functions as the auxiliary control register for HN-F for CMN-600AE R2 features.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

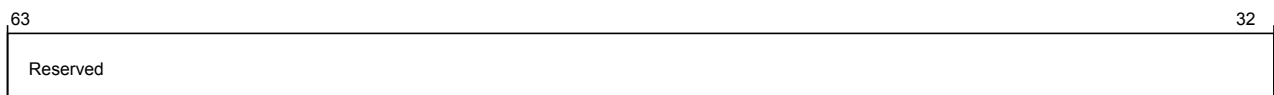


Figure 4-309 por_hnf_por_hnf_r2_aux_ctl (high)

The following table shows the por_hnf_r2_aux_ctl higher register bit assignments.

Table 4-326 por_hnf_por_hnf_r2_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

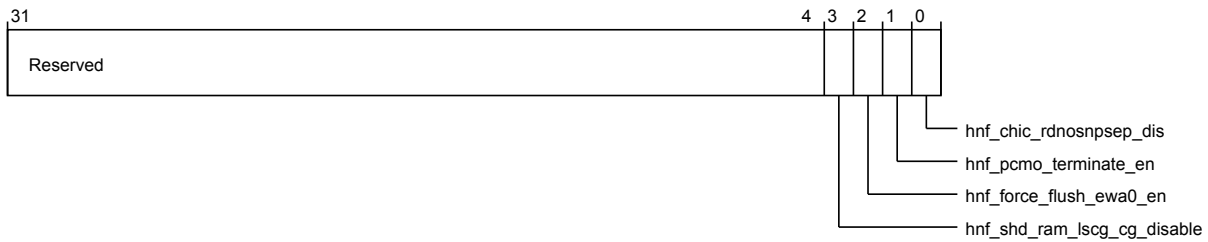


Figure 4-310 `por_hnf_por_hnf_r2_aux_ctl` (low)

The following table shows the `por_hnf_r2_aux_ctl` lower register bit assignments.

Table 4-327 `por_hnf_por_hnf_r2_aux_ctl` (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	<code>hnf_shd_ram_lscg_cg_disable</code>	Disable clock gating for Shared RAM Lock Step checker delay block	RW	1'b0
2	<code>hnf_force_flush_ewa0_en</code>	Force SLC and SF flush to use EWA 0 for SN writes	RW	1'b0
1	<code>hnf_pcmo_terminate_en</code>	Terminate PCMO in HNF when this bit is set to 1'b1	RW	1'b0
0	<code>hnf_chic_rdnosnpsep_dis</code>	Disables separation of Data and Comp in CHIC mode	RW	1'b0

`rdf_hnf_aux_ctl`

Functions as the auxiliary control register for HN-F for functional safety features.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA18

Register reset 64'b0

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

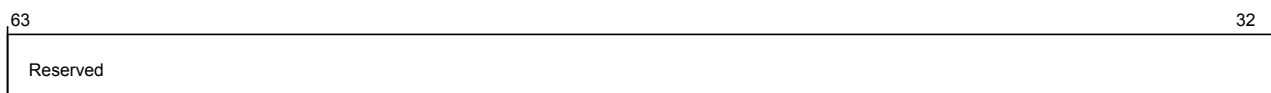


Figure 4-311 `por_hnf_rdf_hnf_aux_ctl` (high)

The following table shows the `rdf_hnf_aux_ctl` higher register bit assignments.

Table 4-328 `por_hnf_rdf_hnf_aux_ctl` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

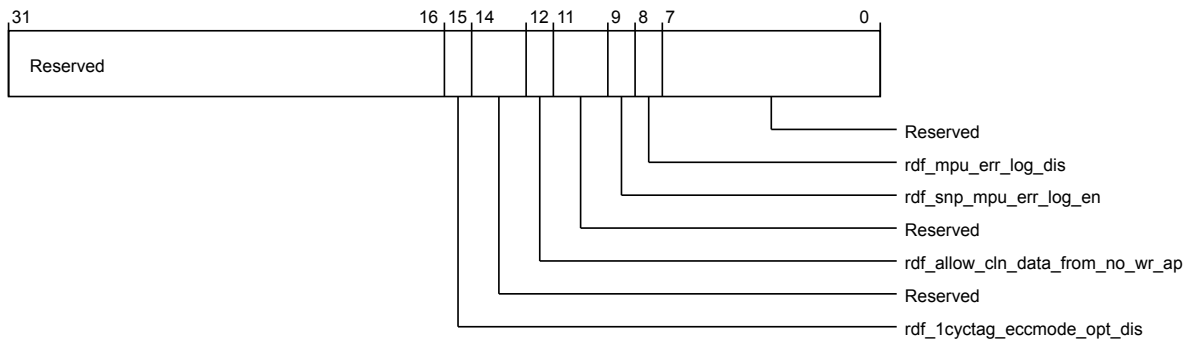


Figure 4-312 `por_hnf_rdf_hnf_aux_ctl (low)`

The following table shows the `rdf_hnf_aux_ctl` lower register bit assignments.

Table 4-329 `por_hnf_rdf_hnf_aux_ctl (low)`

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15	<code>rdf_1cyctag_eccmode_opt_dis</code>	Disables the SLC tag updates to be optimized in ECC pipe mode	RW	1'b0
14:13	Reserved	Reserved	RO	-
12	<code>rdf_allow_cln_data_from_no_wr_ap</code>	Enables consuming Clean data responses from a RN with no write access permissions	RW	1'b0
11:10	Reserved	Reserved	RO	-
9	<code>rdf_snp_mpu_err_log_en</code>	Enable logging of snoop MPU errors in the HNF RAS registers	RW	1'b0
8	<code>rdf_mpu_err_log_dis</code>	Disables logging of all MPU errors in the HNF RAS registers	RW	1'b0
7:0	Reserved	Reserved	RO	-

`por_hnf_ppu_pwpr`

Functions as the power policy register for HN-F.

Its characteristics are:

Type	RW
Register width (Bits)	32
Address offset	14'h1000
Register reset	32'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_hnf_secure_register_groups_override.ppu</code>

The following image shows the lower register bit assignments.

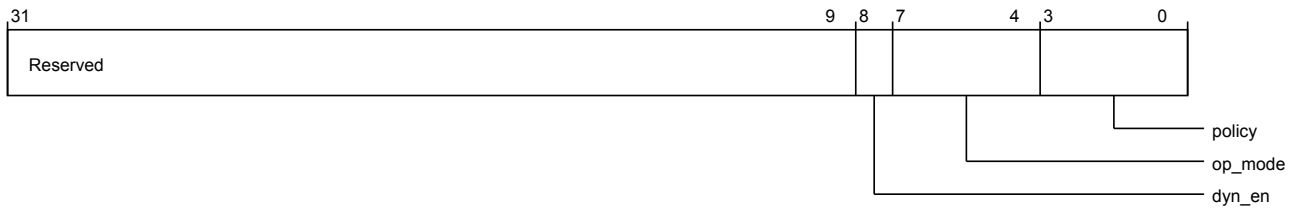


Figure 4-313 `por_hnf_ppu_pwpr`

The following table shows the `por_hnf_ppu_pwpr` register bit assignments.

Table 4-330 `por_hnf_ppu_pwpr` (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	<code>dyn_en</code>	Dynamic transition enable	RW	1'b0
7:4	<code>op_mode</code>	HN-F operational power mode 4'b0011: FAM 4'b0010: HAM 4'b0001: SFONLY 4'b0000: NOSFSLC	RW	4'b0
3:0	<code>policy</code>	HN-F power mode policy 4'b1000: ON 4'b0111: FUNC_RET 4'b0010: MEM_RET 4'b0000: OFF	RW	4'b0

`por_hnf_ppu_pwsr`

Provides power status information for HN-F.

Its characteristics are:

Type	RO
Register width (Bits)	32
Address offset	14'h1008
Register reset	32'b0
Usage constraints	There are no usage constraints.

The following image shows the lower register bit assignments.

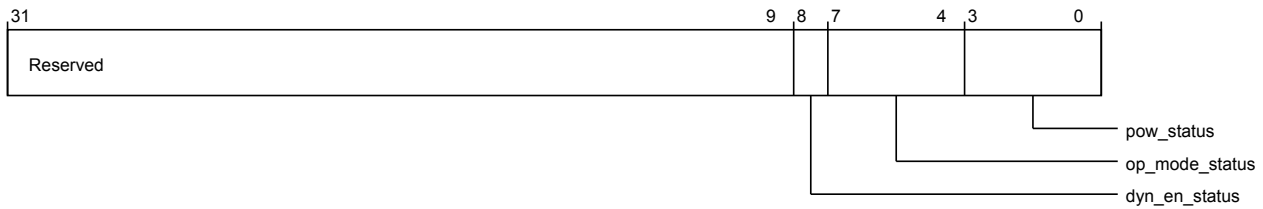


Figure 4-314 por_hnf_por_hnf_ppu_pwsr

The following table shows the por_hnf_ppu_pwsr register bit assignments.

Table 4-331 por_hnf_por_hnf_ppu_pwsr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	dyn_en_status	Dynamic transition status	RO	1'b0
7:4	op_mode_status	HN-F operational mode status 4'b0011: FAM 4'b0010: HAM 4'b0001: SFONLY 4'b0000: NOSFSLC	RO	4'b0
3:0	pow_status	HN-F power mode status 4'b1000: ON 4'b0111: FUNC_RET 4'b0010: MEM_RET 4'b0000: OFF	RO	4'b0

por_hnf_ppu_misr

Functions as the power miscellaneous input current status register for HN-F.

Its characteristics are:

Type	RO
Register width (Bits)	32
Address offset	14'h1014
Register reset	32'b0
Usage constraints	There are no usage constraints.

The following image shows the lower register bit assignments.

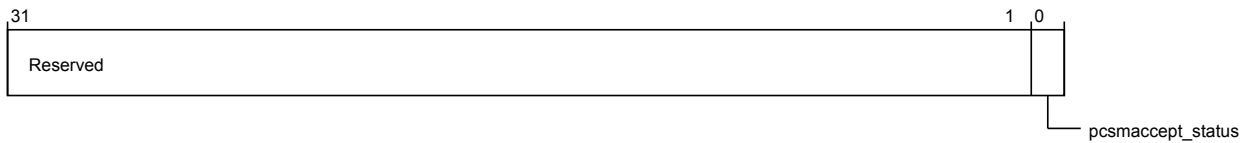


Figure 4-315 por_hnf_por_hnf_ppu_misr

The following table shows the por_hnf_ppu_misr register bit assignments.

Table 4-332 por_hnf_por_hnf_ppu_misr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	pcsmaccept_status	HN-F RAM PCSMACCEPT status	RO	1'b0

por_hnf_ppu_idr0

Provides identification information for the HN-F PPU.

Its characteristics are:

Type	RO
Register width (Bits)	32
Address offset	14'h1FB0
Register reset	32'b00100000000011010010101000
Usage constraints	There are no usage constraints.

The following image shows the lower register bit assignments.

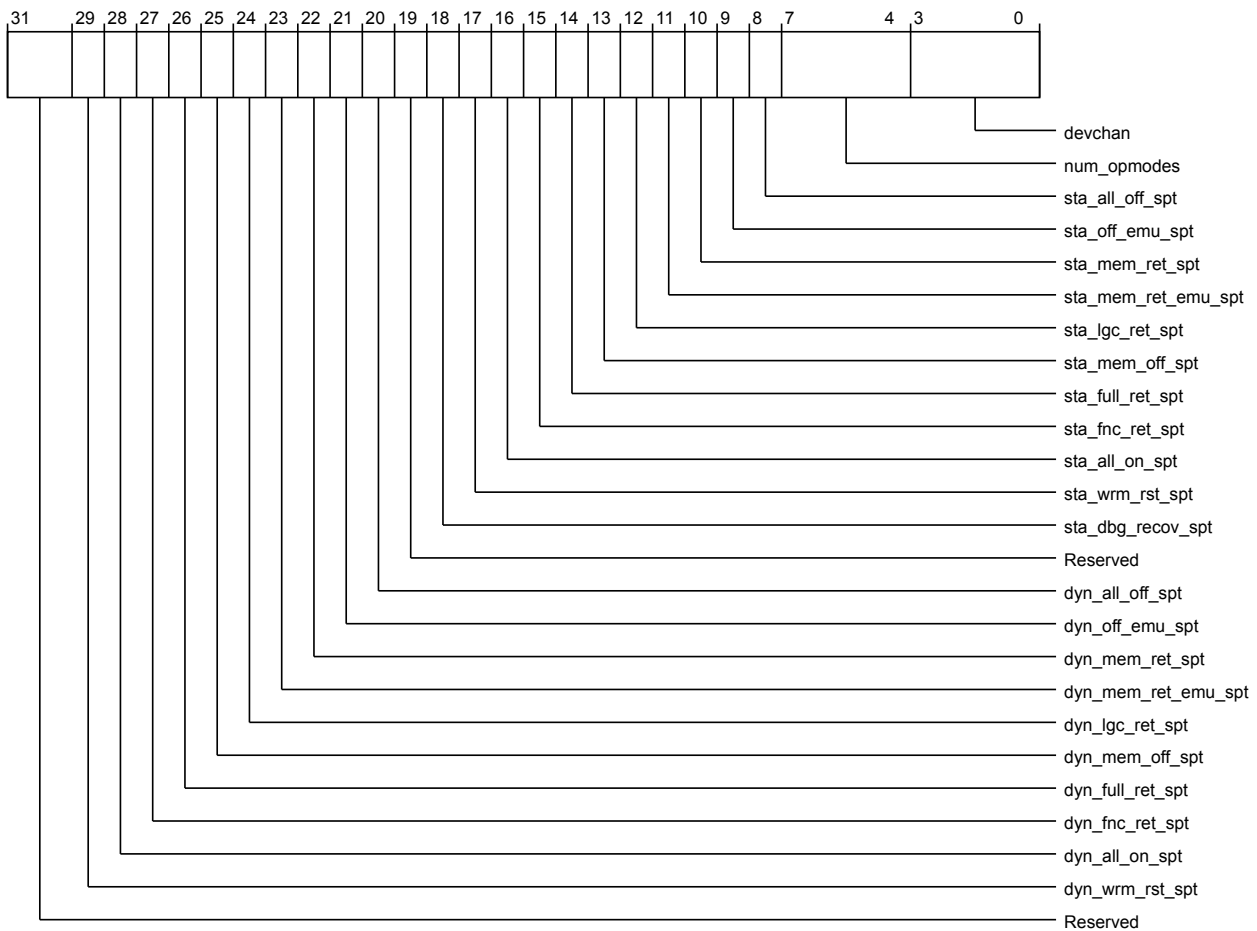


Figure 4-316 por_hnf_por_hnf_ppu_idr0

The following table shows the por_hnf_ppu_idr0 register bit assignments.

Table 4-333 por_hnf_por_hnf_ppu_idr0 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29	dyn_wrm_rst_spt	Dynamic warm_rst support	RO	1'b0
28	dyn_all_on_spt	Dynamic on support	RO	1'b0
27	dyn_fnc_ret_spt	Dynamic func_ret support	RO	1'b1
26	dyn_full_ret_spt	Dynamic full_ret support	RO	1'b0
25	dyn_mem_off_spt	Dynamic mem_off support	RO	1'b0
24	dyn_lgc_ret_spt	Dynamic logic_ret support	RO	1'b0
23	dyn_mem_ret_emu_spt	Dynamic mem_ret_emu support	RO	1'b0
22	dyn_mem_ret_spt	Dynamic mem_ret support	RO	1'b0
21	dyn_off_emu_spt	Dynamic off_emu support	RO	1'b0

Table 4-333 `por_hnf_por_hnf_ppu_idr0` (low) (continued)

Bits	Field name	Description	Type	Reset
20	<code>dyn_all_off_spt</code>	Dynamic off support	RO	1'b0
19	Reserved	Reserved	RO	-
18	<code>sta_dbg_recov_spt</code>	Static <code>dbg_recov</code> support	RO	1'b0
17	<code>sta_wrm_rst_spt</code>	Static <code>warm_rst</code> support	RO	1'b0
16	<code>sta_all_on_spt</code>	Static on support	RO	1'b1
15	<code>sta_fnc_ret_spt</code>	Static <code>func_ret</code> support	RO	1'b1
14	<code>sta_full_ret_spt</code>	Static <code>full_ret</code> support	RO	1'b0
13	<code>sta_mem_off_spt</code>	Static <code>mem_off</code> support	RO	1'b1
12	<code>sta_lgc_ret_spt</code>	Static <code>logic_ret</code> support	RO	1'b0
11	<code>sta_mem_ret_emu_spt</code>	Static <code>mem_ret_emu</code> support	RO	1'b0
10	<code>sta_mem_ret_spt</code>	Static <code>mem_ret</code> support	RO	1'b1
9	<code>sta_off_emu_spt</code>	Static <code>off_emu</code> support	RO	1'b0
8	<code>sta_all_off_spt</code>	Static off support	RO	1'b1
7:4	<code>num_opmodes</code>	Number of operational modes	RO	4'b0100
3:0	<code>devchan</code>	Number of device interface channels	RO	1'b0

`por_hnf_ppu_idr1`

Provides identification information for the HN-F PPU.

Its characteristics are:

Type	RO
Register width (Bits)	32
Address offset	14'h1FB4
Register reset	32'b0
Usage constraints	There are no usage constraints.

The following image shows the lower register bit assignments.

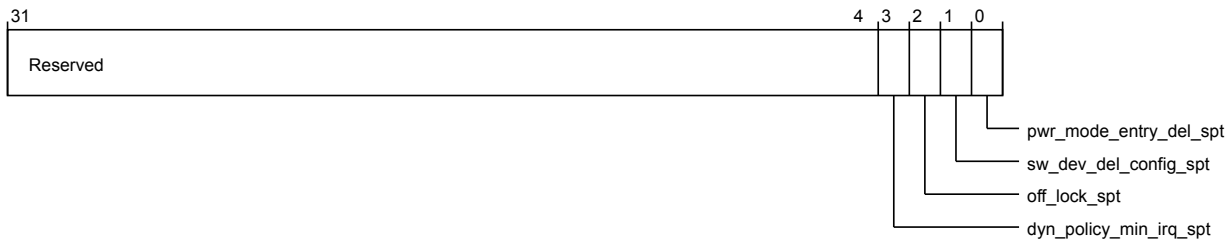


Figure 4-317 `por_hnf_por_hnf_ppu_idr1`

The following table shows the `por_hnf_ppu_idr1` register bit assignments.

Table 4-334 `por_hnf_por_hnf_ppu_idr1` (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	<code>dyn_policy_min_irq_spt</code>	Dynamic minimum policy interrupt support	RO	1'b0
2	<code>off_lock_spt</code>	Off and mem_ret lock support	RO	1'b0
1	<code>sw_dev_del_config_spt</code>	Software device delay control configuration support	RO	1'b0
0	<code>pwr_mode_entry_del_spt</code>	Power mode entry delay support	RO	1'b0

`por_hnf_ppu_iidr`

Functions as the power implementation identification register for HN-F.

Its characteristics are:

Type RO

Register width (Bits) 32

Address offset 14'h1FC8

Register reset 32'b0000100111000000000000100111011

Usage constraints There are no usage constraints.

The following image shows the lower register bit assignments.

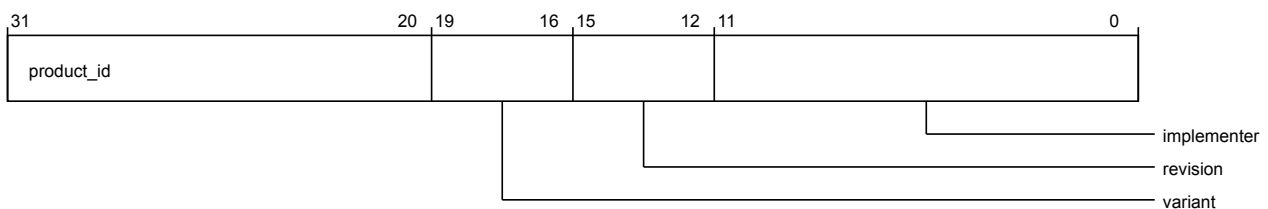


Figure 4-318 `por_hnf_por_hnf_ppu_iidr`

The following table shows the `por_hnf_ppu_iidr` register bit assignments.

Table 4-335 por_hnf_por_hnf_ppu_iidr (low)

Bits	Field name	Description	Type	Reset
31:20	product_id	Implementation identifier	RO	12'h434
19:16	variant	Implementation variant	RO	4'h0
15:12	revision	Implementation revision	RO	4'h0
11:0	implementer	Arm implementation	RO	12'h43B

por_hnf_ppu_aidr

Functions as the power architecture identification register for HN-F.

Its characteristics are:

Type	RO
Register width (Bits)	32
Address offset	14'h1FCC
Register reset	32'b00010001
Usage constraints	There are no usage constraints.

The following image shows the lower register bit assignments.

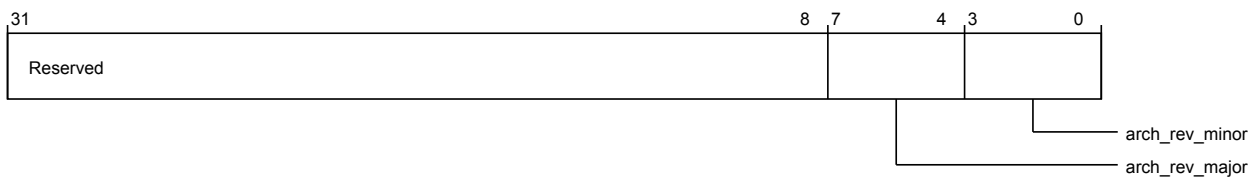


Figure 4-319 por_hnf_por_hnf_ppu_aidr

The following table shows the por_hnf_ppu_aidr register bit assignments.

Table 4-336 por_hnf_por_hnf_ppu_aidr (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:4	arch_rev_major	PPU architecture major revision	RO	4'h1
3:0	arch_rev_minor	PPU architecture minor revision	RO	4'h1

por_hnf_ppu_dyn_ret_threshold

Configures the dynamic retention threshold for SLC and SF RAM.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1100
Register reset	64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.ppu

The following image shows the higher register bit assignments.



Figure 4-320 por_hnf_por_hnf_ppu_dyn_ret_threshold (high)

The following table shows the por_hnf_ppu_dyn_ret_threshold higher register bit assignments.

Table 4-337 por_hnf_por_hnf_ppu_dyn_ret_threshold (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

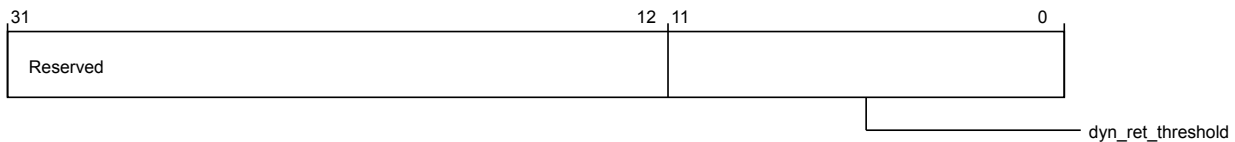


Figure 4-321 por_hnf_por_hnf_ppu_dyn_ret_threshold (low)

The following table shows the por_hnf_ppu_dyn_ret_threshold lower register bit assignments.

Table 4-338 por_hnf_por_hnf_ppu_dyn_ret_threshold (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:0	dyn_ret_threshold	HN-F RAM idle cycle count threshold	RW	32'b0

por_hnf_qos_band

Provides QoS classifications based on the QoS value ranges.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'hA80

Register reset 64'b11111111111011001011100001110000

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.qos

The following image shows the higher register bit assignments.

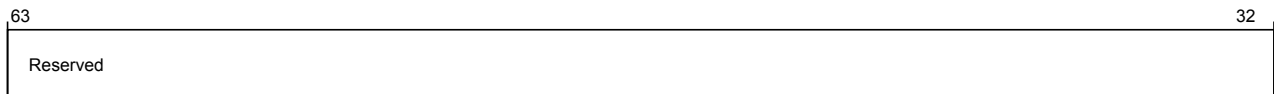


Figure 4-322 por_hnf_por_hnf_qos_band (high)

The following table shows the por_hnf_qos_band higher register bit assignments.

Table 4-339 por_hnf_por_hnf_qos_band (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

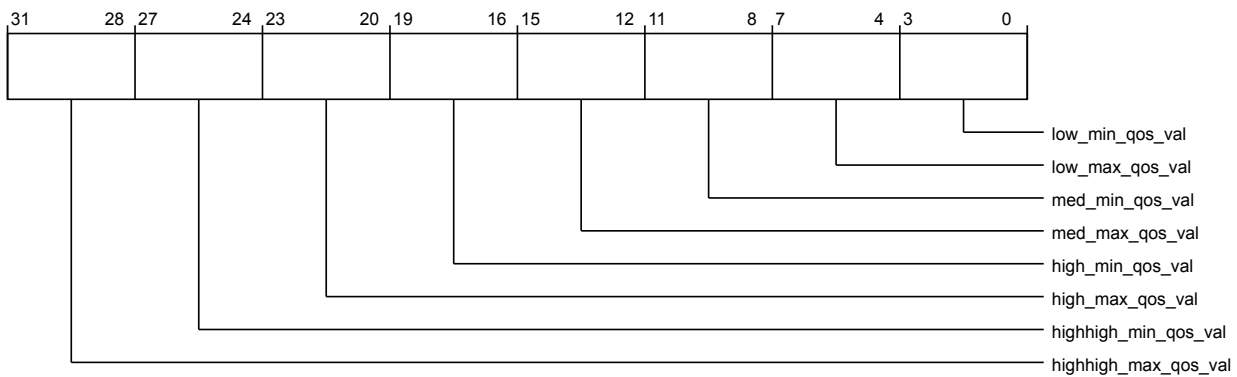


Figure 4-323 por_hnf_por_hnf_qos_band (low)

The following table shows the por_hnf_qos_band lower register bit assignments.

Table 4-340 por_hnf_por_hnf_qos_band (low)

Bits	Field name	Description	Type	Reset
31:28	highhigh_max_qos_val	Maximum value for HighHigh QoS class	RO	4'hF
27:24	highhigh_min_qos_val	Minimum value for HighHigh QoS class	RO	4'hF
23:20	high_max_qos_val	Maximum value for High QoS class	RO	4'hE
19:16	high_min_qos_val	Minimum value for High QoS class	RO	4'hC
15:12	med_max_qos_val	Maximum value for Medium QoS class	RO	4'hB
11:8	med_min_qos_val	Minimum value for Medium QoS class	RO	4'h8
7:4	low_max_qos_val	Maximum value for Low QoS class	RO	4'h7
3:0	low_min_qos_val	Minimum value for Low QoS class	RO	4'h0

por_hnf_qos_reservation

Controls POCQ maximum occupancy counts for each QoS class (HighHigh, High, Medium, and Low).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA88
Register reset	Configuration dependent
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_hnf_secure_register_groups_override.qos

The following image shows the higher register bit assignments.

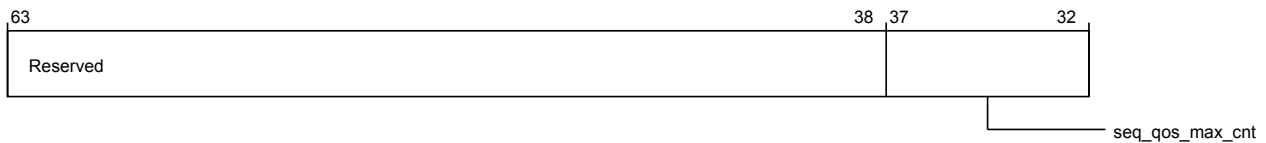


Figure 4-324 `por_hnf_por_hnf_qos_reservation` (high)

The following table shows the `por_hnf_qos_reservation` higher register bit assignments.

Table 4-341 `por_hnf_por_hnf_qos_reservation` (high)

Bits	Field name	Description	Type	Reset
63:38	Reserved	Reserved	RO	-
37:32	<code>seq_qos_max_cnt</code>	Number of entries reserved for SF evictions in POCQ CONSTRAINT: Maximum number is 2 entries.	RW	6'h1

The following image shows the lower register bit assignments.

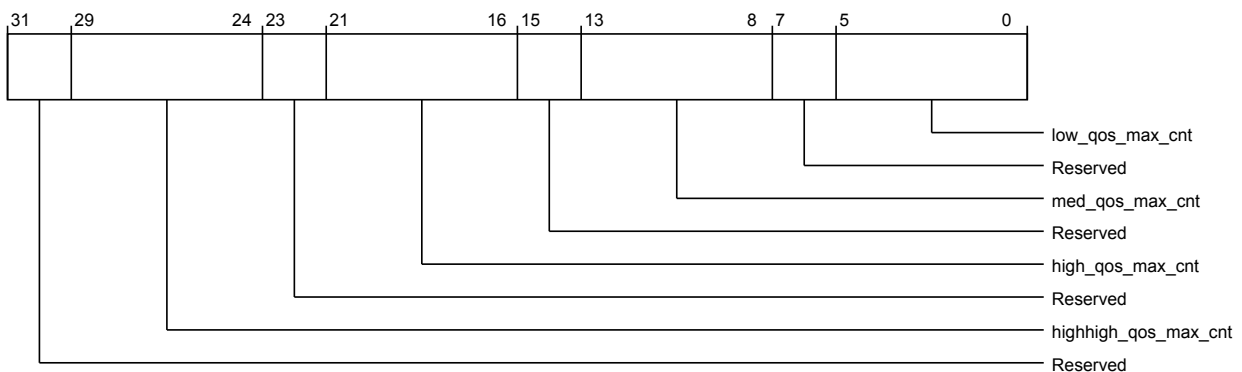


Figure 4-325 `por_hnf_por_hnf_qos_reservation` (low)

The following table shows the `por_hnf_qos_reservation` lower register bit assignments.

Table 4-342 `por_hnf_por_hnf_qos_reservation` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>highhigh_qos_max_cnt</code>	Maximum number of HighHigh QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent
23:22	Reserved	Reserved	RO	-
21:16	<code>high_qos_max_cnt</code>	Maximum number of High QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent
15:14	Reserved	Reserved	RO	-
13:8	<code>med_qos_max_cnt</code>	Maximum number of Medium QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent
7:6	Reserved	Reserved	RO	-
5:0	<code>low_qos_max_cnt</code>	Maximum number of Low QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent

`por_hnf_rn_starvation`

Controls starvation counts for each QoS class. Determines static credit grantee selection.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA90

Register reset 64'b11111111111111110111111111111111

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_hnf_secure_register_groups_override.qos`

The following image shows the higher register bit assignments.

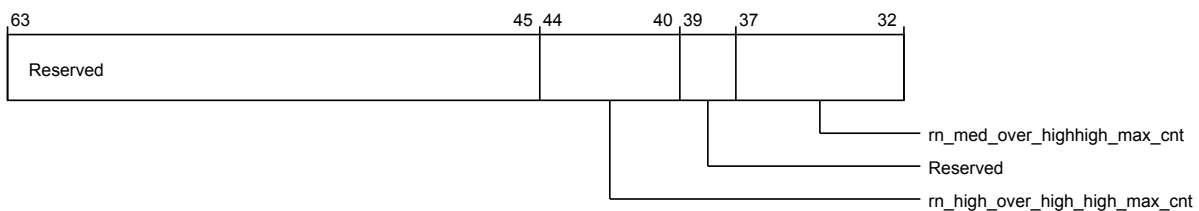


Figure 4-326 `por_hnf_por_hnf_rn_starvation` (high)

The following table shows the `por_hnf_rn_starvation` higher register bit assignments.

Table 4-343 `por_hnf_por_hnf_rn_starvation` (high)

Bits	Field name	Description	Type	Reset
63:45	Reserved	Reserved	RO	-
44:40	<code>rn_high_over_high_high_max_cnt</code>	Maximum number of consecutive instances where HighHigh QoS class wins priority over High QoS class	RW	5'h1F
39:38	Reserved	Reserved	RO	-
37:32	<code>rn_med_over_highhigh_max_cnt</code>	Maximum number of consecutive instances where HighHigh QoS class wins priority over Medium QoS class	RW	6'h3F

The following image shows the lower register bit assignments.

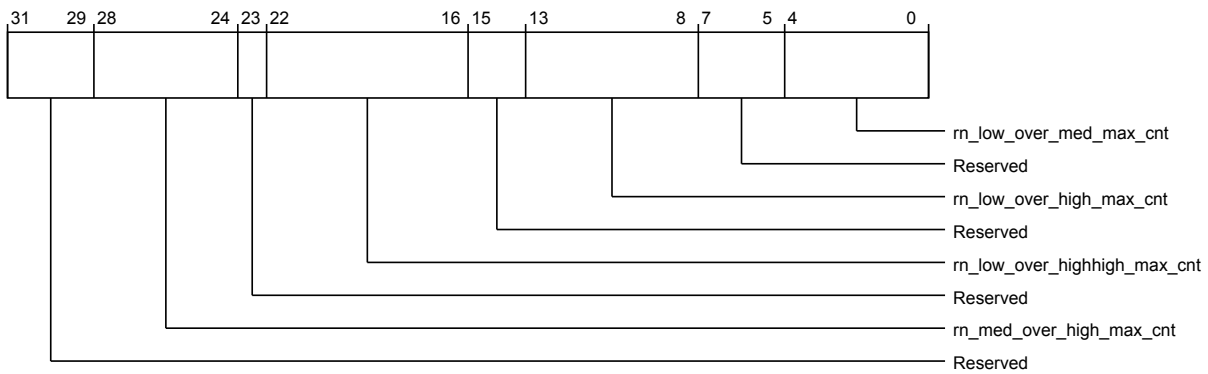


Figure 4-327 `por_hnf_por_hnf_rn_starvation` (low)

The following table shows the `por_hnf_rn_starvation` lower register bit assignments.

Table 4-344 `por_hnf_por_hnf_rn_starvation` (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	<code>rn_med_over_high_max_cnt</code>	Maximum number of consecutive instances where High QoS class wins priority over Medium QoS class	RW	5'h1F
23	Reserved	Reserved	RO	-
22:16	<code>rn_low_over_highhigh_max_cnt</code>	Maximum number of consecutive instances where HighHigh QoS class wins priority over Low QoS class	RW	7'h3F
15:14	Reserved	Reserved	RO	-
13:8	<code>rn_low_over_high_max_cnt</code>	Maximum number of consecutive instances where High QoS class wins priority over Low QoS class	RW	6'h3F
7:5	Reserved	Reserved	RO	-
4:0	<code>rn_low_over_med_max_cnt</code>	Maximum number of consecutive instances where Medium QoS class wins priority over Low QoS class	RW	5'h1F

por_hnf_errfr

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3000
Register reset	64'b1001010100101
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

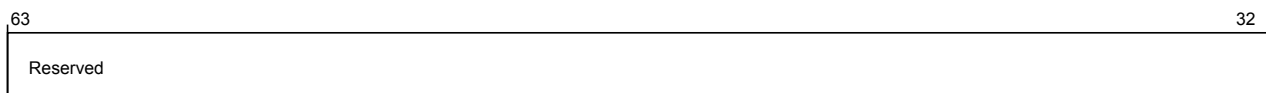


Figure 4-328 por_hnf_errfr (high)

The following table shows the por_hnf_errfr higher register bit assignments.

Table 4-345 por_hnf_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

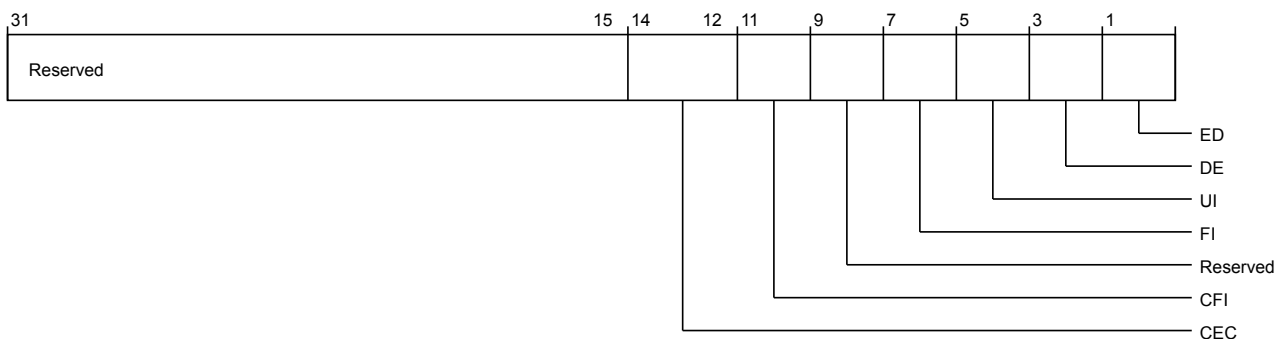


Figure 4-329 por_hnf_errfr (low)

The following table shows the por_hnf_errfr lower register bit assignments.

Table 4-346 `por_hnf_por_hnf_errfr` (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in <code>por_hnf_errmisc[39:32]</code> 3'b100: Implements 16-bit error counter in <code>por_hnf_errmisc[47:32]</code>	RO	3'b100
11:10	CFI	Corrected error interrupt	RO	2'b10
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

`por_hnf_errctlr`

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3008
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

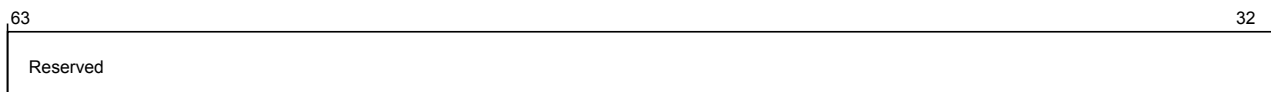


Figure 4-330 `por_hnf_por_hnf_errctlr` (high)

The following table shows the `por_hnf_errctlr` higher register bit assignments.

Table 4-347 `por_hnf_por_hnf_errctlr` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

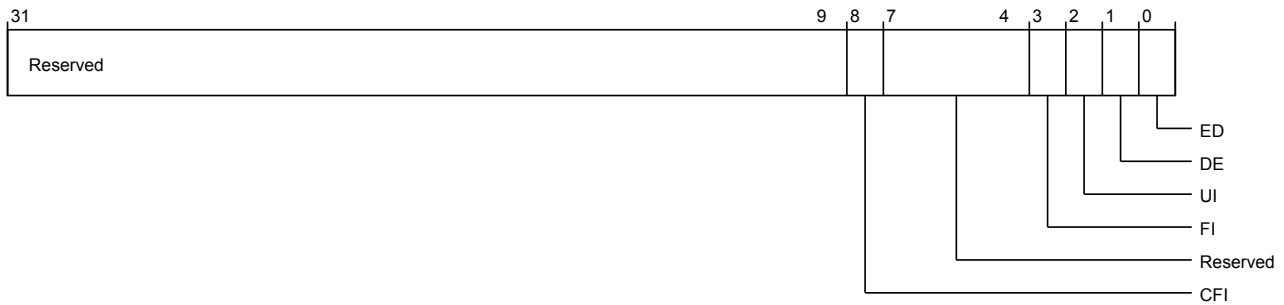


Figure 4-331 `por_hnf_por_hnf_errctlr (low)`

The following table shows the `por_hnf_errctlr` lower register bit assignments.

Table 4-348 `por_hnf_por_hnf_errctlr (low)`

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in <code>por_hnf_errfr.CFI</code>	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in <code>por_hnf_errfr.FI</code>	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in <code>por_hnf_errfr.UI</code>	RW	1'b0
1	DE	Enables error deferment as specified in <code>por_hnf_errfr.DE</code>	RW	1'b0
0	ED	Enables error detection as specified in <code>por_hnf_errfr.ED</code>	RW	1'b0

`por_hnf_errstatus`

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3010
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

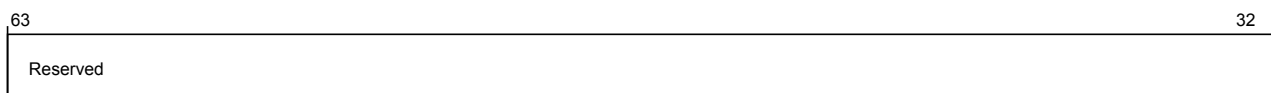


Figure 4-332 `por_hnf_por_hnf_errstatus (high)`

The following table shows the `por_hnf_errstatus` higher register bit assignments.

Table 4-349 por_hnf_por_hnf_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

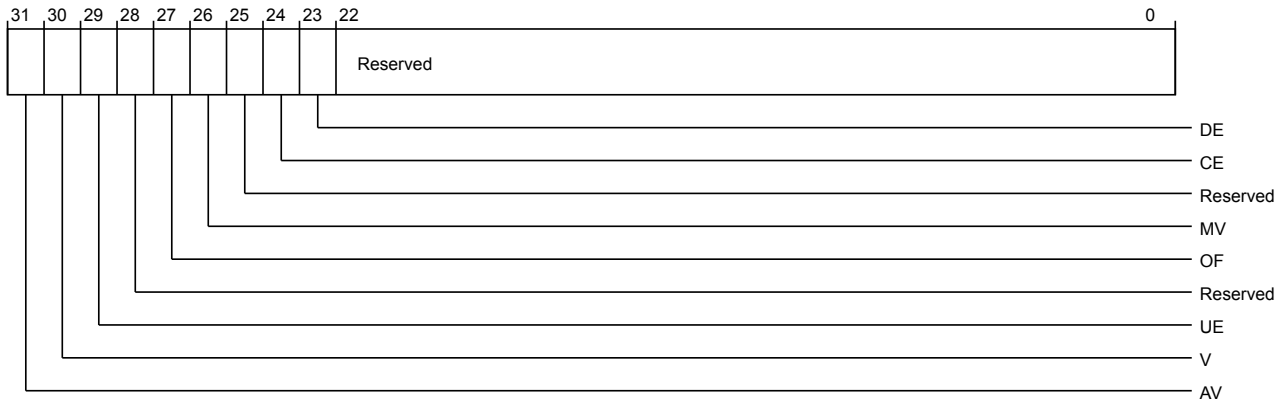


Figure 4-333 por_hnf_por_hnf_errstatus (low)

The following table shows the por_hnf_errstatus lower register bit assignments.

Table 4-350 por_hnf_por_hnf_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_hnf_erraddr contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0

Table 4-350 `por_hnf_por_hnf_errstatus` (low) (continued)

Bits	Field name	Description	Type	Reset
26	MV	<p><code>por_hnf_errmisc</code> valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear</p> <p>1'b1: Miscellaneous registers are valid</p> <p>1'b0: Miscellaneous registers are not valid</p>	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	<p>Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear</p> <p>1'b1: At least one transient corrected error recorded</p> <p>1'b0: No corrected errors recorded</p>	W1C	1'b0
23	DE	<p>Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear</p> <p>1'b1: At least one error is not corrected and is deferred</p> <p>1'b0: No errors deferred</p>	W1C	1'b0
22:0	Reserved	Reserved	RO	-

`por_hnf_erraddr`

Contains the error record address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3018

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

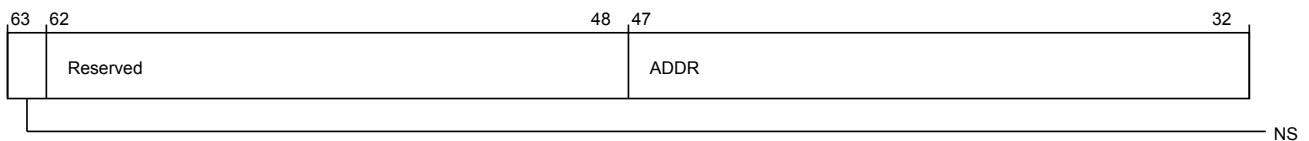


Figure 4-334 `por_hnf_por_hnf_erraddr` (high)

The following table shows the `por_hnf_erraddr` higher register bit assignments.

Table 4-351 por_hnf_por_hnf_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hnf_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

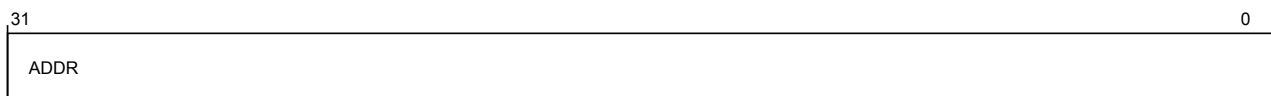


Figure 4-335 por_hnf_por_hnf_erraddr (low)

The following table shows the por_hnf_erraddr lower register bit assignments.

Table 4-352 por_hnf_por_hnf_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_hnf_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3020

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

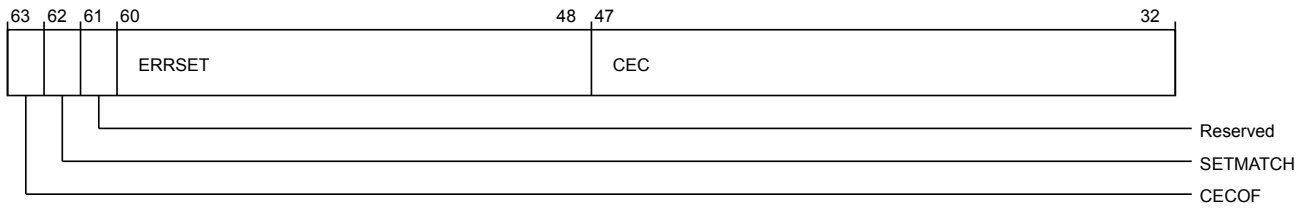


Figure 4-336 por_hnf_errmisc (high)

The following table shows the por_hnf_errmisc higher register bit assignments.

Table 4-353 por_hnf_errmisc (high)

Bits	Field name	Description	Type	Reset
63	CECOF	Corrected error counter overflow	RW	1'b0
62	SETMATCH	Set address match	RW	1'b0
61	Reserved	Reserved	RO	-
60:48	ERRSET	SLC/SF set address for ECC error	RW	13'b0
47:32	CEC	Corrected ECC error count	RW	16'b0

The following image shows the lower register bit assignments.

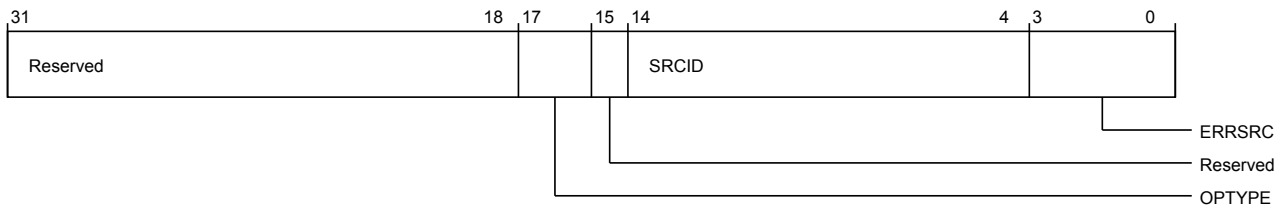


Figure 4-337 por_hnf_errmisc (low)

The following table shows the por_hnf_errmisc lower register bit assignments.

Table 4-354 por_hnf_errmisc (low)

Bits	Field name	Description	Type	Reset
31:18	Reserved	Reserved	RO	-
17:16	OPTYPE	Error op type 2'b00: Writes, CleanShared, Atomics and stash requests with invalid targets 2'b01: WriteBack, Evict, and Stash requests with valid target 2'b10: CMO 2'b11: Other op types	RW	2'b00

Table 4-354 por_hnf_por_hnf_errmisc (low) (continued)

Bits	Field name	Description	Type	Reset
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	ERRSRC	Error source 4'b0001: Data single-bit ECC 4'b0010: Data double-bit ECC 4'b0011: Single-bit ECC overflow 4'b0100: Tag single-bit ECC 4'b0101: Tag double-bit ECC 4'b0111: SF tag single-bit ECC 4'b1000: SF tag double-bit ECC 4'b1010: Data parity error 4'b1011: Data parity and poison 4'b1100: NDE	RW	4'b0000

por_hnf_err_inj

Enables error injection and setup. When enabled for a given source ID and logic processor ID, HN-F returns a slave error and reports an error interrupt. This error interrupt emulates a SLC double-bit data ECC error. This feature enables software to test the error handler. The slave error is reported for cacheable read access for which SLC hit is the data source. No slave error or error interrupt is reported for cacheable read access in which SLC miss is the data source.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3030
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

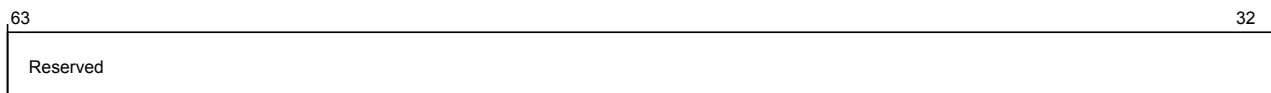


Figure 4-338 por_hnf_por_hnf_err_inj (high)

The following table shows the por_hnf_err_inj higher register bit assignments.

Table 4-355 por_hnf_por_hnf_err_inj (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

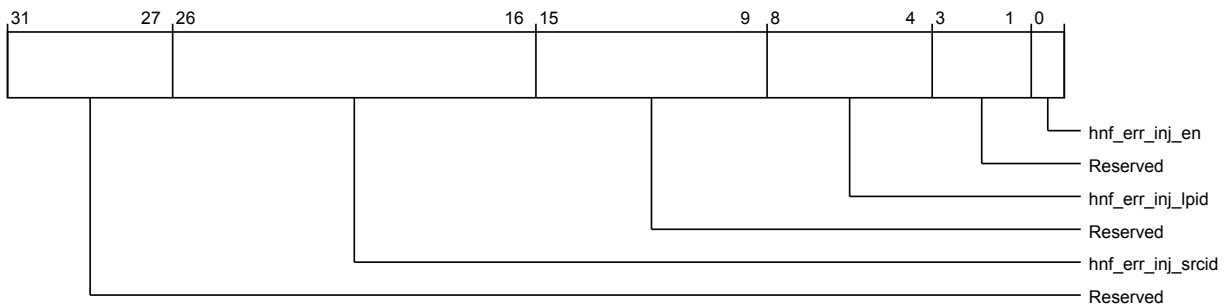


Figure 4-339 por_hnf_por_hnf_err_inj (low)

The following table shows the `por_hnf_err_inj` lower register bit assignments.

Table 4-356 por_hnf_por_hnf_err_inj (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	<code>hnf_err_inj_srcid</code>	RN source ID for read access which results in a SLC miss; does not report slave error or error to match error injection	RW	11'h0
15:9	Reserved	Reserved	RO	-
8:4	<code>hnf_err_inj_lpid</code>	LPID used to match for error injection	RW	5'h0
3:1	Reserved	Reserved	RO	-
0	<code>hnf_err_inj_en</code>	Enables error injection and report	RW	1'b0

por_hnf_byte_par_err_inj

Functions as the byte parity error injection register for HN-F.

Its characteristics are:

Type WO

Register width (Bits) 64

Address offset 14'h3038

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

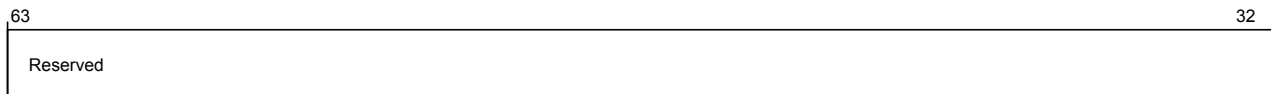


Figure 4-340 por_hnf_por_hnf_byte_par_err_inj (high)

The following table shows the por_hnf_byte_par_err_inj higher register bit assignments.

Table 4-357 por_hnf_por_hnf_byte_par_err_inj (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

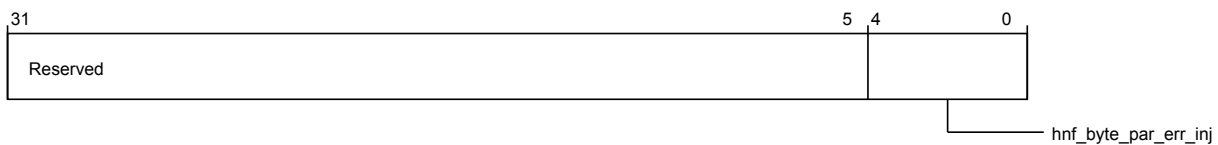


Figure 4-341 por_hnf_por_hnf_byte_par_err_inj (low)

The following table shows the por_hnf_byte_par_err_inj lower register bit assignments.

Table 4-358 por_hnf_por_hnf_byte_par_err_inj (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4:0	hnf_byte_par_err_inj	Specifies a byte lane; once this register is written, a byte parity error is injected in the specified byte lane on the next SLC hit; the error will be injected in all data flits on specified byte (0 to 31)	WO	5'h0

por_hnf_errfr_NS

Functions as the non-secure error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3100
Register reset	64'b1001010100101
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

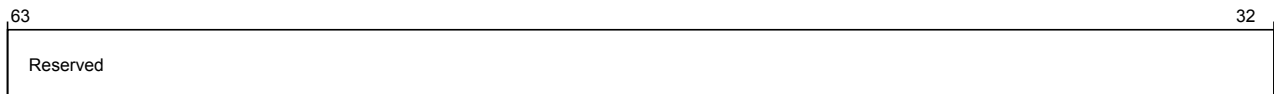


Figure 4-342 por_hnf_errfr_NS (high)

The following table shows the por_hnf_errfr_NS higher register bit assignments.

Table 4-359 por_hnf_errfr_NS (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

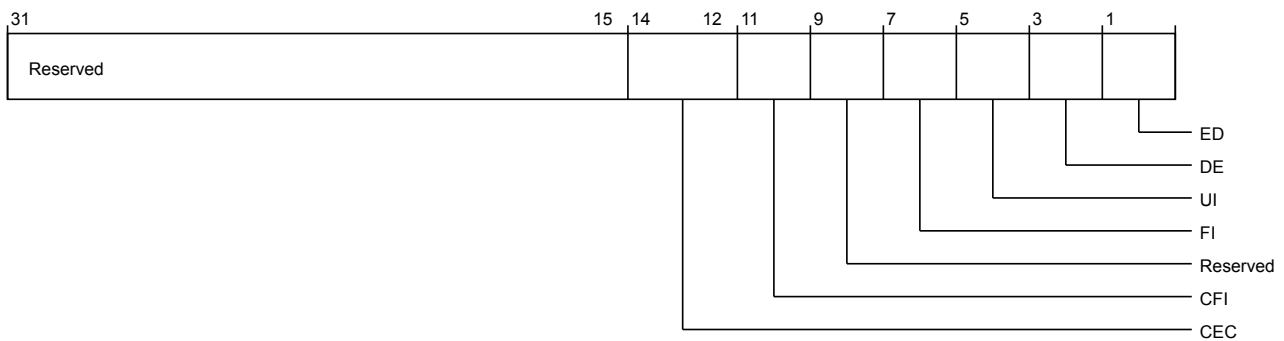


Figure 4-343 por_hnf_errfr_NS (low)

The following table shows the por_hnf_errfr_NS lower register bit assignments.

Table 4-360 por_hnf_errfr_NS (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in por_hnf_errmisc_NS[39:32] 3'b100: Implements 16-bit error counter in por_hnf_errmisc_NS[47:32]	RO	3'b100
11:10	CFI	Corrected error interrupt	RO	2'b10
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_hnf_errctlr_NS

Functions as the non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3108
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

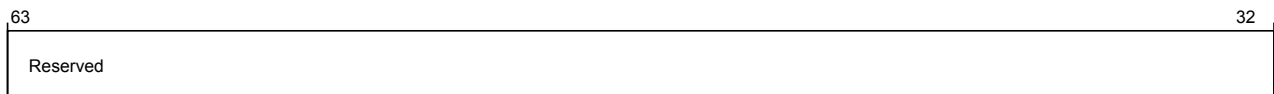


Figure 4-344 por_hnf_errctlr_ns (high)

The following table shows the por_hnf_errctlr_NS higher register bit assignments.

Table 4-361 por_hnf_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

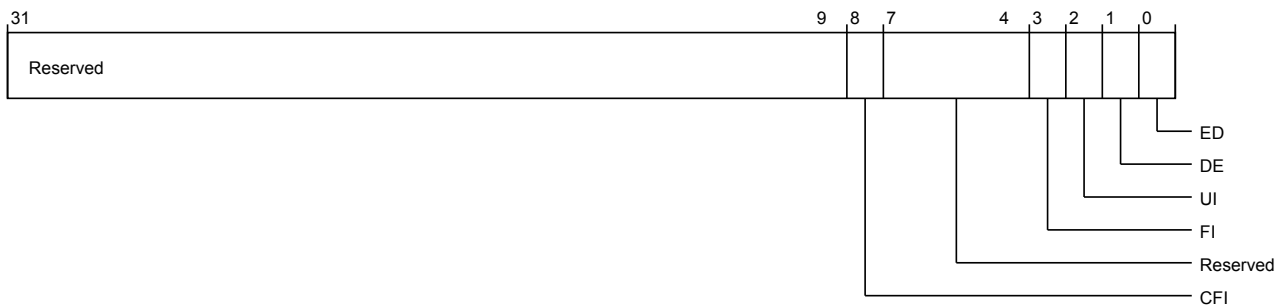


Figure 4-345 por_hnf_errctlr_ns (low)

The following table shows the por_hnf_errctlr_NS lower register bit assignments.

Table 4-362 por_hnf_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hnf_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-

Table 4-362 por_hnf_por_hnf_errctlr_ns (low) (continued)

Bits	Field name	Description	Type	Reset
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hnf_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hnf_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hnf_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hnf_errfr_NS.ED	RW	1'b0

por_hnf_errstatus_NS

Functions as the non-secure error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3110
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

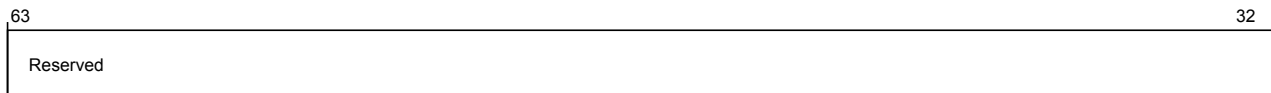


Figure 4-346 por_hnf_por_hnf_errstatus_ns (high)

The following table shows the por_hnf_errstatus_NS higher register bit assignments.

Table 4-363 por_hnf_por_hnf_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

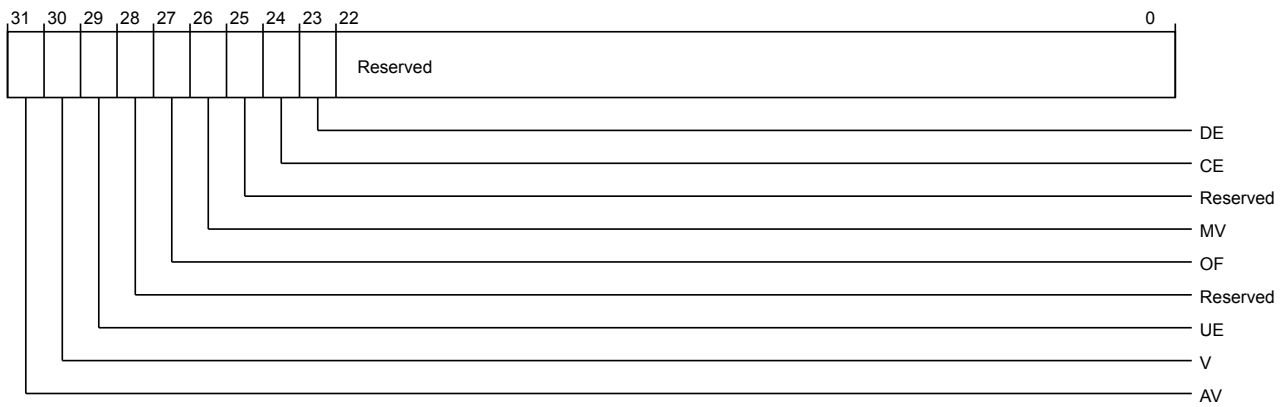


Figure 4-347 `por_hnf_por_hnf_errstatus_ns (low)`

The following table shows the `por_hnf_errstatus_NS` lower register bit assignments.

Table 4-364 `por_hnf_por_hnf_errstatus_ns (low)`

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; <code>por_hnf_erraddr_NS</code> contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	<code>por_hnf_errmisc_NS</code> valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 4-364 `por_hnf_por_hnf_errstatus_ns` (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

`por_hnf_erraddr_NS`

Contains the non-secure error record address.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3118
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

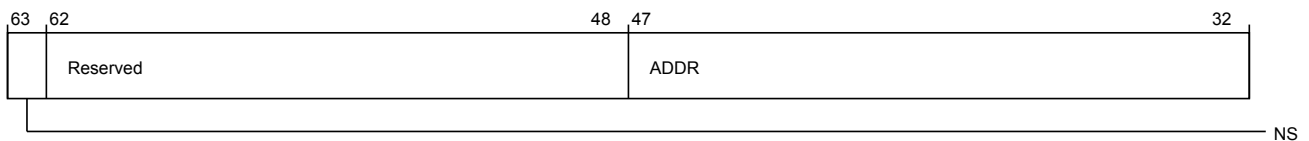


Figure 4-348 `por_hnf_por_hnf_erraddr_ns` (high)

The following table shows the `por_hnf_erraddr_NS` higher register bit assignments.

Table 4-365 `por_hnf_por_hnf_erraddr_ns` (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: <code>por_hnf_erraddr_NS</code> .NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

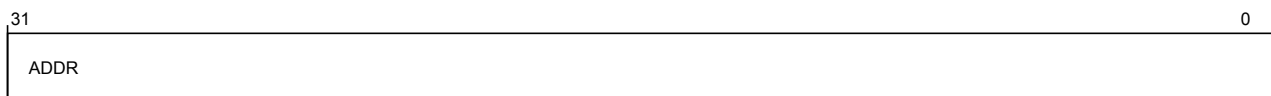


Figure 4-349 `por_hnf_por_hnf_erraddr_ns` (low)

The following table shows the `por_hnf_erraddr_NS` lower register bit assignments.

Table 4-366 `por_hnf_por_hnf_erraddr_ns` (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

`por_hnf_errmisc_NS`

Functions as the non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3120

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

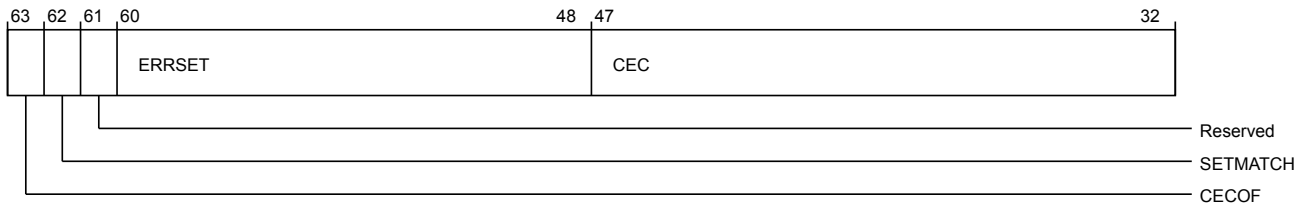


Figure 4-350 `por_hnf_por_hnf_errmisc_ns` (high)

The following table shows the `por_hnf_errmisc_NS` higher register bit assignments.

Table 4-367 `por_hnf_por_hnf_errmisc_ns` (high)

Bits	Field name	Description	Type	Reset
63	CECOF	Corrected error counter overflow	RW	1'b0
62	SETMATCH	Set address match	RW	1'b0
61	Reserved	Reserved	RO	-
60:48	ERRSET	SLC/SF set address for ECC error	RW	13'b0
47:32	CEC	Corrected ECC error count	RW	16'b0

The following image shows the lower register bit assignments.

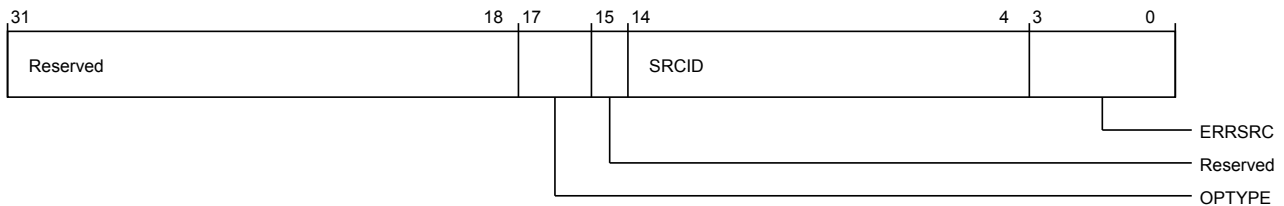


Figure 4-351 `por_hnf_por_hnf_errmisc_ns` (low)

The following table shows the `por_hnf_errmisc_NS` lower register bit assignments.

Table 4-368 `por_hnf_por_hnf_errmisc_ns` (low)

Bits	Field name	Description	Type	Reset
31:18	Reserved	Reserved	RO	-
17:16	OPTYPE	Error op type 2'b00: Writes, CleanShared, Atomics and stash requests with invalid targets 2'b01: WriteBack, Evict, and Stash requests with valid target 2'b10: CMO 2'b11: Other op types	RW	2'b00

Table 4-368 `por_hnf_por_hnf_errmisc_ns` (low) (continued)

Bits	Field name	Description	Type	Reset
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	ERRSRC	Error source 4'b0001: Data single-bit ECC 4'b0010: Data double-bit ECC 4'b0011: Single-bit ECC overflow 4'b0100: Tag single-bit ECC 4'b0101: Tag double-bit ECC 4'b0111: SF tag single-bit ECC 4'b1000: SF tag double-bit ECC 4'b1010: Data parity error 4'b1011: Data parity and poison 4'b1100: NDE	RW	4'b0000

`por_hnf_slc_lock_ways`

Controls SLC way lock settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC00

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Secure group override `por_hnf_secure_register_groups_override.slc_lock_ways`

The following image shows the higher register bit assignments.

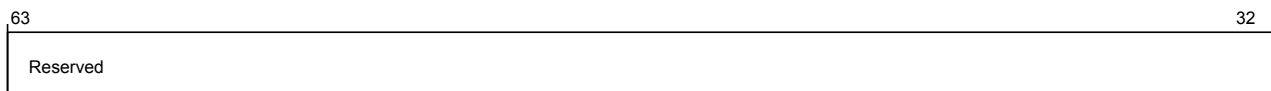


Figure 4-352 `por_hnf_por_hnf_slc_lock_ways` (high)

The following table shows the `por_hnf_slc_lock_ways` higher register bit assignments.

Table 4-369 `por_hnf_por_hnf_slc_lock_ways` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

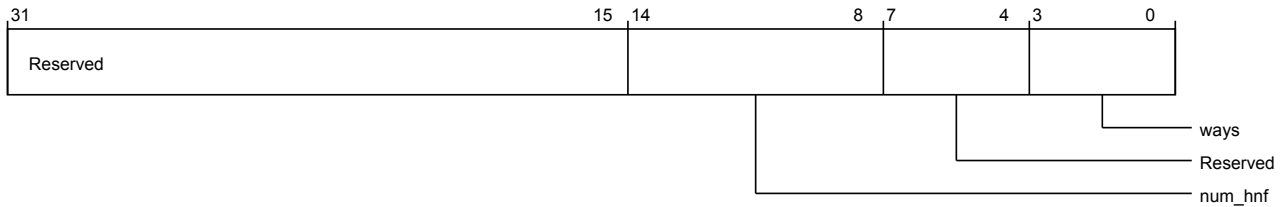


Figure 4-353 `por_hnf_por_hnf_slc_lock_ways` (low)

The following table shows the `por_hnf_slc_lock_ways` lower register bit assignments.

Table 4-370 `por_hnf_por_hnf_slc_lock_ways` (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:8	num_hnf	Number of HN-Fs in NUMA (non-uniform memory access) region	RW	Configuration dependent
7:4	Reserved	Reserved	RO	-
3:0	ways	Number of SLC ways locked (1, 2, 4, 8, 12)	RW	4'b0

`por_hnf_slc_lock_base0`

Functions as the base register for lock region 0 [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Secure group override `por_hnf_secure_register_groups_override.slc_lock_ways`

The following image shows the higher register bit assignments.

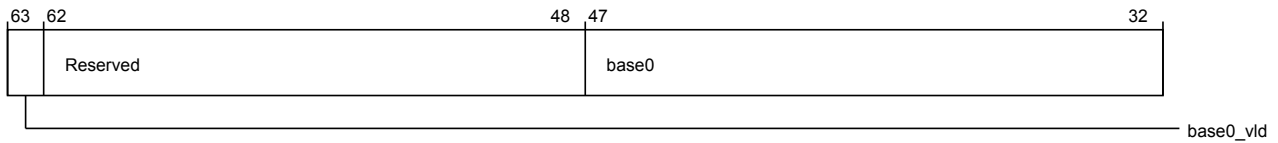


Figure 4-354 `por_hnf_por_hnf_slc_lock_base0` (high)

The following table shows the `por_hnf_slc_lock_base0` higher register bit assignments.

Table 4-371 `por_hnf_por_hnf_slc_lock_base0` (high)

Bits	Field name	Description	Type	Reset
63	<code>base0_vld</code>	Lock region 0 base valid	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	<code>base0</code>	Lock region 0 base address	RW	48'b0

The following image shows the lower register bit assignments.

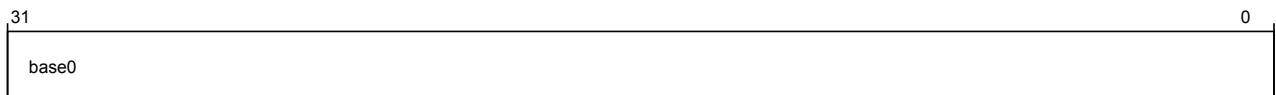


Figure 4-355 `por_hnf_por_hnf_slc_lock_base0` (low)

The following table shows the `por_hnf_slc_lock_base0` lower register bit assignments.

Table 4-372 `por_hnf_por_hnf_slc_lock_base0` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>base0</code>	Lock region 0 base address	RW	48'b0

`por_hnf_slc_lock_base1`

Functions as the base register for lock region 1 [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Secure group override `por_hnf_secure_register_groups_override.slc_lock_ways`

The following image shows the higher register bit assignments.

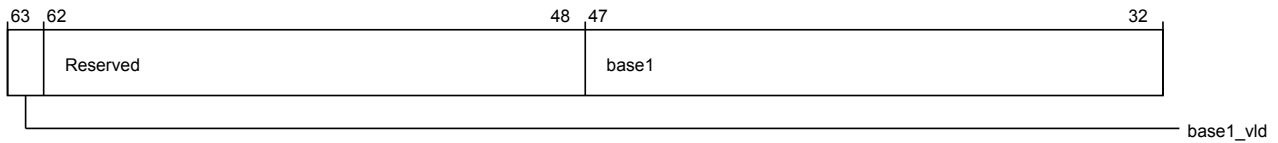


Figure 4-356 por_hnf_por_hnf_slc_lock_base1 (high)

The following table shows the por_hnf_slc_lock_base1 higher register bit assignments.

Table 4-373 por_hnf_por_hnf_slc_lock_base1 (high)

Bits	Field name	Description	Type	Reset
63	base1_vld	Lock region 1 base valid	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	base1	Lock region 1 base address	RW	48'b0

The following image shows the lower register bit assignments.

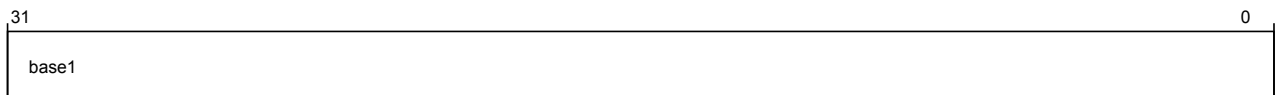


Figure 4-357 por_hnf_por_hnf_slc_lock_base1 (low)

The following table shows the por_hnf_slc_lock_base1 lower register bit assignments.

Table 4-374 por_hnf_por_hnf_slc_lock_base1 (low)

Bits	Field name	Description	Type	Reset
31:0	base1	Lock region 1 base address	RW	48'b0

por_hnf_slc_lock_base2

Functions as the base register for lock region 2 [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC18

Register reset 64'b0

Usage constraints Only accessible by secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

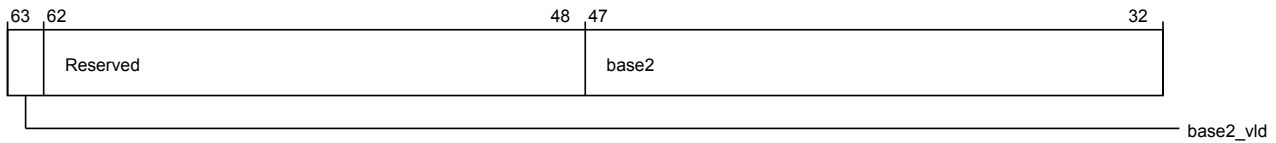


Figure 4-358 `por_hnf_por_hnf_slc_lock_base2` (high)

The following table shows the `por_hnf_slc_lock_base2` higher register bit assignments.

Table 4-375 `por_hnf_por_hnf_slc_lock_base2` (high)

Bits	Field name	Description	Type	Reset
63	<code>base2_vld</code>	Lock region 2 base valid	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	<code>base2</code>	Lock region 2 base address	RW	48'b0

The following image shows the lower register bit assignments.

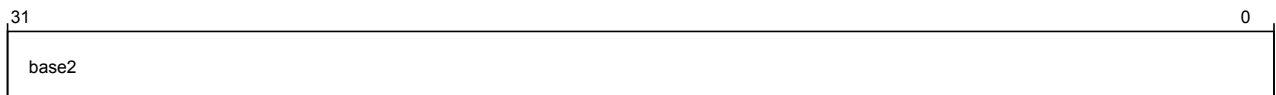


Figure 4-359 `por_hnf_por_hnf_slc_lock_base2` (low)

The following table shows the `por_hnf_slc_lock_base2` lower register bit assignments.

Table 4-376 `por_hnf_por_hnf_slc_lock_base2` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>base2</code>	Lock region 2 base address	RW	48'b0

`por_hnf_slc_lock_base3`

Functions as the base register for lock region 3 [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC20

Register reset 64'b0

Usage constraints Only accessible by secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Secure group override `por_hnf_secure_register_groups_override.slc_lock_ways`

The following image shows the higher register bit assignments.

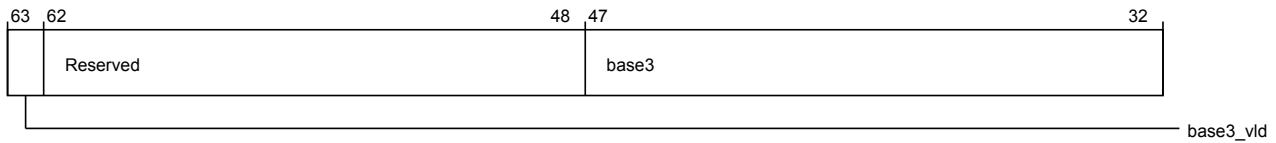


Figure 4-360 por_hnf_por_hnf_slc_lock_base3 (high)

The following table shows the por_hnf_slc_lock_base3 higher register bit assignments.

Table 4-377 por_hnf_por_hnf_slc_lock_base3 (high)

Bits	Field name	Description	Type	Reset
63	base3_vld	Lock region 3 base valid	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	base3	Lock region 3 base address	RW	48'b0

The following image shows the lower register bit assignments.

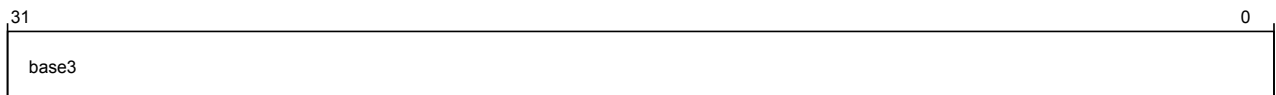


Figure 4-361 por_hnf_por_hnf_slc_lock_base3 (low)

The following table shows the por_hnf_slc_lock_base3 lower register bit assignments.

Table 4-378 por_hnf_por_hnf_slc_lock_base3 (low)

Bits	Field name	Description	Type	Reset
31:0	base3	Lock region 3 base address	RW	48'b0

por_hnf_rni_region_vec

Functions as the control register for RN-I source SLC way allocation.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC30
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

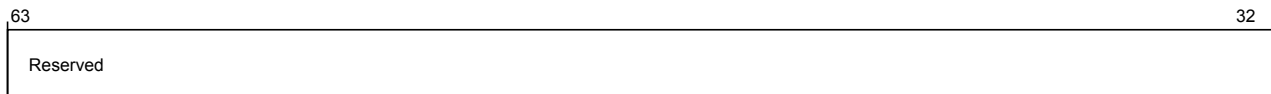


Figure 4-362 por_hnf_por_hnf_rni_region_vec (high)

The following table shows the por_hnf_rni_region_vec higher register bit assignments.

Table 4-379 por_hnf_por_hnf_rni_region_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

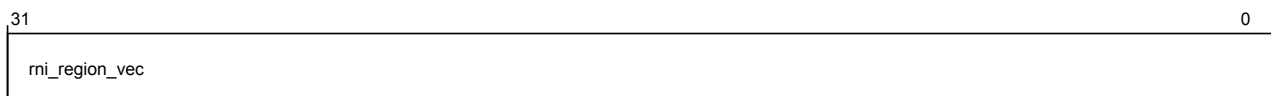


Figure 4-363 por_hnf_por_hnf_rni_region_vec (low)

The following table shows the por_hnf_rni_region_vec lower register bit assignments.

Table 4-380 por_hnf_por_hnf_rni_region_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_region_vec	Bit vector mask; identifies which logical IDs of the RN-Is to allocate to the locked region NOTE: Must be set to 32'b0 if range-based region locking or OCM is enabled.	RW	32'b0

por_hnf_rnf_region_vec

Functions as the control register for RN-F source SLC way allocation.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC38
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

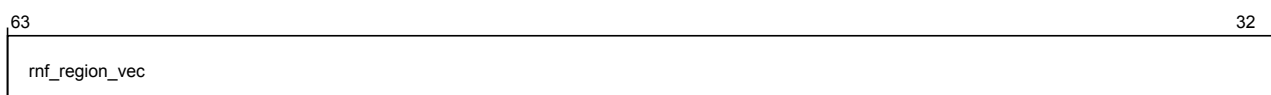


Figure 4-364 por_hnf_por_hnf_rnf_region_vec (high)

The following table shows the por_hnf_rnf_region_vec higher register bit assignments.

Table 4-381 por_hnf_por_hnf_rnf_region_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_region_vec	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

The following image shows the lower register bit assignments.



Figure 4-365 por_hnf_por_hnf_rnf_region_vec (low)

The following table shows the por_hnf_rnf_region_vec lower register bit assignments.

Table 4-382 por_hnf_por_hnf_rnf_region_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_region_vec	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

por_hnf_rnd_region_vec

Functions as the control register for RN-D source SLC way allocation.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC40
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

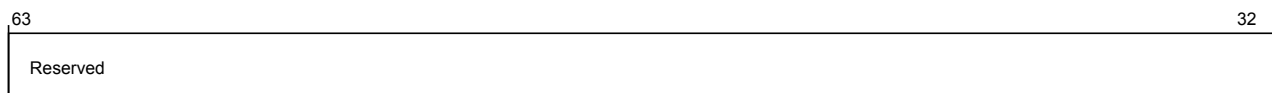


Figure 4-366 por_hnf_por_hnf_rnd_region_vec (high)

The following table shows the por_hnf_rnd_region_vec higher register bit assignments.

Table 4-383 `por_hnf_por_hnf_rnd_region_vec` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

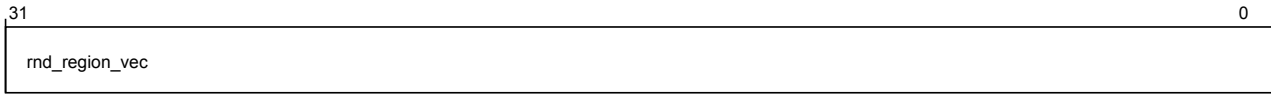


Figure 4-367 `por_hnf_por_hnf_rnd_region_vec` (low)

The following table shows the `por_hnf_rnd_region_vec` lower register bit assignments.

Table 4-384 `por_hnf_por_hnf_rnd_region_vec` (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_region_vec	Bit vector mask; identifies which logical IDs of the RN-Ds to allocate to the locked region NOTE: Must be set to 32'b0 if range-based region locking or OCM is enabled.	RW	32'b0

por_hnf_slcway_partition0_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset	14'hC48
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[illegible]

Usage constraints	Only accessible by secure accesses.
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Secure group override	por_hnf_secure_register_groups_override.slz_lock_ways
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The following image shows the higher register bit assignments.

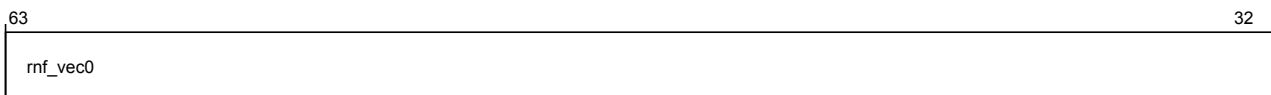


Figure 4-368 `por_hnf_por_hnf_slcway_partition0_rnf_vec` (high)

The following table shows the `por` `hnf` `slcway` `partition0` `rnf` `vec` higher register bit assignments.

Table 4-385 por hnf por hnf slcway partition0 rnf vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec0	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

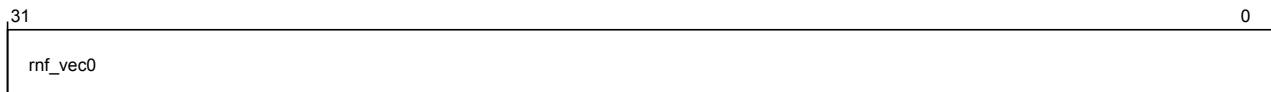


Figure 4-369 `por_hnf_por_hnf_slcway_partition0_rnf_vec` (low)

The following table shows the `por_hnf_slcway_partition0_rnf_vec` lower register bit assignments.

Table 4-386 por_hnf_por_hnf_slcway_partition0_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec0	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition1_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 1 (ways 4, 5, 6, and 7).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC50

[illegible]

Usage constraints	Only accessible by secure accesses.
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Secure group override `por_hnf_secure_register_groups_override.slc_lock_ways`

The following image shows the higher register bit assignments.

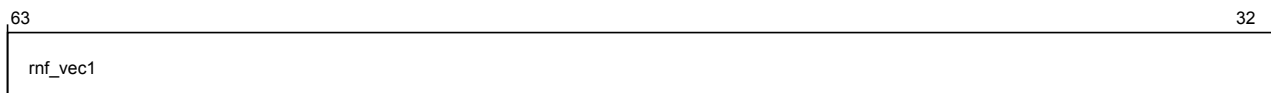


Figure 4-370 `por_hnf_por_hnf_slcway_partition1_rnf_vec` (high)

The following table shows the por_hnf_slcway_partition1_rnf_vec higher register bit assignments.

Table 4-387 `por_hnf_por_hnf_slcway_partition1_rnf_vec` (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec1	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

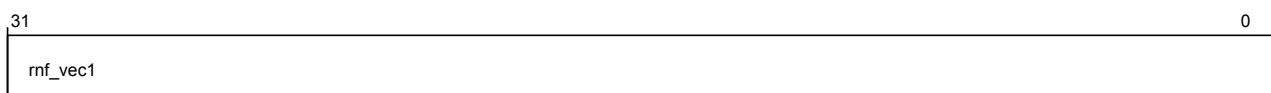


Figure 4-371 `por_hnf_por_hnf_slcway_partition1_rnf_vec` (low)

The following table shows the por_hnf_slcway_partition1_rnf_vec lower register bit assignments.

Table 4-388 por_hnf_por_hnf_slcway_partition1_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec1	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition2_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 2 (ways 8, 9, 10, and 11).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC58

[illegible]

Usage constraints	Only accessible by secure accesses.
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Secure group override `por_hnf_secure_register_groups_override.slc_lock_ways`

The following image shows the higher register bit assignments.

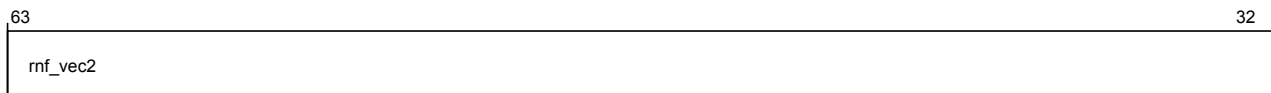


Figure 4-372 `por_hnf_por_hnf_slcway_partition2_rnf_vec` (high)

The following table shows the `por_hnf_slcway_partition2_rnf_vec` higher register bit assignments.

Table 4-389 `por_hnf_por_hnf_slcway_partition2_rnf_vec` (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec2	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

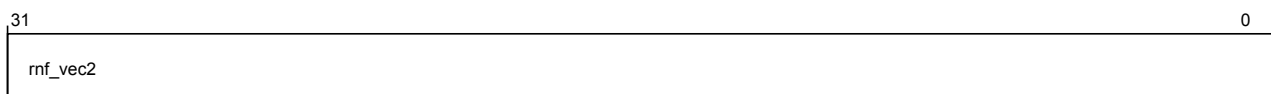


Figure 4-373 `por_hnf_por_hnf_slcway_partition2_rnf_vec` (low)

The following table shows the `por_hnf_slcway_partition2_rnf_vec` lower register bit assignments.

Table 4-390 `por_hnf_por_hnf_slcway_partition2_rnf_vec` (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec2	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition3_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 3 (ways 12, 13, 14, and 15).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC60
Register reset	64'b11
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

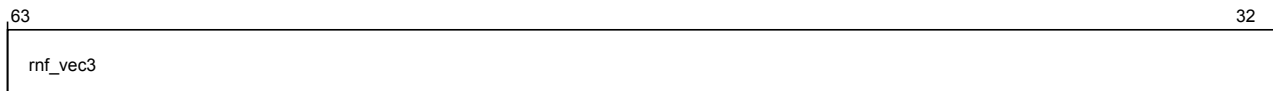


Figure 4-374 por_hnf_por_hnf_slcway_partition3_rnf_vec (high)

The following table shows the por_hnf_slcway_partition3_rnf_vec higher register bit assignments.

Table 4-391 por_hnf_por_hnf_slcway_partition3_rnf_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec3	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

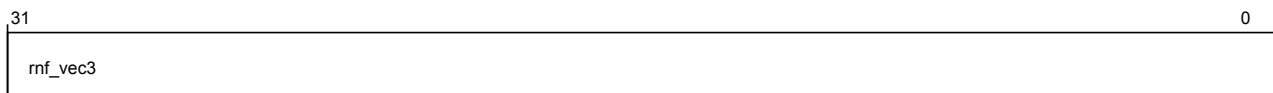


Figure 4-375 por_hnf_por_hnf_slcway_partition3_rnf_vec (low)

The following table shows the por_hnf_slcway_partition3_rnf_vec lower register bit assignments.

Table 4-392 por_hnf_por_hnf_slcway_partition3_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec3	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_rnf_region_vec1

Functions as the control register for RN-F source SLC way allocation for logical IDs 64 through 127.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC28
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways
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The following image shows the higher register bit assignments.

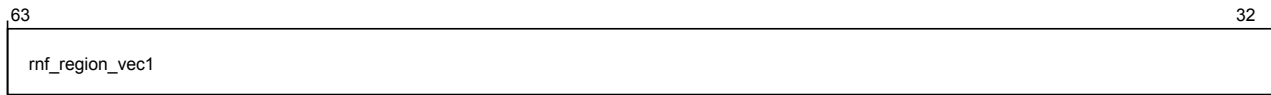


Figure 4-376 `por_hnf_por_hnf_rnf_region_vec1` (high)

The following table shows the `por_hnf_rnf_region_vec1` higher register bit assignments.

Table 4-393 por_hnf_por_hnf_rnf_region_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rmf_region_vec1	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

The following image shows the lower register bit assignments.

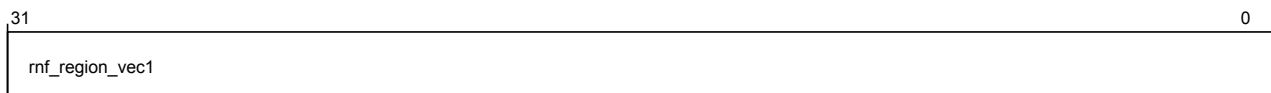


Figure 4-377 `por_hnf_por_hnf_rnf_region_vec1` (low)

The following table shows the `por_hnf_rnf_region_vec1` lower register bit assignments.

Table 4-394 `por_hnf_por_hnf_rnf_region_vec1` (low)

Bits	Field name	Description	Type	Reset
31:0	rmf_region_vec1	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

por_hnf_slcway_partition0_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCB0

[illegible]

Usage constraints	Only accessible by secure accesses.
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Secure group override `por_hnf_secure_register_groups_override.slc_lock_ways`

The following image shows the higher register bit assignments.

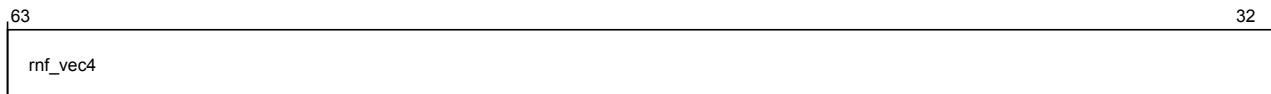


Figure 4-378 por_hnf_por_hnf_slcway_partition0_rnf_vec1 (high)

The following table shows the `por_hnf_slcway_partition0_rnf_vec1` higher register bit assignments.

Table 4-395 por_hnf_por_hnf_slcway_partition0_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec4	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

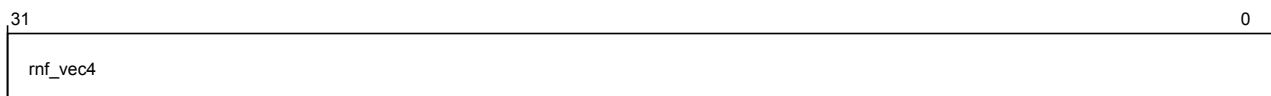


Figure 4-379 por_hnf_por_hnf_slcway_partition0_rnf_vec1 (low)

The following table shows the `por_hnf_slcway_partition0_rnf_vec1` lower register bit assignments.

Table 4-396 `por_hnf_por_hnf_slcway_partition0_rnf_vec1` (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec4	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition1_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 1 (ways 4, 5, 6, and 7) for Logical RNF IDs 64 to 127.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCB8
Register reset	64'b11
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

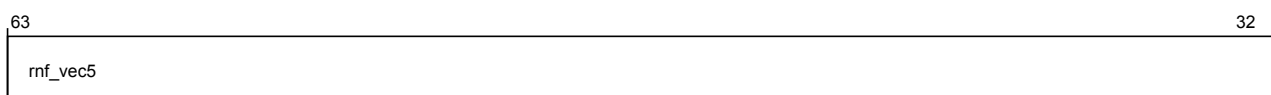


Figure 4-380 por_hnf_por_hnf_slcway_partition1_rnf_vec1 (high)

The following table shows the `por_hnf_slcway_partition1_rnf_vec1` higher register bit assignments.

Table 4-397 por_hnf_por_hnf_slcway_partition1_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec5	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

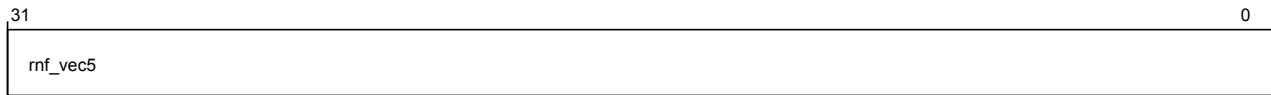


Figure 4-381 `por_hnf_por_hnf_slcway_partition1_rnf_vec1` (low)

The following table shows the `por_hnf_slcway_partition1_rnf_vec1` lower register bit assignments.

Table 4-398 por_hnf_por_hnf_slcway_partition1_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	mf_vec5	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition2_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 2 (ways 8, 9, 10, and 11) for Logical RNF IDs 64 to 127.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset	14'hCC0
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[illegible]

Usage constraints	Only accessible by secure accesses.
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Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways
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The following image shows the higher register bit assignments.

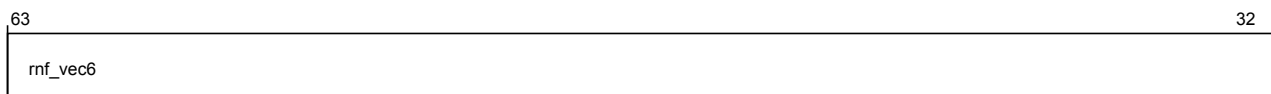


Figure 4-382 `por_hnf_por_hnf_slcway_partition2 rnf_vec1` (high)

The following table shows the `por_hnf_slcway_partition2_rnf_vec1` higher register bit assignments.

Table 4-399 por_hnf_por_hnf_slcway_partition2_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec6	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

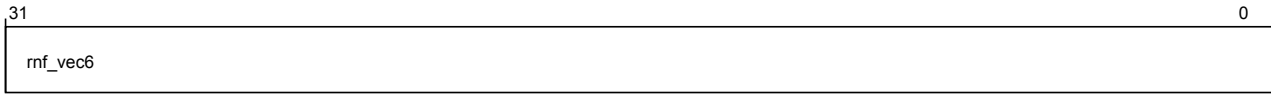


Figure 4-383 por_hnf_por_hnf_slcway_partition2_rnf_vec1 (low)

The following table shows the `por_hnf_slcway_partition2_rnf_vec1` lower register bit assignments.

Table 4-400 por_hnf_por_hnf_slcway_partition2_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec6	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition3_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 3 (ways 12, 13, 14, and 15) for Logical RNF IDs 64 to 127.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCC8

[illegible]

Usage constraints	Only accessible by secure accesses.
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Secure group override `por_hnf_secure_register_groups_override.slc_lock_ways`

The following image shows the higher register bit assignments.

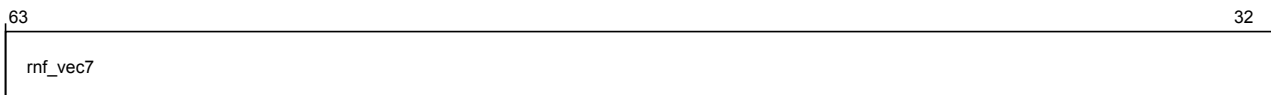


Figure 4-384 `por_hnf_por_hnf_slcway_partition3_rnf_vec1` (high)

The following table shows the `por_hnf_slcway_partition3_rnf_vec1` higher register bit assignments.

Table 4-401 `por_hnf_por_hnf_slcway_partition3_rnf_vec1` (high)

Bits	Field name	Description	Type	Reset
63:32	rmf_vec7	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

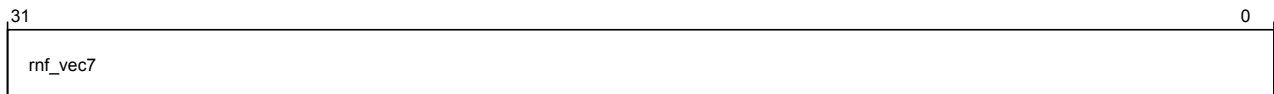


Figure 4-385 por_hnf_por_hnf_slcway_partition3_rnf_vec1 (low)

The following table shows the por_hnf_slcway_partition3_rnf_vec1 lower register bit assignments.

Table 4-402 por_hnf_por_hnf_slcway_partition3_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec7	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition0_rni_vec

Functions as the control register for RN-Is that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC68
Register reset	64'b11111111111111111111111111111111
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

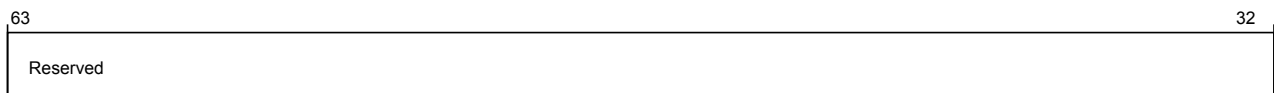


Figure 4-386 por_hnf_por_hnf_slcway_partition0_rni_vec (high)

The following table shows the por_hnf_slcway_partition0_rni_vec higher register bit assignments.

Table 4-403 por_hnf_por_hnf_slcway_partition0_rni_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

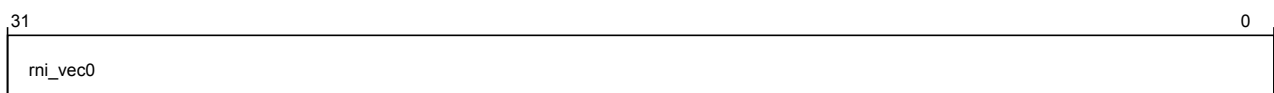


Figure 4-387 por_hnf_por_hnf_slcway_partition0_rni_vec (low)

The following table shows the por_hnf_slcway_partition0_rni_vec lower register bit assignments.

Table 4-404 por_hnf_por_hnf_slcway_partition0_rni_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec0	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition1_rni_vec

Functions as the control register for RN-Is that can allocate to partition 1 (ways 4, 5, 6, and 7).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC70
Register reset	64'b11111111111111111111111111111111
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

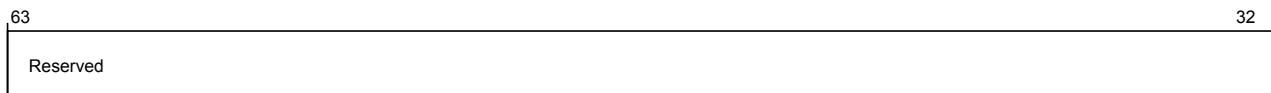


Figure 4-388 por_hnf_por_hnf_slcway_partition1_rni_vec (high)

The following table shows the por_hnf_slcway_partition1_rni_vec higher register bit assignments.

Table 4-405 por_hnf_por_hnf_slcway_partition1_rni_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

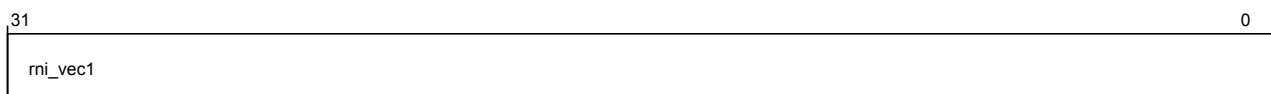


Figure 4-389 por_hnf_por_hnf_slcway_partition1_rni_vec (low)

The following table shows the por_hnf_slcway_partition1_rni_vec lower register bit assignments.

Table 4-406 por_hnf_por_hnf_slcway_partition1_rni_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec1	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition2_rni_vec

Functions as the control register for RN-Is that can allocate to partition 2 (ways 8, 9, 10, and 11).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC78
Register reset	64'b11111111111111111111111111111111
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

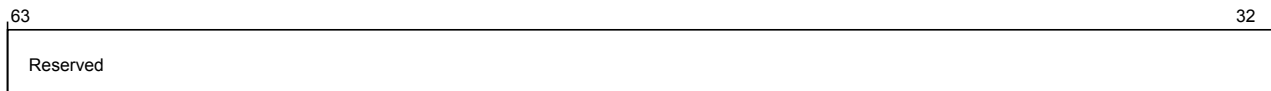


Figure 4-390 `por_hnf_por_hnf_slcway_partition2_rni_vec (high)`

The following table shows the `por_hnf_slcway_partition2_rni_vec` higher register bit assignments.

Table 4-407 `por_hnf_por_hnf_slcway_partition2_rni_vec (high)`

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

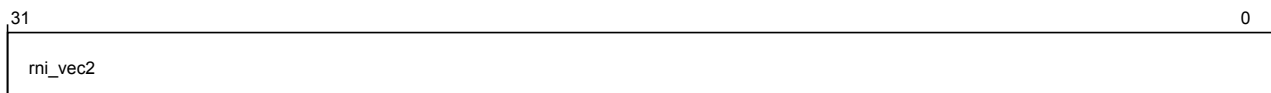


Figure 4-391 `por_hnf_por_hnf_slcway_partition2_rni_vec (low)`

The following table shows the `por_hnf_slcway_partition2_rni_vec` lower register bit assignments.

Table 4-408 `por_hnf_por_hnf_slcway_partition2_rni_vec (low)`

Bits	Field name	Description	Type	Reset
31:0	rni_vec2	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

`por_hnf_slcway_partition3_rni_vec`

Functions as the control register for RN-Is that can allocate to partition 3 (ways 12, 13, 14, and 15).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC80
Register reset	64'b11111111111111111111111111111111
Usage constraints	Only accessible by secure accesses.

Secure group override `por_hnf_secure_register_groups_override.slc_lock_ways`

The following image shows the higher register bit assignments.

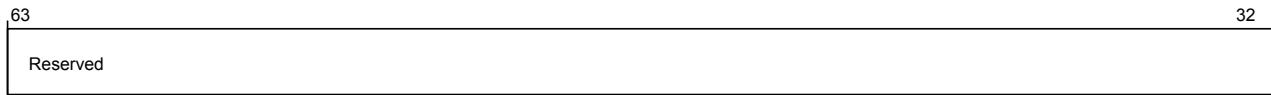


Figure 4-392 `por_hnf_slcway_partition3_rni_vec` (high)

The following table shows the `por_hnf_slcway_partition3_rni_vec` higher register bit assignments.

Table 4-409 `por_hnf_slcway_partition3_rni_vec` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

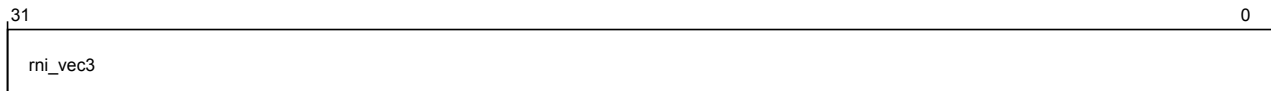


Figure 4-393 `por_hnf_slcway_partition3_rni_vec` (low)

The following table shows the `por_hnf_slcway_partition3_rni_vec` lower register bit assignments.

Table 4-410 `por_hnf_slcway_partition3_rni_vec` (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec3	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

`por_hnf_slcway_partition0_rnd_vec`

Functions as the control register for RN-Ds that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC88

Register reset 64'b11111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override `por_hnf_secure_register_groups_override.slc_lock_ways`

The following image shows the higher register bit assignments.

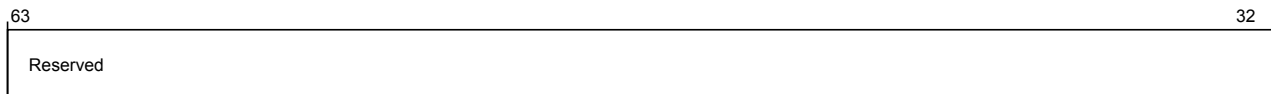


Figure 4-394 por_hnf_por_hnf_slcway_partition0_rnd_vec (high)

The following table shows the por_hnf_slcway_partition0_rnd_vec higher register bit assignments.

Table 4-411 por_hnf_por_hnf_slcway_partition0_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

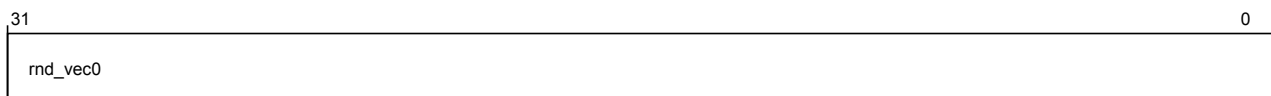


Figure 4-395 por_hnf_por_hnf_slcway_partition0_rnd_vec (low)

The following table shows the por_hnf_slcway_partition0_rnd_vec lower register bit assignments.

Table 4-412 por_hnf_por_hnf_slcway_partition0_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec0	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition1_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 1 (ways 4, 5, 6, and 7).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC90
Register reset	64'b11111111111111111111111111111111
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

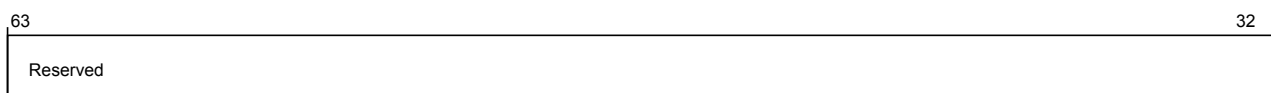


Figure 4-396 por_hnf_por_hnf_slcway_partition1_rnd_vec (high)

The following table shows the por_hnf_slcway_partition1_rnd_vec higher register bit assignments.

Table 4-413 por_hnf_por_hnf_slcway_partition1_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.



Figure 4-397 por_hnf_por_hnf_slcway_partition1_rnd_vec (low)

The following table shows the por_hnf_slcway_partition1_rnd_vec lower register bit assignments.

Table 4-414 por_hnf_por_hnf_slcway_partition1_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec1	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition2_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 2 (ways 8, 9, 10, and 11).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC98
Register reset	64'b11111111111111111111111111111111
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

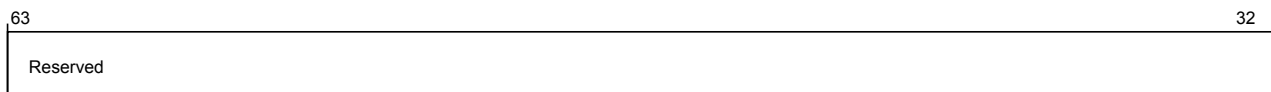


Figure 4-398 por_hnf_por_hnf_slcway_partition2_rnd_vec (high)

The following table shows the por_hnf_slcway_partition2_rnd_vec higher register bit assignments.

Table 4-415 por_hnf_por_hnf_slcway_partition2_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

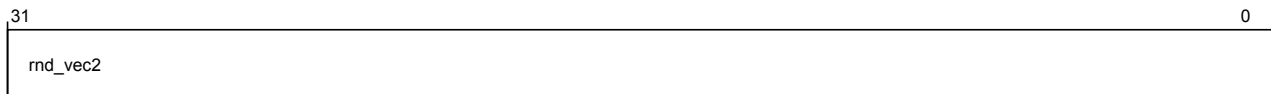


Figure 4-399 por_hnf_slcway_partition2_rnd_vec (low)

The following table shows the por_hnf_slcway_partition2_rnd_vec lower register bit assignments.

Table 4-416 por_hnf_slcway_partition2_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec2	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition3_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 3 (ways 12, 13, 14, and 15).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCA0
Register reset	64'b11111111111111111111111111111111
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.



Figure 4-400 por_hnf_slcway_partition3_rnd_vec (high)

The following table shows the por_hnf_slcway_partition3_rnd_vec higher register bit assignments.

Table 4-417 por_hnf_slcway_partition3_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

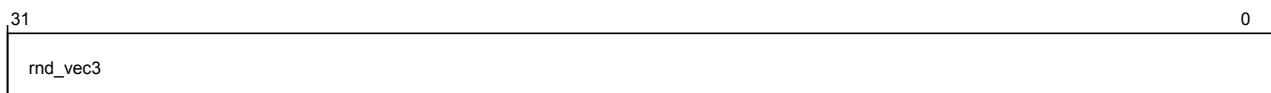


Figure 4-401 por_hnf_slcway_partition3_rnd_vec (low)

The following table shows the por_hnf_slcway_partition3_rnd_vec lower register bit assignments.

Table 4-418 `por_hnf_por_hnf_slcway_partition3_rnd_vec` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>rnd_vec3</code>	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

`por_hnf_rn_region_lock`

Functions as the enable register for source-based SLC way allocation.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hCA8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_hnf_secure_register_groups_override.slc_lock_ways</code>

The following image shows the higher register bit assignments.

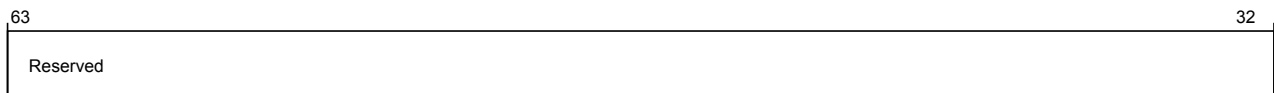


Figure 4-402 `por_hnf_por_hnf_rn_region_lock` (high)

The following table shows the `por_hnf_rn_region_lock` higher register bit assignments.

Table 4-419 `por_hnf_por_hnf_rn_region_lock` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

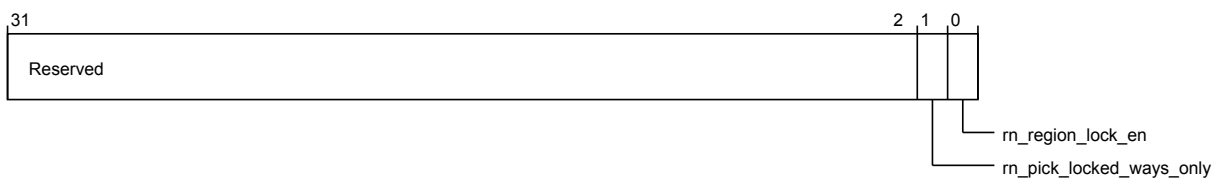


Figure 4-403 `por_hnf_por_hnf_rn_region_lock` (low)

The following table shows the `por_hnf_rn_region_lock` lower register bit assignments.

Table 4-420 `por_hnf_por_hnf_rn_region_lock` (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	<code>rn_pick_locked_ways_only</code>	Specifies which ways the programmed RNs can allocate new cache lines to 1'b0: Programmed RN will choose all ways including locked 1'b1: Programmed RN will only allocate in locked ways	RW	1'b0
0	<code>rn_region_lock_en</code>	Enables SRC-based region locking 1'b0: SRC based way locking is disabled 1'b1: SRC based way locking is enabled	RW	1'b0

`por_hnf_sam_control`

Configures HN-F SAM. All `top_address_bit` fields must be between bits 47 and 28 of the address.
`top_address_bit2 > top_address_bit1 > top_address_bit0`. Must be configured to match corresponding `por_rnsam_sys_cache_grp_sn_sam_cfgN` register in the RN SAM.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_hnf_secure_register_groups_override.sam_control</code>

The following image shows the higher register bit assignments.

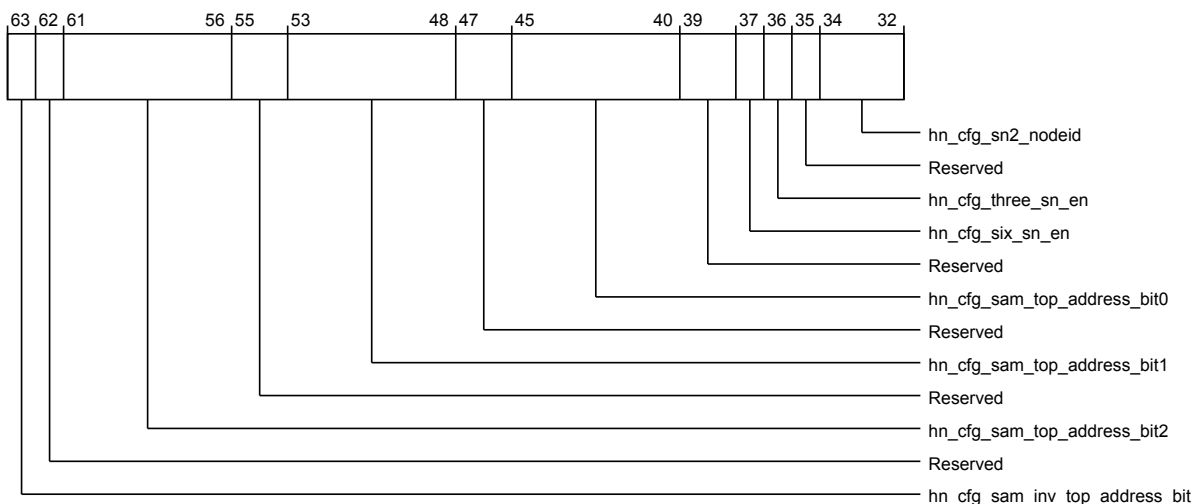


Figure 4-404 `por_hnf_por_hnf_sam_control` (high)

The following table shows the `por_hnf_sam_control` higher register bit assignments.

Table 4-421 por_hnf_por_hnf_sam_control (high)

Bits	Field name	Description	Type	Reset
63	hn_cfg_sam_inv_top_address_bit	Inverts the top address bit (hn_cfg_sam_top_address_bit1 if 3-SN, hn_cfg_sam_top_address_bit2 if 6-SN) NOTE: Can only be used when the address map does not have unique address bit combinations.	RW	1'h0
62	Reserved	Reserved	RO	-
61:56	hn_cfg_sam_top_address_bit2	Bit position of top_address_bit2; used for address hashing in 6-SN configuration	RW	6'h00
55:54	Reserved	Reserved	RO	-
53:48	hn_cfg_sam_top_address_bit1	Bit position of top_address_bit1; used for address hashing in 3-SN/6-SN configuration	RW	6'h00
47:46	Reserved	Reserved	RO	-
45:40	hn_cfg_sam_top_address_bit0	Bit position of top_address_bit0; used for address hashing in 3-SN/6-SN configuration	RW	6'h00
39:38	Reserved	Reserved	RO	-
37	hn_cfg_six_sn_en	Enables 6-SN configuration	RW	1'b0
36	hn_cfg_three_sn_en	Enables 3-SN configuration	RW	1'b0
35	Reserved	Reserved	RO	-
34:32	hn_cfg_sn2_nodeid	SN 2 node ID	RW	11'h0

The following image shows the lower register bit assignments.

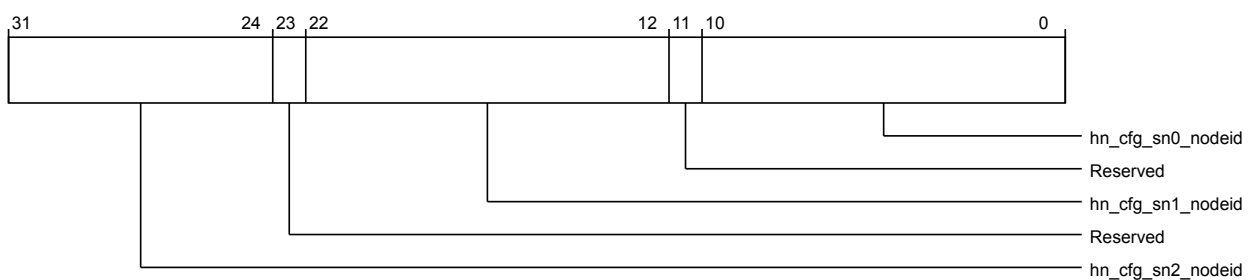


Figure 4-405 por_hnf_por_hnf_sam_control (low)

The following table shows the `por_hnf_sam_control` lower register bit assignments.

Table 4-422 por_hnf_por_hnf_sam_control (low)

Bits	Field name	Description	Type	Reset
31:24	hn_cfg_sn2_nodeid	SN 2 node ID	RW	11'h0
23	Reserved	Reserved	RO	-

Table 4-422 `por_hnf_por_hnf_sam_control` (low) (continued)

Bits	Field name	Description	Type	Reset
22:12	<code>hn_cfg_sn1_nodeid</code>	SN 1 node ID	RW	11'h0
11	Reserved	Reserved	RO	-
10:0	<code>hn_cfg_sn0_nodeid</code>	SN 0 node ID	RW	11'h0

`por_hnf_sam_memregion0`

Configures range-based memory region 0 in HN-F SAM.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD08
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_hnf_secure_register_groups_override.sam_control</code>

The following image shows the higher register bit assignments.

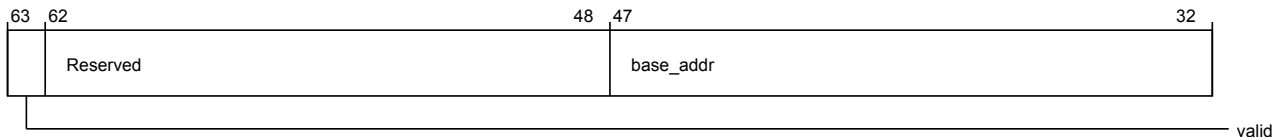


Figure 4-406 `por_hnf_por_hnf_sam_memregion0` (high)

The following table shows the `por_hnf_sam_memregion0` higher register bit assignments.

Table 4-423 `por_hnf_por_hnf_sam_memregion0` (high)

Bits	Field name	Description	Type	Reset
63	valid	Memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'h0
62:48	Reserved	Reserved	RO	-
47:32	<code>base_addr</code>	Base address of memory region 0 CONSTRAINT: Must be an integer multiple of region size.	RW	22'h0

The following image shows the lower register bit assignments.

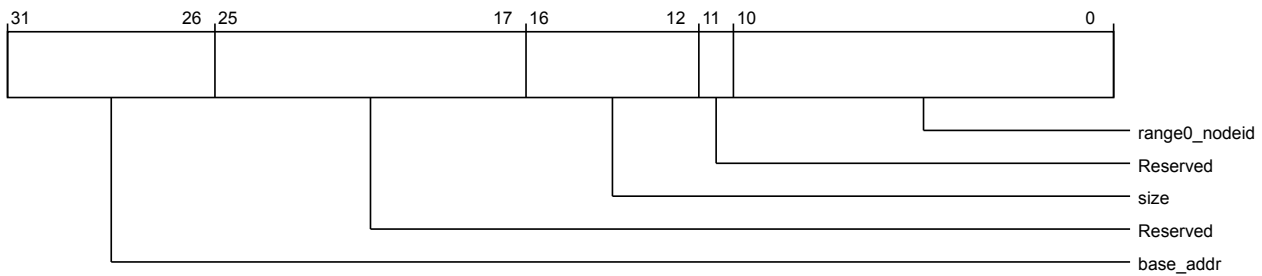


Figure 4-407 por_hnf_por_hnf_sam_memregion0 (low)

The following table shows the por_hnf_sam_memregion0 lower register bit assignments.

Table 4-424 por_hnf_por_hnf_sam_memregion0 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Base address of memory region 0 CONSTRAINT: Must be an integer multiple of region size.	RW	22'h0
25:17	Reserved	Reserved	RO	-
16:12	size	Memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2 ^{address width}).	RW	5'h0
11	Reserved	Reserved	RO	-
10:0	range0_nodeid	Memory region 0 target node ID	RW	11'h0

por_hnf_sam_memregion1

Configures range-based memory region 1 in HN-F SAM.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD10
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

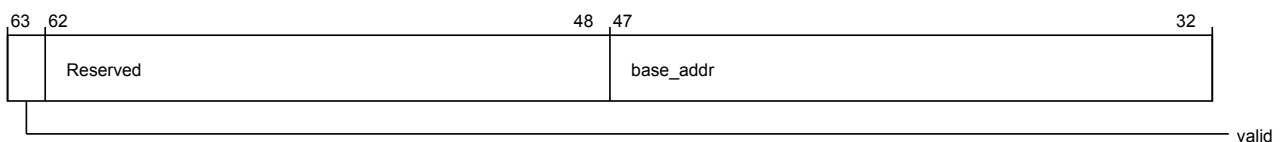


Figure 4-408 por_hnf_por_hnf_sam_memregion1 (high)

The following table shows the por_hnf_sam_memregion1 higher register bit assignments.

Table 4-425 por_hnf_por_hnf_sam_memregion1 (high)

Bits	Field name	Description	Type	Reset
63	valid	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'h0
62:48	Reserved	Reserved	RO	-
47:32	base_addr	Base address of memory region 1 CONSTRAINT: Must be an integer multiple of region size.	RW	22'h0

The following image shows the lower register bit assignments.

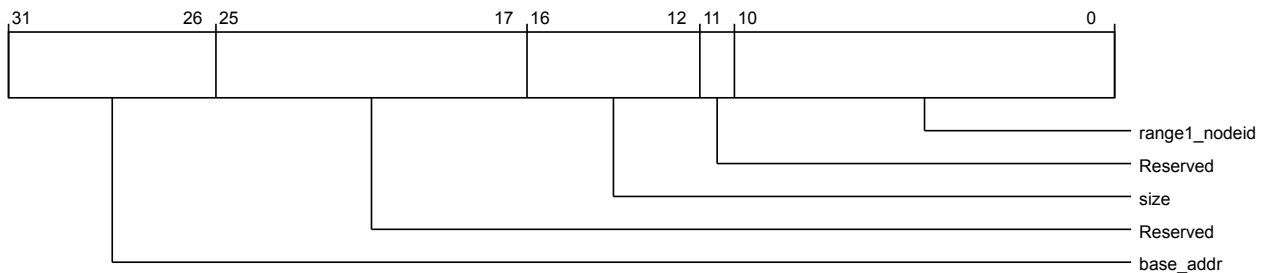


Figure 4-409 por_hnf_por_hnf_sam_memregion1 (low)

The following table shows the por_hnf_sam_memregion1 lower register bit assignments.

Table 4-426 por_hnf_por_hnf_sam_memregion1 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Base address of memory region 1 CONSTRAINT: Must be an integer multiple of region size.	RW	22'h0
25:17	Reserved	Reserved	RO	-
16:12	size	Memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'h0
11	Reserved	Reserved	RO	-
10:0	range1_nodeid	Memory region 1 target node ID	RW	11'h0

por_hnf_sam_sn_properties

Configures properties for all six SN targets and two range-based SN targets.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD18
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

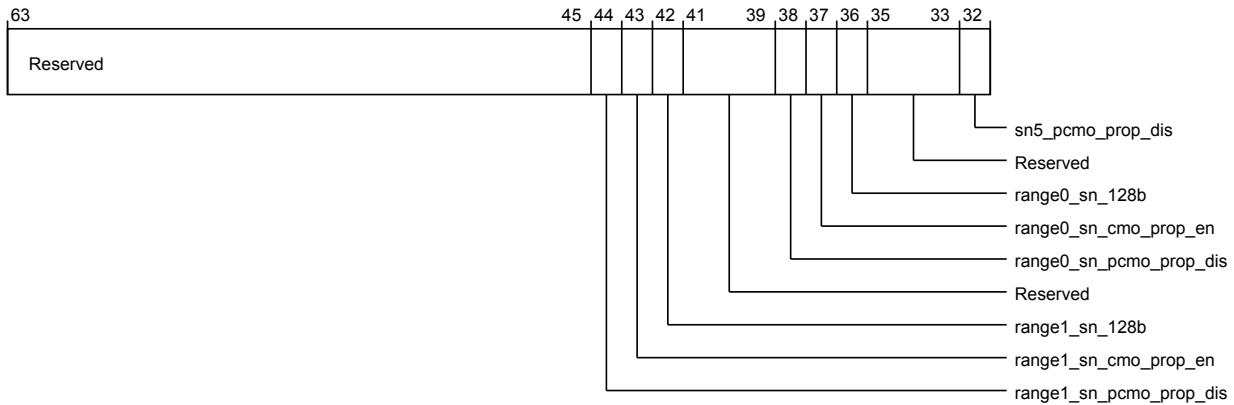


Figure 4-410 por_hnf_por_hnf_sam_sn_properties (high)

The following table shows the por_hnf_sam_sn_properties higher register bit assignments.

Table 4-427 por_hnf_por_hnf_sam_sn_properties (high)

Bits	Field name	Description	Type	Reset
63:45	Reserved	Reserved	RO	-
44	range1_sn_pcmo_prop_dis	Disables PCMO (persistent CMO) propagation for range 1 SN when set	RW	1'b0
43	range1_sn_cmo_prop_en	Enables CMO propagation for range 1 SN	RW	1'b0
42	range1_sn_128b	Data width of range 1 SN 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
41:39	Reserved	Reserved	RO	-
38	range0_sn_pcmo_prop_dis	Disables PCMO (persistent CMO) propagation for range 0 SN when set	RW	1'b0
37	range0_sn_cmo_prop_en	Enables CMO propagation for range 0 SN	RW	1'b0
36	range0_sn_128b	Data width of range 0 SN 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
35:33	Reserved	Reserved	RO	-
32	sn5_pcmo_prop_dis	Disables PCMO propagation for SN 5 when set	RW	1'b0

The following image shows the lower register bit assignments.

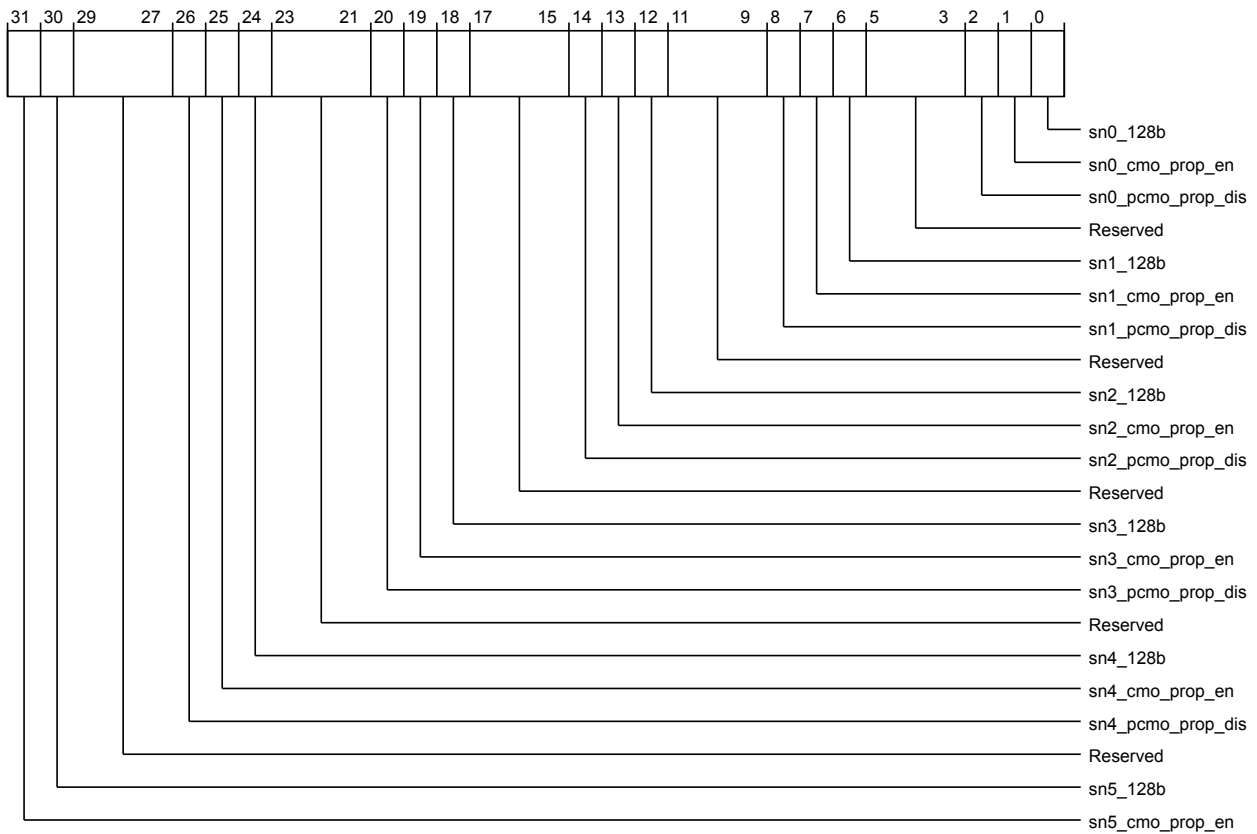


Figure 4-411 por_hnf_por_hnf_sam_sn_properties (low)

The following table shows the por_hnf_sam_sn_properties lower register bit assignments.

Table 4-428 por_hnf_por_hnf_sam_sn_properties (low)

Bits	Field name	Description	Type	Reset
31	sn5_cmo_prop_en	Enables CMO propagation for SN 5 when set	RW	1'b0
30	sn5_128b	Data width of SN 5 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
29:27	Reserved	Reserved	RO	-
26	sn4_pcmo_prop_dis	Disables PCMO propagation for SN 4 when set	RW	1'b0
25	sn4_cmo_prop_en	Enables CMO propagation for SN 4 when set	RW	1'b0
24	sn4_128b	Data width of SN 4 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
23:21	Reserved	Reserved	RO	-

Table 4-428 `por_hnf_por_hnf_sam_sn_properties` (low) (continued)

Bits	Field name	Description	Type	Reset
20	<code>sn3_pcmo_prop_dis</code>	Disables PCMO propagation for SN 3 when set	RW	1'b0
19	<code>sn3_cmo_prop_en</code>	Enables CMO propagation for SN 3 when set	RW	1'b0
18	<code>sn3_128b</code>	Data width of SN 3 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
17:15	Reserved	Reserved	RO	-
14	<code>sn2_pcmo_prop_dis</code>	Disables PCMO propagation for SN 2 when set	RW	1'b0
13	<code>sn2_cmo_prop_en</code>	Enables CMO propagation for SN 2 when set	RW	1'b0
12	<code>sn2_128b</code>	Data width of SN 2 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
11:9	Reserved	Reserved	RO	-
8	<code>sn1_pcmo_prop_dis</code>	Disables PCMO propagation for SN 1 when set	RW	1'b0
7	<code>sn1_cmo_prop_en</code>	Enables CMO propagation for SN 1 when set	RW	1'b0
6	<code>sn1_128b</code>	Data width of SN 1 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
5:3	Reserved	Reserved	RO	-
2	<code>sn0_pcmo_prop_dis</code>	Disables PCMO propagation for SN 0 when set	RW	1'b0
1	<code>sn0_cmo_prop_en</code>	Enables CMO propagation for SN 0 when set	RW	1'b0
0	<code>sn0_128b</code>	Data width of SN 0 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0

`por_hnf_sam_6sn_nodeid`

Configures node IDs for slave nodes 3 to 5 in 6-SN configuration mode.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD20

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override `por_hnf_secure_register_groups_override.sam_control`

The following image shows the higher register bit assignments.

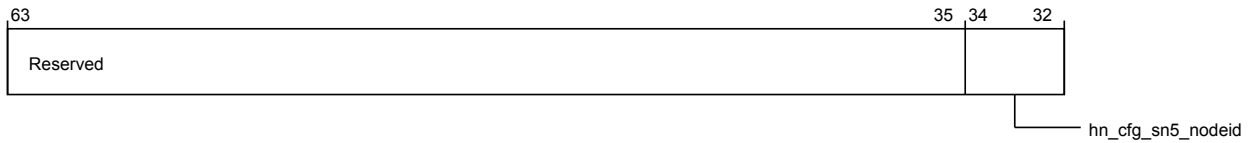


Figure 4-412 `por_hnf_por_hnf_sam_6sn_nodeid (high)`

The following table shows the `por_hnf_sam_6sn_nodeid` higher register bit assignments.

Table 4-429 `por_hnf_por_hnf_sam_6sn_nodeid (high)`

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	<code>hn_cfg_sn5_nodeid</code>	SN 5 node ID	RW	11'h0

The following image shows the lower register bit assignments.

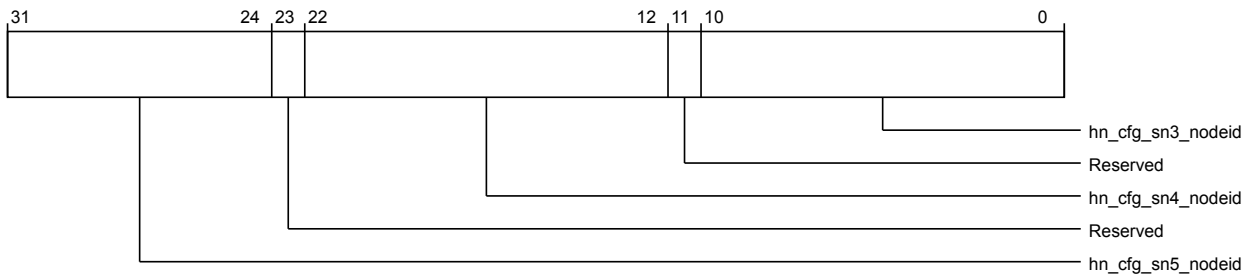


Figure 4-413 `por_hnf_por_hnf_sam_6sn_nodeid (low)`

The following table shows the `por_hnf_sam_6sn_nodeid` lower register bit assignments.

Table 4-430 `por_hnf_por_hnf_sam_6sn_nodeid (low)`

Bits	Field name	Description	Type	Reset
31:24	<code>hn_cfg_sn5_nodeid</code>	SN 5 node ID	RW	11'h0
23	Reserved	Reserved	RO	-
22:12	<code>hn_cfg_sn4_nodeid</code>	SN 4 node ID	RW	11'h0
11	Reserved	Reserved	RO	-
10:0	<code>hn_cfg_sn3_nodeid</code>	SN 3 node ID	RW	11'h0

`por_hnf_rn_phys_id0`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD28
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

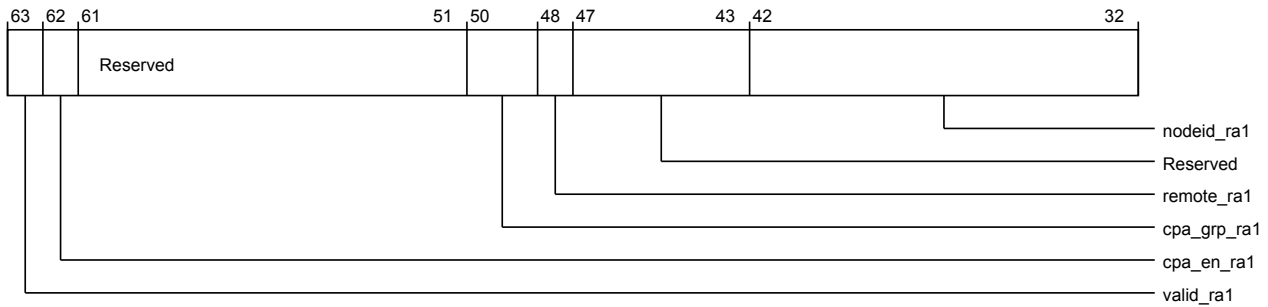


Figure 4-414 por_hnf_por_hnf_rn_phys_id0 (high)

The following table shows the por_hnf_rn_phys_id0 higher register bit assignments.

Table 4-431 por_hnf_por_hnf_rn_phys_id0 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra1	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra1	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra1	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra1	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0

Table 4-431 por_hnf_por_hnf_rn_phys_id0 (high) (continued)

Bits	Field name	Description	Type	Reset
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra1	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

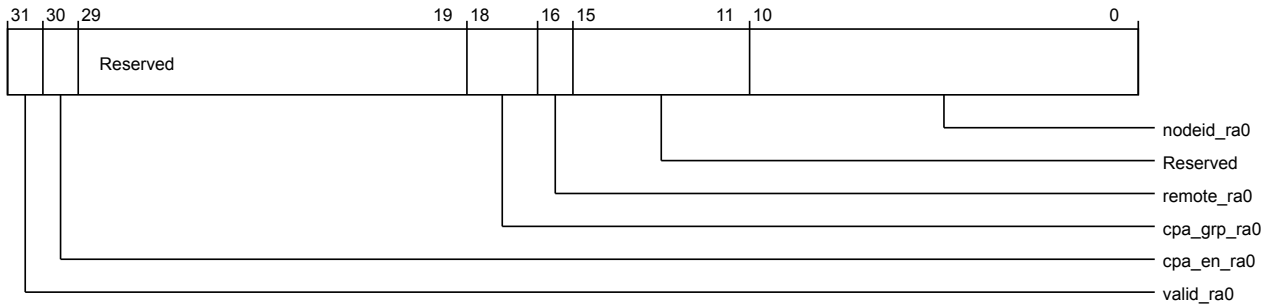


Figure 4-415 por_hnf_por_hnf_rn_phys_id0 (low)

The following table shows the por_hnf_rn_phys_id0 lower register bit assignments.

Table 4-432 por_hnf_por_hnf_rn_phys_id0 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra0	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra0	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra0	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra0	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra0	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id1

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD30
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

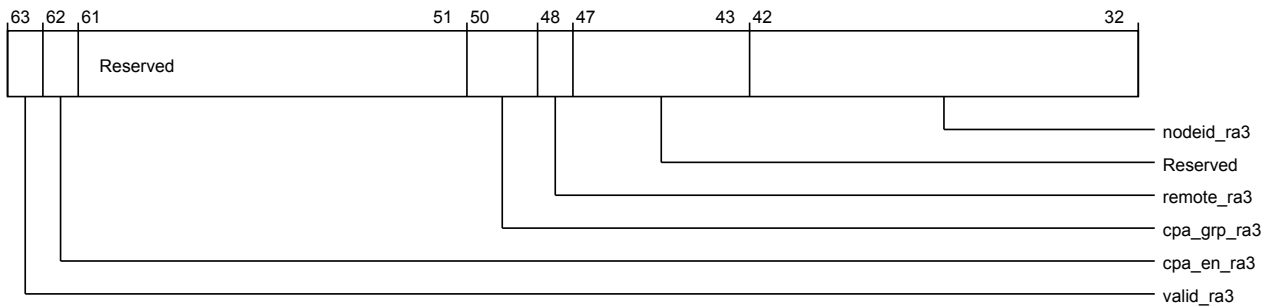


Figure 4-416 por_hnf_rn_phys_id1 (high)

The following table shows the por_hnf_rn_phys_id1 higher register bit assignments.

Table 4-433 por_hnf_rn_phys_id1 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra3	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra3	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra3	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0

Table 4-433 por_hnf_por_hnf_rn_phys_id1 (high) (continued)

Bits	Field name	Description	Type	Reset
48	remote_ra3	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra3	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

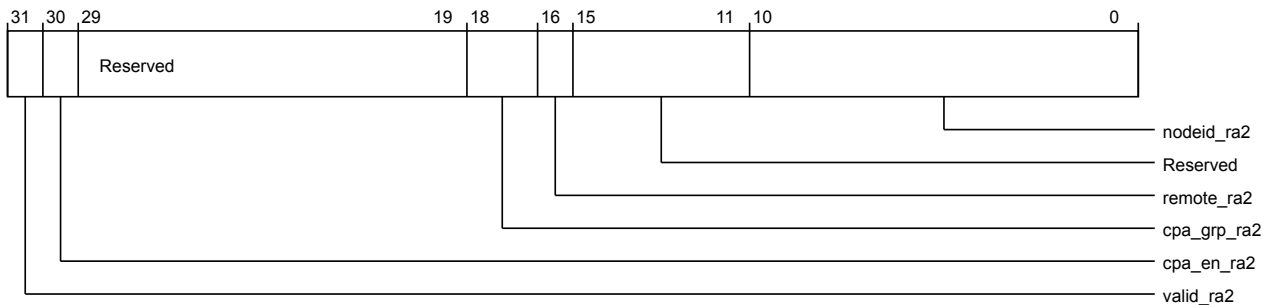


Figure 4-417 por_hnf_por_hnf_rn_phys_id1 (low)

The following table shows the `por_hnf_rn_phys_id1` lower register bit assignments.

Table 4-434 por_hnf_por_hnf_rn_phys_id1 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra2	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra2	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra2	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0

Table 4-434 por_hnf_por_hnf_rn_phys_id1 (low) (continued)

Bits	Field name	Description	Type	Reset
16	remote_ra2	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra2	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id2

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD38
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

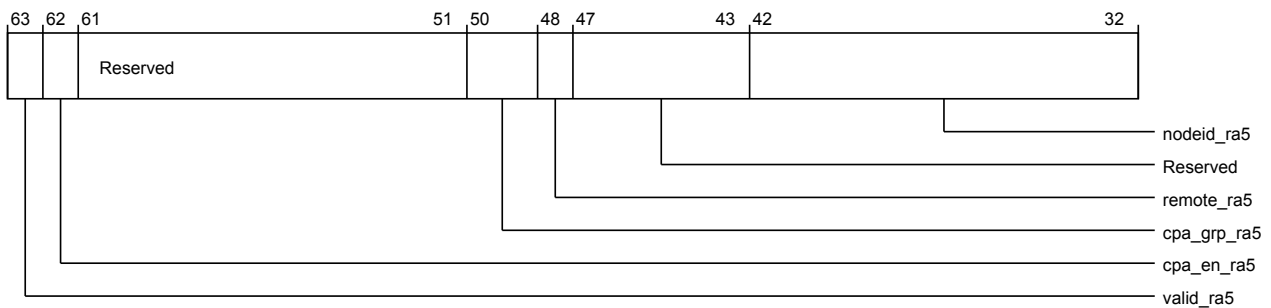


Figure 4-418 por_hnf_por_hnf_rn_phys_id2 (high)

The following table shows the `por_hnf_rn_phys_id2` higher register bit assignments.

Table 4-435 `por_hnf_por_hnf_rn_phys_id2` (high)

Bits	Field name	Description	Type	Reset
63	<code>valid_ra5</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	<code>cpa_en_ra5</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	<code>cpa_grp_ra5</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	<code>remote_ra5</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>nodeid_ra5</code>	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

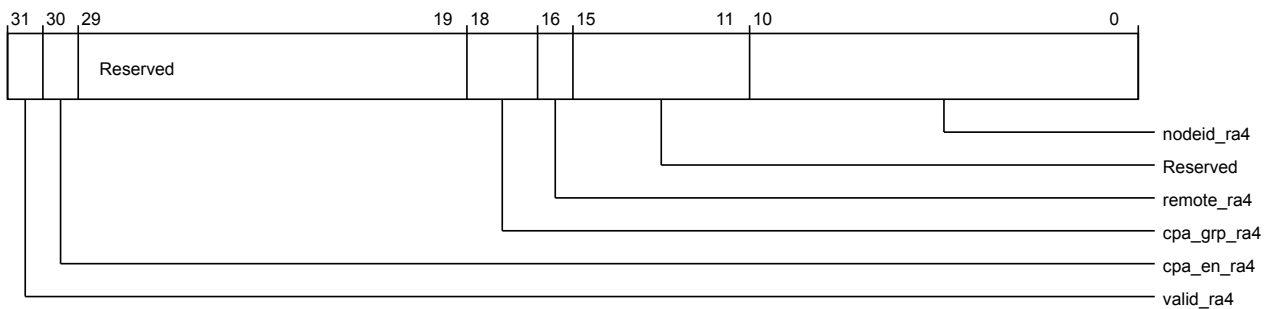


Figure 4-419 `por_hnf_por_hnf_rn_phys_id2` (low)

The following table shows the `por_hnf_rn_phys_id2` lower register bit assignments.

Table 4-436 `por_hnf_por_hnf_rn_phys_id2` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra4</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra4</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra4</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra4</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra4</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id3`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD40
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_hnf_secure_register_groups_override.sam_control</code>

The following image shows the higher register bit assignments.

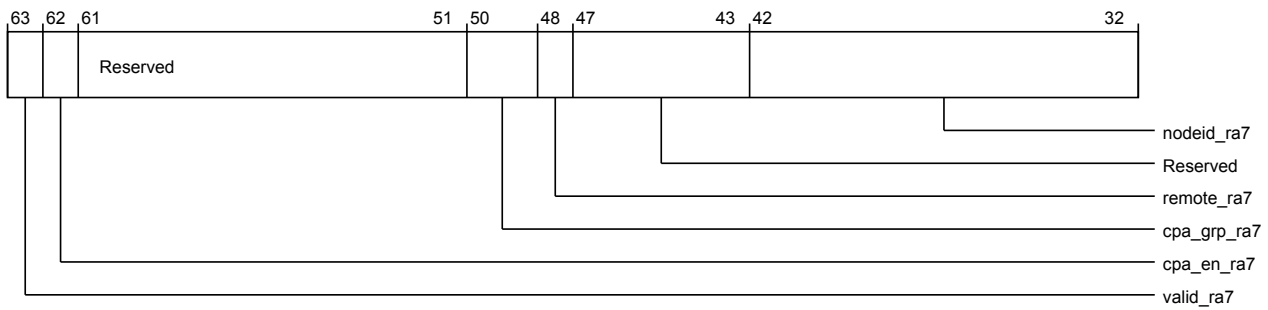


Figure 4-420 por_hnf_por_hnf_rn_phys_id3 (high)

The following table shows the por_hnf_rn_phys_id3 higher register bit assignments.

Table 4-437 por_hnf_por_hnf_rn_phys_id3 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra7	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra7	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra7	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra7	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra7	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

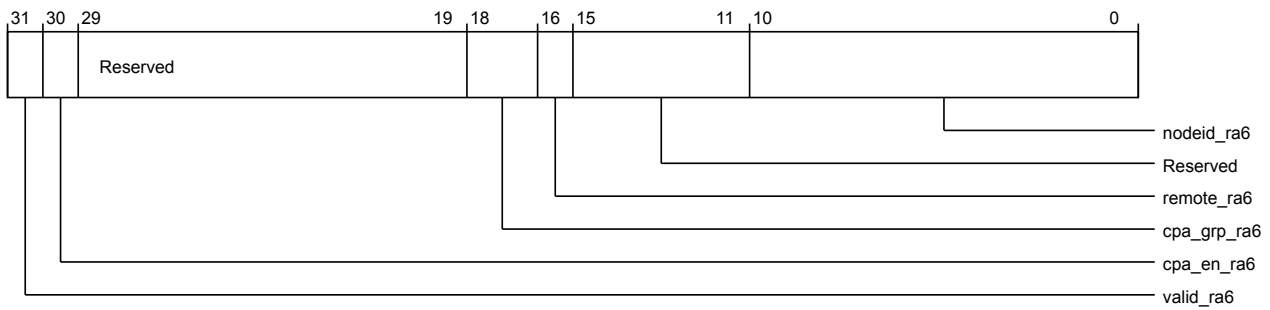


Figure 4-421 por_hnf_por_hnf_rn_phys_id3 (low)

The following table shows the por_hnf_rn_phys_id3 lower register bit assignments.

Table 4-438 por_hnf_por_hnf_rn_phys_id3 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra6	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra6	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra6	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra6	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra6	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id4

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD48

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

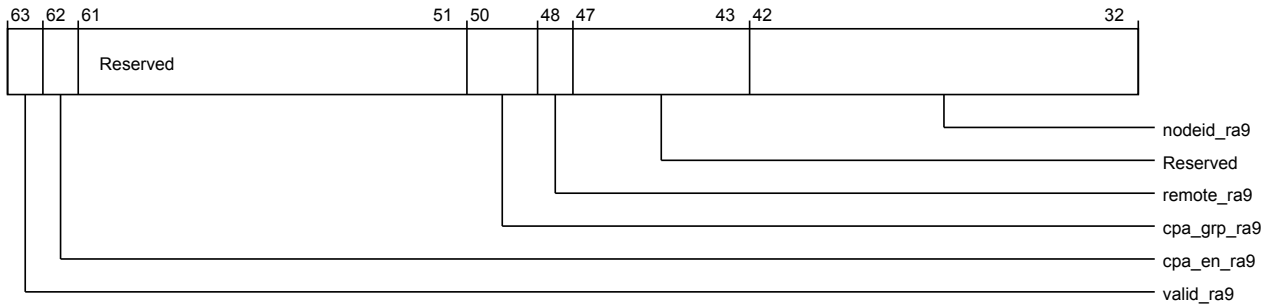


Figure 4-422 por_hnf_por_hnf_rn_phys_id4 (high)

The following table shows the por_hnf_rn_phys_id4 higher register bit assignments.

Table 4-439 por_hnf_por_hnf_rn_phys_id4 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra9	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra9	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra9	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra9	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra9	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

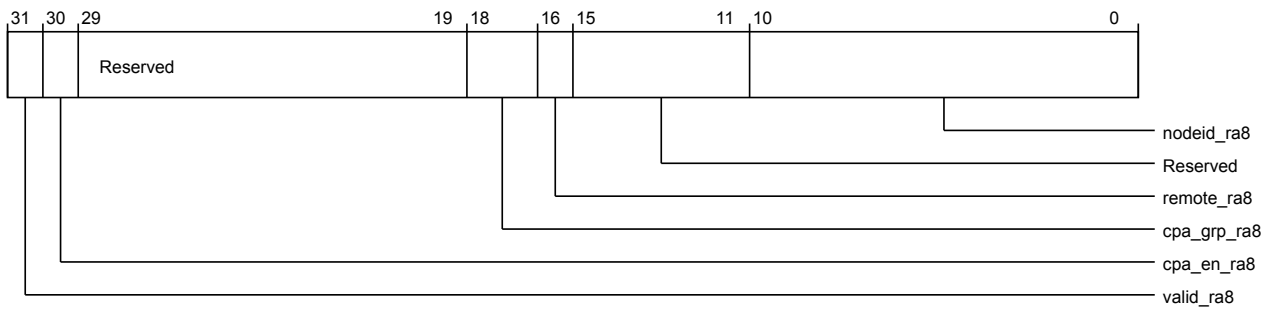


Figure 4-423 por_hnf_por_hnf_rn_phys_id4 (low)

The following table shows the por_hnf_rn_phys_id4 lower register bit assignments.

Table 4-440 por_hnf_por_hnf_rn_phys_id4 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra8	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra8	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra8	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra8	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra8	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id5

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD50

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

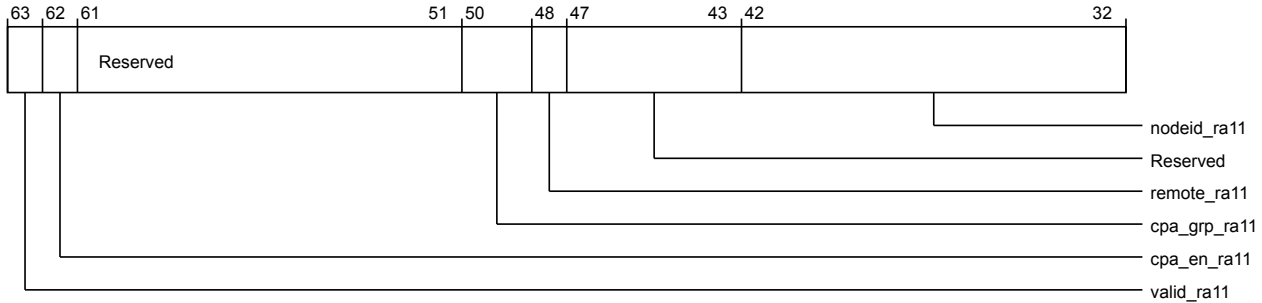


Figure 4-424 por_hnf_por_hnf_rn_phys_id5 (high)

The following table shows the por_hnf_rn_phys_id5 higher register bit assignments.

Table 4-441 por_hnf_por_hnf_rn_phys_id5 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra11	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra11	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra11	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra11	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra11	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

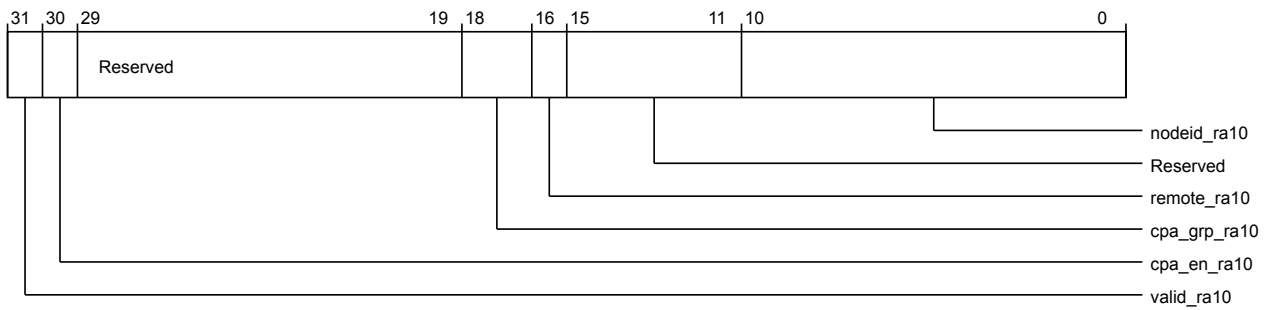


Figure 4-425 `por_hnf_por_hnf_rn_phys_id5` (low)

The following table shows the `por_hnf_rn_phys_id5` lower register bit assignments.

Table 4-442 `por_hnf_por_hnf_rn_phys_id5` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra10</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra10</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra10</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra10</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra10</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id6`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD58

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

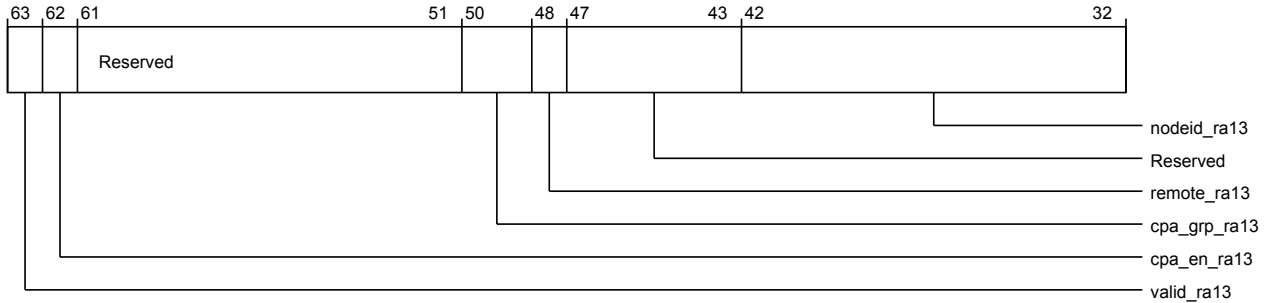


Figure 4-426 por_hnf_por_hnf_rn_phys_id6 (high)

The following table shows the por_hnf_rn_phys_id6 higher register bit assignments.

Table 4-443 por_hnf_por_hnf_rn_phys_id6 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra13	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra13	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra13	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra13	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra13	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

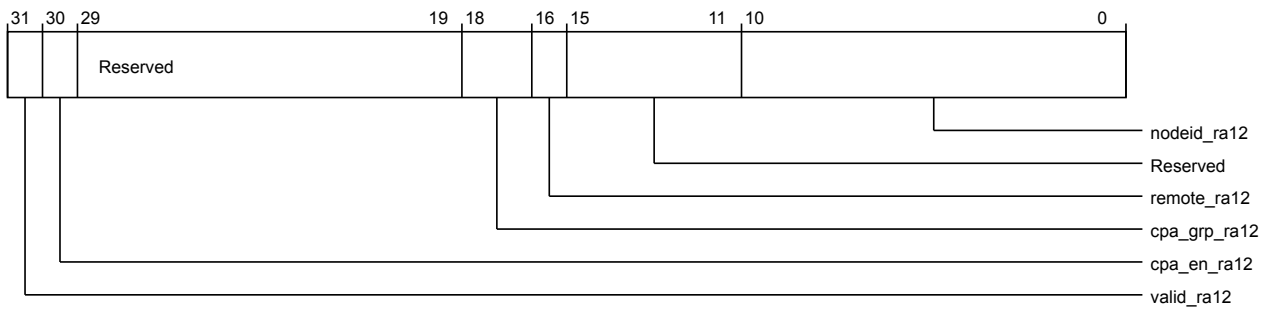


Figure 4-427 `por_hnf_por_hnf_rn_phys_id6` (low)

The following table shows the `por_hnf_rn_phys_id6` lower register bit assignments.

Table 4-444 `por_hnf_por_hnf_rn_phys_id6` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra12</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra12</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra12</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra12</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra12</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id7`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD60

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

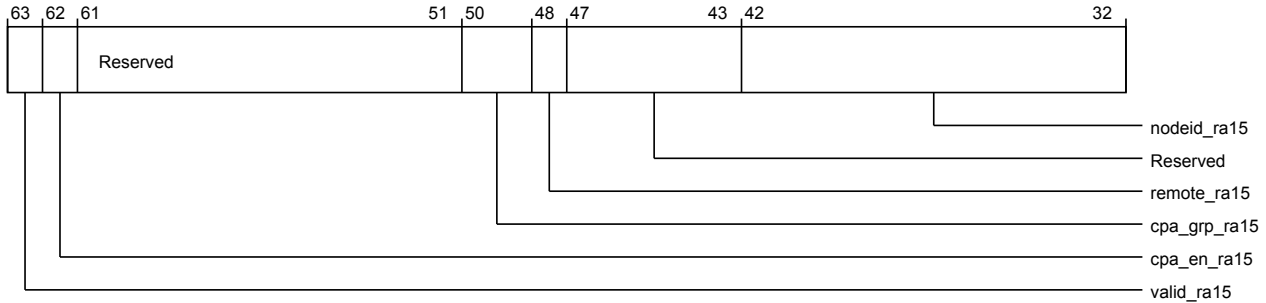


Figure 4-428 por_hnf_por_hnf_rn_phys_id7 (high)

The following table shows the por_hnf_rn_phys_id7 higher register bit assignments.

Table 4-445 por_hnf_por_hnf_rn_phys_id7 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra15	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra15	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra15	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra15	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra15	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

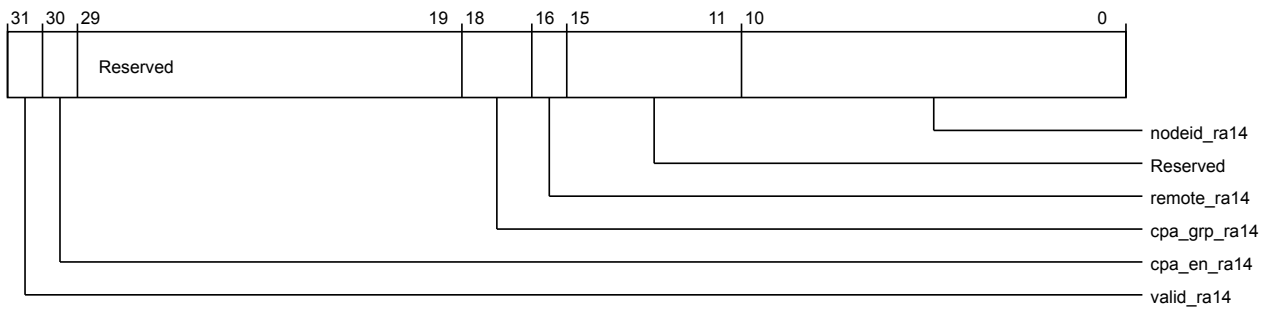


Figure 4-429 por_hnf_por_hnf_rn_phys_id7 (low)

The following table shows the por_hnf_rn_phys_id7 lower register bit assignments.

Table 4-446 por_hnf_por_hnf_rn_phys_id7 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra14	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra14	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra14	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra14	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra14	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id8

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD68

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

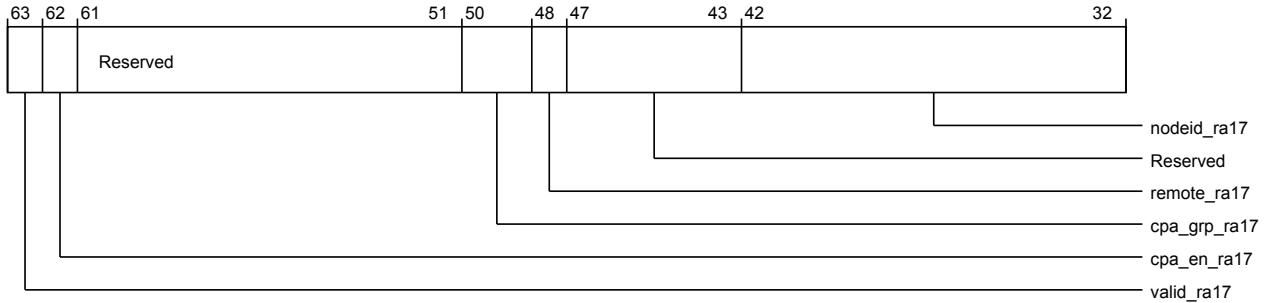


Figure 4-430 por_hnf_por_hnf_rn_phys_id8 (high)

The following table shows the por_hnf_rn_phys_id8 higher register bit assignments.

Table 4-447 por_hnf_por_hnf_rn_phys_id8 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra17	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra17	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra17	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra17	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra17	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

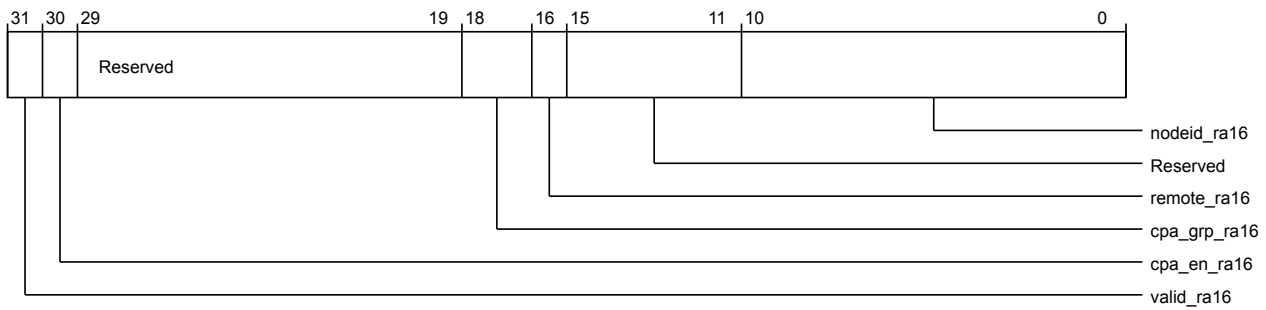


Figure 4-431 por_hnf_por_hnf_rn_phys_id8 (low)

The following table shows the por_hnf_rn_phys_id8 lower register bit assignments.

Table 4-448 por_hnf_por_hnf_rn_phys_id8 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra16	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra16	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra16	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra16	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra16	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id9

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD70

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

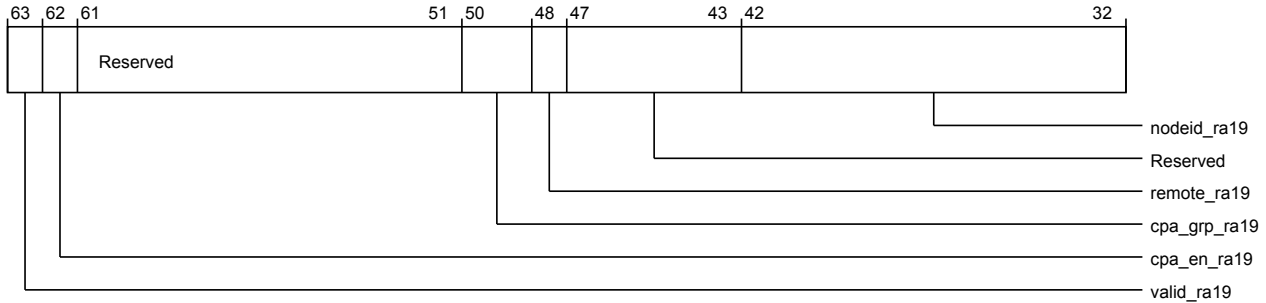


Figure 4-432 por_hnf_por_hnf_rn_phys_id9 (high)

The following table shows the por_hnf_rn_phys_id9 higher register bit assignments.

Table 4-449 por_hnf_por_hnf_rn_phys_id9 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra19	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra19	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra19	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra19	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra19	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

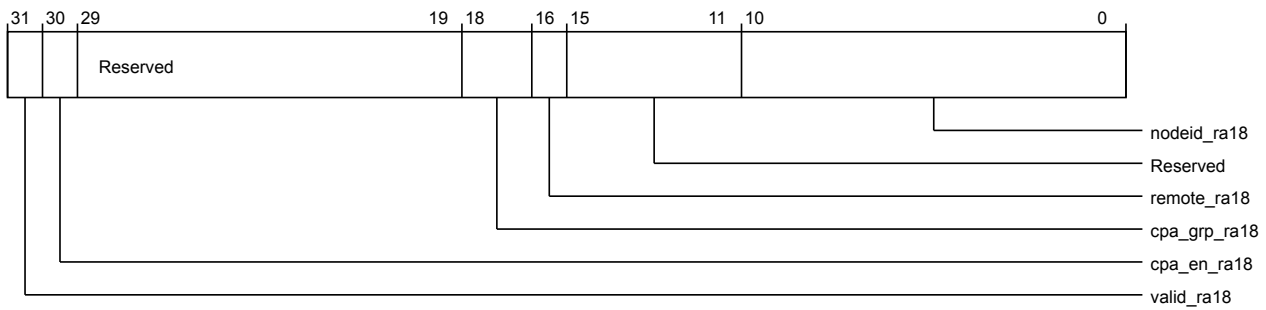


Figure 4-433 por_hnf_por_hnf_rn_phys_id9 (low)

The following table shows the por_hnf_rn_phys_id9 lower register bit assignments.

Table 4-450 por_hnf_por_hnf_rn_phys_id9 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra18	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpn_en_ra18	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpn_grp_ra18	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra18	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra18	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id10

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

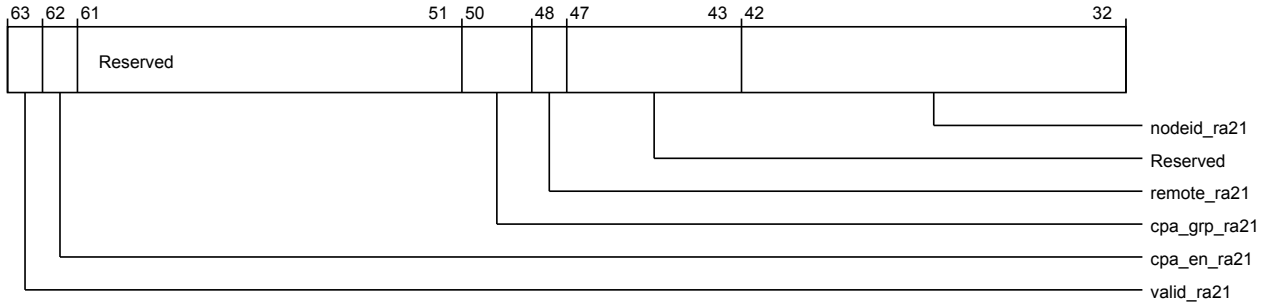


Figure 4-434 por_hnf_por_hnf_rn_phys_id10 (high)

The following table shows the por_hnf_rn_phys_id10 higher register bit assignments.

Table 4-451 por_hnf_por_hnf_rn_phys_id10 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra21	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra21	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra21	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra21	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra21	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

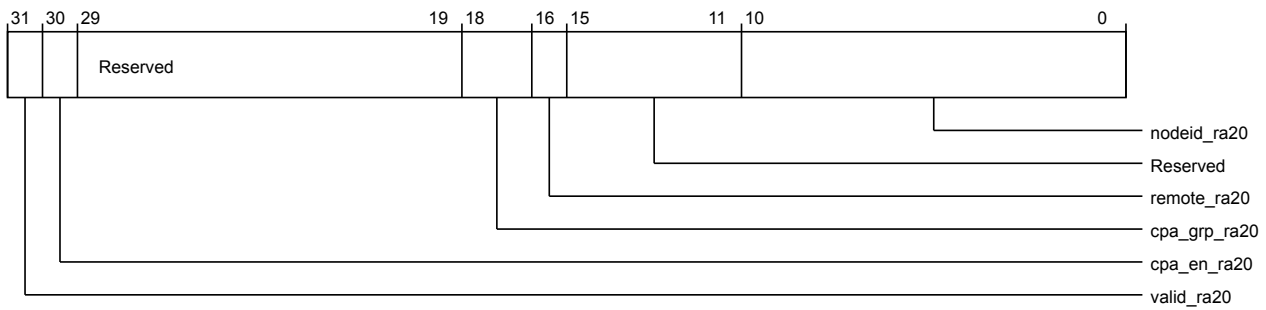


Figure 4-435 por_hnf_por_hnf_rn_phys_id10 (low)

The following table shows the por_hnf_rn_phys_id10 lower register bit assignments.

Table 4-452 por_hnf_por_hnf_rn_phys_id10 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra20	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra20	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra20	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra20	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra20	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id11

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD80

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

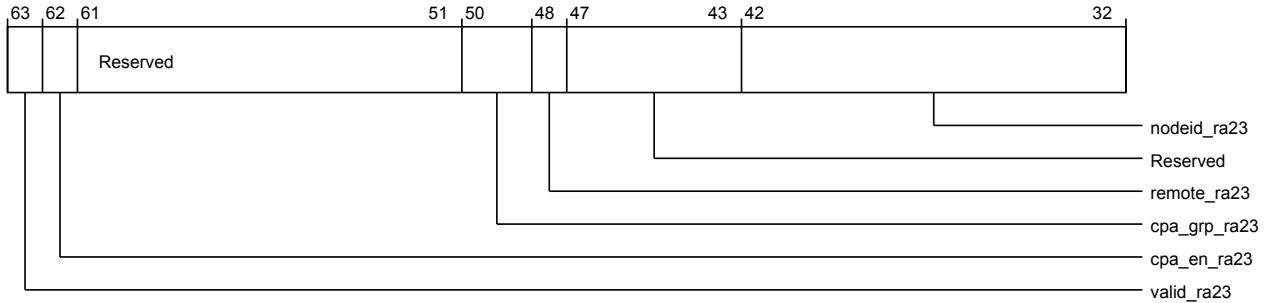


Figure 4-436 por_hnf_por_hnf_rn_phys_id11 (high)

The following table shows the por_hnf_rn_phys_id11 higher register bit assignments.

Table 4-453 por_hnf_por_hnf_rn_phys_id11 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra23	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra23	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra23	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra23	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra23	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

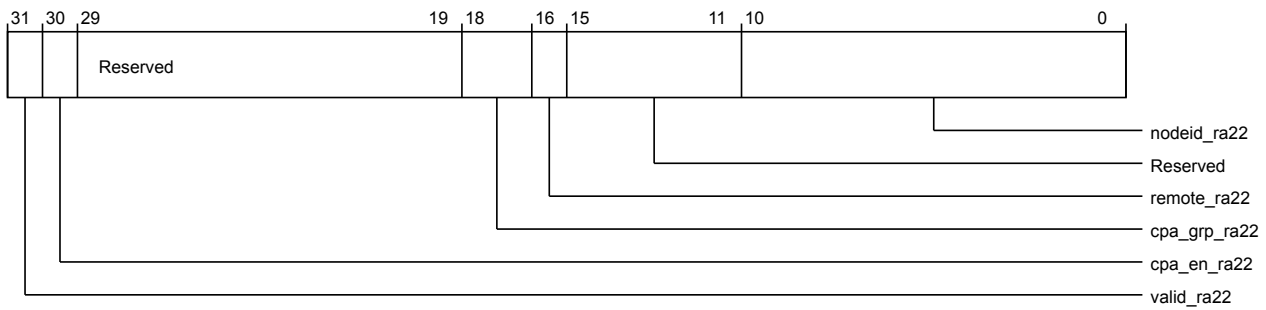


Figure 4-437 `por_hnf_por_hnf_rn_phys_id11` (low)

The following table shows the `por_hnf_rn_phys_id11` lower register bit assignments.

Table 4-454 `por_hnf_por_hnf_rn_phys_id11` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra22</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra22</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra22</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra22</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra22</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id12`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD88

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

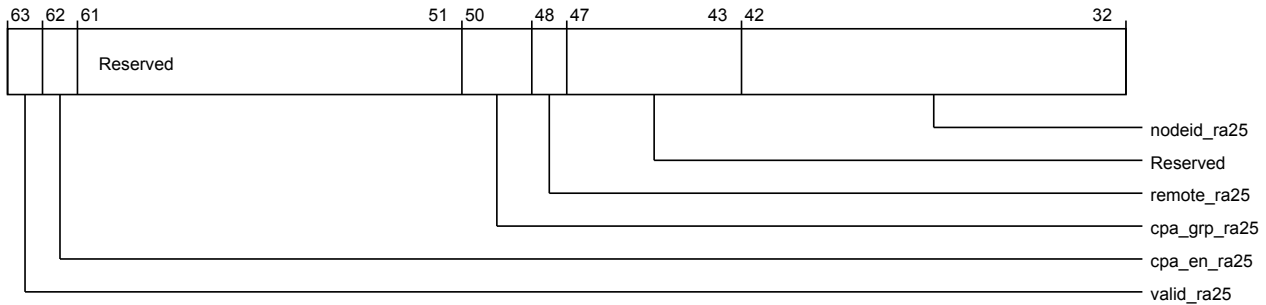


Figure 4-438 por_hnf_por_hnf_rn_phys_id12 (high)

The following table shows the por_hnf_rn_phys_id12 higher register bit assignments.

Table 4-455 por_hnf_por_hnf_rn_phys_id12 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra25	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra25	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra25	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra25	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra25	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

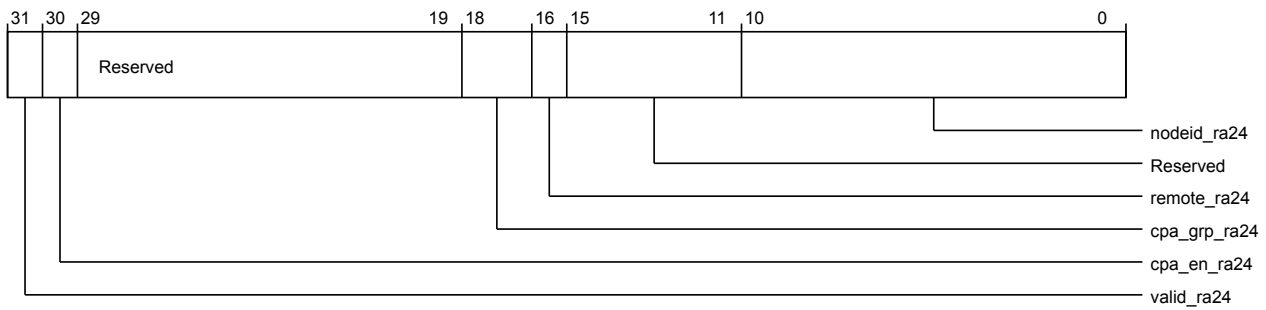


Figure 4-439 por_hnf_por_hnf_rn_phys_id12 (low)

The following table shows the por_hnf_rn_phys_id12 lower register bit assignments.

Table 4-456 por_hnf_por_hnf_rn_phys_id12 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra24	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra24	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra24	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra24	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra24	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id13

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD90

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

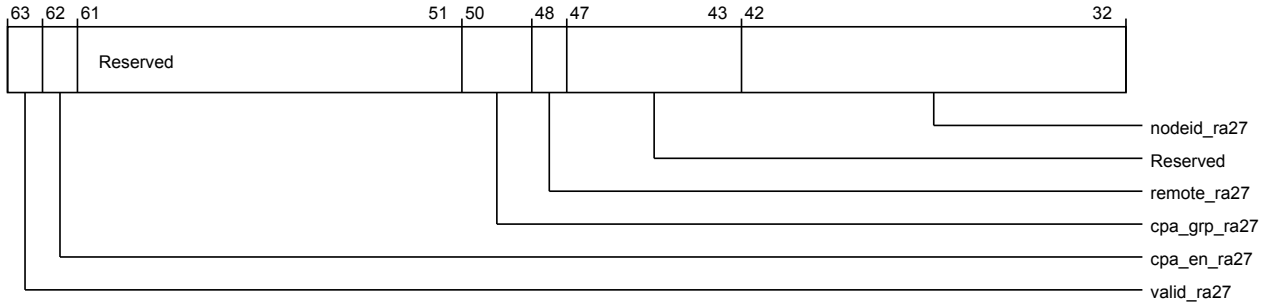


Figure 4-440 por_hnf_por_hnf_rn_phys_id13 (high)

The following table shows the por_hnf_rn_phys_id13 higher register bit assignments.

Table 4-457 por_hnf_por_hnf_rn_phys_id13 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra27	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra27	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra27	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra27	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra27	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

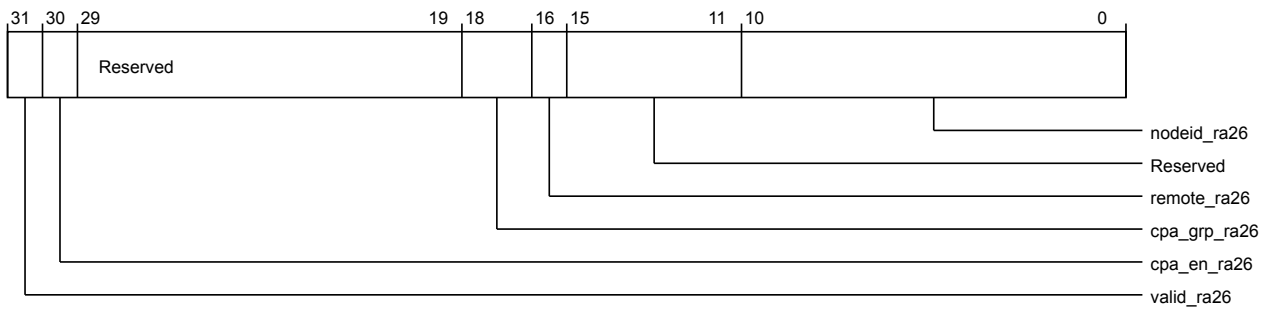


Figure 4-441 por_hnf_por_hnf_rn_phys_id13 (low)

The following table shows the por_hnf_rn_phys_id13 lower register bit assignments.

Table 4-458 por_hnf_por_hnf_rn_phys_id13 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra26	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra26	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra26	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra26	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra26	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id14

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD98

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

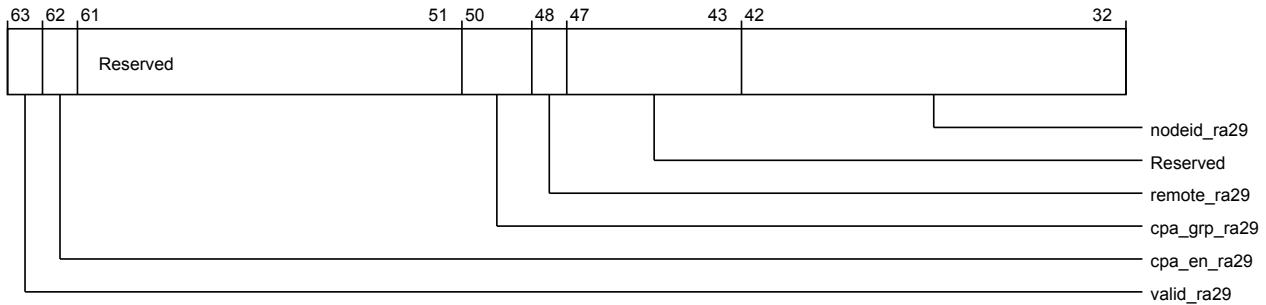


Figure 4-442 por_hnf_por_hnf_rn_phys_id14 (high)

The following table shows the por_hnf_rn_phys_id14 higher register bit assignments.

Table 4-459 por_hnf_por_hnf_rn_phys_id14 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra29	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra29	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra29	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra29	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra29	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

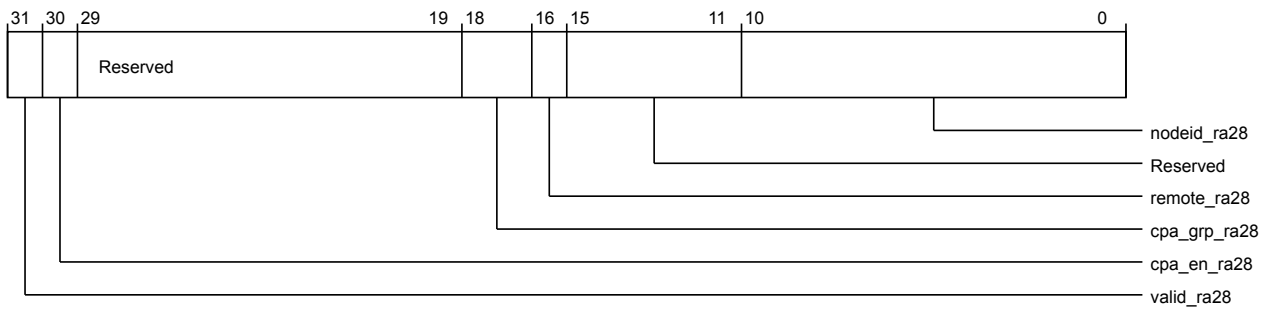


Figure 4-443 `por_hnf_por_hnf_rn_phys_id14 (low)`

The following table shows the `por_hnf_rn_phys_id14` lower register bit assignments.

Table 4-460 `por_hnf_por_hnf_rn_phys_id14 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra28</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra28</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra28</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra28</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra28</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id15`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDA0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

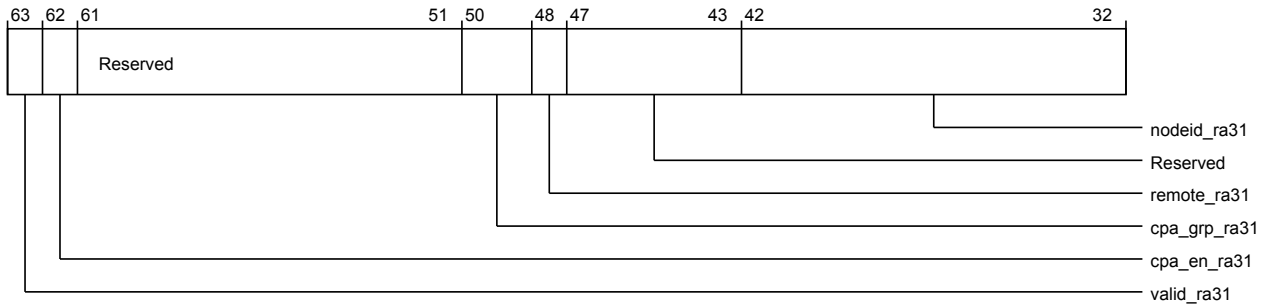


Figure 4-444 por_hnf_por_hnf_rn_phys_id15 (high)

The following table shows the por_hnf_rn_phys_id15 higher register bit assignments.

Table 4-461 por_hnf_por_hnf_rn_phys_id15 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra31	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra31	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra31	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra31	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra31	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

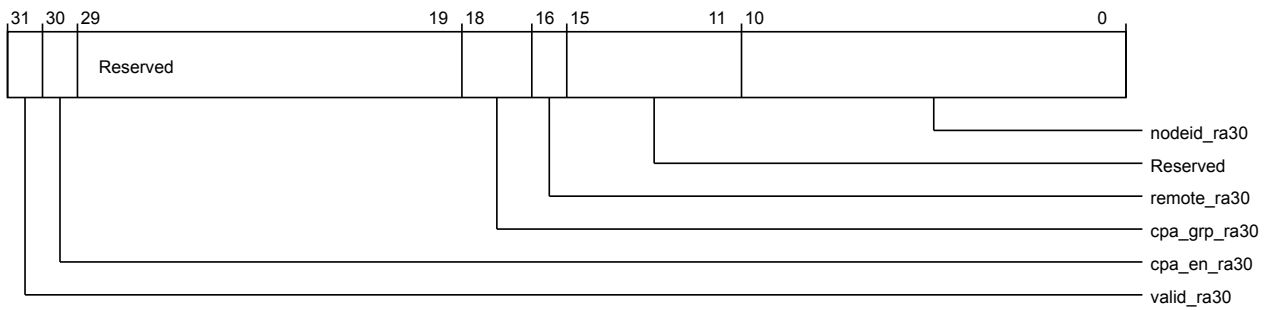


Figure 4-445 `por_hnf_por_hnf_rn_phys_id15` (low)

The following table shows the `por_hnf_rn_phys_id15` lower register bit assignments.

Table 4-462 `por_hnf_por_hnf_rn_phys_id15` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra30</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra30</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra30</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra30</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra30</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id16`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

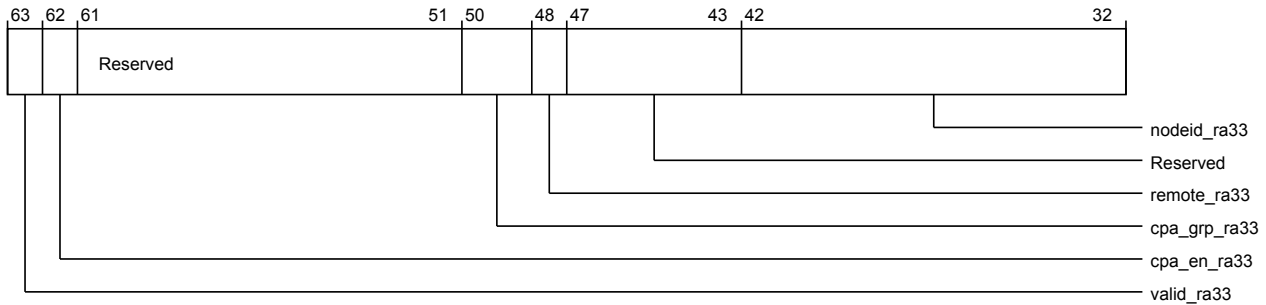


Figure 4-446 por_hnf_por_hnf_rn_phys_id16 (high)

The following table shows the por_hnf_rn_phys_id16 higher register bit assignments.

Table 4-463 por_hnf_por_hnf_rn_phys_id16 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra33	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra33	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra33	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra33	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra33	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

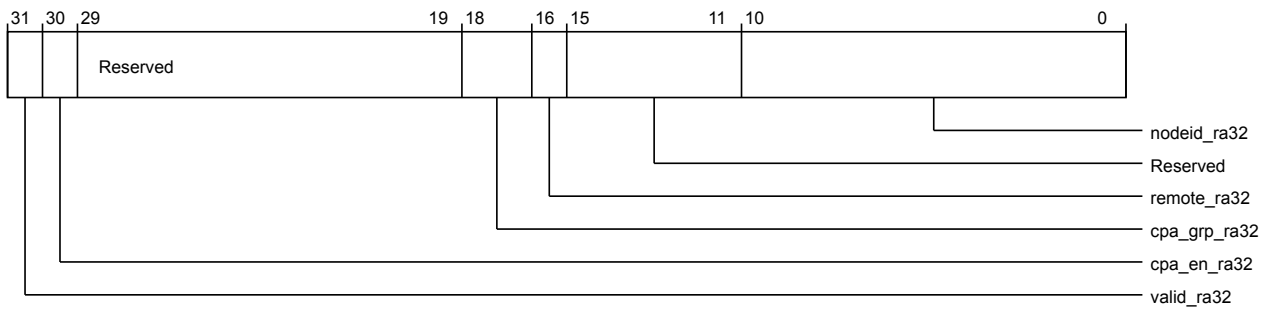


Figure 4-447 `por_hnf_por_hnf_rn_phys_id16 (low)`

The following table shows the `por_hnf_rn_phys_id16` lower register bit assignments.

Table 4-464 `por_hnf_por_hnf_rn_phys_id16 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra32</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra32</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra32</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra32</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra32</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id17`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

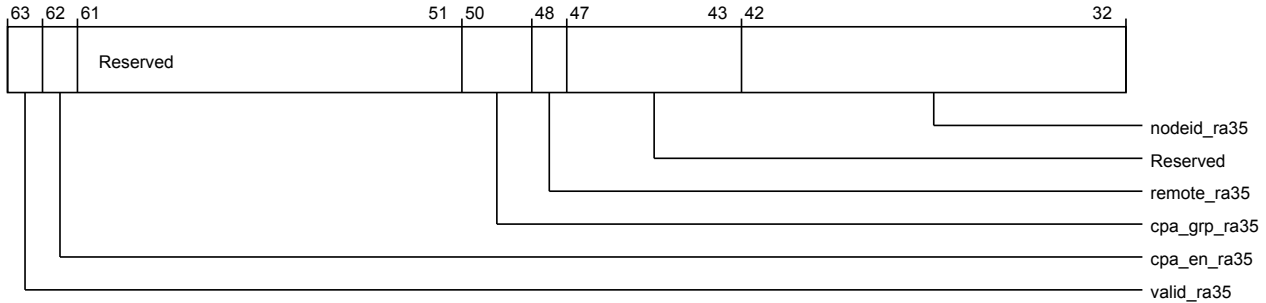


Figure 4-448 por_hnf_por_hnf_rn_phys_id17 (high)

The following table shows the por_hnf_rn_phys_id17 higher register bit assignments.

Table 4-465 por_hnf_por_hnf_rn_phys_id17 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra35	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra35	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra35	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra35	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra35	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

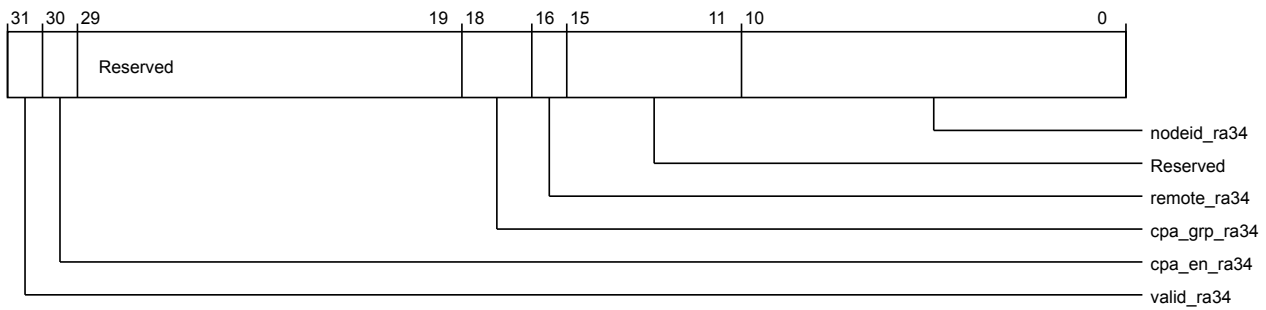


Figure 4-449 por_hnf_por_hnf_rn_phys_id17 (low)

The following table shows the por_hnf_rn_phys_id17 lower register bit assignments.

Table 4-466 por_hnf_por_hnf_rn_phys_id17 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra34	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra34	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra34	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra34	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra34	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id18

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

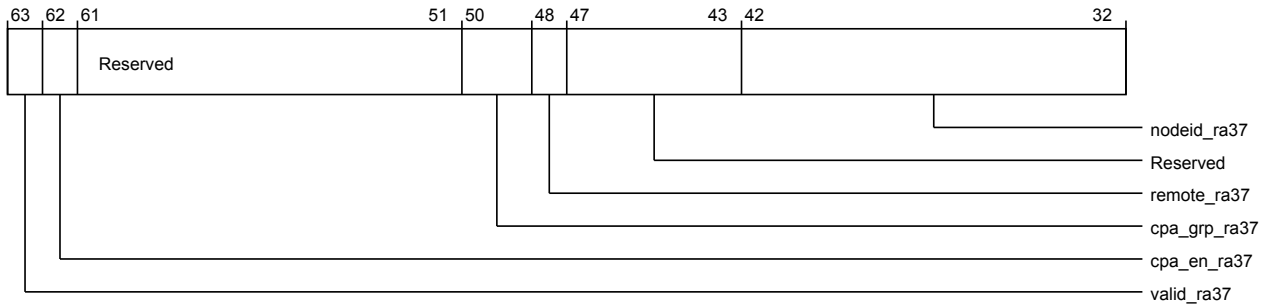


Figure 4-450 por_hnf_por_hnf_rn_phys_id18 (high)

The following table shows the por_hnf_rn_phys_id18 higher register bit assignments.

Table 4-467 por_hnf_por_hnf_rn_phys_id18 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra37	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra37	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra37	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra37	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra37	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

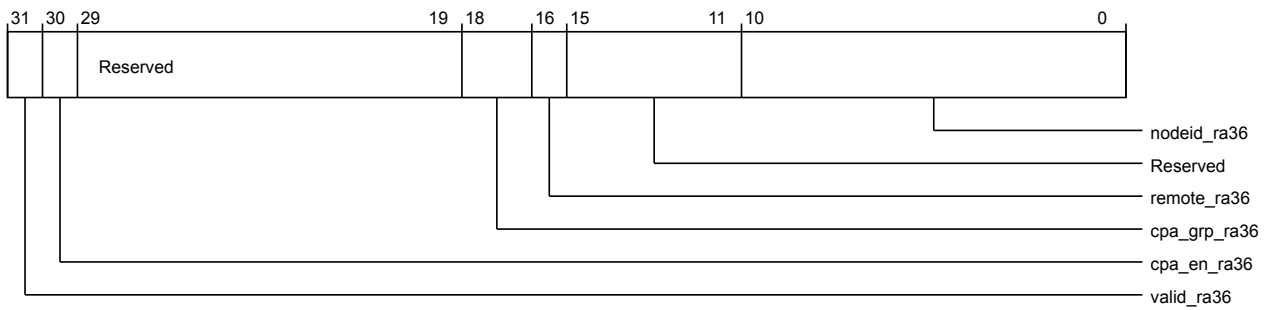


Figure 4-451 `por_hnf_por_hnf_rn_phys_id18` (low)

The following table shows the `por_hnf_rn_phys_id18` lower register bit assignments.

Table 4-468 `por_hnf_por_hnf_rn_phys_id18` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra36</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra36</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra36</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra36</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra36</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id19`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDC0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

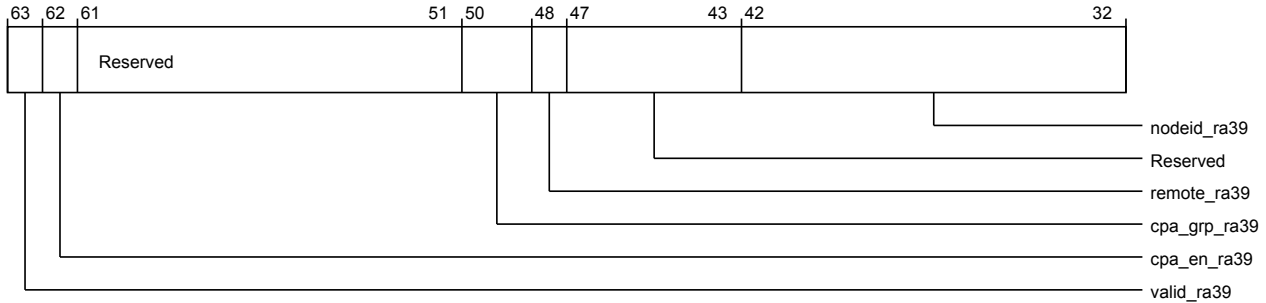


Figure 4-452 por_hnf_por_hnf_rn_phys_id19 (high)

The following table shows the por_hnf_rn_phys_id19 higher register bit assignments.

Table 4-469 por_hnf_por_hnf_rn_phys_id19 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra39	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra39	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra39	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra39	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra39	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

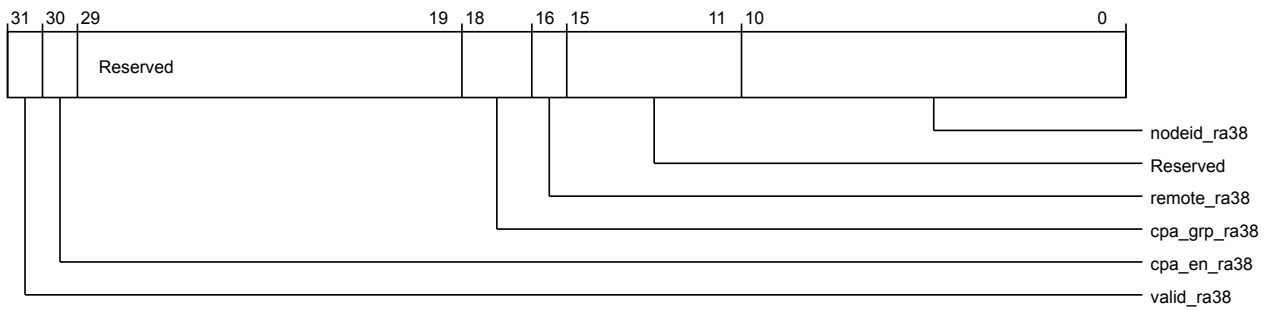


Figure 4-453 `por_hnf_por_hnf_rn_phys_id19` (low)

The following table shows the `por_hnf_rn_phys_id19` lower register bit assignments.

Table 4-470 `por_hnf_por_hnf_rn_phys_id19` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra38</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra38</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra38</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra38</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra38</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id20`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

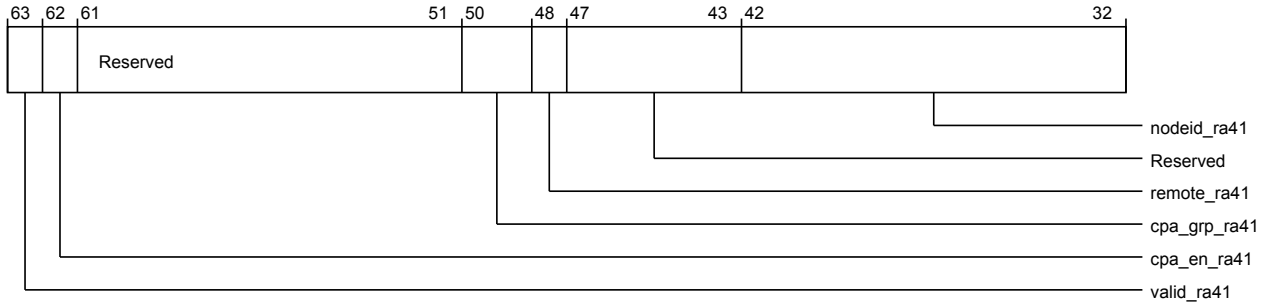


Figure 4-454 por_hnf_por_hnf_rn_phys_id20 (high)

The following table shows the por_hnf_rn_phys_id20 higher register bit assignments.

Table 4-471 por_hnf_por_hnf_rn_phys_id20 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra41	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra41	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra41	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra41	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra41	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

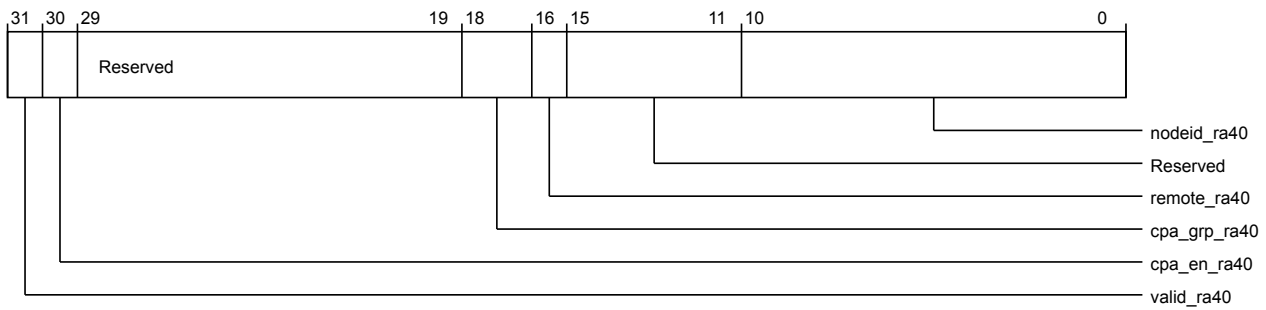


Figure 4-455 `por_hnf_por_hnf_rn_phys_id20` (low)

The following table shows the `por_hnf_rn_phys_id20` lower register bit assignments.

Table 4-472 `por_hnf_por_hnf_rn_phys_id20` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra40</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra40</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra40</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra40</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra40</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id21`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDD0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

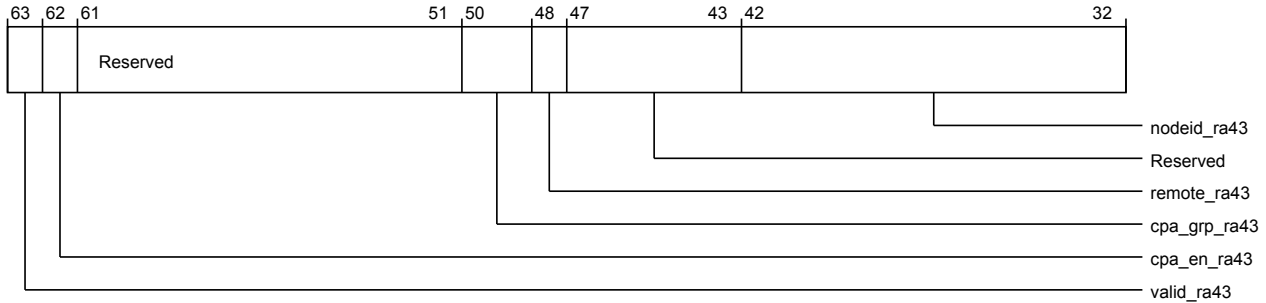


Figure 4-456 por_hnf_por_hnf_rn_phys_id21 (high)

The following table shows the por_hnf_rn_phys_id21 higher register bit assignments.

Table 4-473 por_hnf_por_hnf_rn_phys_id21 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra43	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra43	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra43	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra43	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra43	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

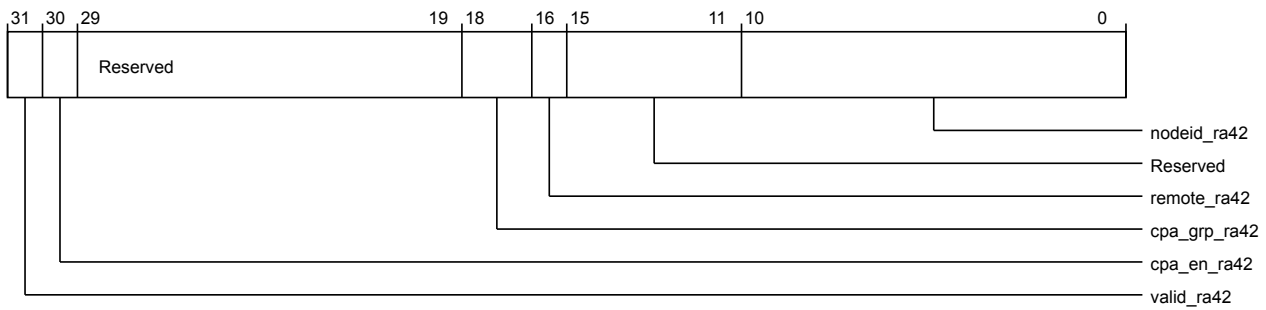


Figure 4-457 `por_hnf_por_hnf_rn_phys_id21 (low)`

The following table shows the `por_hnf_rn_phys_id21` lower register bit assignments.

Table 4-474 `por_hnf_por_hnf_rn_phys_id21 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra2</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra2</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra2</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra2</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra2</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id22`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

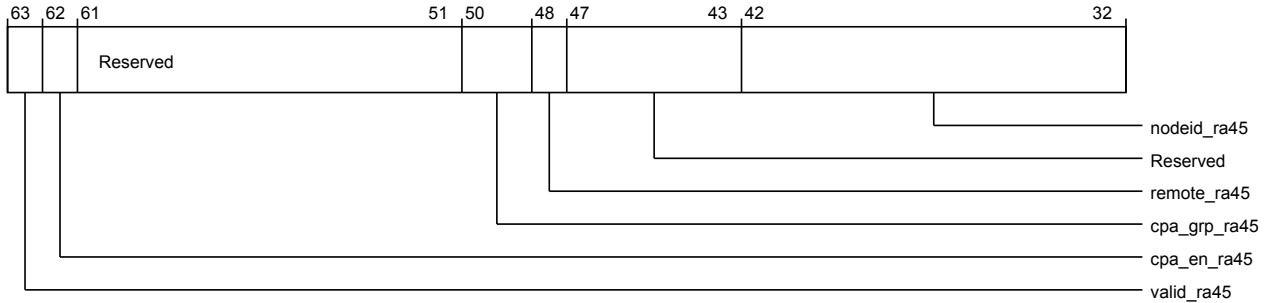


Figure 4-458 por_hnf_por_hnf_rn_phys_id22 (high)

The following table shows the por_hnf_rn_phys_id22 higher register bit assignments.

Table 4-475 por_hnf_por_hnf_rn_phys_id22 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra45	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra45	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra45	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra45	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra45	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

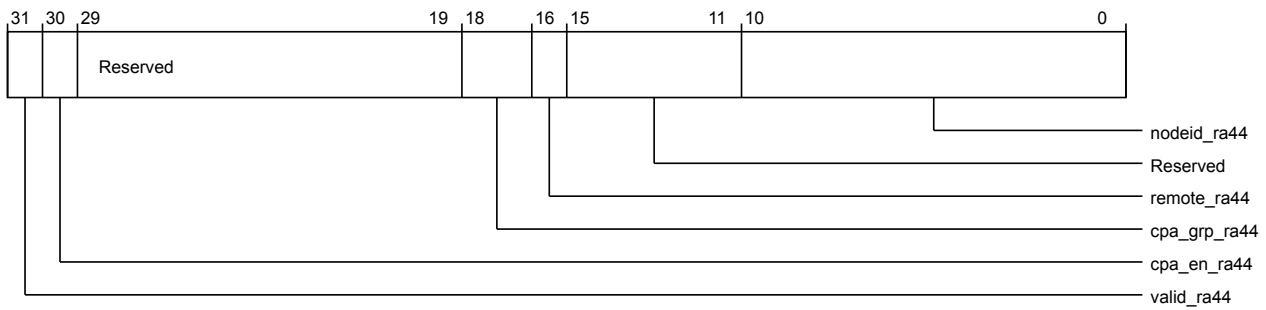


Figure 4-459 `por_hnf_por_hnf_rn_phys_id22 (low)`

The following table shows the `por_hnf_rn_phys_id22` lower register bit assignments.

Table 4-476 `por_hnf_por_hnf_rn_phys_id22 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra44</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra44</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra44</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra44</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra44</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id23`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDE0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

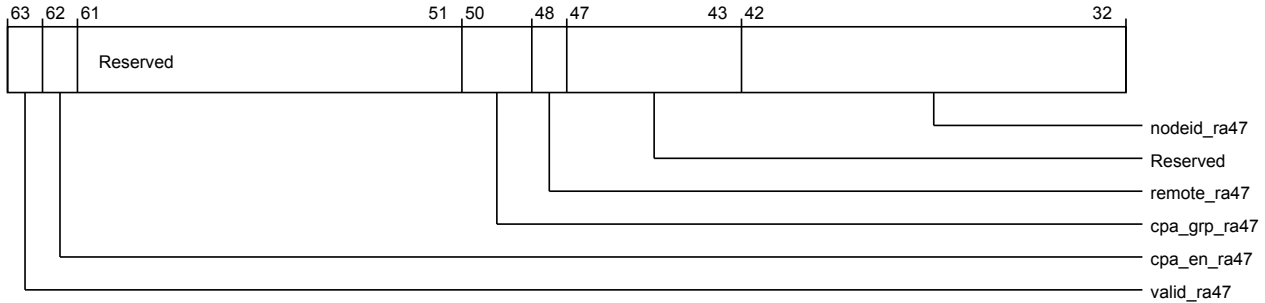


Figure 4-460 por_hnf_por_hnf_rn_phys_id23 (high)

The following table shows the por_hnf_rn_phys_id23 higher register bit assignments.

Table 4-477 por_hnf_por_hnf_rn_phys_id23 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra47	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra47	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra47	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra47	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra47	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

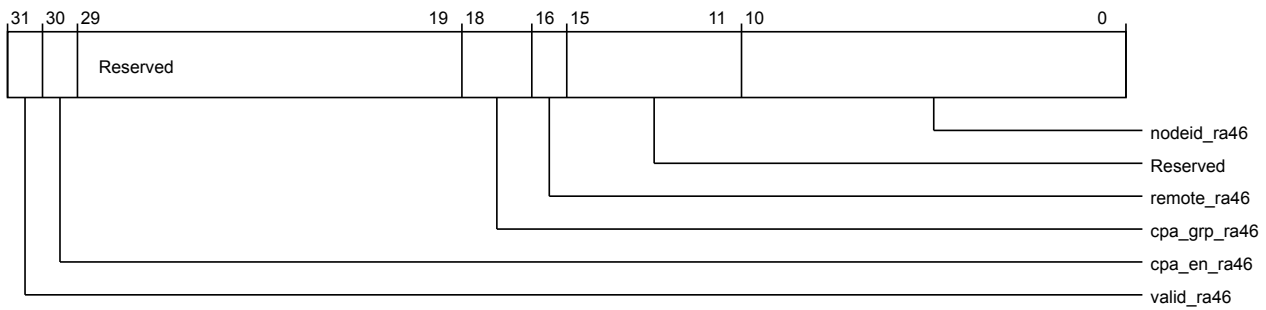


Figure 4-461 `por_hnf_por_hnf_rn_phys_id23 (low)`

The following table shows the `por_hnf_rn_phys_id23` lower register bit assignments.

Table 4-478 `por_hnf_por_hnf_rn_phys_id23 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra46</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra46</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra46</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra46</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra46</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id24`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

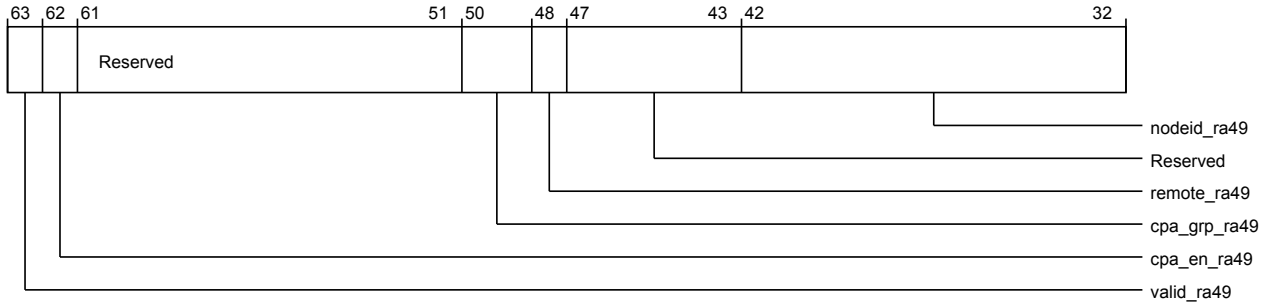


Figure 4-462 por_hnf_por_hnf_rn_phys_id24 (high)

The following table shows the por_hnf_rn_phys_id24 higher register bit assignments.

Table 4-479 por_hnf_por_hnf_rn_phys_id24 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra49	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra49	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra49	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra49	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra49	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

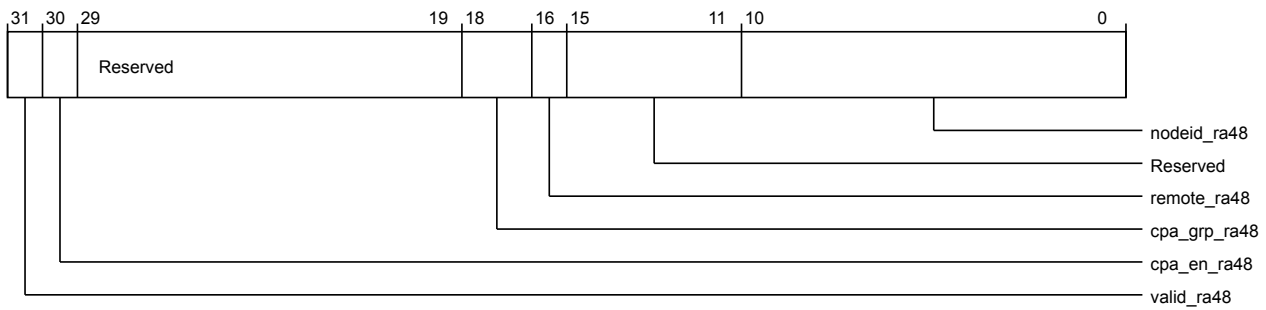


Figure 4-463 por_hnf_por_hnf_rn_phys_id24 (low)

The following table shows the por_hnf_rn_phys_id24 lower register bit assignments.

Table 4-480 por_hnf_por_hnf_rn_phys_id24 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra48	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra48	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra48	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra48	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra48	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id25

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDF0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

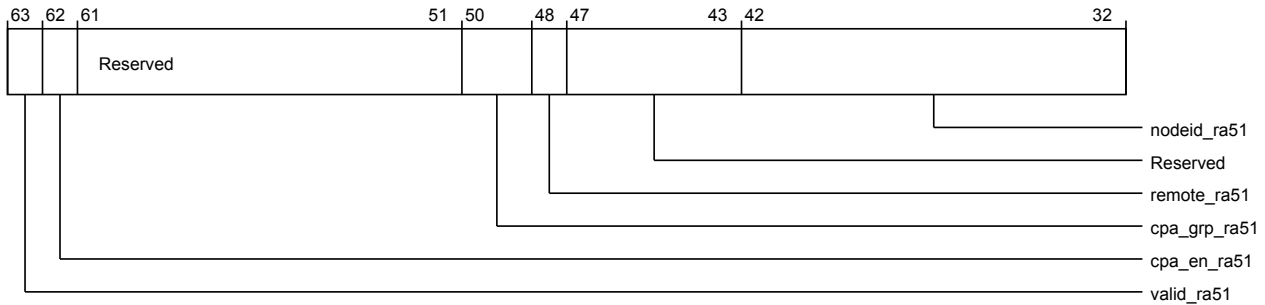


Figure 4-464 por_hnf_por_hnf_rn_phys_id25 (high)

The following table shows the por_hnf_rn_phys_id25 higher register bit assignments.

Table 4-481 por_hnf_por_hnf_rn_phys_id25 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra51	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra51	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra51	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra51	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra51	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

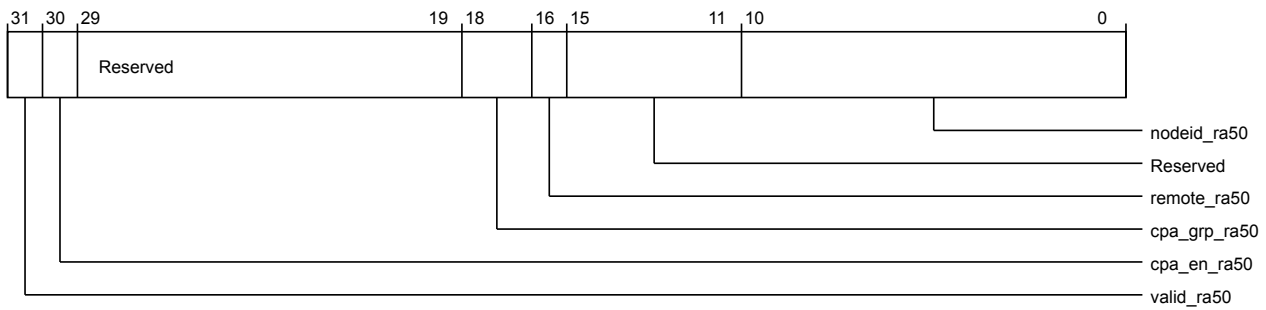


Figure 4-465 por_hnf_por_hnf_rn_phys_id25 (low)

The following table shows the por_hnf_rn_phys_id25 lower register bit assignments.

Table 4-482 por_hnf_por_hnf_rn_phys_id25 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra50	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra50	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra50	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra50	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra50	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id26

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

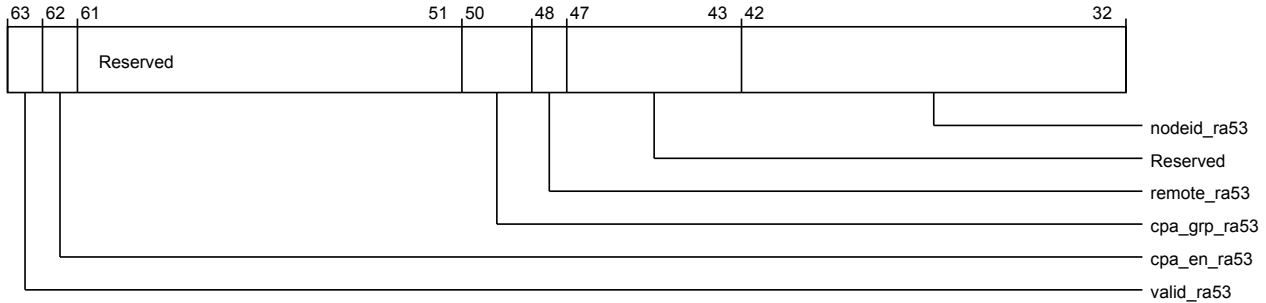


Figure 4-466 por_hnf_por_hnf_rn_phys_id26 (high)

The following table shows the por_hnf_rn_phys_id26 higher register bit assignments.

Table 4-483 por_hnf_por_hnf_rn_phys_id26 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra53	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra53	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra53	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra53	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra53	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

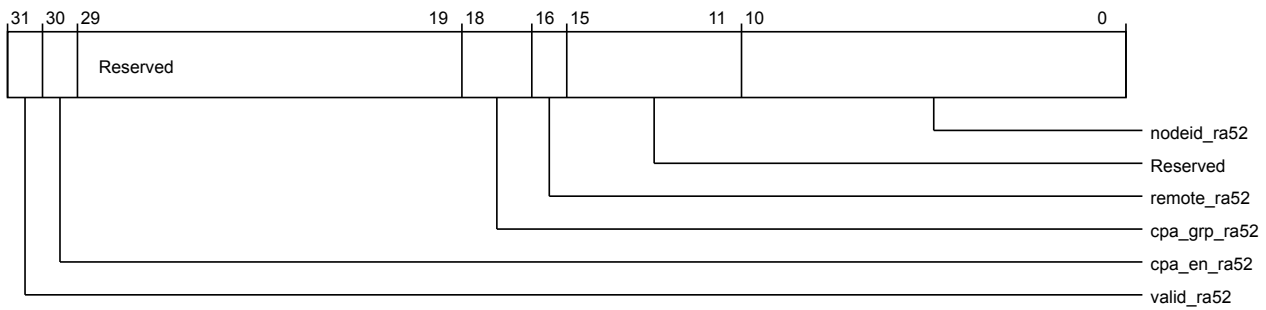


Figure 4-467 por_hnf_por_hnf_rn_phys_id26 (low)

The following table shows the por_hnf_rn_phys_id26 lower register bit assignments.

Table 4-484 por_hnf_por_hnf_rn_phys_id26 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra52	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra52	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra52	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra52	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra52	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id27

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE00

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

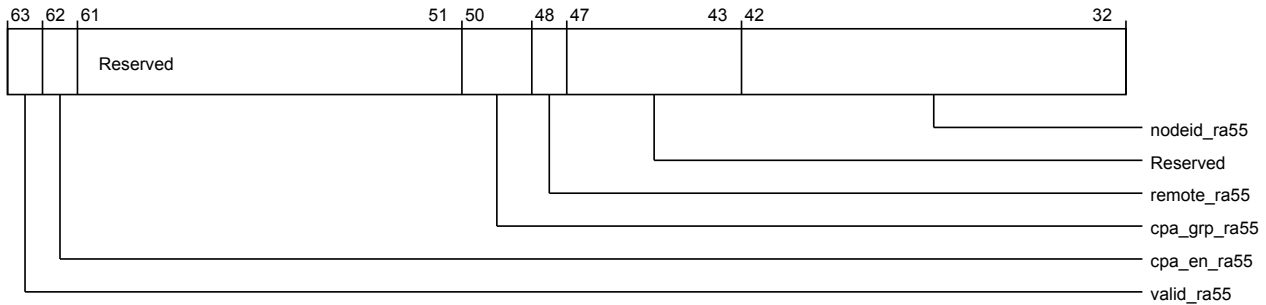


Figure 4-468 por_hnf_por_hnf_rn_phys_id27 (high)

The following table shows the por_hnf_rn_phys_id27 higher register bit assignments.

Table 4-485 por_hnf_por_hnf_rn_phys_id27 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra55	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra55	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra55	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra55	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra55	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

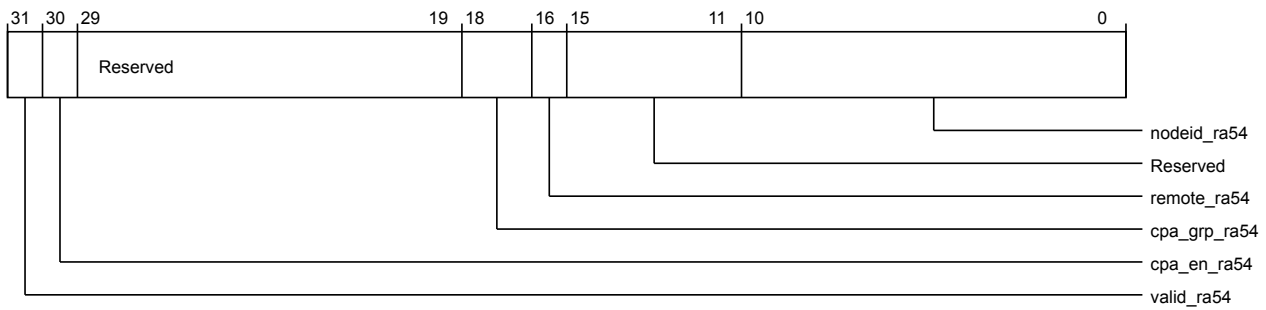


Figure 4-469 `por_hnf_por_hnf_rn_phys_id27 (low)`

The following table shows the `por_hnf_rn_phys_id27` lower register bit assignments.

Table 4-486 `por_hnf_por_hnf_rn_phys_id27 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra54</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra54</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra54</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra54</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra54</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id28`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE08

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

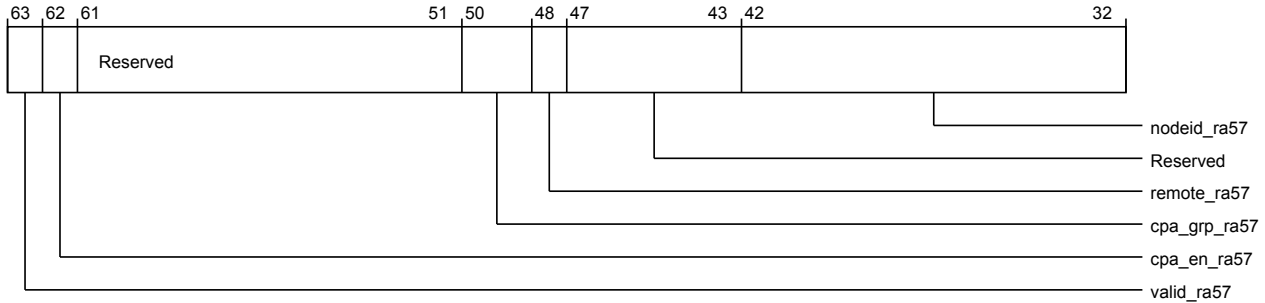


Figure 4-470 por_hnf_por_hnf_rn_phys_id28 (high)

The following table shows the por_hnf_rn_phys_id28 higher register bit assignments.

Table 4-487 por_hnf_por_hnf_rn_phys_id28 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra57	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra57	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra57	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra57	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra57	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

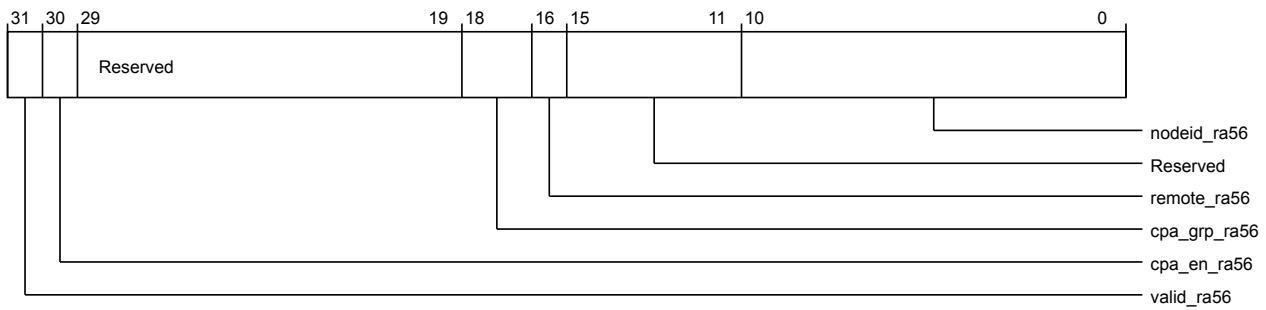


Figure 4-471 por_hnf_por_hnf_rn_phys_id28 (low)

The following table shows the por_hnf_rn_phys_id28 lower register bit assignments.

Table 4-488 por_hnf_por_hnf_rn_phys_id28 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra56	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra56	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra56	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra56	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra56	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id29

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE10

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

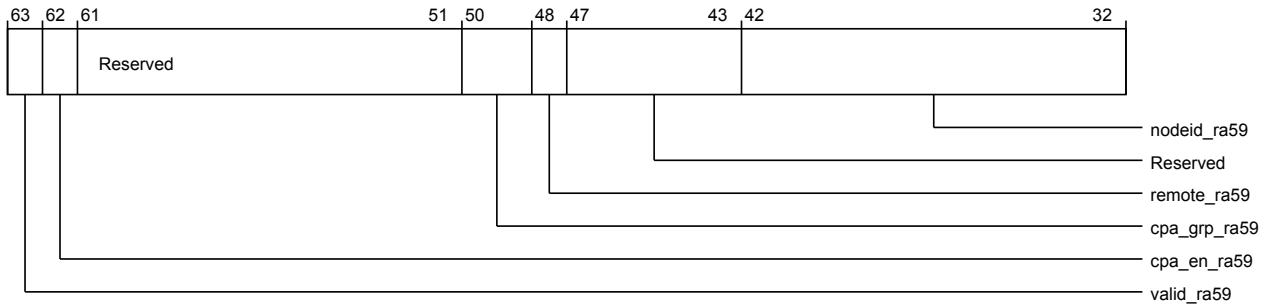


Figure 4-472 `por_hnf_por_hnf_rn_phys_id29 (high)`

The following table shows the `por_hnf_rn_phys_id29` higher register bit assignments.

Table 4-489 `por_hnf_por_hnf_rn_phys_id29 (high)`

Bits	Field name	Description	Type	Reset
63	<code>valid_ra59</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	<code>cpa_en_ra59</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	<code>cpa_grp_ra59</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	<code>remote_ra59</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>nodeid_ra59</code>	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

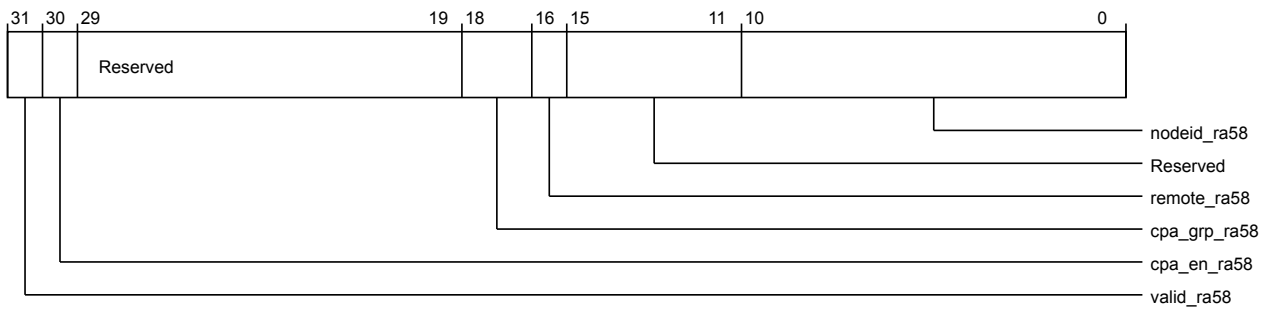


Figure 4-473 `por_hnf_por_hnf_rn_phys_id29 (low)`

The following table shows the `por_hnf_rn_phys_id29` lower register bit assignments.

Table 4-490 `por_hnf_por_hnf_rn_phys_id29 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra58</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra58</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra58</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra58</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra58</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id30`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE18

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

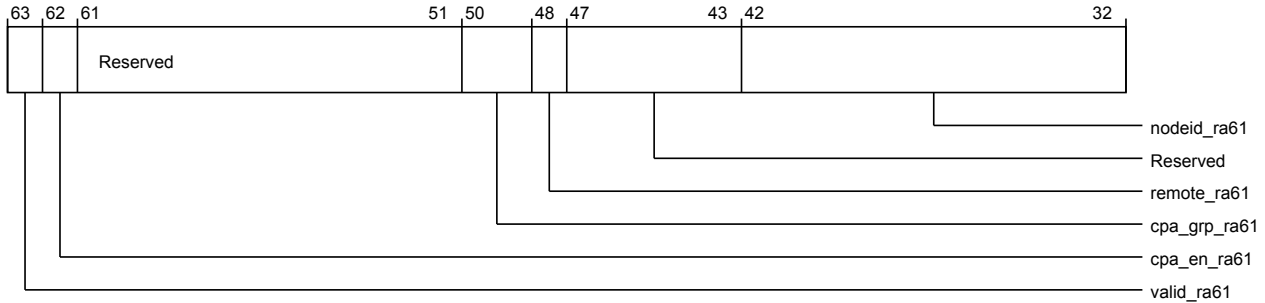


Figure 4-474 por_hnf_por_hnf_rn_phys_id30 (high)

The following table shows the por_hnf_rn_phys_id30 higher register bit assignments.

Table 4-491 por_hnf_por_hnf_rn_phys_id30 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra61	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra61	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra61	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra61	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra61	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

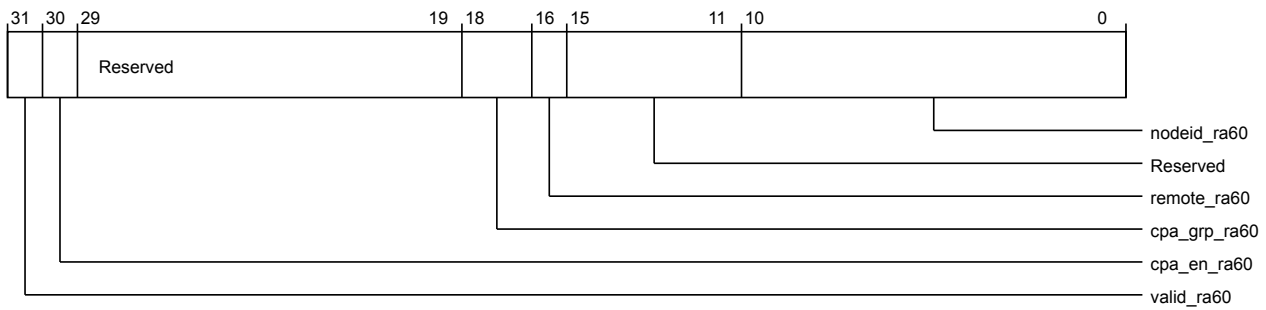


Figure 4-475 `por_hnf_por_hnf_rn_phys_id30` (low)

The following table shows the `por_hnf_rn_phys_id30` lower register bit assignments.

Table 4-492 `por_hnf_por_hnf_rn_phys_id30` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra60</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra60</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra60</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra60</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra60</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id31`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE20

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

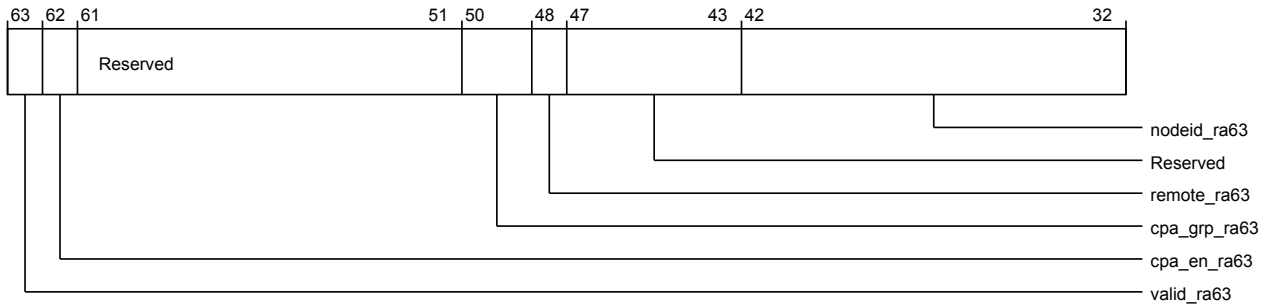


Figure 4-476 por_hnf_por_hnf_rn_phys_id31 (high)

The following table shows the por_hnf_rn_phys_id31 higher register bit assignments.

Table 4-493 por_hnf_por_hnf_rn_phys_id31 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra63	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra63	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra63	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra63	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra63	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

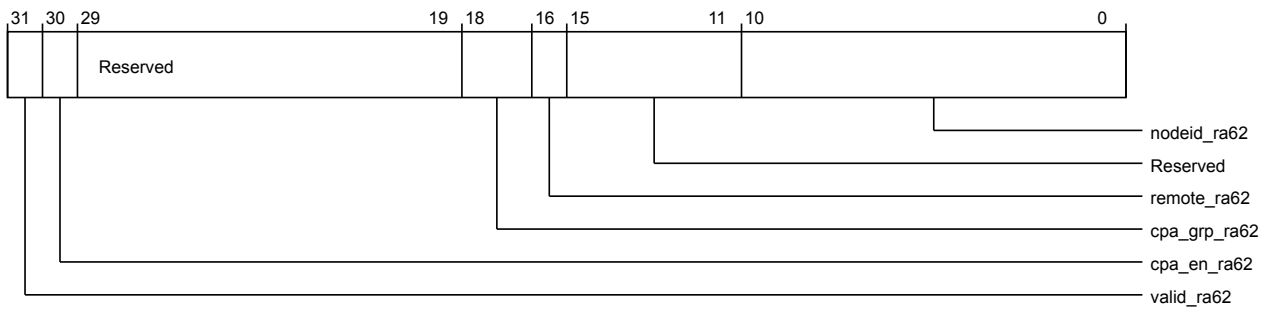


Figure 4-477 `por_hnf_por_hnf_rn_phys_id31` (low)

The following table shows the `por_hnf_rn_phys_id31` lower register bit assignments.

Table 4-494 `por_hnf_por_hnf_rn_phys_id31` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra62</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra62</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra62</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra62</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra62</code>	Specifies the node ID	RW	11'h0

`por_hnf_sf_cxg_blocked_ways`

Specifies the SF ways that are blocked for remote chip to use in CML mode.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hF00

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

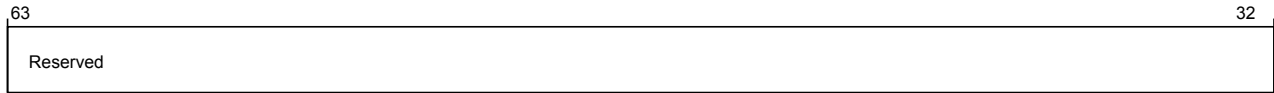


Figure 4-478 por_hnf_por_hnf_sf_cxg_blocked_ways (high)

The following table shows the por_hnf_sf_cxg_blocked_ways higher register bit assignments.

Table 4-495 por_hnf_por_hnf_sf_cxg_blocked_ways (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

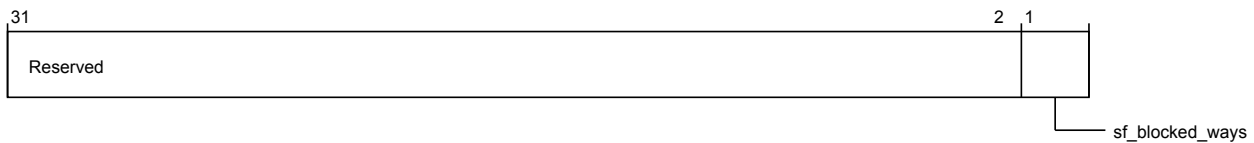


Figure 4-479 por_hnf_por_hnf_sf_cxg_blocked_ways (low)

The following table shows the por_hnf_sf_cxg_blocked_ways lower register bit assignments.

Table 4-496 por_hnf_por_hnf_sf_cxg_blocked_ways (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1:0	sf_blocked_ways	Number of SF ways blocked for remote chips to use in CML mode (0, 4, 8, or 12) 2'b00: No ways are blocked; all 16 SF ways could be used by local or remote RN-Fs 2'b01: Lower 4 ways are blocked from remote RN-Fs; ways 3:0 for local RN-Fs only; ways 15:4 for local and remote RN-Fs 2'b10: Lower 8 ways are blocked from remote RN-Fs; ways 7:0 for local RN-Fs only; ways 15:8 for local and remote RN-Fs 2'b11: Lower 12 ways are blocked from remote RN-Fs; ways 11:0 for local RN-Fs only; ways 15:12 for local and remote RN-Fs	RW	2'b00

por_hnf_cml_port_aggr_grp0_add_mask

Configures the CCIX port aggregation address mask for group 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF10
Register reset	64'b1
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

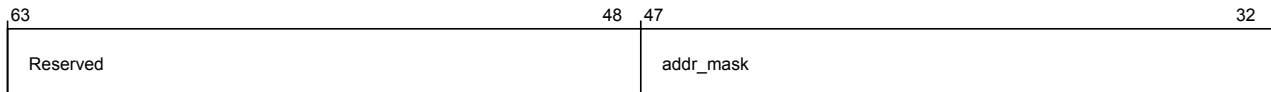


Figure 4-480 por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (high)

The following table shows the por_hnf_cml_port_aggr_grp0_add_mask higher register bit assignments.

Table 4-497 por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask to be applied before hashing	RW	42'b1

The following image shows the lower register bit assignments.

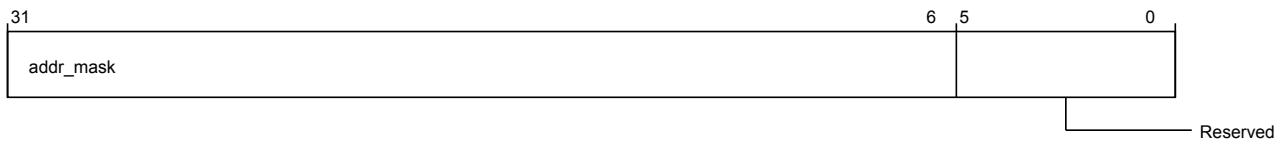


Figure 4-481 por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (low)

The following table shows the por_hnf_cml_port_aggr_grp0_add_mask lower register bit assignments.

Table 4-498 por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	42'b1
5:0	Reserved	Reserved	RO	-

por_hnf_cml_port_aggr_grp1_add_mask

Configures the CCIX port aggregation address mask for group 1.

Its characteristics are:

Type	RW
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Register width (Bits) 64
Address offset 14'hF18
Register reset 64'b1
Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

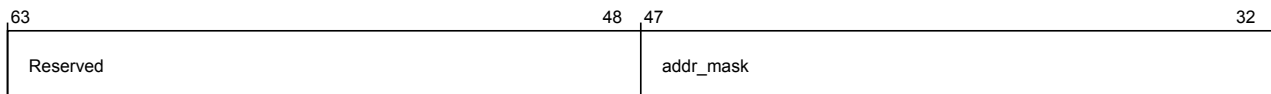


Figure 4-482 por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (high)

The following table shows the por_hnf_cml_port_aggr_grp1_add_mask higher register bit assignments.

Table 4-499 por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask to be applied before hashing	RW	42'b1

The following image shows the lower register bit assignments.

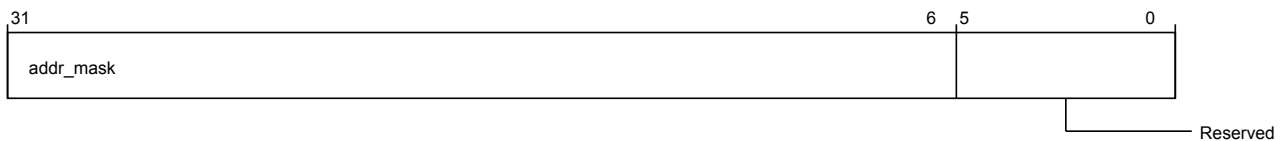


Figure 4-483 por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (low)

The following table shows the por_hnf_cml_port_aggr_grp1_add_mask lower register bit assignments.

Table 4-500 por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	42'b1
5:0	Reserved	Reserved	RO	-

por_hnf_cml_port_aggr_grp0_reg

Configures the CCIX port aggregation port IDs for group 0.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset	14'hF28
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

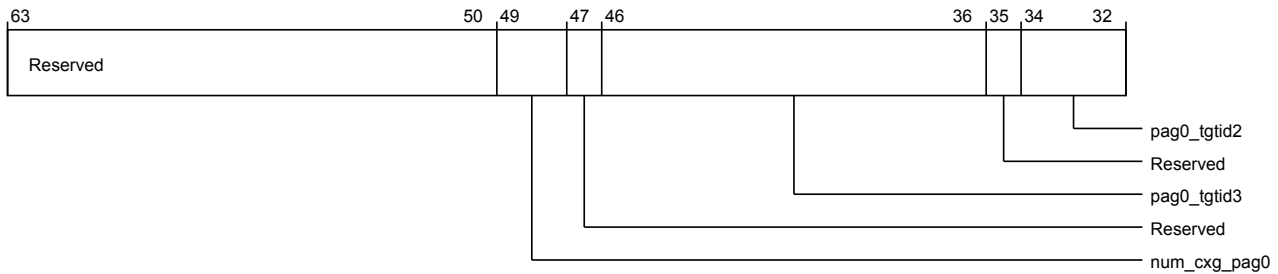


Figure 4-484 por_hnf_por_hnf_cml_port_aggr_grp0_reg (high)

The following table shows the por_hnf_cml_port_aggr_grp0_reg higher register bit assignments.

Table 4-501 por_hnf_por_hnf_cml_port_aggr_grp0_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	num_cxg_pag0	Specifies the number of CXRAs in CPAG 2'b00: 1 port used 2'b01: 2 ports used 2'b10: 4 ports used 2'b11: Reserved	RW	2'b0
47	Reserved	Reserved	RO	-
46:36	pag0_tgtid3	Specifies the target ID for CPAG	RW	11'b0
35	Reserved	Reserved	RO	-
34:32	pag0_tgtid2	Specifies the target ID for CPAG	RW	11'b0

The following image shows the lower register bit assignments.

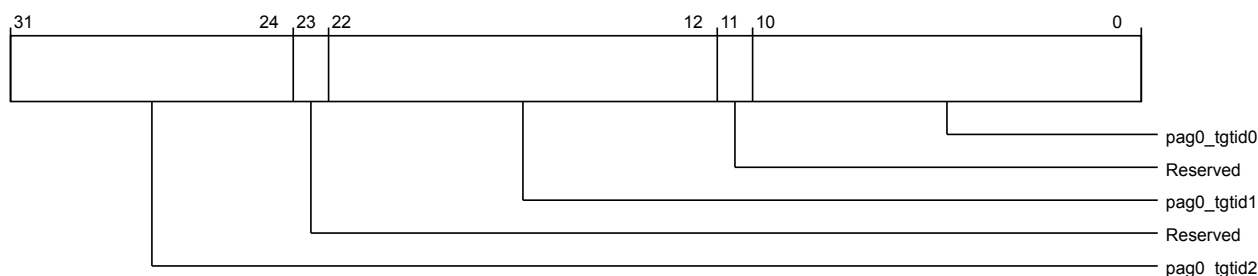


Figure 4-485 por_hnf_por_hnf_cml_port_aggr_grp0_reg (low)

The following table shows the por_hnf_cml_port_aggr_grp0_reg lower register bit assignments.

Table 4-502 por_hnf_por_hnf_cml_port_aggr_grp0_reg (low)

Bits	Field name	Description	Type	Reset
31:24	pag0_tgtid2	Specifies the target ID for CPAG	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag0_tgtid1	Specifies the target ID for CPAG	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	pag0_tgtid0	Specifies the target ID for CPAG	RW	11'b0

por_hnf_cml_port_aggr_grp1_reg

Configures the CCIX port aggregation port IDs for group 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF30

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

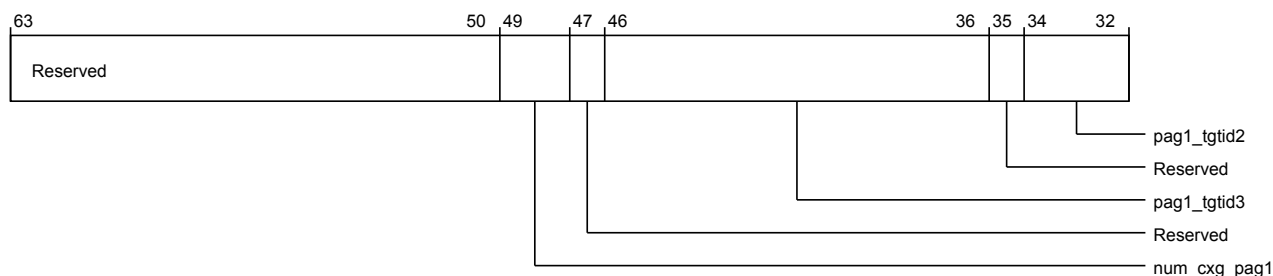


Figure 4-486 por_hnf_por_hnf_cml_port_aggr_grp1_reg (high)

The following table shows the `por_hnf_cml_port_aggr_grpl_reg` higher register bit assignments.

Table 4-503 por_hnf_por_hnf_cml_port_aggr_grp1_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	num_cxg_pag1	Specifies the number of CXRAs in CPAG	RW	2'b0
47	Reserved	Reserved	RO	-
46:36	pag1_tgtid3	Specifies the target ID for CPAG	RW	11'b0
35	Reserved	Reserved	RO	-
34:32	pag1_tgtid2	Specifies the target ID for CPAG	RW	11'b0

The following image shows the lower register bit assignments.

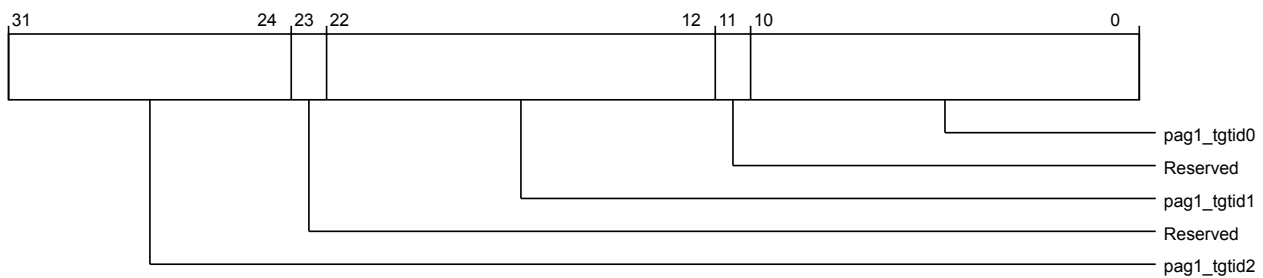


Figure 4-487 `por_hnf_por_hnf_cml_port_aggr_grp1_reg` (low)

The following table shows the `por_hnf_cml_port_aggr_grpl_reg` lower register bit assignments.

Table 4-504 `por_hnf_por_hnf_cml_port_aggr_grp1_reg` (low)

Bits	Field name	Description	Type	Reset
31:24	pag1_tgtid2	Specifies the target ID for CPAG	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag1_tgtid1	Specifies the target ID for CPAG	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	pag1_tgtid0	Specifies the target ID for CPAG	RW	11'b0

hn_sam_hash_addr_mask_reg

Configures the address mask that is applied before hashing the address bits.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF40

[illegible]

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

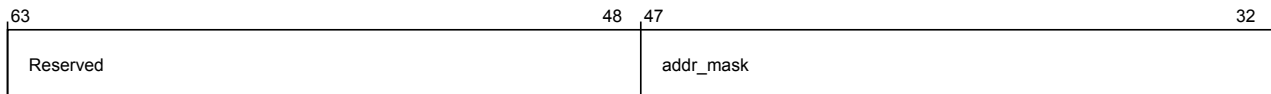


Figure 4-488 por_hnf_hn_sam_hash_addr_mask_reg (high)

The following table shows the hn_sam_hash_addr_mask_reg higher register bit assignments.

Table 4-505 por_hnf_hn_sam_hash_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask applied before hashing	RW	42'h3FFFFFFFFF

The following image shows the lower register bit assignments.

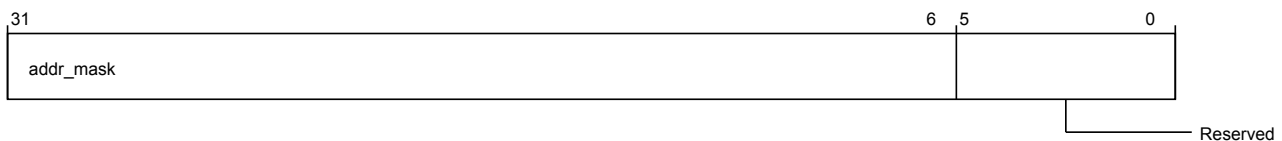


Figure 4-489 por_hnf_hn_sam_hash_addr_mask_reg (low)

The following table shows the hn_sam_hash_addr_mask_reg lower register bit assignments.

Table 4-506 por_hnf_hn_sam_hash_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask applied before hashing	RW	42'h3FFFFFFFFF
5:0	Reserved	Reserved	RO	-

hn_sam_region_cmp_addr_mask_reg

Configures the address mask that is applied before memory region compare.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF48
Register reset	64'b11111111111111111111111111111111

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

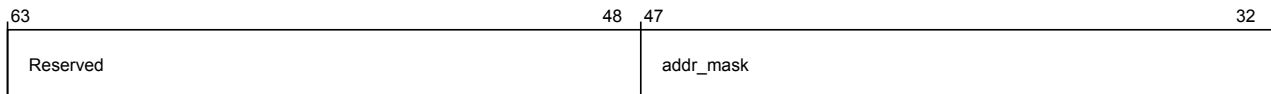


Figure 4-490 por_hnf_hn_sam_region_cmp_addr_mask_reg (high)

The following table shows the hn_sam_region_cmp_addr_mask_reg higher register bit assignments.

Table 4-507 por_hnf_hn_sam_region_cmp_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask applied before memory region compare	RW	22'h3FFFFFF

The following image shows the lower register bit assignments.

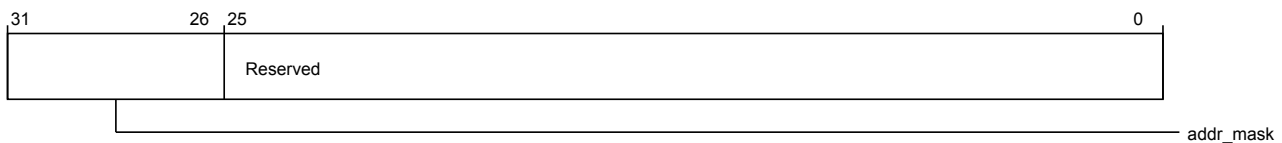


Figure 4-491 por_hnf_hn_sam_region_cmp_addr_mask_reg (low)

The following table shows the hn_sam_region_cmp_addr_mask_reg lower register bit assignments.

Table 4-508 por_hnf_hn_sam_region_cmp_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:26	addr_mask	Address mask applied before memory region compare	RW	22'h3FFFFFF
25:0	Reserved	Reserved	RO	-

por_hnf_abf_lo_addr

Lower address range for Address Based Flush (ABF) [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF50

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_hnf_secure_register_groups_override.ppu`

The following image shows the higher register bit assignments.

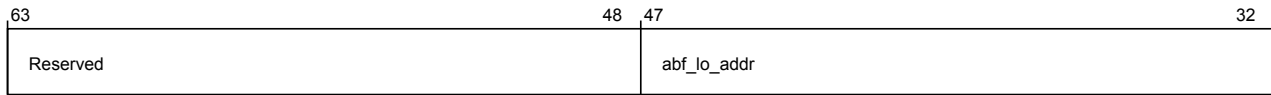


Figure 4-492 `por_hnf_por_hnf_abf_lo_addr` (high)

The following table shows the `por_hnf_abf_lo_addr` higher register bit assignments.

Table 4-509 `por_hnf_por_hnf_abf_lo_addr` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	abf_lo_addr	Lower address range for ABF	RW	48'b0

The following image shows the lower register bit assignments.

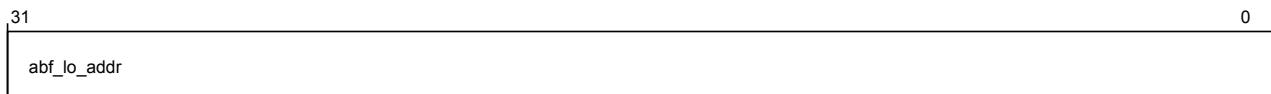


Figure 4-493 `por_hnf_por_hnf_abf_lo_addr` (low)

The following table shows the `por_hnf_abf_lo_addr` lower register bit assignments.

Table 4-510 `por_hnf_por_hnf_abf_lo_addr` (low)

Bits	Field name	Description	Type	Reset
31:0	abf_lo_addr	Lower address range for ABF	RW	48'b0

`por_hnf_abf_hi_addr`

Upper address range for Address Based Flush (ABF) [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF58

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_hnf_secure_register_groups_override.ppu`

The following image shows the higher register bit assignments.

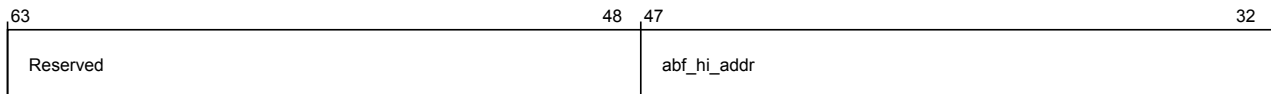


Figure 4-494 por_hnf_por_hnf_abf_hi_addr (high)

The following table shows the por_hnf_abf_hi_addr higher register bit assignments.

Table 4-511 por_hnf_por_hnf_abf_hi_addr (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	abf_hi_addr	Upper address range for ABF	RW	48'b0

The following image shows the lower register bit assignments.

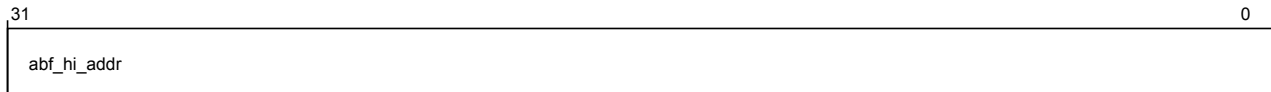


Figure 4-495 por_hnf_por_hnf_abf_hi_addr (low)

The following table shows the por_hnf_abf_hi_addr lower register bit assignments.

Table 4-512 por_hnf_por_hnf_abf_hi_addr (low)

Bits	Field name	Description	Type	Reset
31:0	abf_hi_addr	Upper address range for ABF	RW	48'b0

por_hnf_abf_pr

Functions as the Address Based Flush (ABF) policy register.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF60
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_hnf_secure_register_groups_override.ppu

The following image shows the higher register bit assignments.

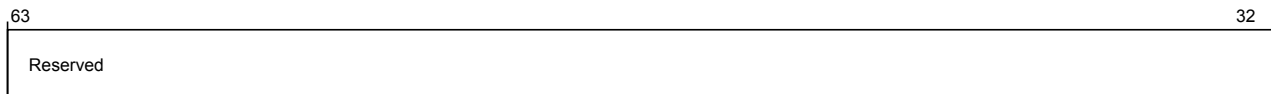


Figure 4-496 `por_hnf_por_hnf_abf_pr` (high)

The following table shows the `por_hnf_abf_pr` higher register bit assignments.

Table 4-513 `por_hnf_por_hnf_abf_pr` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

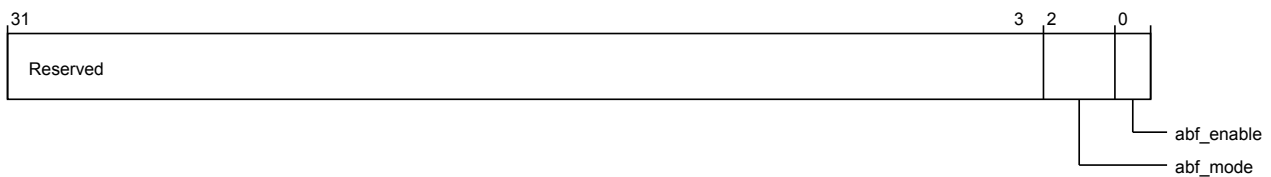


Figure 4-497 `por_hnf_por_hnf_abf_pr` (low)

The following table shows the `por_hnf_abf_pr` lower register bit assignments.

Table 4-514 `por_hnf_por_hnf_abf_pr` (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2:1	abf_mode	ABF mode 2'b00: Clean Invalidate; WB dirty data and invalidate local copy 2'b01: Make Invalidate; invalidate without writing back dirty data 2'b10: Clean Shared; WB dirty data and can keep clean copy 2'b11: Reserved	RW	2'b00
0	abf_enable	Start Address Based Flushing based on high and low address ranges	RW	1'b0

`por_hnf_abf_sr`

Functions as the Address Based Flush (ABF) status register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'hF68
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-498 por_hnf_por_hnf_abf_sr (high)

The following table shows the por_hnf_abf_sr higher register bit assignments.

Table 4-515 por_hnf_por_hnf_abf_sr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

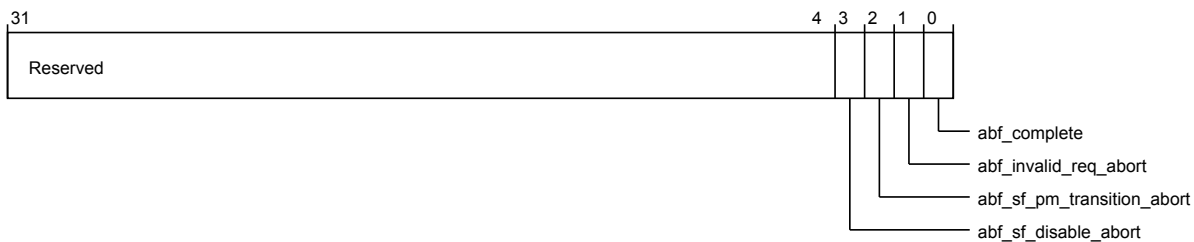


Figure 4-499 por_hnf_por_hnf_abf_sr (low)

The following table shows the por_hnf_abf_sr lower register bit assignments.

Table 4-516 por_hnf_por_hnf_abf_sr (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	abf_sf_disable_abort	ABF aborted due to SF not being enabled, either by configuration or double-bit ECC error	RO	1'b0
2	abf_sf_pm_transition_abort	ABF aborted due to PM transition while ABF in progress, or both PM and ABF requested at the same time	RO	1'b0
1	abf_invalid_req_abort	ABF request made while PM is not in FAM/HAM/SF_ONLY mode; request aborted in this case	RO	1'b0
0	abf_complete	ABF completed	RO	1'b0

por_hnf_rn_phys_id32

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE28
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

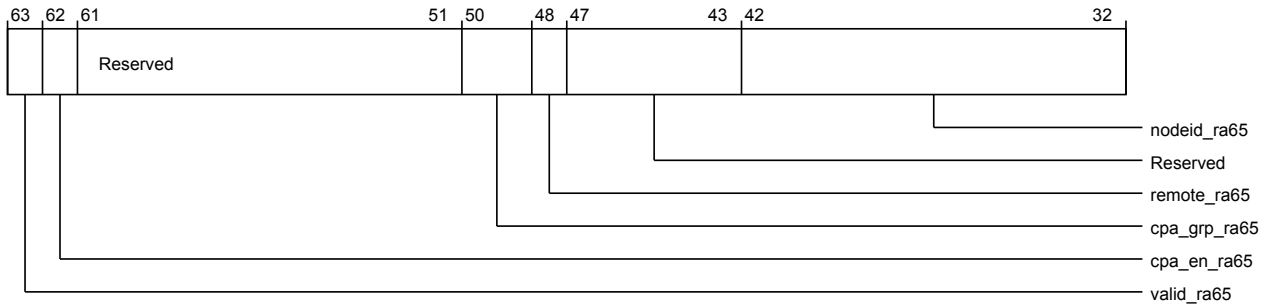


Figure 4-500 por_hnf_por_hnf_rn_phys_id32 (high)

The following table shows the por_hnf_rn_phys_id32 higher register bit assignments.

Table 4-517 por_hnf_por_hnf_rn_phys_id32 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra65	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra65	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra65	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra65	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra65	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

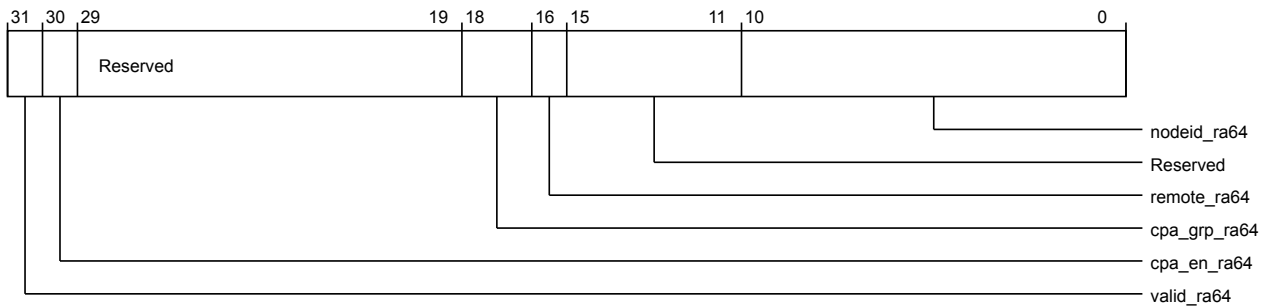


Figure 4-501 por_hnf_por_hnf_rn_phys_id32 (low)

The following table shows the por_hnf_rn_phys_id32 lower register bit assignments.

Table 4-518 por_hnf_por_hnf_rn_phys_id32 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra64	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra64	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra64	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra64	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra64	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id33

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE30
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

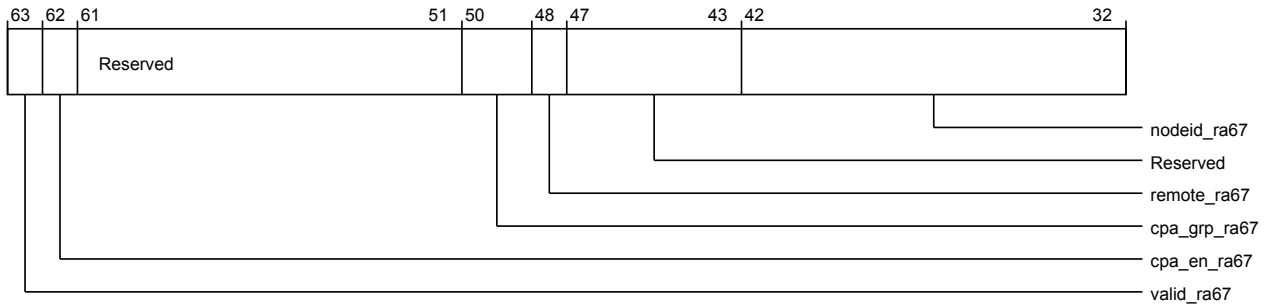


Figure 4-502 por_hnf_por_hnf_rn_phys_id33 (high)

The following table shows the por_hnf_rn_phys_id33 higher register bit assignments.

Table 4-519 por_hnf_por_hnf_rn_phys_id33 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra67	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra67	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra67	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra67	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra67	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

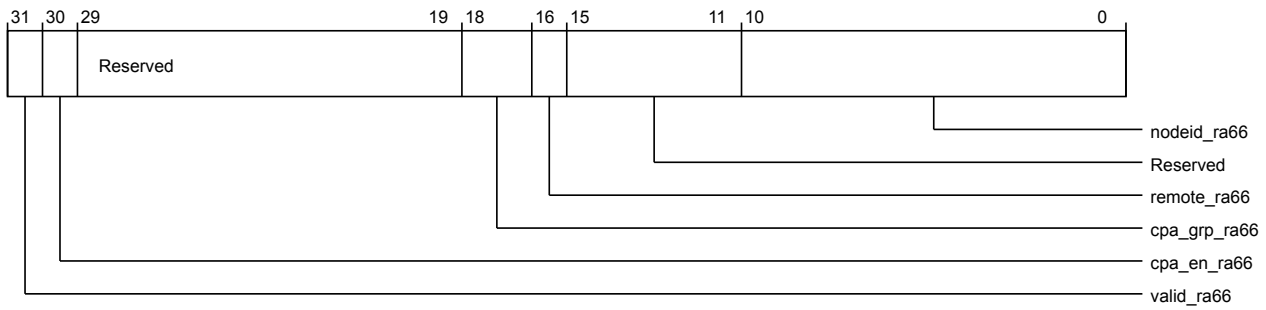


Figure 4-503 `por_hnf_por_hnf_rn_phys_id33 (low)`

The following table shows the `por_hnf_rn_phys_id33` lower register bit assignments.

Table 4-520 `por_hnf_por_hnf_rn_phys_id33 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra66</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra66</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra66</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra66</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra66</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id34`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE38
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

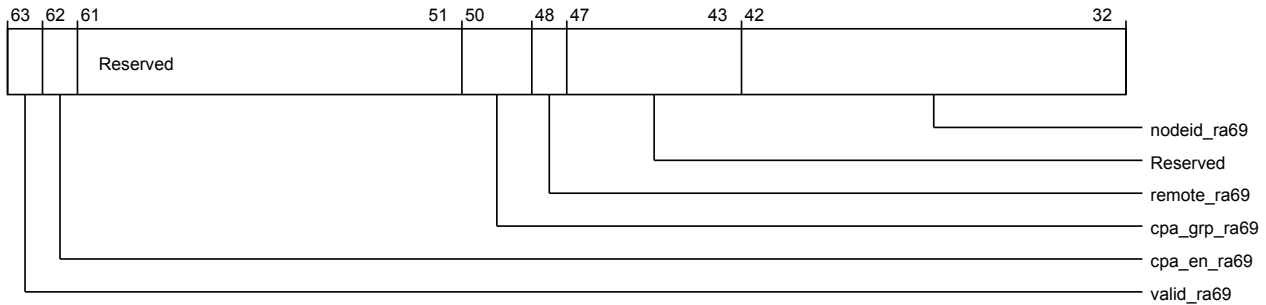


Figure 4-504 por_hnf_por_hnf_rn_phys_id34 (high)

The following table shows the por_hnf_rn_phys_id34 higher register bit assignments.

Table 4-521 por_hnf_por_hnf_rn_phys_id34 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra69	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra69	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra69	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra69	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra69	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

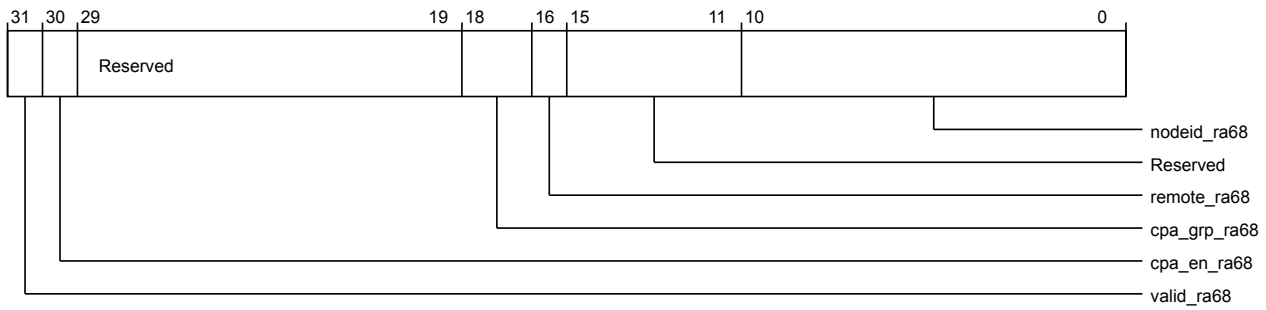


Figure 4-505 por_hnf_por_hnf_rn_phys_id34 (low)

The following table shows the por_hnf_rn_phys_id34 lower register bit assignments.

Table 4-522 por_hnf_por_hnf_rn_phys_id34 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra68	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra68	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra68	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra68	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra68	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id35

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE40
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

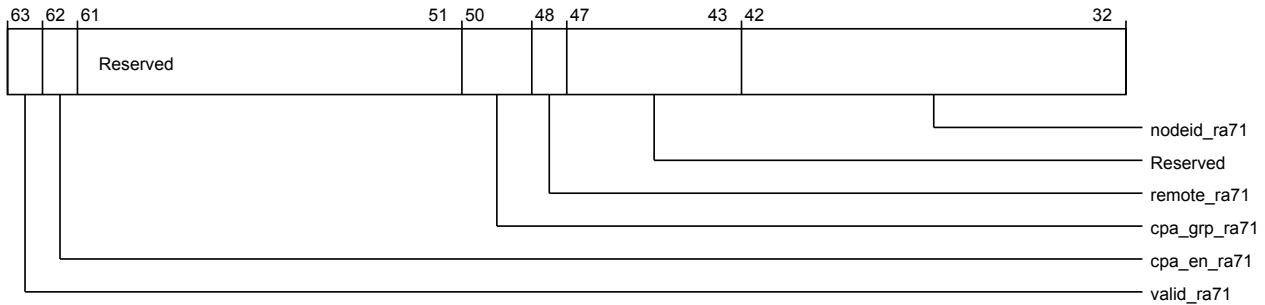


Figure 4-506 por_hnf_por_hnf_rn_phys_id35 (high)

The following table shows the por_hnf_rn_phys_id35 higher register bit assignments.

Table 4-523 por_hnf_por_hnf_rn_phys_id35 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra71	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra71	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra71	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra71	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra71	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

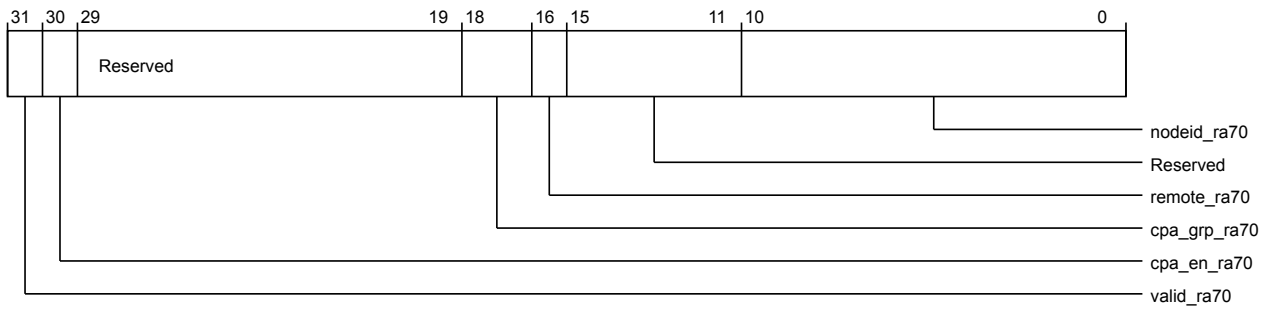


Figure 4-507 por_hnf_por_hnf_rn_phys_id35 (low)

The following table shows the por_hnf_rn_phys_id35 lower register bit assignments.

Table 4-524 por_hnf_por_hnf_rn_phys_id35 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra70	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra70	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra70	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra70	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra70	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id36

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE48
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

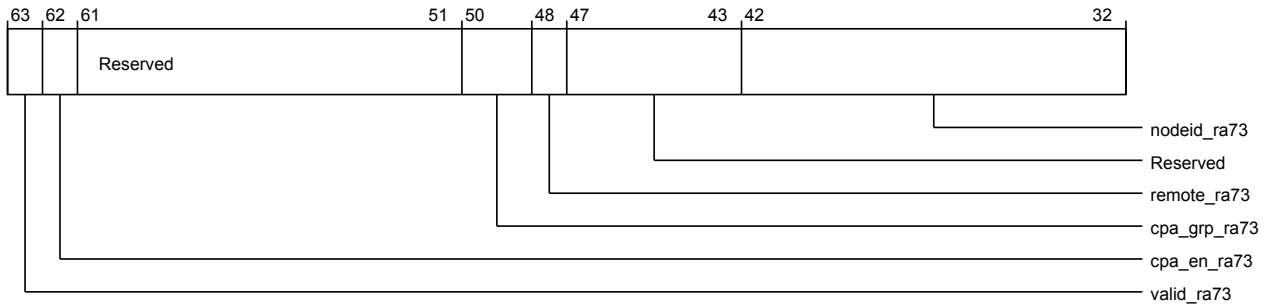


Figure 4-508 por_hnf_por_hnf_rn_phys_id36 (high)

The following table shows the por_hnf_rn_phys_id36 higher register bit assignments.

Table 4-525 por_hnf_por_hnf_rn_phys_id36 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra73	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra73	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra73	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra73	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra73	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

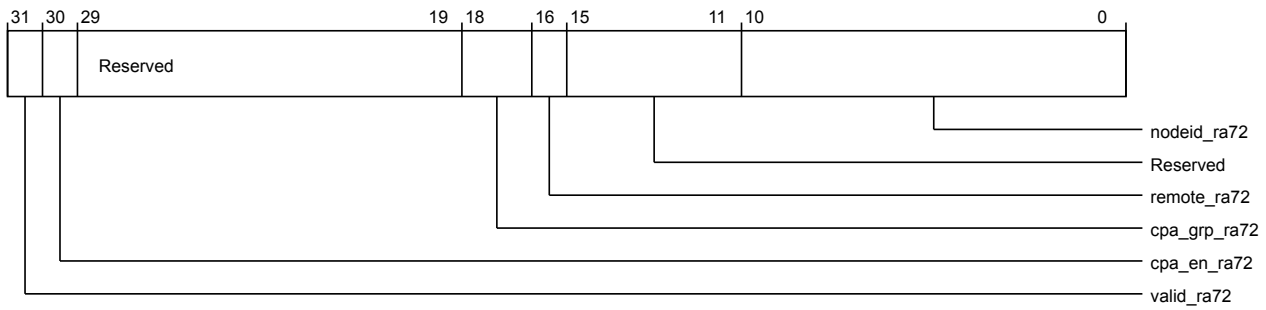


Figure 4-509 por_hnf_por_hnf_rn_phys_id36 (low)

The following table shows the por_hnf_rn_phys_id36 lower register bit assignments.

Table 4-526 por_hnf_por_hnf_rn_phys_id36 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra72	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra72	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra72	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra72	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra72	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id37

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE50
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

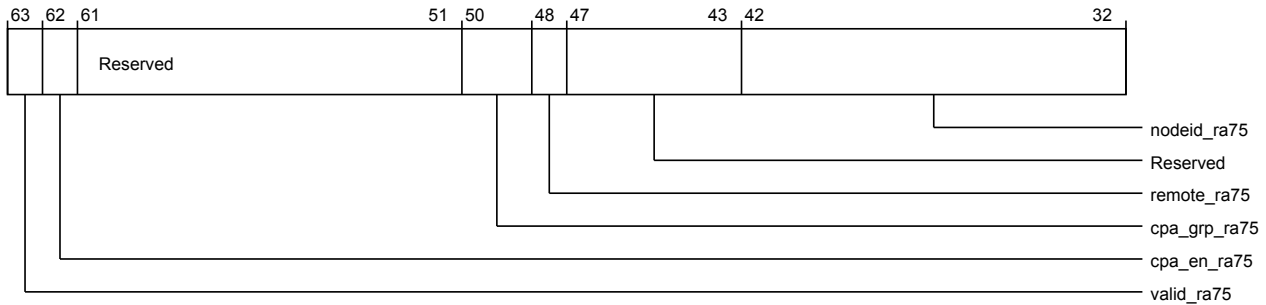


Figure 4-510 `por_hnf_por_hnf_rn_phys_id37 (high)`

The following table shows the `por_hnf_rn_phys_id37` higher register bit assignments.

Table 4-527 `por_hnf_por_hnf_rn_phys_id37 (high)`

Bits	Field name	Description	Type	Reset
63	<code>valid_ra75</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	<code>cpa_en_ra75</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	<code>cpa_grp_ra75</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	<code>remote_ra75</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>nodeid_ra75</code>	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

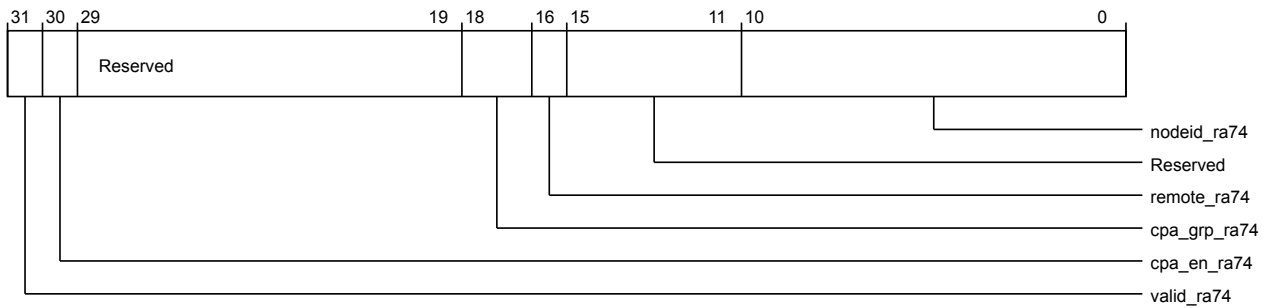


Figure 4-511 por_hnf_por_hnf_rn_phys_id37 (low)

The following table shows the por_hnf_rn_phys_id37 lower register bit assignments.

Table 4-528 por_hnf_por_hnf_rn_phys_id37 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra74	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra74	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra74	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra74	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra74	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id38

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE58
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

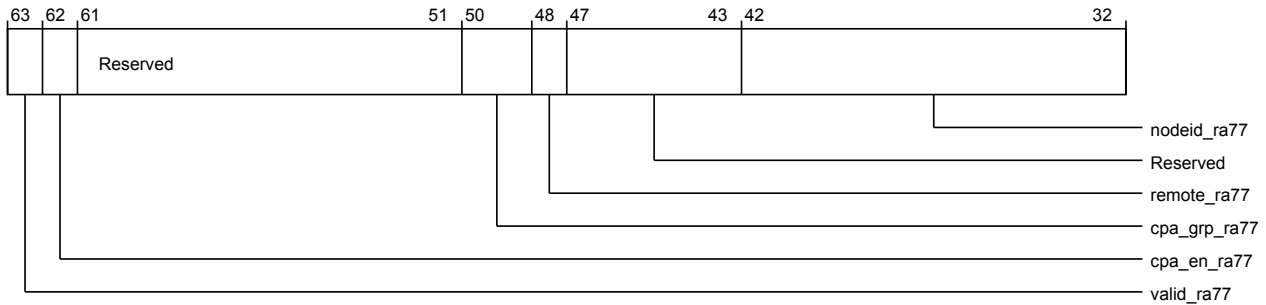


Figure 4-512 `por_hnf_por_hnf_rn_phys_id38` (high)

The following table shows the `por_hnf_rn_phys_id38` higher register bit assignments.

Table 4-529 `por_hnf_por_hnf_rn_phys_id38` (high)

Bits	Field name	Description	Type	Reset
63	<code>valid_ra77</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	<code>cpa_en_ra77</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	<code>cpa_grp_ra77</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	<code>remote_ra77</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>nodeid_ra77</code>	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

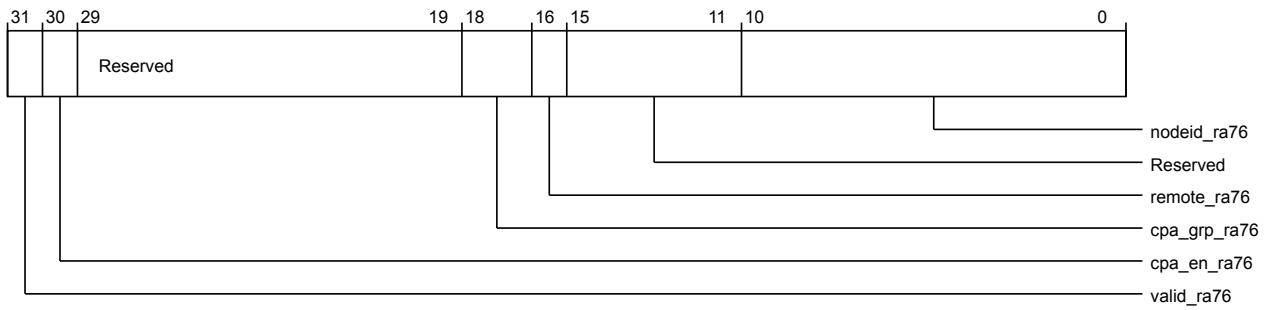


Figure 4-513 por_hnf_por_hnf_rn_phys_id38 (low)

The following table shows the por_hnf_rn_phys_id38 lower register bit assignments.

Table 4-530 por_hnf_por_hnf_rn_phys_id38 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra76	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra76	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra76	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra76	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra76	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id39

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE60
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

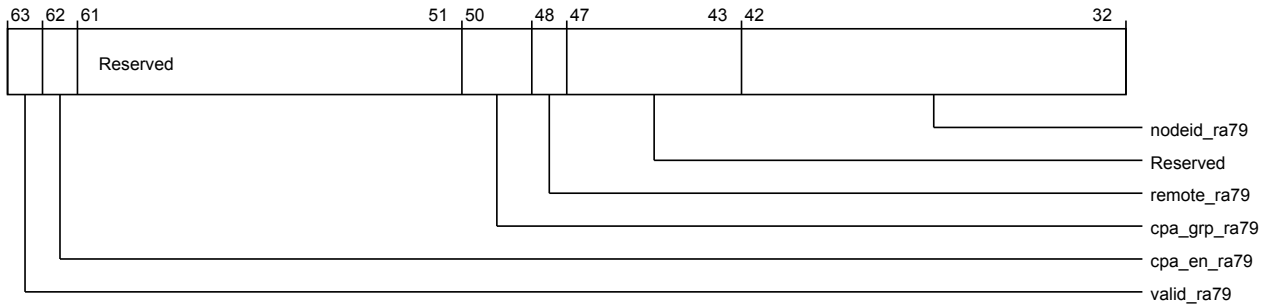


Figure 4-514 `por_hnf_por_hnf_rn_phys_id39` (high)

The following table shows the `por_hnf_rn_phys_id39` higher register bit assignments.

Table 4-531 `por_hnf_por_hnf_rn_phys_id39` (high)

Bits	Field name	Description	Type	Reset
63	<code>valid_ra79</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	<code>cpa_en_ra79</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	<code>cpagrpa79</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	<code>remote_ra79</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>nodeid_ra79</code>	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

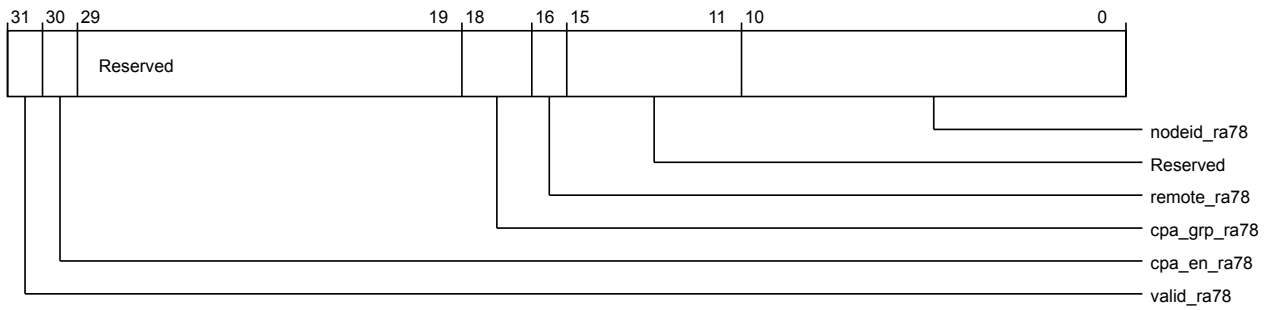


Figure 4-515 por_hnf_por_hnf_rn_phys_id39 (low)

The following table shows the por_hnf_rn_phys_id39 lower register bit assignments.

Table 4-532 por_hnf_por_hnf_rn_phys_id39 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra78	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra78	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra78	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra78	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra78	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id40

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE68
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

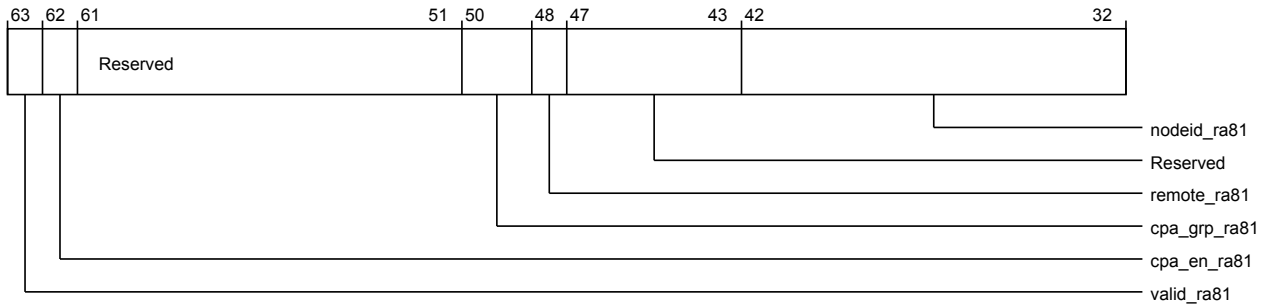


Figure 4-516 por_hnf_por_hnf_rn_phys_id40 (high)

The following table shows the por_hnf_rn_phys_id40 higher register bit assignments.

Table 4-533 por_hnf_por_hnf_rn_phys_id40 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra81	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra81	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra81	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra81	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra81	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

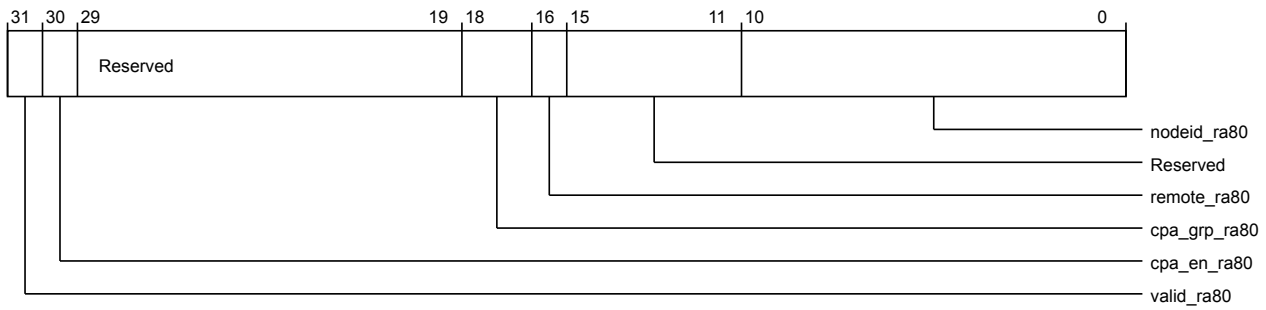


Figure 4-517 `por_hnf_por_hnf_rn_phys_id40 (low)`

The following table shows the `por_hnf_rn_phys_id40` lower register bit assignments.

Table 4-534 `por_hnf_por_hnf_rn_phys_id40 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra80</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra80</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra80</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra80</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra80</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id41`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE70
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

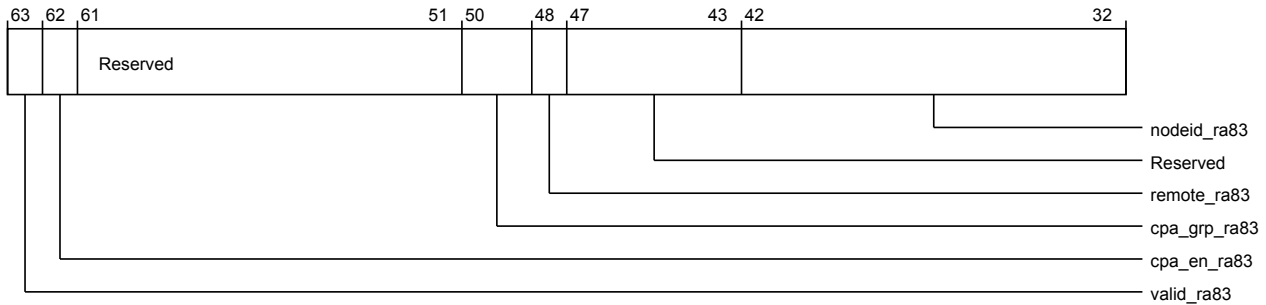


Figure 4-518 por_hnf_por_hnf_rn_phys_id41 (high)

The following table shows the por_hnf_rn_phys_id41 higher register bit assignments.

Table 4-535 por_hnf_por_hnf_rn_phys_id41 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra83	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra83	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra83	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra83	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra83	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

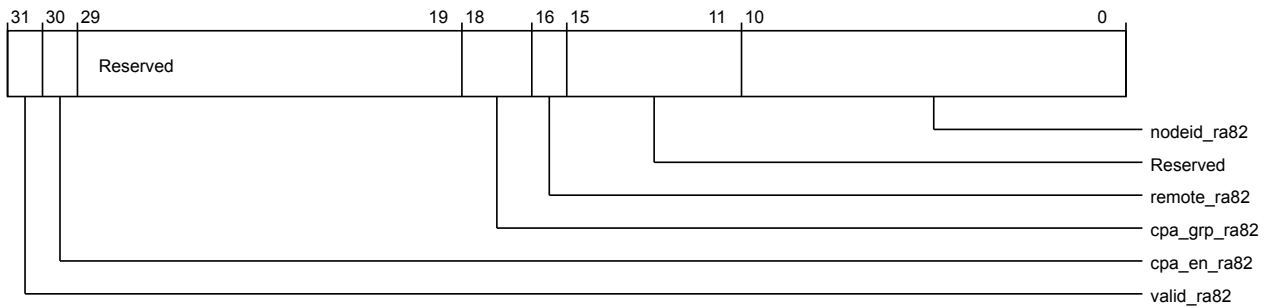


Figure 4-519 `por_hnf_por_hnf_rn_phys_id41 (low)`

The following table shows the `por_hnf_rn_phys_id41` lower register bit assignments.

Table 4-536 `por_hnf_por_hnf_rn_phys_id41 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra82</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra82</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra82</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra82</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra82</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id42`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE78
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

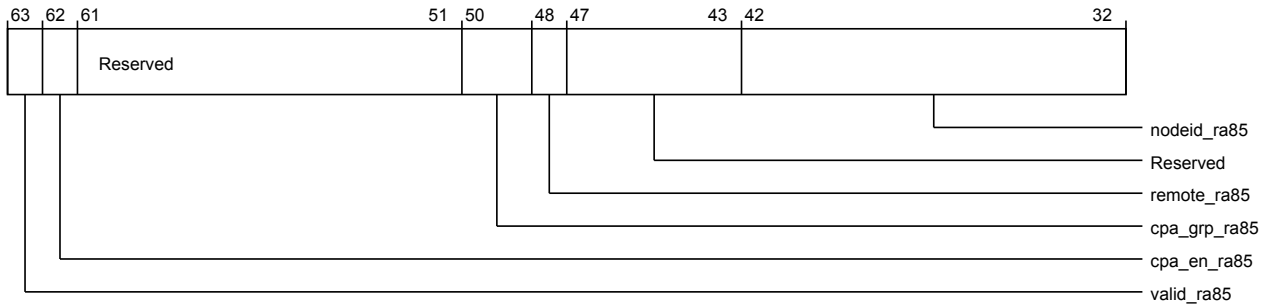


Figure 4-520 por_hnf_por_hnf_rn_phys_id42 (high)

The following table shows the por_hnf_rn_phys_id42 higher register bit assignments.

Table 4-537 por_hnf_por_hnf_rn_phys_id42 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra85	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra85	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra85	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra85	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra85	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

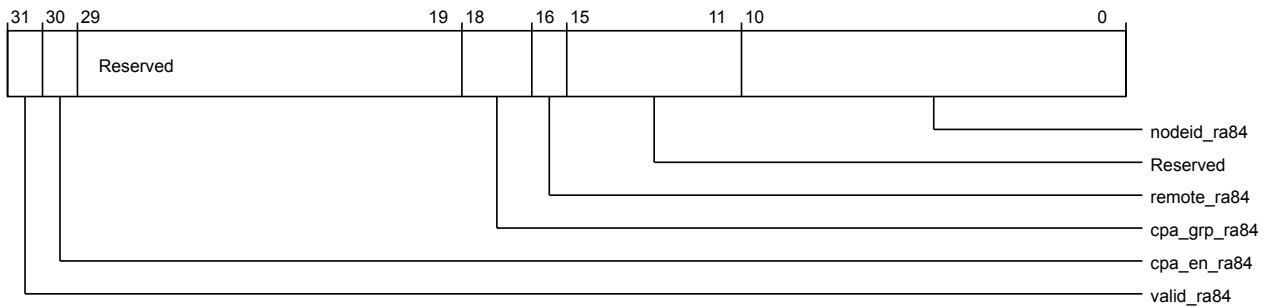


Figure 4-521 por_hnf_por_hnf_rn_phys_id42 (low)

The following table shows the por_hnf_rn_phys_id42 lower register bit assignments.

Table 4-538 por_hnf_por_hnf_rn_phys_id42 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra84	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra84	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra84	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra84	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra84	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id43

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE80
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

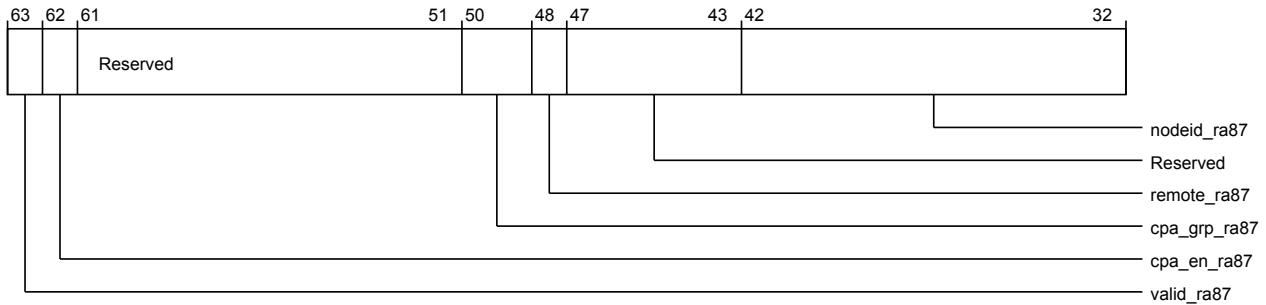


Figure 4-522 `por_hnf_por_hnf_rn_phys_id43` (high)

The following table shows the `por_hnf_rn_phys_id43` higher register bit assignments.

Table 4-539 `por_hnf_por_hnf_rn_phys_id43` (high)

Bits	Field name	Description	Type	Reset
63	<code>valid_ra87</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	<code>cpa_en_ra87</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	<code>cpa_grp_ra87</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	<code>remote_ra87</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>nodeid_ra87</code>	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

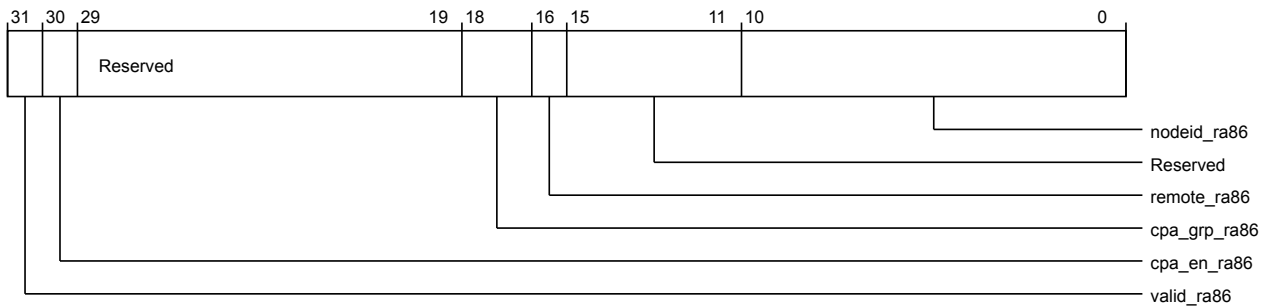


Figure 4-523 por_hnf_por_hnf_rn_phys_id43 (low)

The following table shows the por_hnf_rn_phys_id43 lower register bit assignments.

Table 4-540 por_hnf_por_hnf_rn_phys_id43 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra86	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra86	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra86	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra86	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra86	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id44

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE88
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

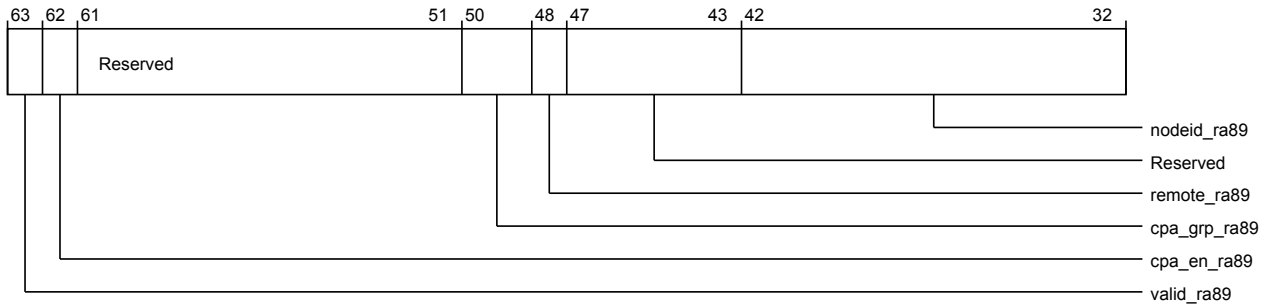


Figure 4-524 por_hnf_por_hnf_rn_phys_id44 (high)

The following table shows the por_hnf_rn_phys_id44 higher register bit assignments.

Table 4-541 por_hnf_por_hnf_rn_phys_id44 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra89	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra89	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra89	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra89	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra89	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

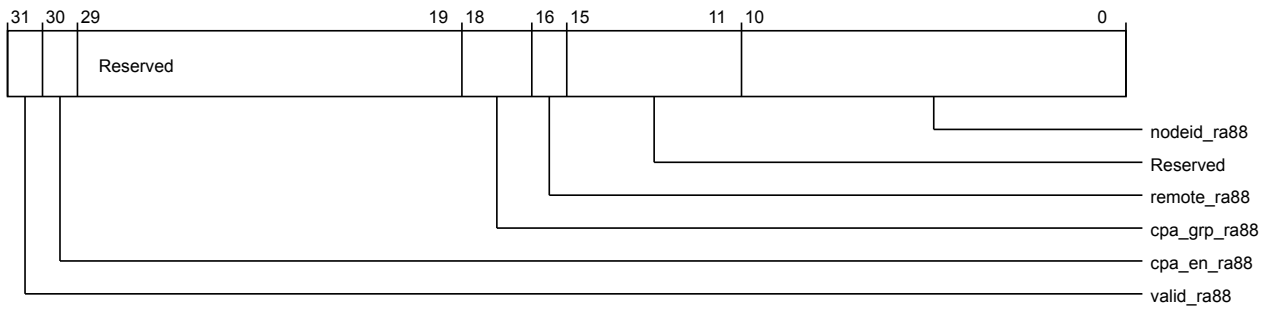


Figure 4-525 `por_hnf_por_hnf_rn_phys_id44 (low)`

The following table shows the `por_hnf_rn_phys_id44` lower register bit assignments.

Table 4-542 `por_hnf_por_hnf_rn_phys_id44 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra88</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpn_en_ra88</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpn_grp_ra88</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra88</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra88</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id45`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE90
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

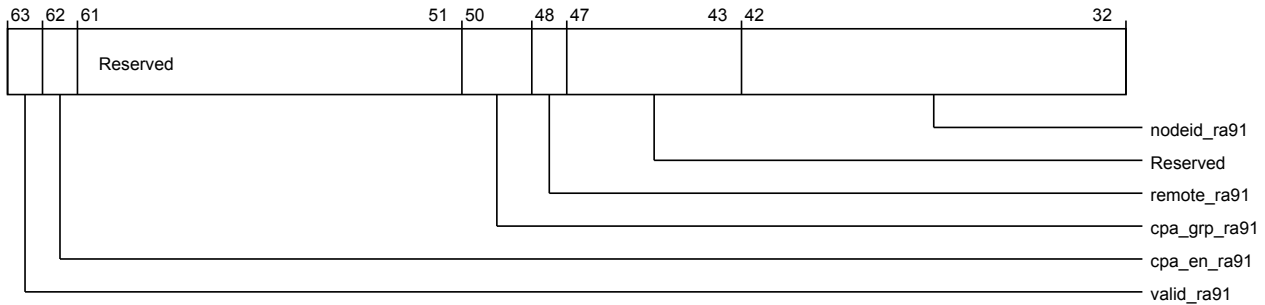


Figure 4-526 por_hnf_por_hnf_rn_phys_id45 (high)

The following table shows the por_hnf_rn_phys_id45 higher register bit assignments.

Table 4-543 por_hnf_por_hnf_rn_phys_id45 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra91	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra91	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra91	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra91	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra91	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

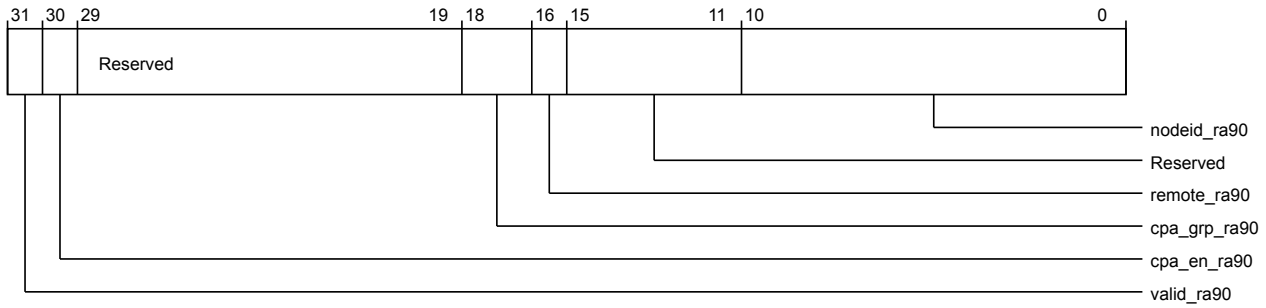


Figure 4-527 `por_hnf_por_hnf_rn_phys_id45 (low)`

The following table shows the `por_hnf_rn_phys_id45` lower register bit assignments.

Table 4-544 `por_hnf_por_hnf_rn_phys_id45 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra90</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra90</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpagrpa90</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra90</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra90</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id46`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE98
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

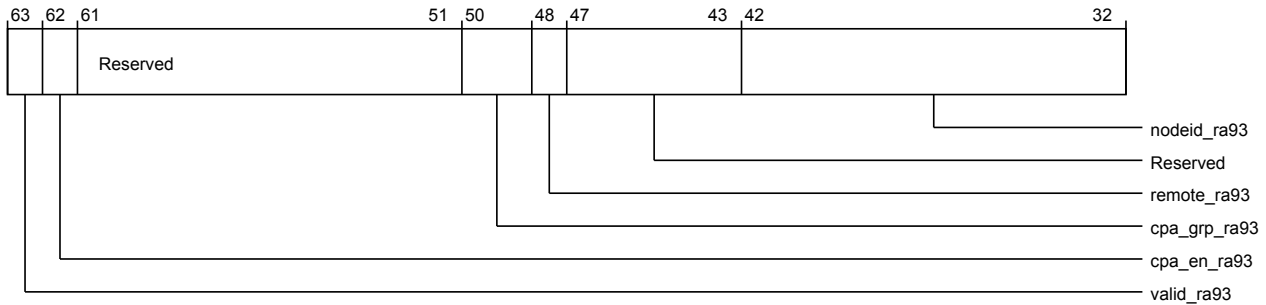


Figure 4-528 `por_hnf_por_hnf_rn_phys_id46` (high)

The following table shows the `por_hnf_rn_phys_id46` higher register bit assignments.

Table 4-545 `por_hnf_por_hnf_rn_phys_id46` (high)

Bits	Field name	Description	Type	Reset
63	<code>valid_ra93</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	<code>cpa_en_ra93</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	<code>cpagrpa93</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	<code>remote_ra93</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>nodeid_ra93</code>	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

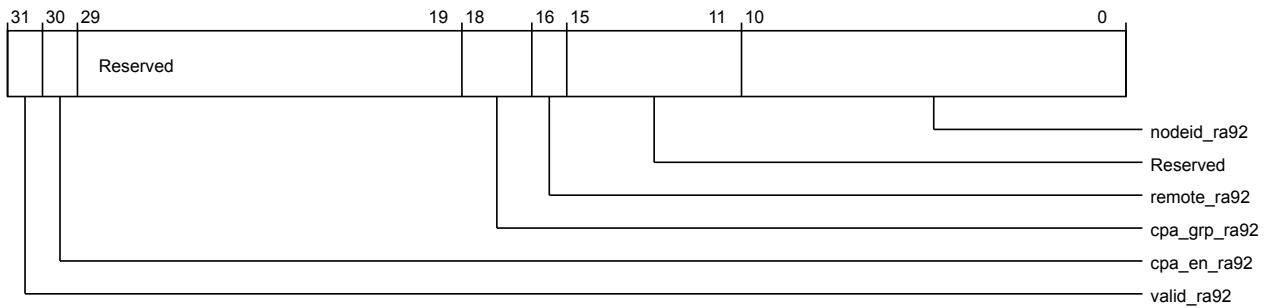


Figure 4-529 por_hnf_por_hnf_rn_phys_id46 (low)

The following table shows the por_hnf_rn_phys_id46 lower register bit assignments.

Table 4-546 por_hnf_por_hnf_rn_phys_id46 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra92	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra92	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra92	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra92	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra92	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id47

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'HEA0
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

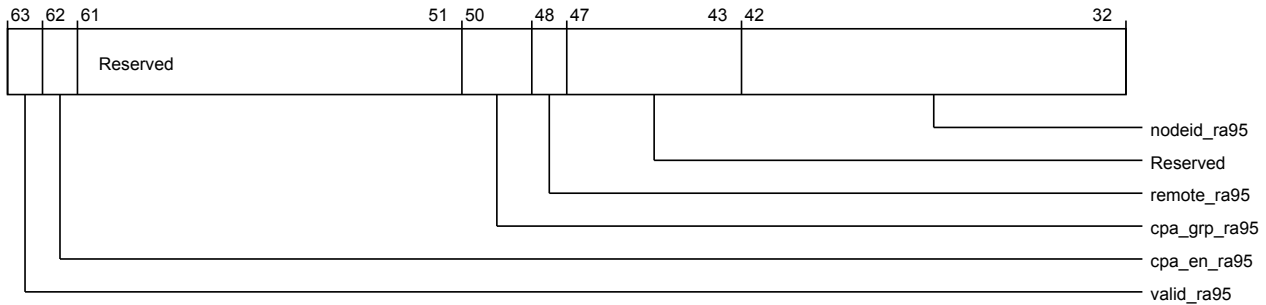


Figure 4-530 por_hnf_por_hnf_rn_phys_id47 (high)

The following table shows the por_hnf_rn_phys_id47 higher register bit assignments.

Table 4-547 por_hnf_por_hnf_rn_phys_id47 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra95	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra95	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra95	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra95	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra95	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

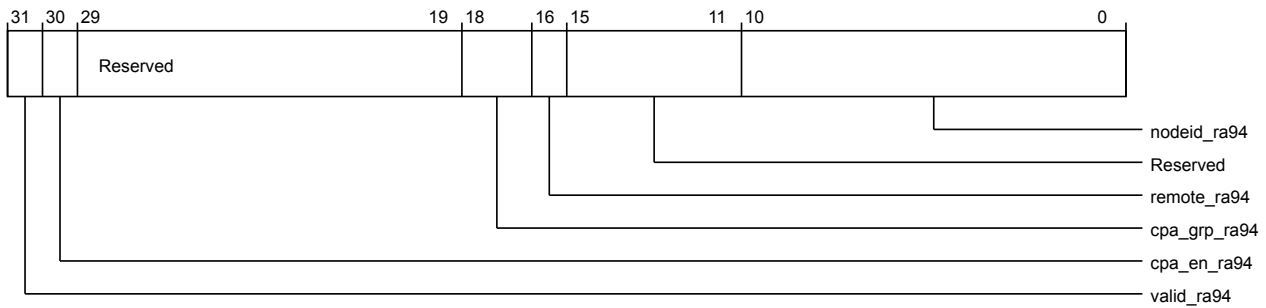


Figure 4-531 por_hnf_por_hnf_rn_phys_id47 (low)

The following table shows the por_hnf_rn_phys_id47 lower register bit assignments.

Table 4-548 por_hnf_por_hnf_rn_phys_id47 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra94	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra94	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra94	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra94	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra94	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id48

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEA8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

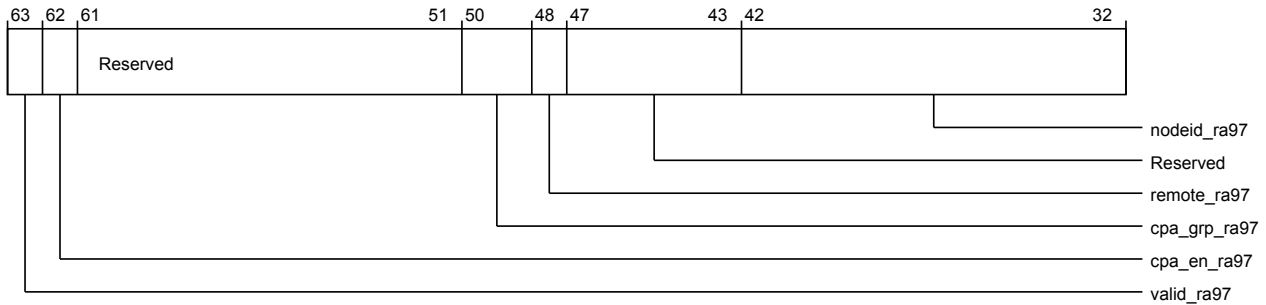


Figure 4-532 por_hnf_por_hnf_rn_phys_id48 (high)

The following table shows the por_hnf_rn_phys_id48 higher register bit assignments.

Table 4-549 por_hnf_por_hnf_rn_phys_id48 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra97	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra97	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra97	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra97	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra97	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

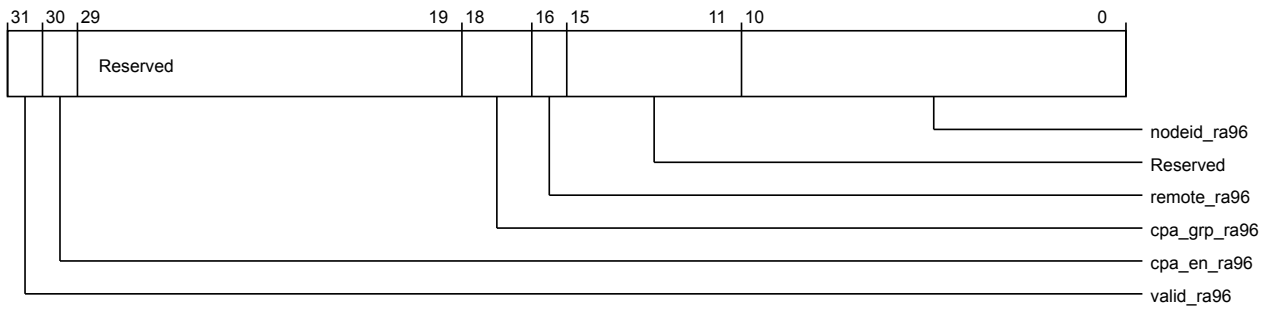


Figure 4-533 `por_hnf_por_hnf_rn_phys_id48 (low)`

The following table shows the `por_hnf_rn_phys_id48` lower register bit assignments.

Table 4-550 `por_hnf_por_hnf_rn_phys_id48 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra96</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra96</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra96</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra96</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra96</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id49`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEB0
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

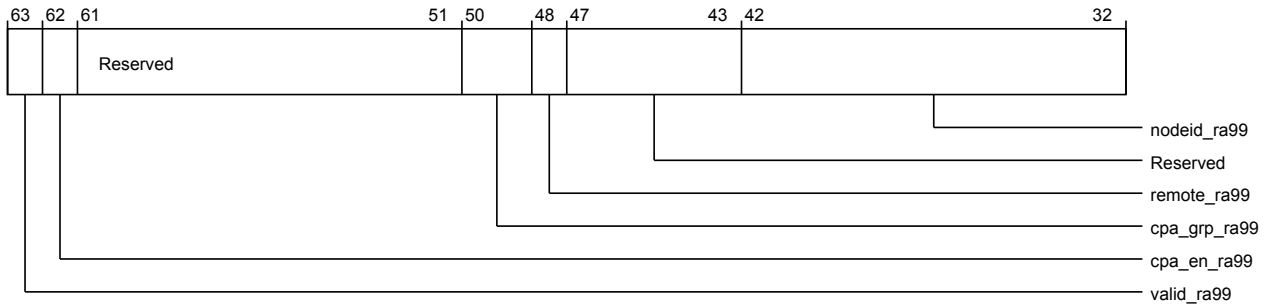


Figure 4-534 por_hnf_por_hnf_rn_phys_id49 (high)

The following table shows the por_hnf_rn_phys_id49 higher register bit assignments.

Table 4-551 por_hnf_por_hnf_rn_phys_id49 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra99	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra99	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra99	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra99	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra99	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

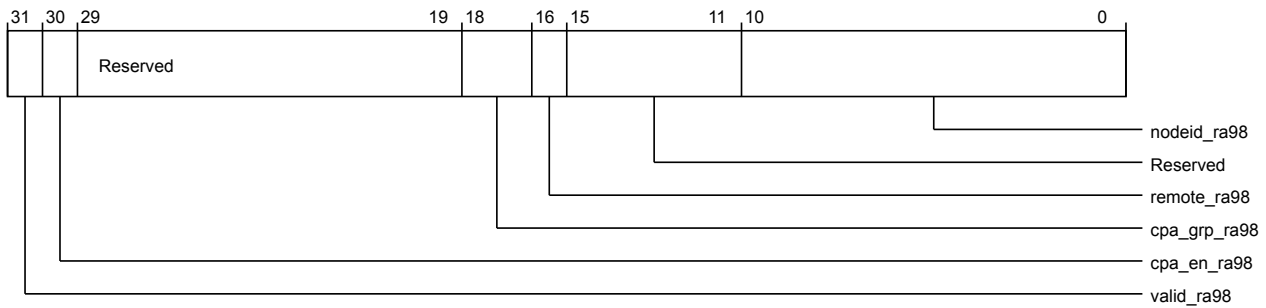


Figure 4-535 por_hnf_por_hnf_rn_phys_id49 (low)

The following table shows the por_hnf_rn_phys_id49 lower register bit assignments.

Table 4-552 por_hnf_por_hnf_rn_phys_id49 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra98	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra98	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra98	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra98	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra98	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id50

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEB8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

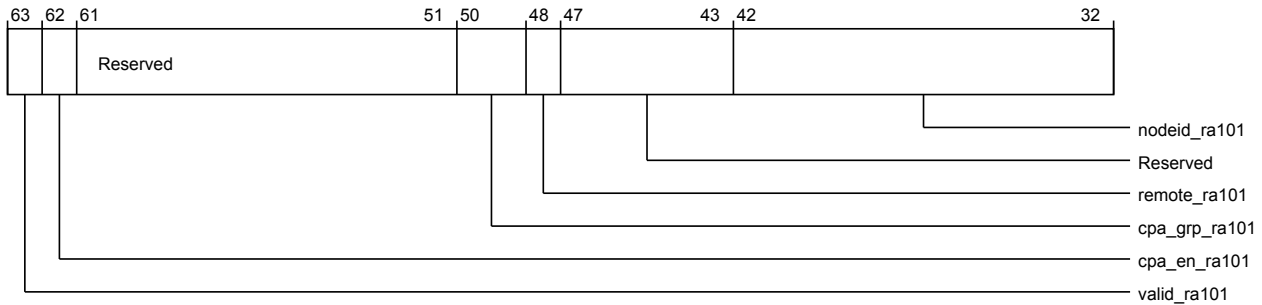


Figure 4-536 por_hnf_por_hnf_rn_phys_id50 (high)

The following table shows the por_hnf_rn_phys_id50 higher register bit assignments.

Table 4-553 por_hnf_por_hnf_rn_phys_id50 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra101	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra101	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra101	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra101	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra101	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

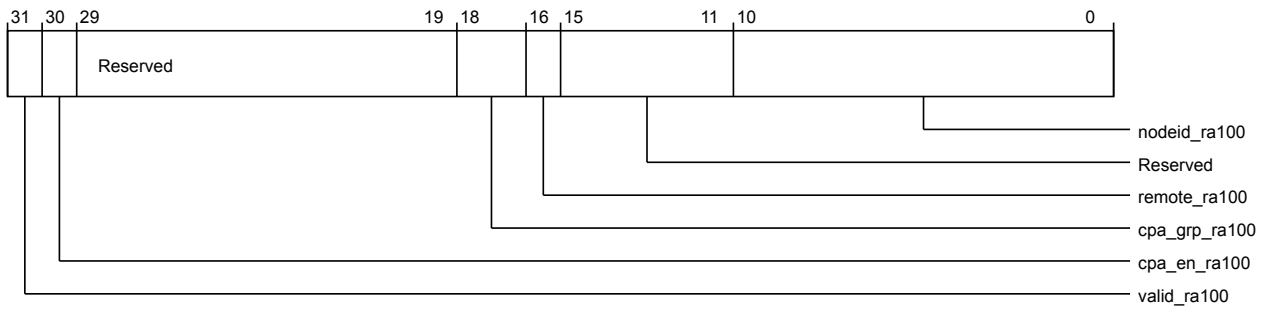


Figure 4-537 por_hnf_por_hnf_rn_phys_id50 (low)

The following table shows the por_hnf_rn_phys_id50 lower register bit assignments.

Table 4-554 por_hnf_por_hnf_rn_phys_id50 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra100	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra100	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra100	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra100	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra100	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id51

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEC0
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

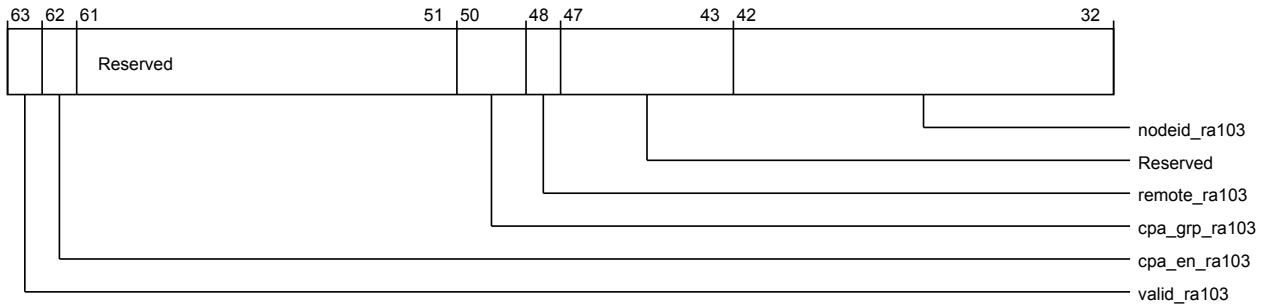


Figure 4-538 `por_hnf_por_hnf_rn_phys_id51` (high)

The following table shows the `por_hnf_rn_phys_id51` higher register bit assignments.

Table 4-555 `por_hnf_por_hnf_rn_phys_id51` (high)

Bits	Field name	Description	Type	Reset
63	<code>valid_ra103</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	<code>cpa_en_ra103</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	<code>cpa_grp_ra103</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	<code>remote_ra103</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>nodeid_ra103</code>	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

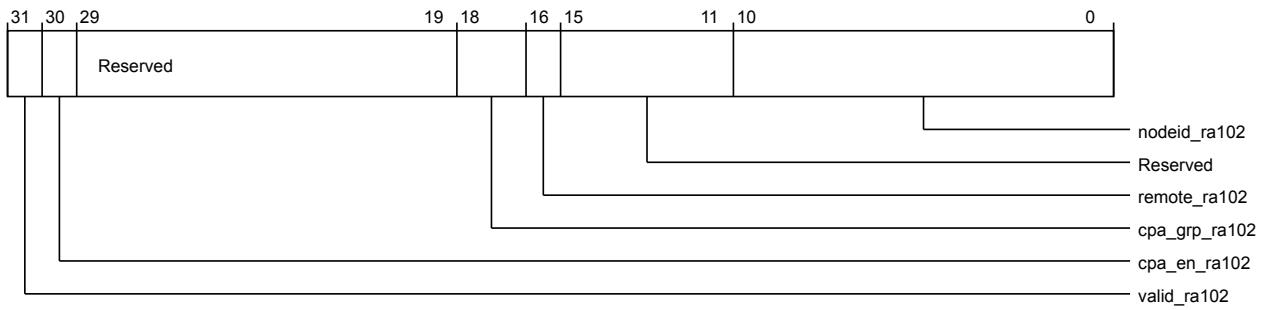


Figure 4-539 `por_hnf_por_hnf_rn_phys_id51` (low)

The following table shows the `por_hnf_rn_phys_id51` lower register bit assignments.

Table 4-556 `por_hnf_por_hnf_rn_phys_id51` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_ra102</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra102</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra102</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra102</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra102</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id52`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEC8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

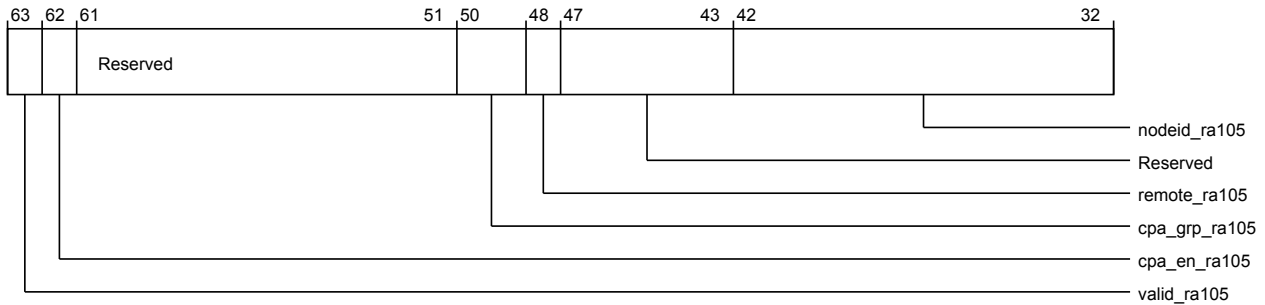


Figure 4-540 por_hnf_por_hnf_rn_phys_id52 (high)

The following table shows the por_hnf_rn_phys_id52 higher register bit assignments.

Table 4-557 por_hnf_por_hnf_rn_phys_id52 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra105	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra105	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra105	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra105	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra105	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

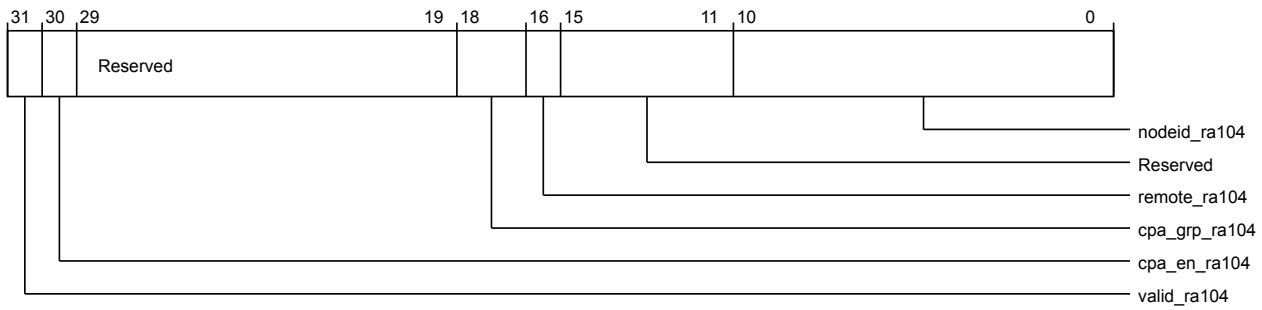


Figure 4-541 `por_hnf_por_hnf_rn_phys_id52 (low)`

The following table shows the `por_hnf_rn_phys_id52` lower register bit assignments.

Table 4-558 `por_hnf_por_hnf_rn_phys_id52 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra104</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpn_en_ra104</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpn_grp_ra104</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra104</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra104</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id53`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hED0
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

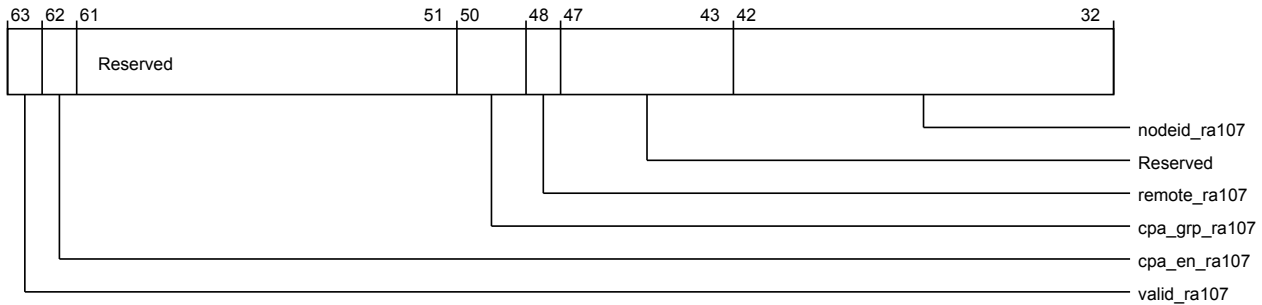


Figure 4-542 por_hnf_por_hnf_rn_phys_id53 (high)

The following table shows the `por_hnf_rn_phys_id53` higher register bit assignments.

Table 4-559 por_hnf_por_hnf_rn_phys_id53 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra107	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra107	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra107	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra107	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra107	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

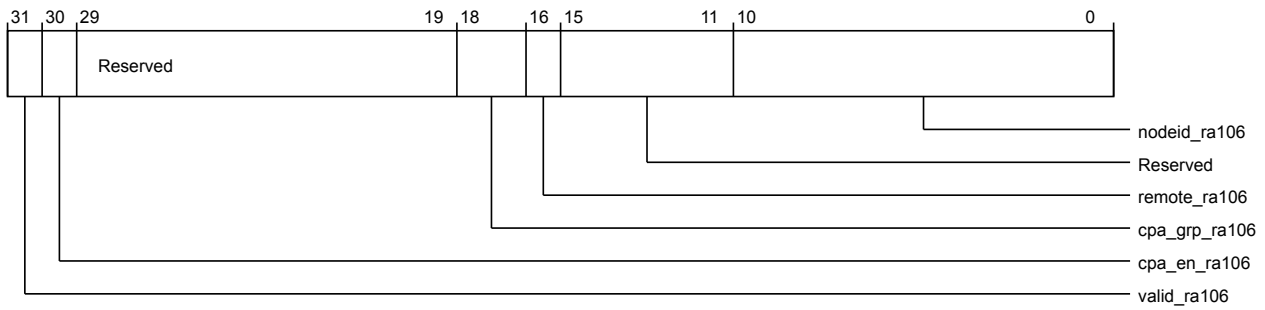


Figure 4-543 por_hnf_por_hnf_rn_phys_id53 (low)

The following table shows the por_hnf_rn_phys_id53 lower register bit assignments.

Table 4-560 por_hnf_por_hnf_rn_phys_id53 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra106	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra106	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra106	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra106	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra106	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id54

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hED8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

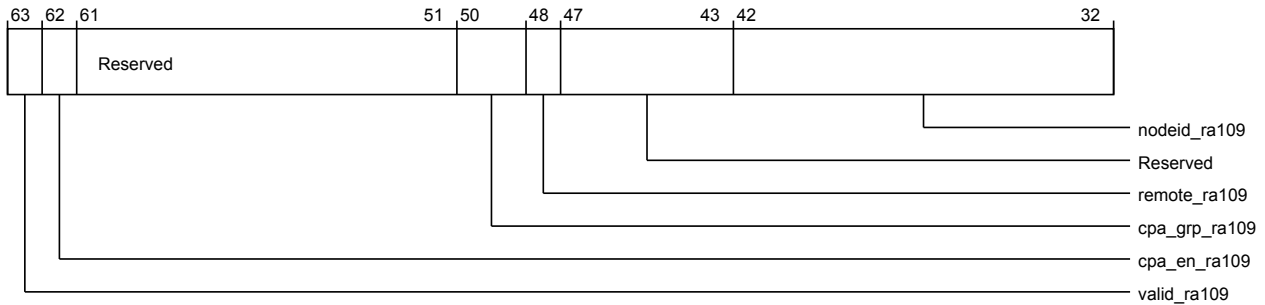


Figure 4-544 por_hnf_por_hnf_rn_phys_id54 (high)

The following table shows the por_hnf_rn_phys_id54 higher register bit assignments.

Table 4-561 por_hnf_por_hnf_rn_phys_id54 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra109	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra109	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra109	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra109	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra109	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

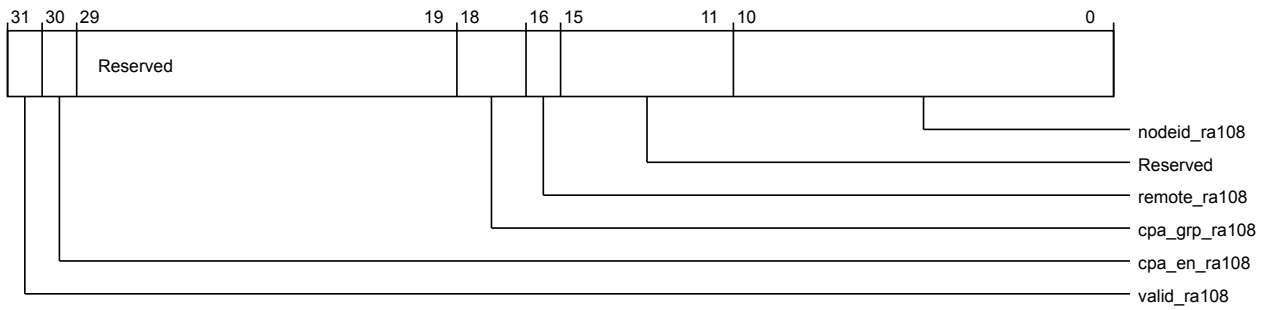


Figure 4-545 `por_hnf_por_hnf_rn_phys_id54 (low)`

The following table shows the `por_hnf_rn_phys_id54` lower register bit assignments.

Table 4-562 `por_hnf_por_hnf_rn_phys_id54 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra108</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra108</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra108</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra108</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra108</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id55`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEE0
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

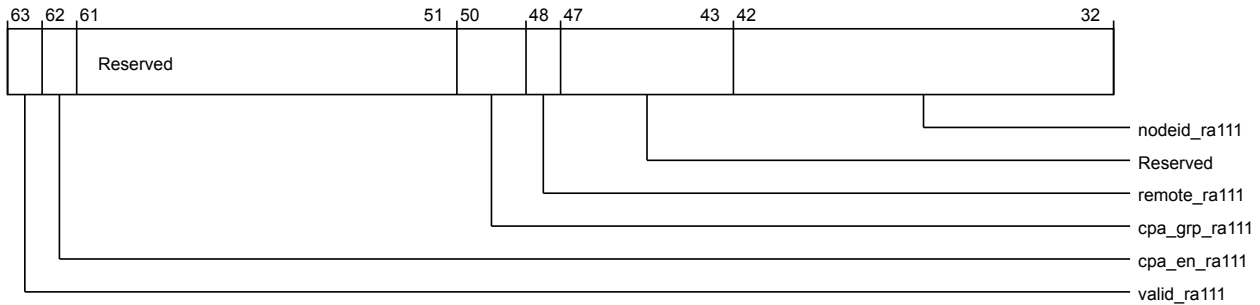


Figure 4-546 por_hnf_por_hnf_rn_phys_id55 (high)

The following table shows the por_hnf_rn_phys_id55 higher register bit assignments.

Table 4-563 por_hnf_por_hnf_rn_phys_id55 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra111	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra111	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra111	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra111	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra111	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

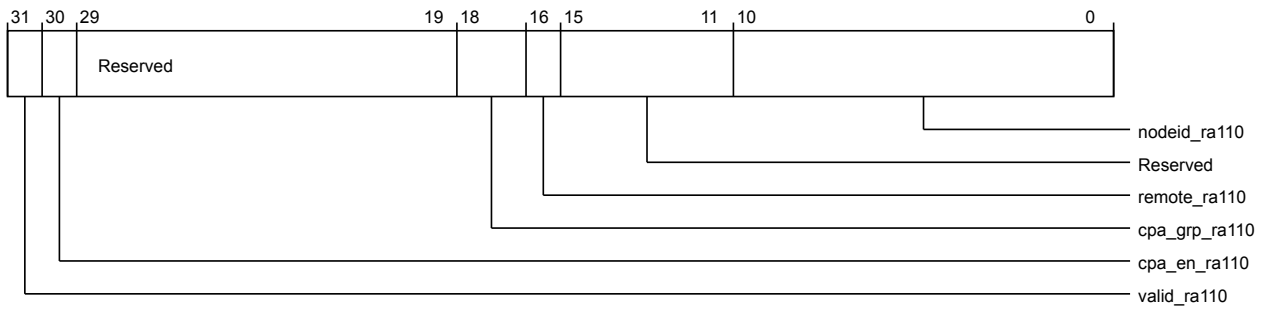


Figure 4-547 `por_hnf_por_hnf_rn_phys_id55 (low)`

The following table shows the `por_hnf_rn_phys_id55` lower register bit assignments.

Table 4-564 `por_hnf_por_hnf_rn_phys_id55 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra110</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra110</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra110</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra110</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra110</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id56`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEE8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

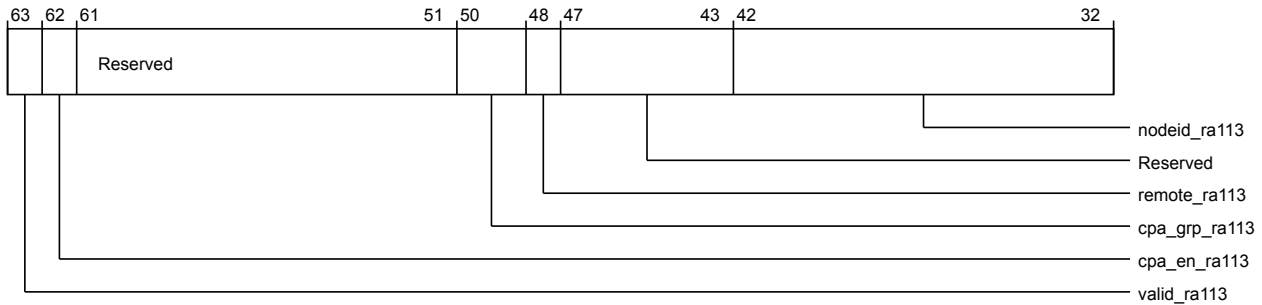


Figure 4-548 `por_hnf_por_hnf_rn_phys_id56` (high)

The following table shows the `por_hnf_rn_phys_id56` higher register bit assignments.

Table 4-565 `por_hnf_por_hnf_rn_phys_id56` (high)

Bits	Field name	Description	Type	Reset
63	<code>valid_ra113</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	<code>cpa_en_ra113</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	<code>cpa_grp_ra113</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	<code>remote_ra113</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>nodeid_ra113</code>	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

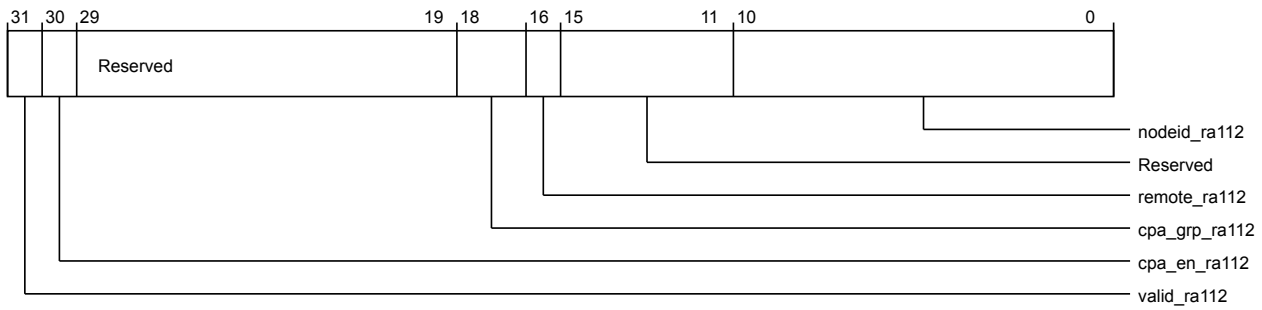


Figure 4-549 `por_hnf_por_hnf_rn_phys_id56 (low)`

The following table shows the `por_hnf_rn_phys_id56` lower register bit assignments.

Table 4-566 `por_hnf_por_hnf_rn_phys_id56 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra112</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra112</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra112</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra112</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra112</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id57`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEF0
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

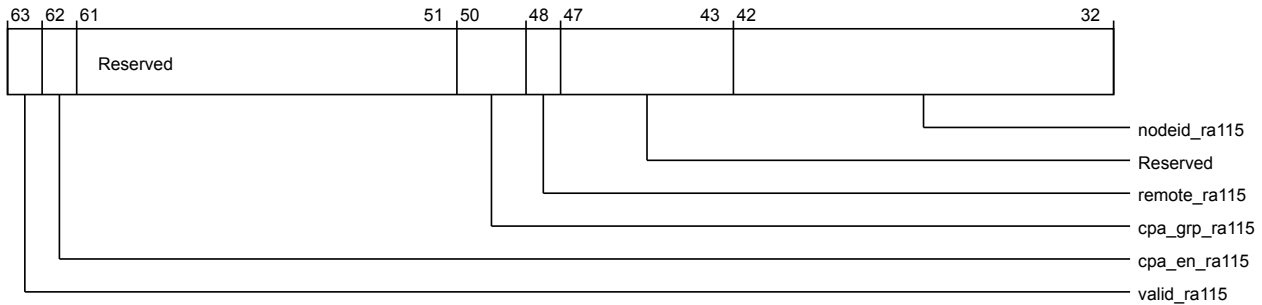


Figure 4-550 por_hnf_por_hnf_rn_phys_id57 (high)

The following table shows the por_hnf_rn_phys_id57 higher register bit assignments.

Table 4-567 por_hnf_por_hnf_rn_phys_id57 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra115	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra115	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra115	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra115	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra115	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

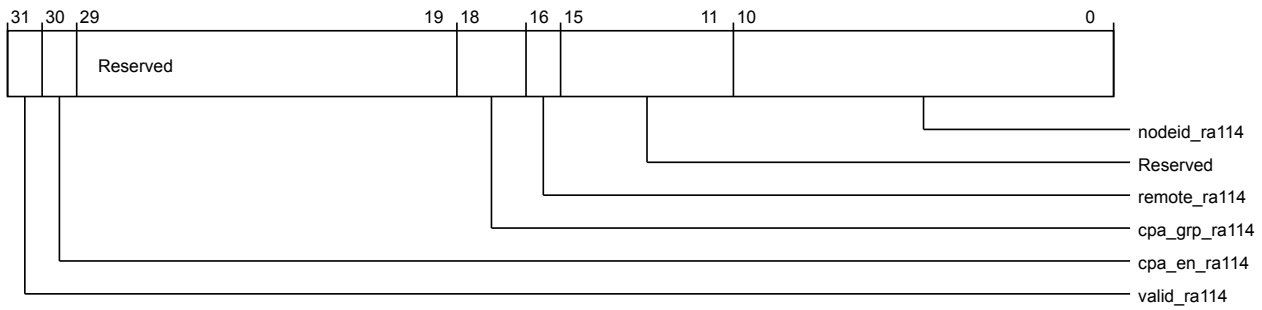


Figure 4-551 `por_hnf_por_hnf_rn_phys_id57 (low)`

The following table shows the `por_hnf_rn_phys_id57` lower register bit assignments.

Table 4-568 `por_hnf_por_hnf_rn_phys_id57 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra114</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpn_en_ra114</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpn_grp_ra114</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra114</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra114</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id58`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEF8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

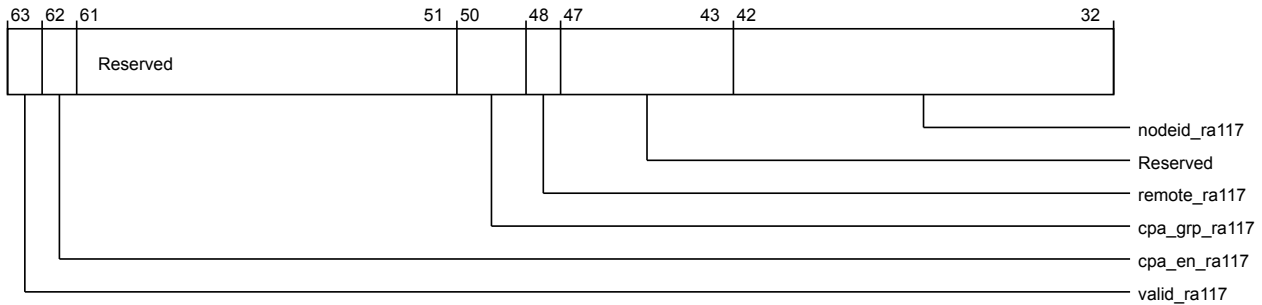


Figure 4-552 por_hnf_por_hnf_rn_phys_id58 (high)

The following table shows the por_hnf_rn_phys_id58 higher register bit assignments.

Table 4-569 por_hnf_por_hnf_rn_phys_id58 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra117	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra117	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra117	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra117	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra117	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

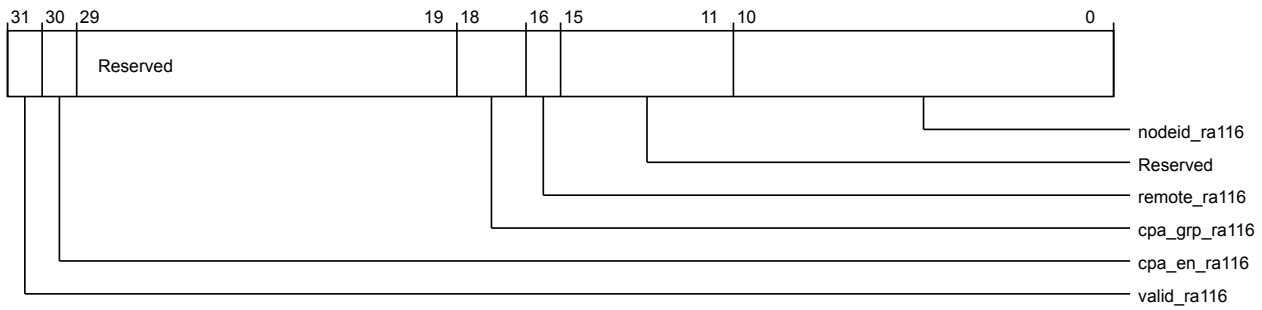


Figure 4-553 por_hnf_por_hnf_rn_phys_id58 (low)

The following table shows the por_hnf_rn_phys_id58 lower register bit assignments.

Table 4-570 por_hnf_por_hnf_rn_phys_id58 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra116	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra116	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra116	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra116	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra116	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id59

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF70
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

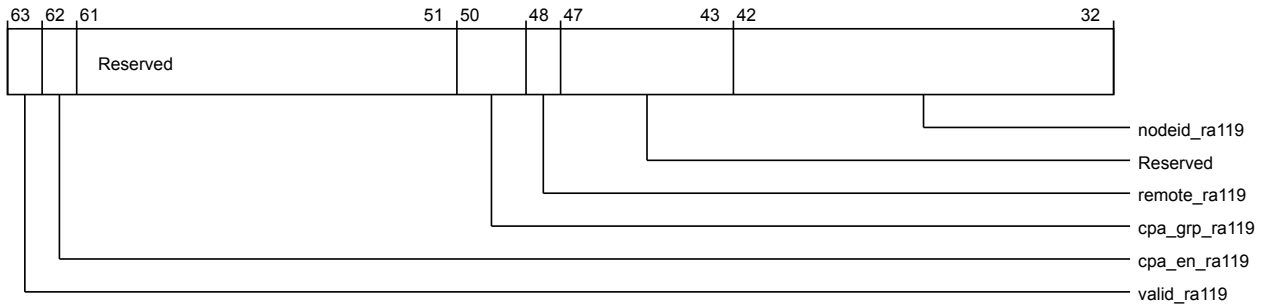


Figure 4-554 por_hnf_por_hnf_rn_phys_id59 (high)

The following table shows the por_hnf_rn_phys_id59 higher register bit assignments.

Table 4-571 por_hnf_por_hnf_rn_phys_id59 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra119	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra119	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra119	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra119	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra119	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

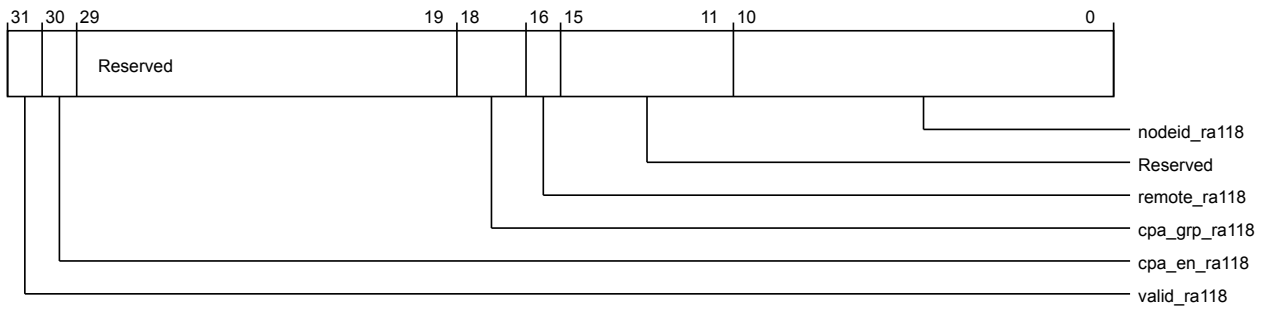


Figure 4-555 `por_hnf_por_hnf_rn_phys_id59 (low)`

The following table shows the `por_hnf_rn_phys_id59` lower register bit assignments.

Table 4-572 `por_hnf_por_hnf_rn_phys_id59 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra118</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra118</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra118</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra118</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra118</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id60`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF78
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

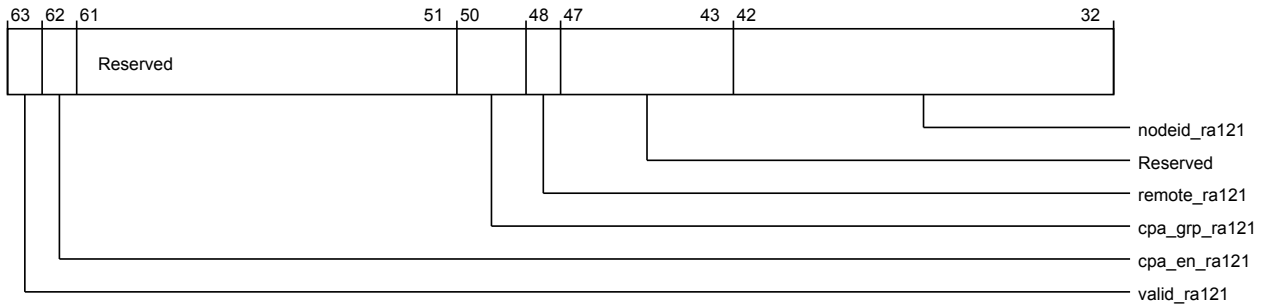


Figure 4-556 por_hnf_por_hnf_rn_phys_id60 (high)

The following table shows the por_hnf_rn_phys_id60 higher register bit assignments.

Table 4-573 por_hnf_por_hnf_rn_phys_id60 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra121	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra121	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra121	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra121	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra121	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

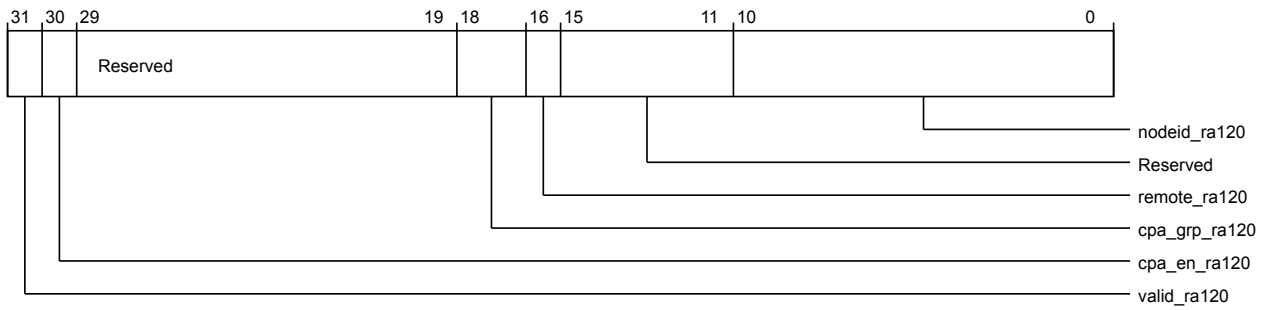


Figure 4-557 `por_hnf_por_hnf_rn_phys_id60 (low)`

The following table shows the `por_hnf_rn_phys_id60` lower register bit assignments.

Table 4-574 `por_hnf_por_hnf_rn_phys_id60 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra120</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra120</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra120</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra120</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra120</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id61`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF80
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

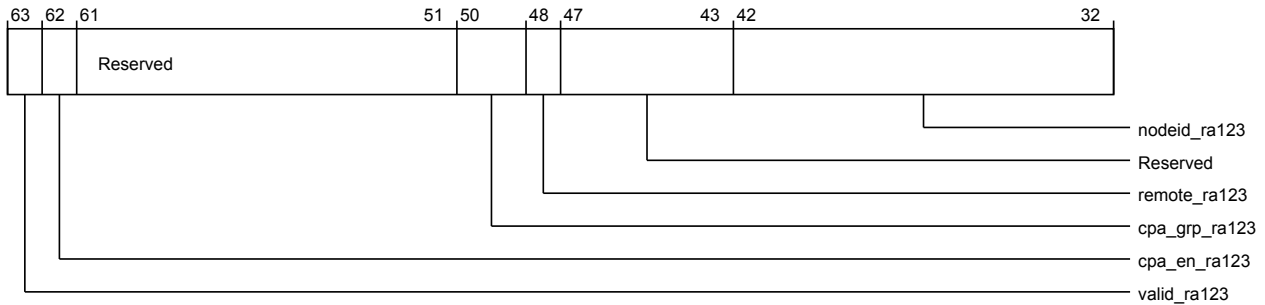


Figure 4-558 por_hnf_por_hnf_rn_phys_id61 (high)

The following table shows the por_hnf_rn_phys_id61 higher register bit assignments.

Table 4-575 por_hnf_por_hnf_rn_phys_id61 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra123	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra123	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra123	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra123	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra123	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

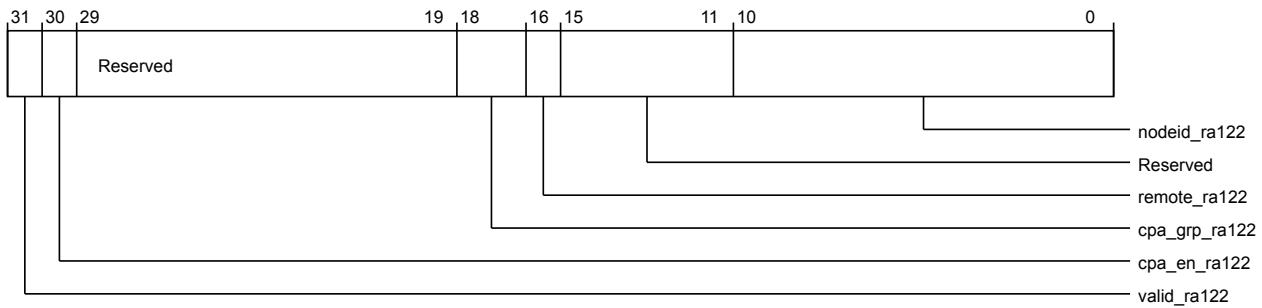


Figure 4-559 por_hnf_por_hnf_rn_phys_id61 (low)

The following table shows the por_hnf_rn_phys_id61 lower register bit assignments.

Table 4-576 por_hnf_por_hnf_rn_phys_id61 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra122	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra122	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra122	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra122	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra122	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id62

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF88
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

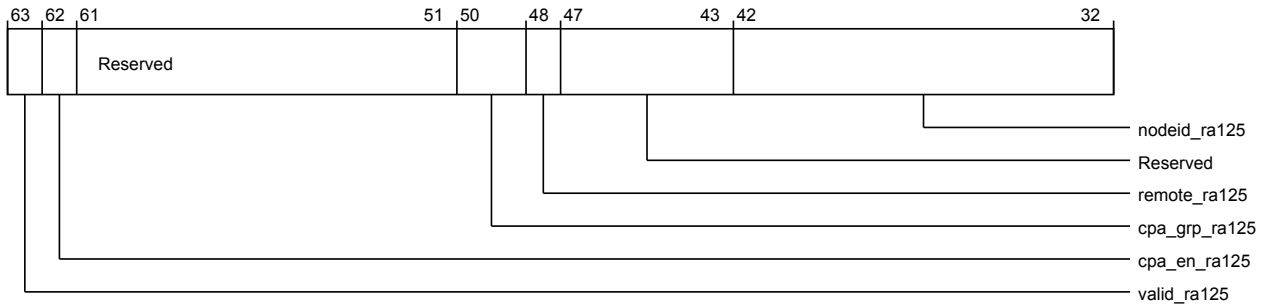


Figure 4-560 por_hnf_por_hnf_rn_phys_id62 (high)

The following table shows the por_hnf_rn_phys_id62 higher register bit assignments.

Table 4-577 por_hnf_por_hnf_rn_phys_id62 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra125	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra125	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra125	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra125	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra125	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

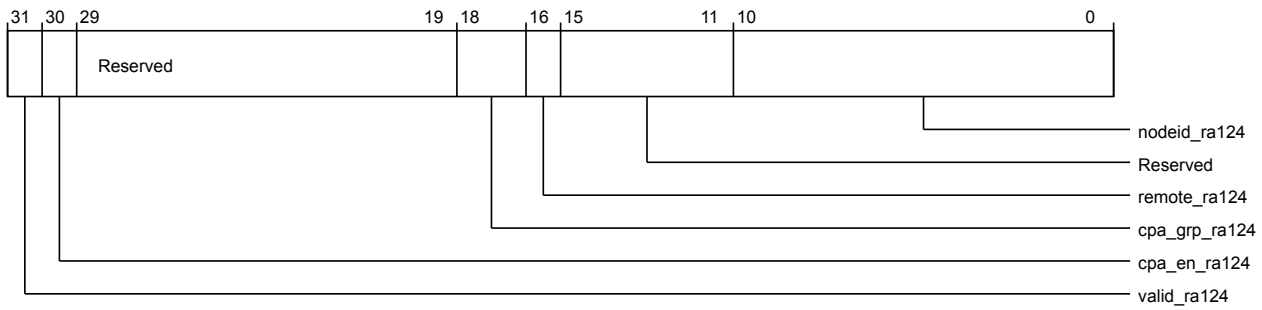


Figure 4-561 `por_hnf_por_hnf_rn_phys_id62 (low)`

The following table shows the `por_hnf_rn_phys_id62` lower register bit assignments.

Table 4-578 `por_hnf_por_hnf_rn_phys_id62 (low)`

Bits	Field name	Description	Type	Reset
31	<code>valid_ra124</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	<code>cpa_en_ra124</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	<code>cpa_grp_ra124</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	<code>remote_ra124</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	<code>nodeid_ra124</code>	Specifies the node ID	RW	11'h0

`por_hnf_rn_phys_id63`

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF90
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

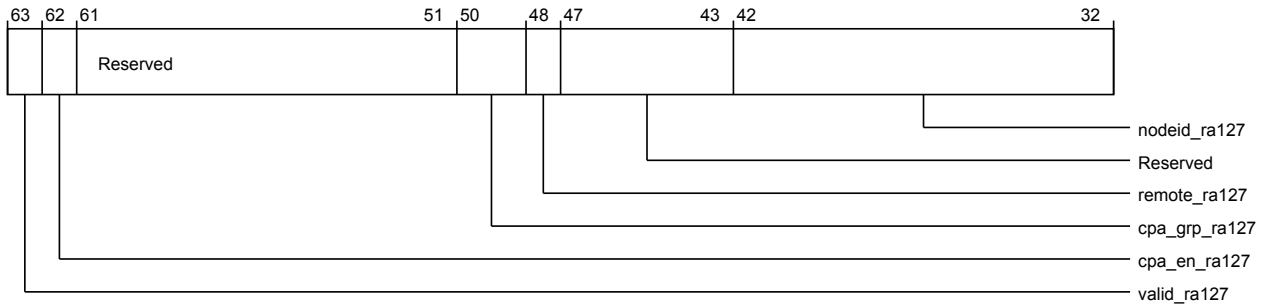


Figure 4-562 `por_hnf_por_hnf_rn_phys_id63` (high)

The following table shows the `por_hnf_rn_phys_id63` higher register bit assignments.

Table 4-579 `por_hnf_por_hnf_rn_phys_id63` (high)

Bits	Field name	Description	Type	Reset
63	<code>valid_ra127</code>	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	<code>cpa_en_ra127</code>	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	<code>cpa_grp_ra127</code>	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	<code>remote_ra127</code>	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>nodeid_ra127</code>	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

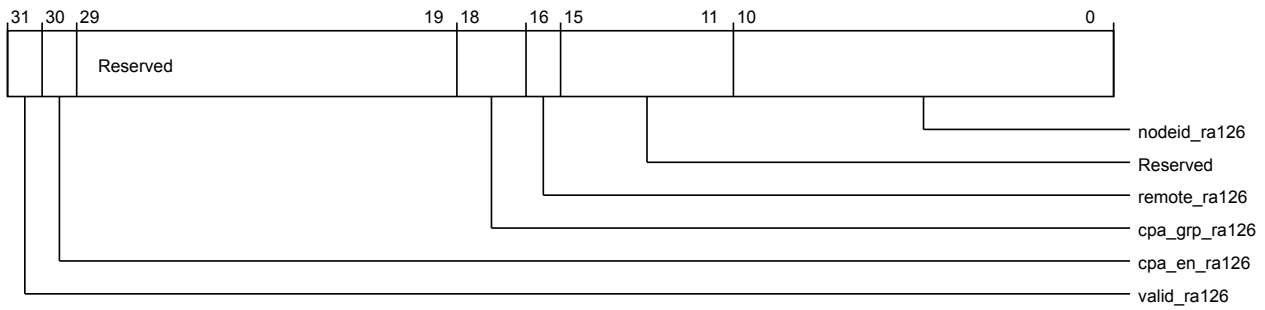


Figure 4-563 por_hnf_por_hnf_rn_phys_id63 (low)

The following table shows the por_hnf_rn_phys_id63 lower register bit assignments.

Table 4-580 por_hnf_por_hnf_rn_phys_id63 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra126	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra126	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra126	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra126	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra126	Specifies the node ID	RW	11'h0

por_hnf_ldid_map_table_reg0

Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF98
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

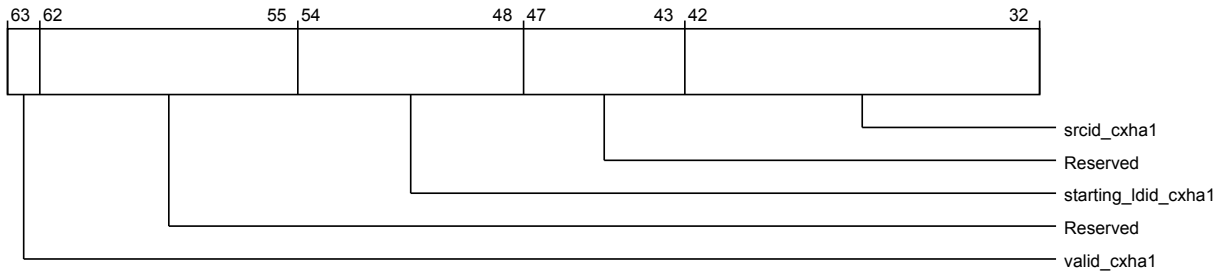


Figure 4-564 por_hnf_por_hnf_ldid_map_table_reg0 (high)

The following table shows the por_hnf_ldid_map_table_reg0 higher register bit assignments.

Table 4-581 por_hnf_por_hnf_ldid_map_table_reg0 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha1	Specifies CXHA 1 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha1	Specifies the starting LDID for RN-F's behind CXHA 1	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha1	Specifies the node ID for CXHA 1	RW	11'h0

The following image shows the lower register bit assignments.

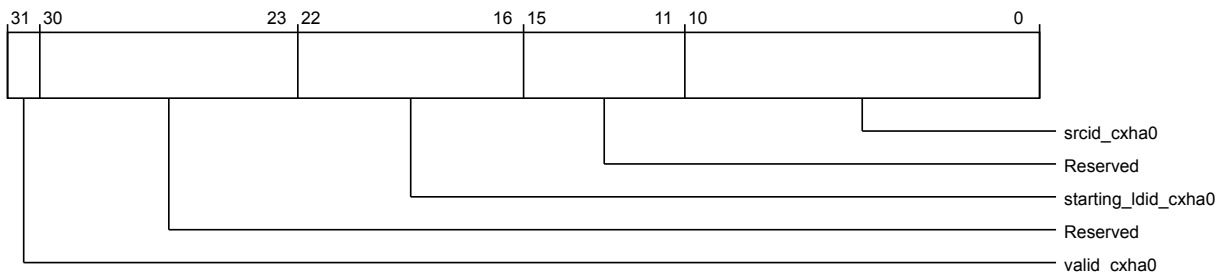


Figure 4-565 por_hnf_por_hnf_ldid_map_table_reg0 (low)

The following table shows the por_hnf_ldid_map_table_reg0 lower register bit assignments.

Table 4-582 por_hnf_por_hnf_ldid_map_table_reg0 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha0	Specifies CXHA 0 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha0	Specifies the starting LDID for RN-F's behind CXHA 0	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha0	Specifies the node ID for CXHA 0	RW	11'h0

por_hnf_ldid_map_table_reg1

Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hFA0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

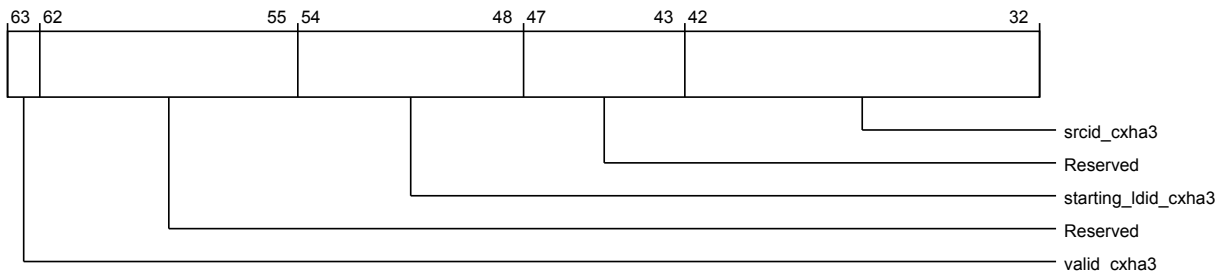


Figure 4-566 por_hnf_por_hnf_ldid_map_table_reg1 (high)

The following table shows the por_hnf_ldid_map_table_reg1 higher register bit assignments.

Table 4-583 por_hnf_por_hnf_ldid_map_table_reg1 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha3	Specifies CXHA 3 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha3	Specifies the starting LDID for RN-F's behind CXHA 3	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha3	Specifies the node ID for CXHA 3	RW	11'h0

The following image shows the lower register bit assignments.

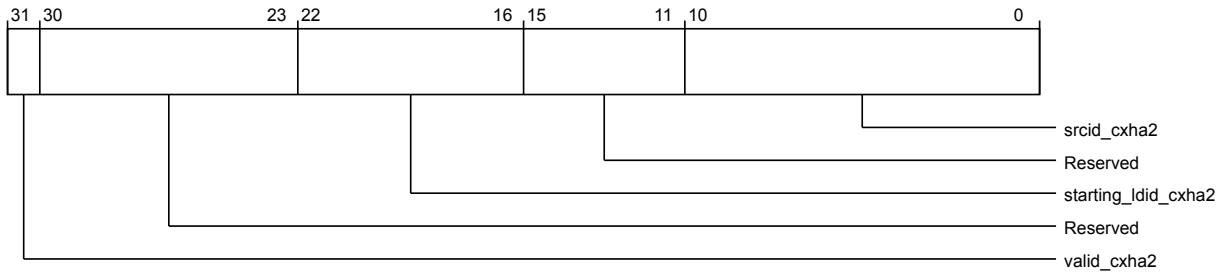


Figure 4-567 por_hnf_por_hnf_ldid_map_table_reg1 (low)

The following table shows the por_hnf_ldid_map_table_reg1 lower register bit assignments.

Table 4-584 por_hnf_por_hnf_ldid_map_table_reg1 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha2	Specifies CXHA 2 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha2	Specifies the starting LDID for RN-F's behind CXHA 2	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha2	Specifies the node ID for CXHA 2	RW	11'h0

por_hnf_ldid_map_table_reg2

Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hFA8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

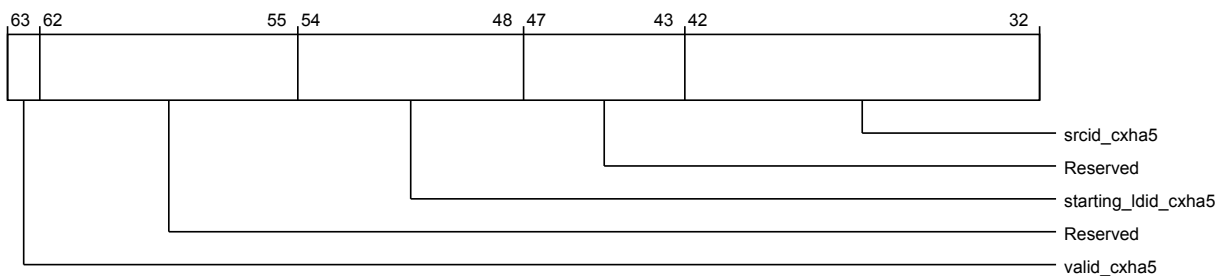


Figure 4-568 por_hnf_por_hnf_ldid_map_table_reg2 (high)

The following table shows the por_hnf_ldid_map_table_reg2 higher register bit assignments.

Table 4-585 por_hnf_por_hnf_ldid_map_table_reg2 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha5	Specifies CXHA 5 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha5	Specifies the starting LDID for RN-F's behind CXHA 5	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha5	Specifies the node ID for CXHA 5	RW	11'h0

The following image shows the lower register bit assignments.

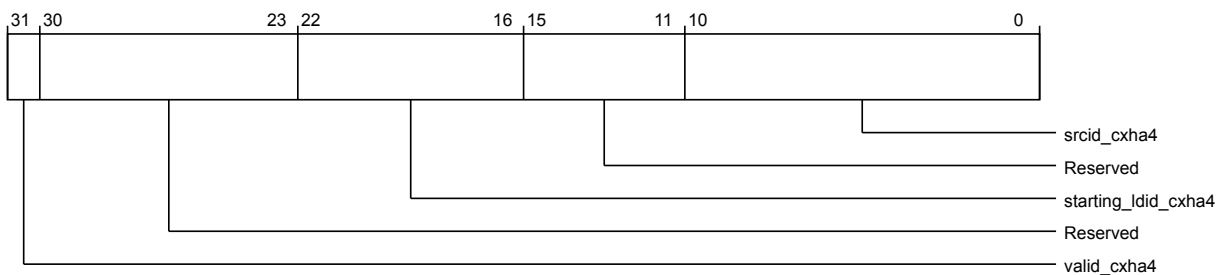


Figure 4-569 por_hnf_por_hnf_ldid_map_table_reg2 (low)

The following table shows the por_hnf_ldid_map_table_reg2 lower register bit assignments.

Table 4-586 por_hnf_por_hnf_ldid_map_table_reg2 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha4	Specifies CXHA 4 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha4	Specifies the starting LDID for RN-F's behind CXHA 4	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha4	Specifies the node ID for CXHA 4	RW	11'h0

por_hnf_ldid_map_table_reg3

Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hFB0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

Secure group override `por_hnf_secure_register_groups_override.sam_control`

The following image shows the higher register bit assignments.

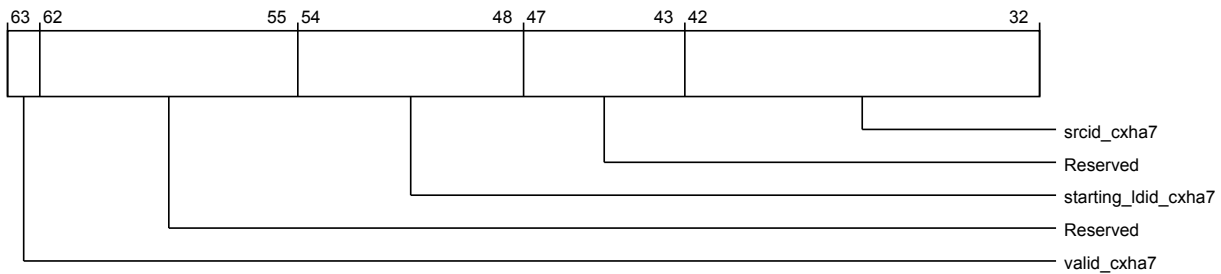


Figure 4-570 `por_hnf_por_hnf_ldid_map_table_reg3` (high)

The following table shows the `por_hnf_ldid_map_table_reg3` higher register bit assignments.

Table 4-587 `por_hnf_por_hnf_ldid_map_table_reg3` (high)

Bits	Field name	Description	Type	Reset
63	<code>valid_cxha7</code>	Specifies CXHA 7 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	<code>starting_ldid_cxha7</code>	Specifies the starting LDID for RN-F's behind CXHA 7	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	<code>srcid_cxha7</code>	Specifies the node ID for CXHA 7	RW	11'h0

The following image shows the lower register bit assignments.

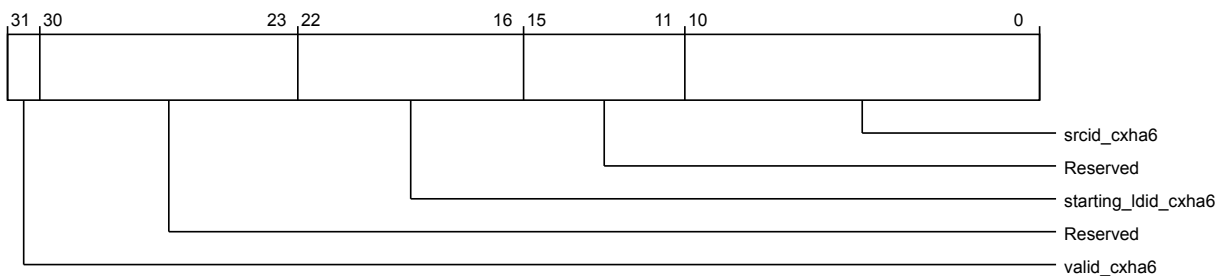


Figure 4-571 `por_hnf_por_hnf_ldid_map_table_reg3` (low)

The following table shows the `por_hnf_ldid_map_table_reg3` lower register bit assignments.

Table 4-588 `por_hnf_por_hnf_ldid_map_table_reg3` (low)

Bits	Field name	Description	Type	Reset
31	<code>valid_cxha6</code>	Specifies CXHA 6 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	<code>starting_ldid_cxha6</code>	Specifies the starting LDID for RN-F's behind CXHA 6	RW	7'h0

Table 4-588 por_hnf_por_hnf_ldid_map_table_reg3 (low) (continued)

Bits	Field name	Description	Type	Reset
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha6	Specifies the node ID for CXHA 6	RW	11'h0

por_hnf_cfg_slcsf_dbgrd

Controls access modes for SLC tasg, SLC data, and SF tag debug read.

Its characteristics are:

Type	WO
Register width (Bits)	64
Address offset	14'hB80
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.



Figure 4-572 por_hnf_por_hnf_cfg_slcsf_dbgrd (high)

The following table shows the por_hnf_cfg_slcsf_dbgrd higher register bit assignments.

Table 4-589 por_hnf_por_hnf_cfg_slcsf_dbgrd (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

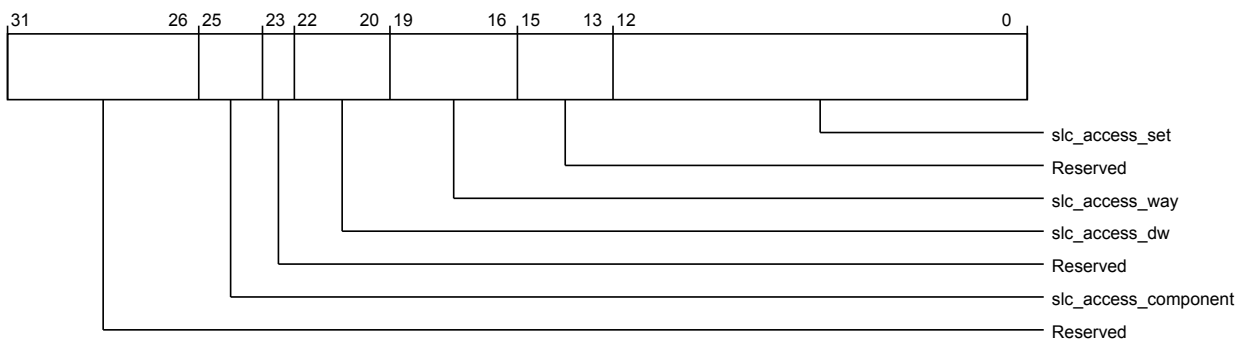


Figure 4-573 por_hnf_por_hnf_cfg_slcsf_dbgrd (low)

The following table shows the por_hnf_cfg_slcsf_dbgrd lower register bit assignments.

Table 4-590 por_hnf_por_hnf_cfg_slcsf_dbgdr (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	slc_access_component	Specifies SLC/SF array debug read 2'b01: SLC data read 2'b10: SLC tag read 2'b11: SF tag read	WO	2'b00
23	Reserved	Reserved	RO	-
22:20	slc_access_dw	64-bit chunk address for SLC data debug read access	WO	3'h0
19:16	slc_access_way	Way address for SLC/SF debug read access	WO	4'h0
15:13	Reserved	Reserved	RO	-
12:0	slc_access_set	Set address for SLC/SF debug read access	WO	13'h0

por_hnf_slc_cache_access_slc_tag

Contains SLC tag debug read data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'hB88
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slcsf_dbgdr

The following image shows the higher register bit assignments.

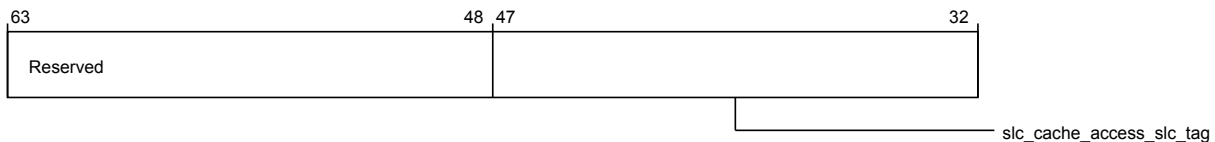


Figure 4-574 por_hnf_por_hnf_slc_cache_access_slc_tag (high)

The following table shows the `por_hnf_slc_cache_access_slc_tag` higher register bit assignments.

Table 4-591 por_hnf_por_hnf_slc_cache_access_slc_tag (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	slc_cache_access_slc_tag	SLC tag debug read data	RO	48'h0

The following image shows the lower register bit assignments.



Figure 4-575 por_hnf_por_hnf_slc_cache_access_slc_tag (low)

The following table shows the por_hnf_slc_cache_access_slc_tag lower register bit assignments.

Table 4-592 por_hnf_por_hnf_slc_cache_access_slc_tag (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_slc_tag	SLC tag debug read data	RO	48'h0

por_hnf_slc_cache_access_slc_data

Contains SLC data RAM debug read data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'hB90
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.

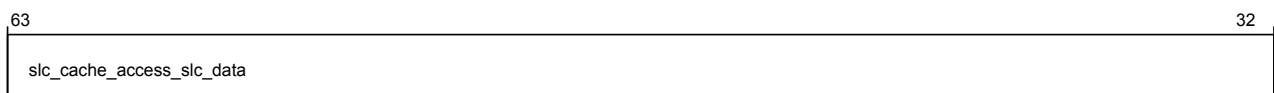


Figure 4-576 por_hnf_por_hnf_slc_cache_access_slc_data (high)

The following table shows the por_hnf_slc_cache_access_slc_data higher register bit assignments.

Table 4-593 por_hnf_por_hnf_slc_cache_access_slc_data (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_slc_data	SLC data RAM debug read data	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-577 por_hnf_por_hnf_slc_cache_access_slc_data (low)

The following table shows the por_hnf_slc_cache_access_slc_data lower register bit assignments.

Table 4-594 por_hnf_por_hnf_slc_cache_access_slc_data (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_slc_data	SLC data RAM debug read data	RO	64'h0

por_hnf_slc_cache_access_sf_tag

Contains SF tag debug read data. Bits[63:0]

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'hB98
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.

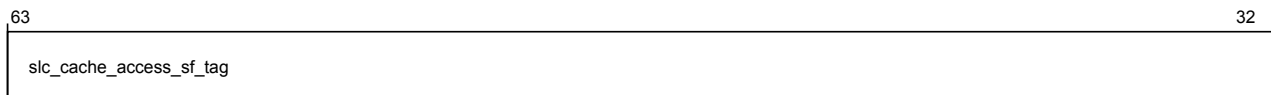


Figure 4-578 por_hnf_por_hnf_slc_cache_access_sf_tag (high)

The following table shows the por_hnf_slc_cache_access_sf_tag higher register bit assignments.

Table 4-595 por_hnf_por_hnf_slc_cache_access_sf_tag (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_sf_tag	SF tag debug read data	RO	64'h0

The following image shows the lower register bit assignments.

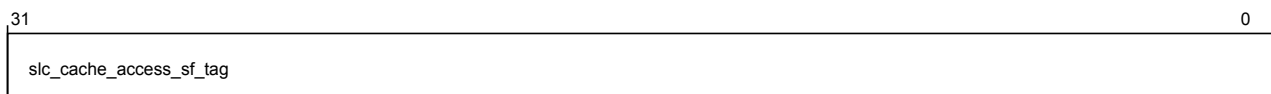


Figure 4-579 por_hnf_por_hnf_slc_cache_access_sf_tag (low)

The following table shows the por_hnf_slc_cache_access_sf_tag lower register bit assignments.

Table 4-596 por_hnf_por_hnf_slc_cache_access_sf_tag (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_sf_tag	SF tag debug read data	RO	64'h0

por_hnf_slc_cache_access_sf_tag1

Contains SF tag debug read data bits [127:64], when present in SF Tag

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'hBA0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.

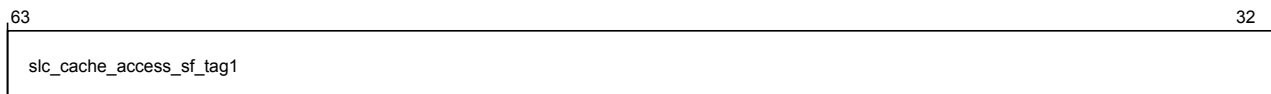


Figure 4-580 por_hnf_por_hnf_slc_cache_access_sf_tag1 (high)

The following table shows the por_hnf_slc_cache_access_sf_tag1 higher register bit assignments.

Table 4-597 por_hnf_por_hnf_slc_cache_access_sf_tag1 (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_sf_tag1	SF tag debug read data	RO	64'h0

The following image shows the lower register bit assignments.

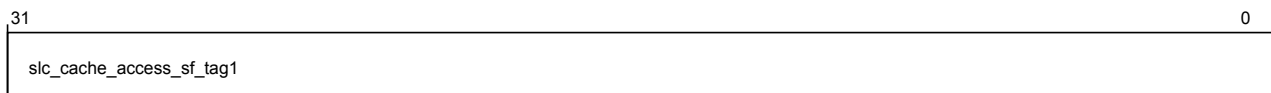


Figure 4-581 por_hnf_por_hnf_slc_cache_access_sf_tag1 (low)

The following table shows the por_hnf_slc_cache_access_sf_tag1 lower register bit assignments.

Table 4-598 por_hnf_por_hnf_slc_cache_access_sf_tag1 (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_sf_tag1	SF tag debug read data	RO	64'h0

por_hnf_slc_cache_access_sf_tag2

Contains SF tag debug read data bits [128:191], when present in SF Tag

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'hBA8

Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.

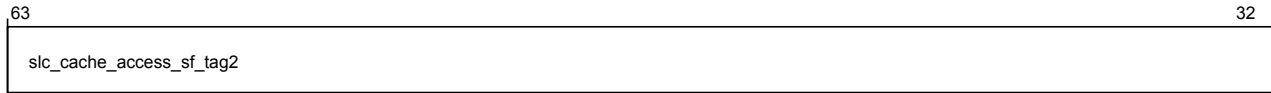


Figure 4-582 por_hnf_por_hnf_slc_cache_access_sf_tag2 (high)

The following table shows the por_hnf_slc_cache_access_sf_tag2 higher register bit assignments.

Table 4-599 por_hnf_por_hnf_slc_cache_access_sf_tag2 (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_sf_tag2	SF tag debug read data	RO	64'h0

The following image shows the lower register bit assignments.

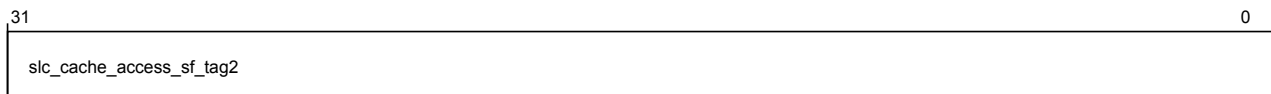


Figure 4-583 por_hnf_por_hnf_slc_cache_access_sf_tag2 (low)

The following table shows the por_hnf_slc_cache_access_sf_tag2 lower register bit assignments.

Table 4-600 por_hnf_por_hnf_slc_cache_access_sf_tag2 (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_sf_tag2	SF tag debug read data	RO	64'h0

por_hnf_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2000
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

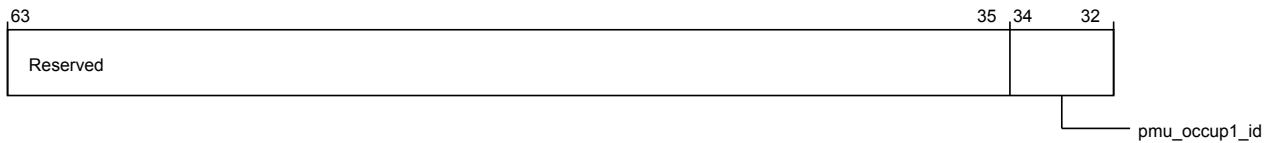


Figure 4-584 `por_hnf_por_hnf_pmu_event_sel` (high)

The following table shows the `por_hnf_pmu_event_sel` higher register bit assignments.

Table 4-601 `por_hnf_por_hnf_pmu_event_sel` (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	<code>pmu_occup1_id</code>	HN-F PMU occupancy 1 select 3'b000: All occupancy selected 3'b001: Read requests 3'b010: Write requests 3'b011: Atomic operation requests 3'b100: Stash requests	RW	3'h0

The following image shows the lower register bit assignments.

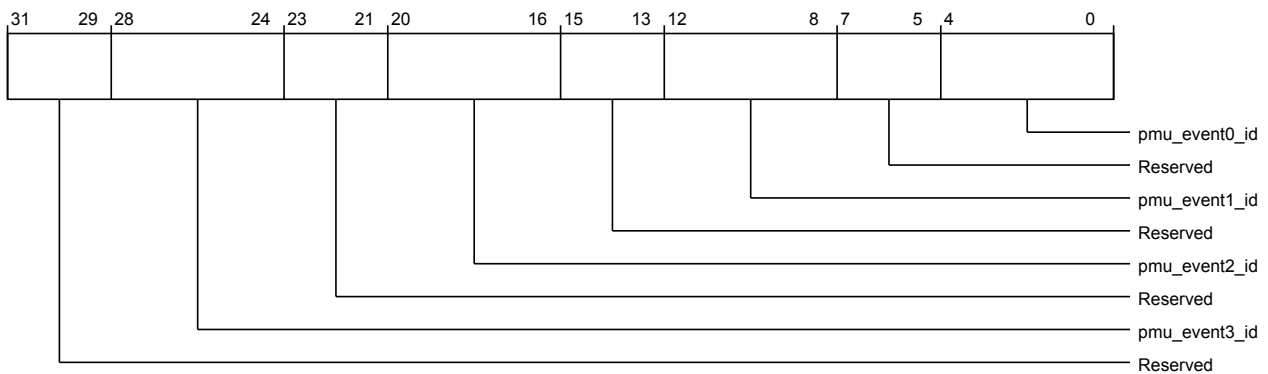


Figure 4-585 `por_hnf_por_hnf_pmu_event_sel` (low)

The following table shows the `por_hnf_pmu_event_sel` lower register bit assignments.

Table 4-602 `por_hnf_por_hnf_pmu_event_sel` (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	<code>pmu_event3_id</code>	HN-F PMU Event 3 select; see <code>pmu_event0_id</code> for encodings	RW	5'h00
23:21	Reserved	Reserved	RO	-
20:16	<code>pmu_event2_id</code>	HN-F PMU Event 2 select; see <code>pmu_event0_id</code> for encodings	RW	5'h00
15:13	Reserved	Reserved	RO	-

Table 4-602 por_hnf_por_hnf_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
12:8	pmu_event1_id	HN-F PMU Event 1 select; see pmu_event0_id for encodings	RW	5'h00
7:5	Reserved	Reserved	RO	-

Table 4-602 `por_hnf_por_hnf_pmu_event_sel` (low) (continued)

Bits	Field name	Description	Type	Reset
4:0	<code>pmu_event0_id</code>	<p>HN-F PMU Event 0 select</p> <p>5'h00: No event</p> <p>5'h01: <code>PMU_HN_CACHE_MISS_EVENT</code>; counts total cache misses in first lookup result (high priority)</p> <p>5'h02: <code>PMU_HN_SLCSF_CACHE_ACCESS_EVENT</code>; counts number of cache accesses in first access (high priority)</p> <p>5'h03: <code>PMU_HN_CACHE_FILL_EVENT</code>; counts total allocations in HN SLC (all cache line allocations to SLC)</p> <p>5'h04: <code>PMU_HN_POCQ_RETRY_EVENT</code>; counts number of retried requests</p> <p>5'h05: <code>PMU_HN_POCQ_REQS_RECVD_EVENT</code>; counts number of requests received by HN</p> <p>5'h06: <code>PMU_HN_SF_HIT_EVENT</code>; counts number of SF hits</p> <p>5'h07: <code>PMU_HN_SF_EVICTIONS_EVENT</code>; counts number of SF eviction cache invalidations initiated</p> <p>5'h08: <code>PMU_HN_DIR_SNOOPS_SENT_EVENT</code>; counts number of directed snoops sent (not including SF back invalidation)</p> <p>5'h09: <code>PMU_HN_BRD_SNOOPS_SENTEVENT</code>; counts number of multicast snoops sent (not including SF back invalidation)</p> <p>5'h0A: <code>PMU_HN_SLC_EVICTION_EVENT</code>; counts number of SLC evictions (dirty only)</p> <p>5'h0B: <code>PMU_HN_SLC_FILL_INVALID_WAY_EVENT</code>; counts number of SLC fills to an invalid way</p> <p>5'h0C: <code>PMU_HN_MC_RETRIES_EVENT</code>; counts number of retried transactions by the MC</p> <p>5'h0D: <code>PMU_HN_MC_REQS_EVENT</code>; counts number of requests sent to MC</p> <p>5'h0E: <code>PMU_HN_QOS_HH_RETRY_EVENT</code>; counts number of times a HighHigh priority request is protocol retried at the HN-F</p> <p>5'h0F: <code>PMU_HN_POCQ_OCCUPANCY_EVENT</code>; counts the POCQ occupancy in HN-F; occupancy filtering is programmed in <code>pmu_occup1_id</code></p> <p>5'h10: <code>PMU_HN_POCQ_ADDRHAZ_EVENT</code>; counts number of POCQ address hazards upon allocation</p> <p>5'h11: <code>PMU_HN_POCQ_ATOMICS_ADDRHAZ_EVENT</code>; counts number of POCQ address hazards upon allocation for atomic operations</p> <p>5'h12: <code>PMU_HN_LD_ST_SWP_ADQ_FULL_EVENT</code>; counts number of times ADQ is full for Ld/St/SWP type atomic operations while POCQ has pending operations</p> <p>5'h13: <code>PMU_HN_CMP_ADQ_FULL_EVENT</code>; counts number of times ADQ is full for CMP type atomic operations while POCQ has pending operations</p> <p>5'h14: <code>PMU_HN_TXDAT_STALL_EVENT</code>; counts number of times HN-F has a pending TXDAT flit but no credits to upload</p> <p>5'h15: <code>PMU_HN_TXRSP_STALL_EVENT</code>; counts number of times HN-F has a pending TXRSP flit but no credits to upload</p>	RW	5'h00

Table 4-602 por_hnf_por_hnf_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
4:0	pmu_event0_id	<p>5'h16: PMU_HN_SEQ_FULL_EVENT; counts number of times requests are replayed in SLC pipe due to SEQ being full</p> <p>5'h17: PMU_HN_SEQ_HIT_EVENT; counts number of times a request in SLC hit a pending SF eviction in SEQ</p> <p>5'h18: PMU_HN_SNP_SENT_EVENT; counts number of snoops sent including directed/multicast/SF back invalidation</p> <p>5'h19: PMU_HN_SFBI_DIR_SNP_SENT_EVENT; counts number of times directed snoops were sent due to SF back invalidation</p> <p>5'h1a: PMU_HN_SFBI_BRD_SNP_SENT_EVENT; counts number of times multicast snoops were sent due to SF back invalidation</p> <p>5'h1b: PMU_HN_SNP_SENT_UNTRK_EVENT; counts number of times snooped were sent due to untracked RN-Fs</p> <p>5'h1c: PMU_HN_INTV_DIRTY_EVENT; counts number of times SF back invalidation resulted in dirty line intervention from the RN</p> <p>5'h1d: PMU_HN_STASH_SNP_SENT_EVENT; counts number of times stash snoops sent</p> <p>5'h1e: PMU_HN_STASH_DATA_PULL_EVENT; counts number of times stash snoops resulted in data pull from the RN</p> <p>5'h1f: PMU_HN_SNP_FWDED_EVENT; counts number of times data forward snoops sent</p>	RW	5'h00

4.3.5 HN-I register descriptions

This section lists the HN-I registers.

por_hni_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

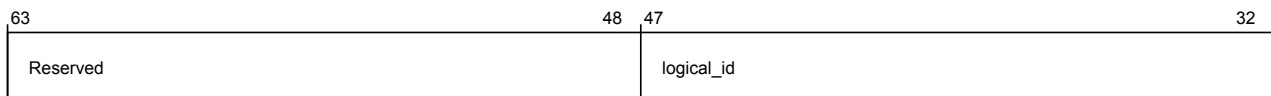


Figure 4-586 por_hni_node_info (high)

The following table shows the por_hni_node_info higher register bit assignments.

Table 4-603 por_hni_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

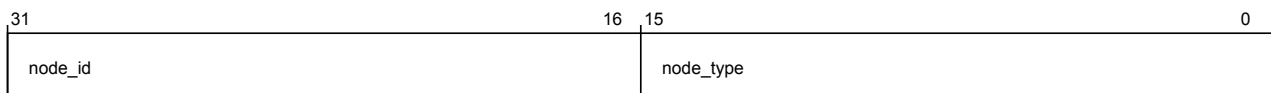


Figure 4-587 por_hni_node_info (low)

The following table shows the por_hni_node_info lower register bit assignments.

Table 4-604 por_hni_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0004

por_hni_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-588 por_hni_por_hni_child_info (high)

The following table shows the por_hni_child_info higher register bit assignments.

Table 4-605 por_hni_por_hni_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

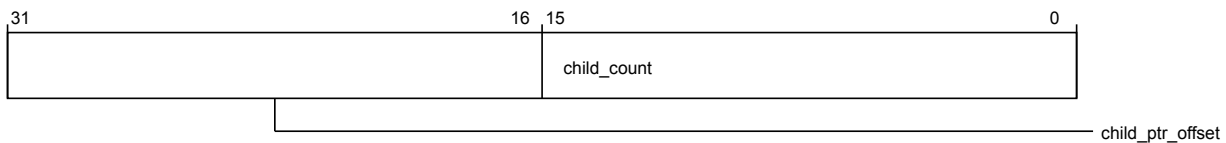


Figure 4-589 por_hni_por_hni_child_info (low)

The following table shows the por_hni_child_info lower register bit assignments.

Table 4-606 por_hni_por_hni_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_hni_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type	RW
Register width (Bits)	64

Address offset	14'h980
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

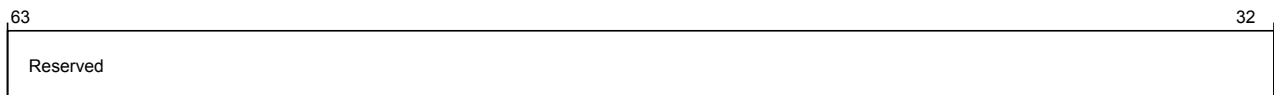


Figure 4-590 por_hni_por_hni_secure_register_groups_override (high)

The following table shows the por_hni_secure_register_groups_override higher register bit assignments.

Table 4-607 por_hni_por_hni_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

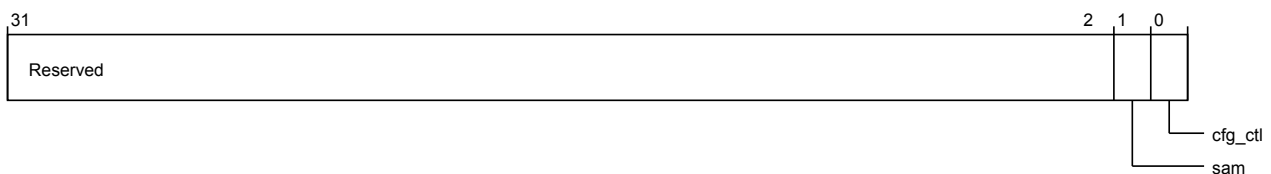


Figure 4-591 por_hni_por_hni_secure_register_groups_override (low)

The following table shows the por_hni_secure_register_groups_override lower register bit assignments.

Table 4-608 por_hni_por_hni_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	sam	Allows non-secure access to secure SAM registers	RW	1'b0
0	cfg_ctl	Allows non-secure access to secure configuration control register	RW	1'b0

por_hni_unit_info

Provides component identification information for HN-I.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h900
Register reset	Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-592 por_hni_por_hni_unit_info (high)

The following table shows the por_hni_unit_info higher register bit assignments.

Table 4-609 por_hni_por_hni_unit_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

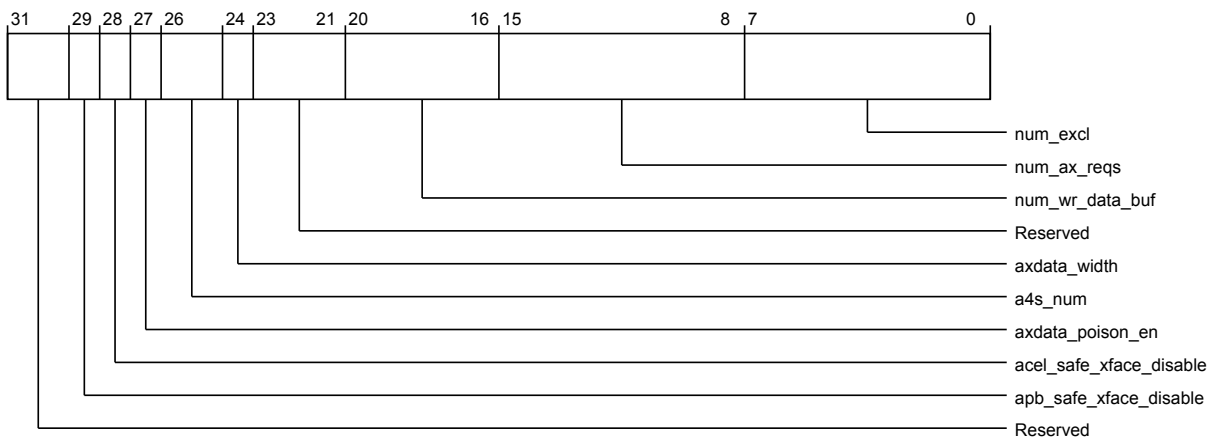


Figure 4-593 por_hni_por_hni_unit_info (low)

The following table shows the por_hni_unit_info lower register bit assignments.

Table 4-610 por_hni_por_hni_unit_info (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29	apb_safe_xface_disable	APB safe interface disable 1'b0: Not disabled 1'b1: Disabled	RO	Configuration dependent
28	acel_safe_xface_disable	ACE-Lite/AXI4 safe interface disable 1'b0: Not disabled 1'b1: Disabled	RO	Configuration dependent

Table 4-610 por_hni_por_hni_unit_info (low) (continued)

Bits	Field name	Description	Type	Reset
27	axdata_poison_en	Data poison support on ACE-Lite/AXI4 interface 1'b0: Not supported 1'b1: Supported	RO	Configuration dependent
26:25	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent
24	axdata_width	Data width on ACE-Lite/AXI4 interface 1'b0: 128 bits 1'b1: 256 bits	RO	Configuration dependent
23:21	Reserved	Reserved	RO	-
20:16	num_wr_data_buf	Number of write data buffers in HN-I	RO	Configuration dependent
15:8	num_ax_reqs	Maximum number of outstanding ACE-Lite/AXI4 requests	RO	Configuration dependent
7:0	num_excl	Number of exclusive monitors in HN-I	RO	Configuration dependent

por_hni_sam_addrregion0_cfg

Configures Address Region 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC00

Register reset 64'b1100011111

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hni_secure_register_groups_override.sam

The following image shows the higher register bit assignments.

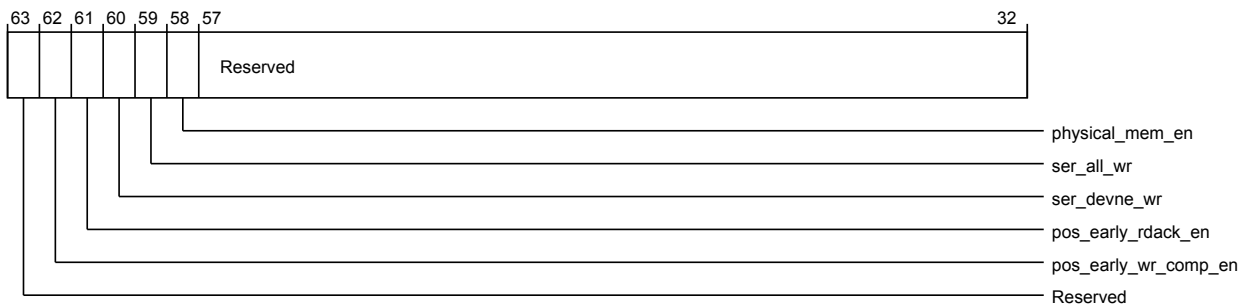


Figure 4-594 por_hni_por_hni_sam_addrregion0_cfg (high)

The following table shows the por_hni_sam_addrregion0_cfg higher register bit assignments.

Table 4-611 `por_hni_por_hni_sam_addrregion0_cfg` (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 0; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 0; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 0	RW	1'b0
59	ser_all_wr	Used to serialize all writes within Address Region 0	RW	1'b0
58	physical_mem_en	Address Region 0 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

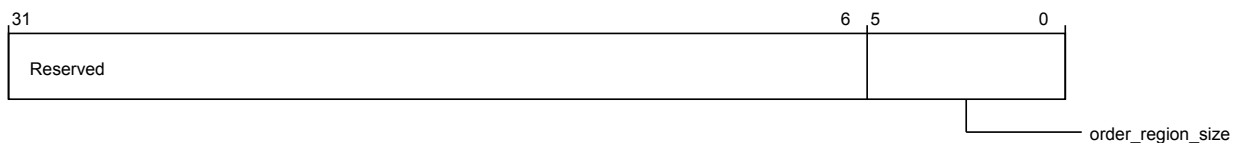


Figure 4-595 `por_hni_por_hni_sam_addrregion0_cfg` (low)

The following table shows the por_hni_sam_addrregion0_cfg lower register bit assignments.

Table 4-612 `por_hni_por_hni_sam_addrregion0_cfg` (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 0 size within Address Region 0 ($2^n \times 4\text{KB}$)	RW	6'b111111

por_hni_sam_addrregion1_cfg

Configures Address Region 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC08

[illegible]

Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
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Secure group override	por_hni_secure_register_groups_override.sam
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The following image shows the higher register bit assignments.

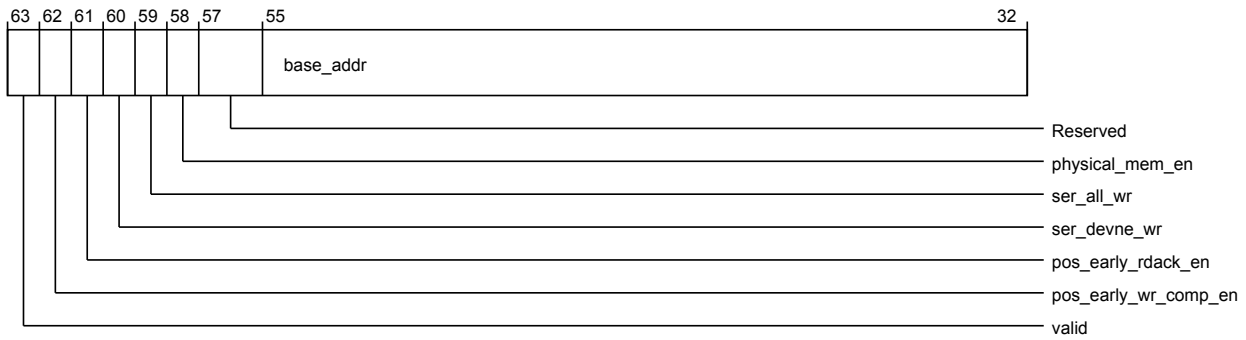


Figure 4-596 `por_hni_por_hni_sam_addrregion1_cfg` (high)

The following table shows the `por_hni_sam_addrregion1_cfg` higher register bit assignments.

Table 4-613 `por_hni_por_hni_sam_addrregion1_cfg` (high)

Bits	Field name	Description	Type	Reset
63	<code>valid</code>	Address Region 1 fields are programmed and valid	RW	1'h0
62	<code>pos_early_wr_comp_en</code>	Enables early write acknowledgment in Address Region 1; used to improve write performance	RW	1'b1
61	<code>pos_early_rdack_en</code>	Enables sending early read receipts from HN-I in Address Region 1; used to improve ordered read performance	RW	1'b1
60	<code>ser_devne_wr</code>	Used to serialize Device-nGnRnE writes within Address Region 1	RW	1'b0
59	<code>ser_all_wr</code>	Used to serialize all writes within Address Region 1	RW	1'b0
58	<code>physical_mem_en</code>	Address Region 1 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:56	Reserved	Reserved	RO	-
55:32	<code>base_addr</code>	Address Region 1 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 1 size.	RW	36'h0

The following image shows the lower register bit assignments.

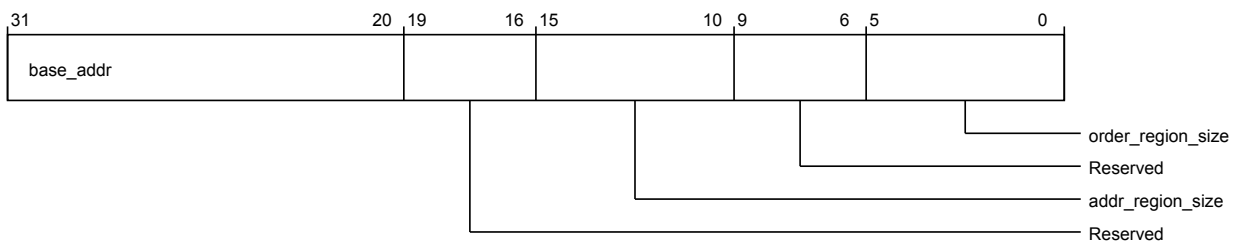


Figure 4-597 `por_hni_por_hni_sam_addrregion1_cfg` (low)

The following table shows the `por_hni_sam_addrregion1_cfg` lower register bit assignments.

Table 4-614 por_hni_por_hni_sam_addrregion1_cfg (low)

Bits	Field name	Description	Type	Reset
31:20	base_addr	Address Region 1 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 1 size.	RW	36'h0
19:16	Reserved	Reserved	RO	-
15:10	addr_region_size	<n>; used to calculate Address Region 1 size ($2^n \times 4\text{KB}$) CONSTRAINT: <n> must be configured so that the Address Region 1 size is less than or equal to $2^{\text{(address width)}}$.	RW	6'h0
9:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 1 size within Address Region 1 ($2^n \times 4\text{KB}$)	RW	6'h0

por_hni_sam_addrregion2_cfg

Configures Address Region 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC10

Register reset 64'b011000

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hni_secure_register_groups_override.sam

The following image shows the higher register bit assignments.

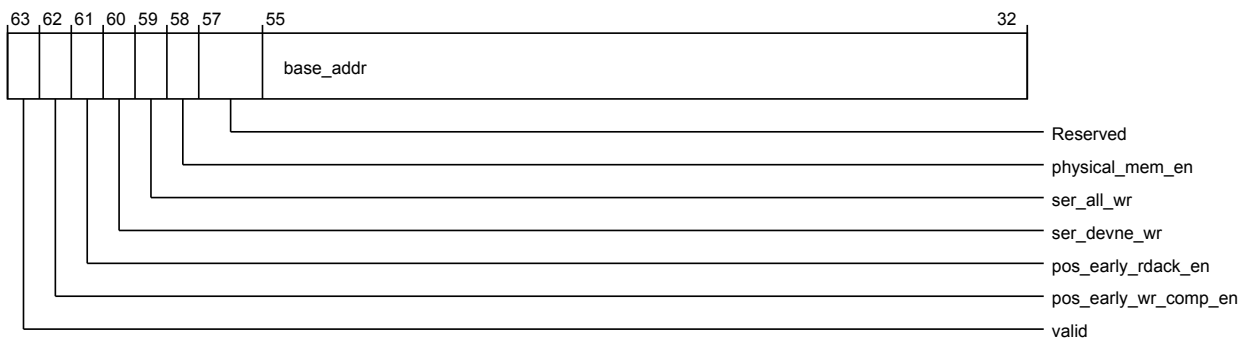


Figure 4-598 por_hni_por_hni_sam_addrregion2_cfg (high)

The following table shows the por_hni_sam_addrregion2_cfg higher register bit assignments.

Table 4-615 por_hni_por_hni_sam_addrregion2_cfg (high)

Bits	Field name	Description	Type	Reset
63	valid	Address Region 2 fields are programmed and valid	RW	1'h0
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 2; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 2; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 2	RW	1'b0
59	ser_all_wr	Used to serialize all writes within Address Region 2	RW	1'b0
58	physical_mem_en	Address Region 2 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:56	Reserved	Reserved	RO	-
55:32	base_addr	Address Region 2 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 2 size	RW	36'h0

The following image shows the lower register bit assignments.

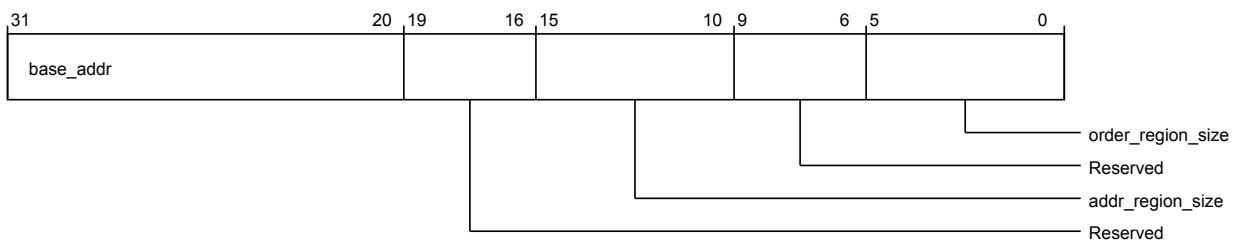


Figure 4-599 por_hni_por_hni_sam_addrregion2_cfg (low)

The following table shows the por_hni_sam_addrregion2_cfg lower register bit assignments.

Table 4-616 por_hni_por_hni_sam_addrregion2_cfg (low)

Bits	Field name	Description	Type	Reset
31:20	base_addr	Address Region 2 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 2 size	RW	36'h0
19:16	Reserved	Reserved	RO	-
15:10	addr_region_size	<n>; used to calculate Address Region 2 size ($2^n \times 4\text{KB}$) CONSTRAINT: <n> must be configured so that the Address Region 2 size is less than or equal to $2^{\text{address width}}$.	RW	6'h0
9:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 2 size within Address Region 2 ($2^n \times 4\text{KB}$)	RW	6'h0

por_hni_sam_addrregion3_cfg

Configures Address Region 3.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC18
Register reset	64'b011000
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_hni_secure_register_groups_override.sam

The following image shows the higher register bit assignments.

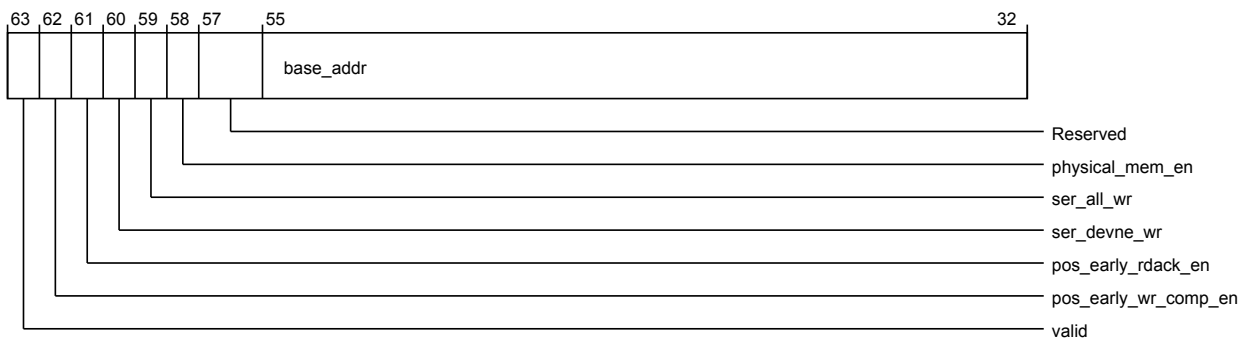


Figure 4-600 por_hni_por_hni_sam_addrregion3_cfg (high)

The following table shows the por_hni_sam_addrregion3_cfg higher register bit assignments.

Table 4-617 por_hni_por_hni_sam_addrregion3_cfg (high)

Bits	Field name	Description	Type	Reset
63	valid	Fields of Address Region 3 are programmed and valid	RW	1'h0
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 3; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 3; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 3	RW	1'b0
59	ser_all_wr	Used to serialize all writes within Address Region 3	RW	1'b0
58	physical_mem_en	Address Region 3 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:56	Reserved	Reserved	RO	-
55:32	base_addr	Address Region 3 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 3 size	RW	36'h0

The following image shows the lower register bit assignments.

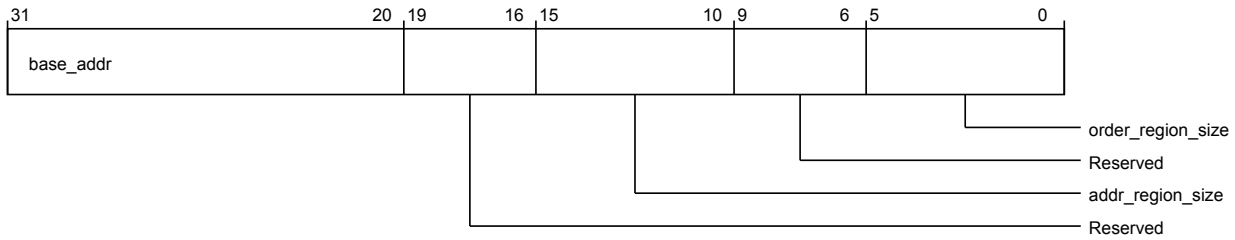


Figure 4-601 por_hni_por_hni_sam_addrregion3_cfg (low)

The following table shows the por_hni_sam_addrregion3_cfg lower register bit assignments.

Table 4-618 por_hni_por_hni_sam_addrregion3_cfg (low)

Bits	Field name	Description	Type	Reset
31:20	base_addr	Address Region 3 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 3 size	RW	36'h0
19:16	Reserved	Reserved	RO	-
15:10	addr_region_size	<n>; used to calculate Address Region 3 size ($2^n \times 4\text{KB}$) CONSTRAINT: <n> must be configured so that the Address Region 3 size is less than or equal to $2^{\text{(address width)}}$.	RW	6'h0
9:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 3 size within Address Region 3 ($2^n \times 4\text{KB}$)	RW	6'h0

por_hni_cfg_ctl

Functions as the configuration control register for HN-I.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA00
Register reset	64'b1
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_hni_secure_register_groups_override.cfg_ctl

The following image shows the higher register bit assignments.

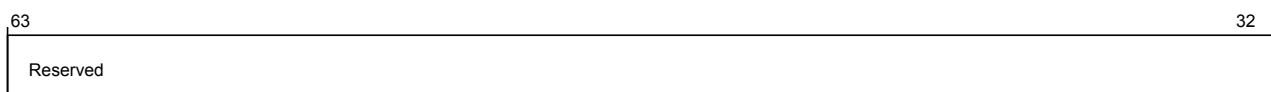


Figure 4-602 por_hni_por_hni_cfg_ctl (high)

The following table shows the por_hni_cfg_ctl higher register bit assignments.

Table 4-619 por_hni_por_hni_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

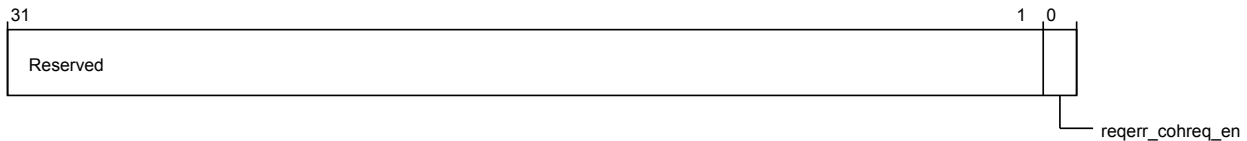


Figure 4-603 por_hni_por_hni_cfg_ctl (low)

The following table shows the por_hni_cfg_ctl lower register bit assignments.

Table 4-620 por_hni_por_hni_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	reqerr_cohreq_en	Enables sending of NDE response error to RN and logging of error information for the following requests: 1. Coherent Read 2. CleanUnique/MakeUnique 3. Coherent/CopyBack Write	RW	1'b1

por_hni_aux_ctl

Functions as the auxiliary control register for HN-I.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

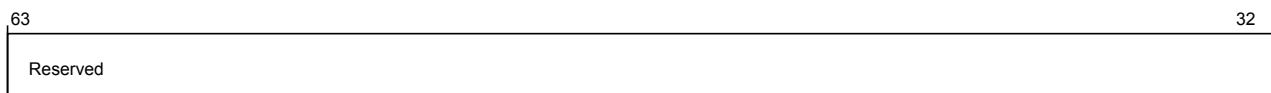


Figure 4-604 por_hni_por_hni_aux_ctl (high)

The following table shows the por_hni_aux_ctl higher register bit assignments.

Table 4-621 por_hni_por_hni_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

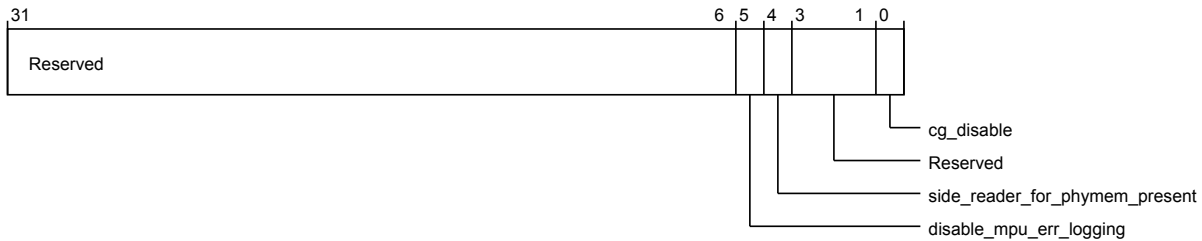


Figure 4-605 por_hni_por_hni_aux_ctl (low)

The following table shows the por_hni_aux_ctl lower register bit assignments.

Table 4-622 por_hni_por_hni_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5	disable_mpu_err_logging	Disables error logging for MPU errors	RW	1'b0
4	side_reader_for_phymem_present	Enables side reader in physical memory range	RW	1'b0
3:1	Reserved	Reserved	RO	-
0	cg_disable	Disables HN-I architectural clock gates	RW	1'b0

por_hni_errfr

Functions as the error feature register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3000

Register reset 64'b0000010100101

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

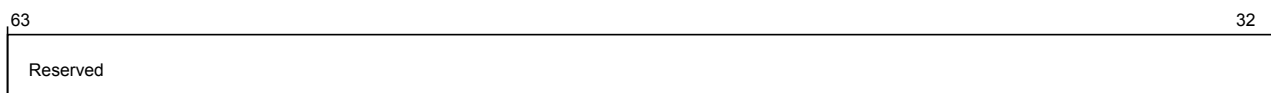


Figure 4-606 por_hni_por_hni_errfr (high)

The following table shows the por_hni_errfr higher register bit assignments.

Table 4-623 por_hni_por_hni_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

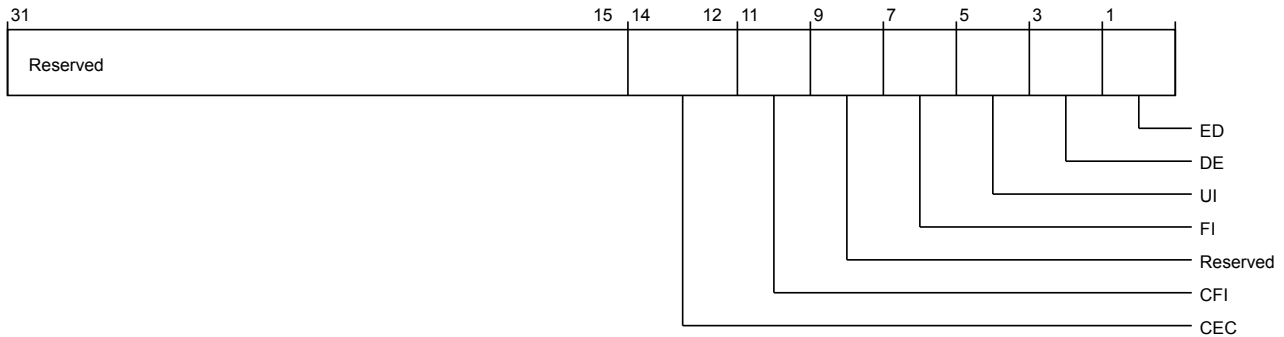


Figure 4-607 por_hni_por_hni_errfr (low)

The following table shows the por_hni_errfr lower register bit assignments.

Table 4-624 por_hni_por_hni_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_hni_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3008

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-608 por_hni_errctlr (high)

The following table shows the por_hni_errctlr higher register bit assignments.

Table 4-625 por_hni_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

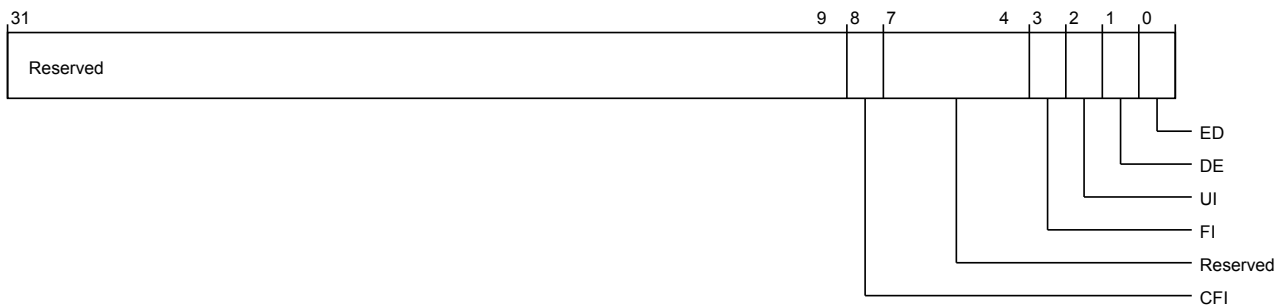


Figure 4-609 por_hni_errctlr (low)

The following table shows the por_hni_errctlr lower register bit assignments.

Table 4-626 por_hni_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hni_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hni_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hni_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hni_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hni_errfr.ED	RW	1'b0

por_hni_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3010
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-610 por_hni_errstatus (high)

The following table shows the por_hni_errstatus higher register bit assignments.

Table 4-627 por_hni_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.



Figure 4-611 por_hni_errstatus (low)

The following table shows the por_hni_errstatus lower register bit assignments.

Table 4-628 `por_hni_por_hni_errstatus` (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; <code>por_hni_erraddr</code> contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	<code>por_hni_ermisc</code> valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

`por_hni_erraddr`

Contains the error record address.

Its characteristics are:

Type RW

Register width (Bits) 64
Address offset 14'h3018
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

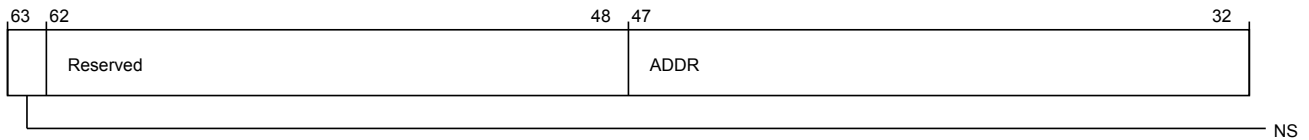


Figure 4-612 por_hni_erraddr (high)

The following table shows the por_hni_erraddr higher register bit assignments.

Table 4-629 por_hni_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hni_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

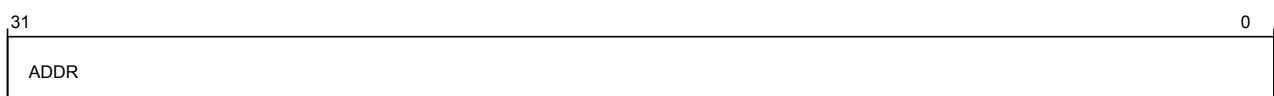


Figure 4-613 por_hni_erraddr (low)

The following table shows the por_hni_erraddr lower register bit assignments.

Table 4-630 por_hni_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_hni_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3020
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

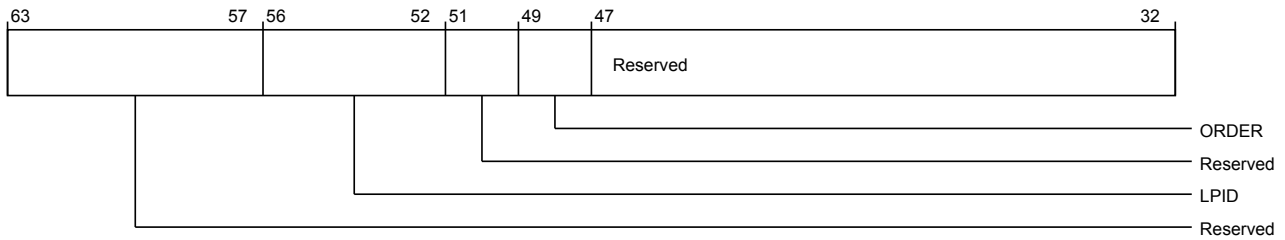


Figure 4-614 `por_hni_errmisc` (high)

The following table shows the `por_hni_errmisc` higher register bit assignments.

Table 4-631 `por_hni_errmisc` (high)

Bits	Field name	Description	Type	Reset
63:57	Reserved	Reserved	RO	-
56:52	LPID	Error logic processor ID	RW	5'b0
51:50	Reserved	Reserved	RO	-
49:48	ORDER	Error order	RW	4'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

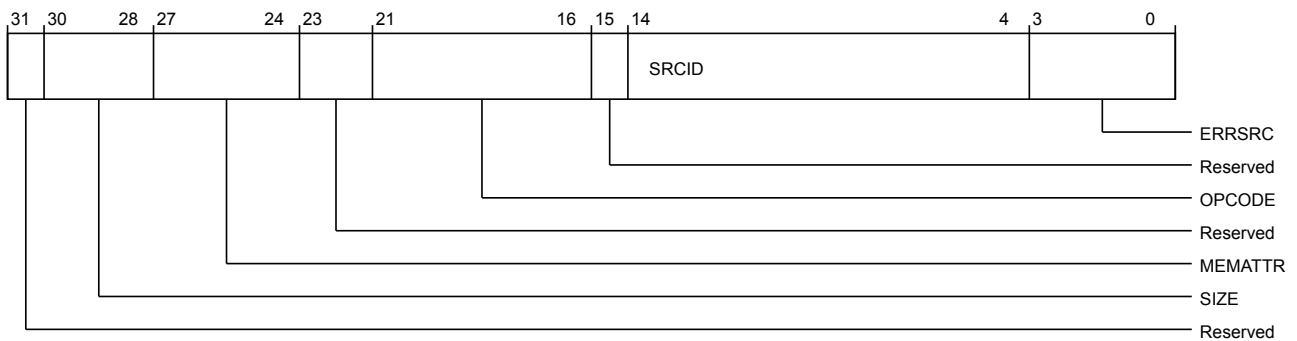


Figure 4-615 `por_hni_errmisc` (low)

The following table shows the `por_hni_errmisc` lower register bit assignments.

Table 4-632 por_hni_por_hni_errmisc (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23:22	Reserved	Reserved	RO	-
21:16	OPCODE	Error opcode	RW	6'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	ERRSRC	Error source 4'b0000: Coherent read 4'b0001: Coherent write 4'b0010: CleanUnique/MakeUnique 4'b0011: Atomic 4'b0100: Illegal configuration read 4'b0101: Illegal configuration write 4'b0110: Configuration write data partial byte enable error 4'b0111: Configuration write data parity error or poison error 4'b1000: BRESP error 4'b1001: Poison error 4'b1010: BRESP error and poison error NOTE: For configuration write data, BRESP, and poison errors, por_hni_errmisc.SRCID is the only valid field. For other error types, all fields are valid.	RW	4'b0

por_hni_errfr_NS

Functions as the non-secure error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3100
Register reset	64'b0000010100101
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

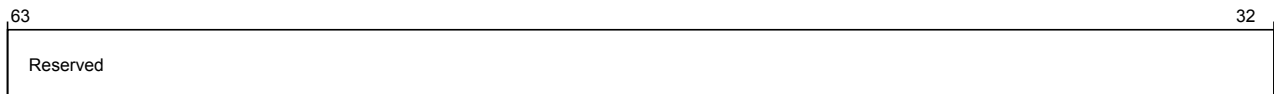


Figure 4-616 por_hni_errfr_NS (high)

The following table shows the por_hni_errfr_NS higher register bit assignments.

Table 4-633 por_hni_errfr_NS (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

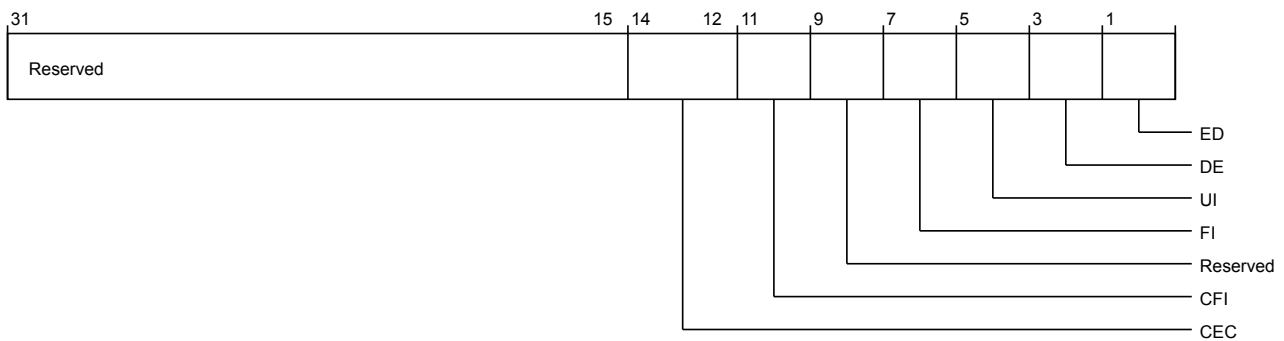


Figure 4-617 por_hni_errfr_NS (low)

The following table shows the por_hni_errfr_NS lower register bit assignments.

Table 4-634 por_hni_errfr_NS (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_hni_errctlr_NS

Functions as the non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3108
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

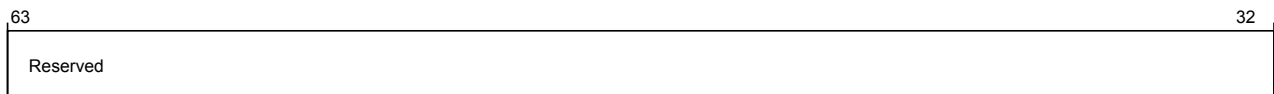


Figure 4-618 por_hni_errctlr_ns (high)

The following table shows the por_hni_errctlr_NS higher register bit assignments.

Table 4-635 por_hni_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

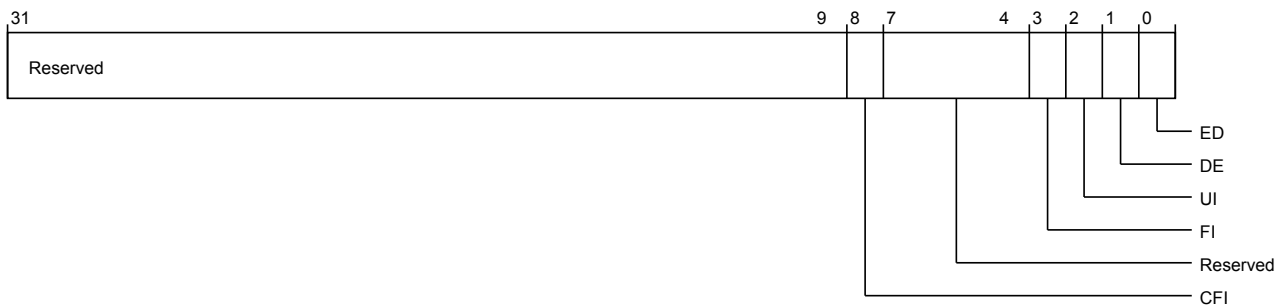


Figure 4-619 por_hni_errctlr_ns (low)

The following table shows the por_hni_errctlr_NS lower register bit assignments.

Table 4-636 por_hni_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hni_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-

Table 4-636 por_hni_por_hni_errctlr_ns (low) (continued)

Bits	Field name	Description	Type	Reset
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hni_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hni_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hni_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hni_errfr_NS.ED	RW	1'b0

por_hni_errstatus_NS

Functions as the non-secure error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3110
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

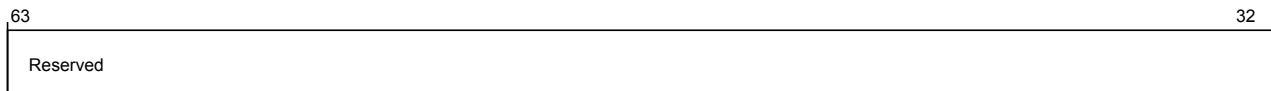


Figure 4-620 por_hni_por_hni_errstatus_ns (high)

The following table shows the por_hni_errstatus_NS higher register bit assignments.

Table 4-637 por_hni_por_hni_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.



Figure 4-621 `por_hni_por_hni_errstatus_ns` (low)

The following table shows the `por_hni_errstatus_NS` lower register bit assignments.

Table 4-638 `por_hni_por_hni_errstatus_ns` (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; <code>por_hni_erraddr_NS</code> contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	<code>por_hni_ermisc_NS</code> valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 4-638 por_hni_por_hni_errstatus_ns (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_hni_erraddr_NS

Contains the non-secure error record address.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3118
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

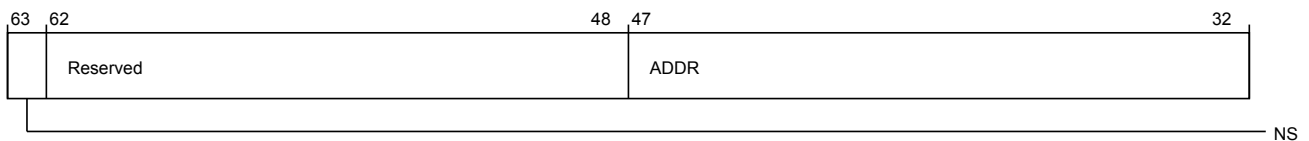


Figure 4-622 por_hni_por_hni_erraddr_ns (high)

The following table shows the por_hni_erraddr_NS higher register bit assignments.

Table 4-639 por_hni_por_hni_erraddr_ns (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hni_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

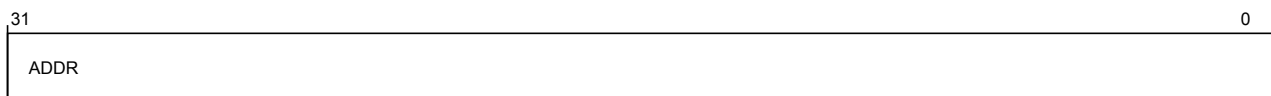


Figure 4-623 por_hni_por_hni_erraddr_ns (low)

The following table shows the por_hni_erraddr_NS lower register bit assignments.

Table 4-640 por_hni_por_hni_erraddr_ns (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_hni_errmisc_NS

Functions as the non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3120

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

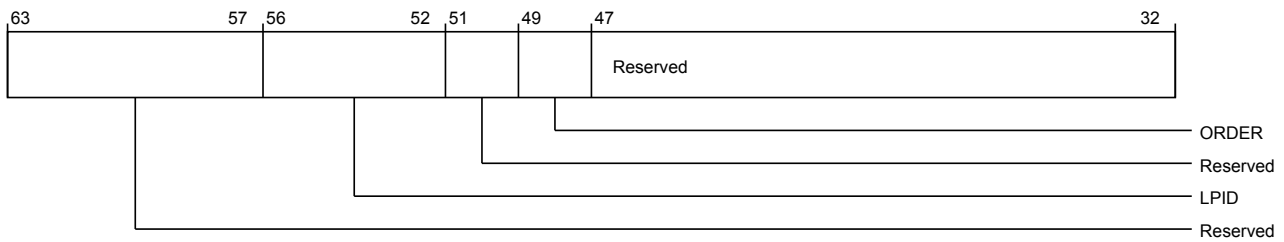


Figure 4-624 `por_hni_por_hni_errmisc_ns` (high)

The following table shows the `por_hni_errmisc_NS` higher register bit assignments.

Table 4-641 `por_hni_por_hni_errmisc_ns` (high)

Bits	Field name	Description	Type	Reset
63:57	Reserved	Reserved	RO	-
56:52	LPID	Error logic processor ID	RW	5'b0
51:50	Reserved	Reserved	RO	-
49:48	ORDER	Error order	RW	4'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

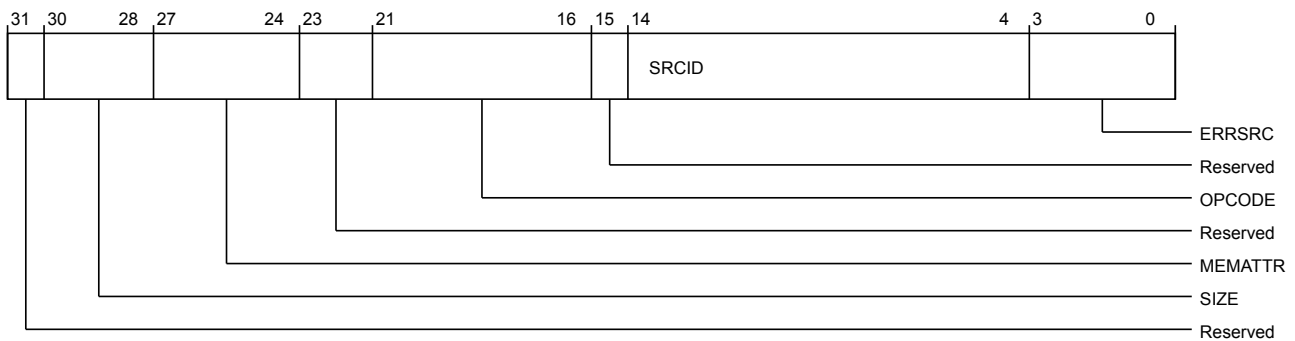


Figure 4-625 `por_hni_por_hni_errmisc_ns` (low)

The following table shows the `por_hni_errmisc_NS` lower register bit assignments.

Table 4-642 `por_hni_por_hni_errmisc_ns` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23:22	Reserved	Reserved	RO	-

Table 4-642 `por_hni_por_hni_errmisc_ns` (low) (continued)

Bits	Field name	Description	Type	Reset
21:16	OPCODE	Error opcode	RW	6'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	ERRSRC	<p>Error source</p> <p>4'b0000: Coherent read</p> <p>4'b0001: Coherent write</p> <p>4'b0010: CleanUnique/MakeUnique</p> <p>4'b0011: Atomic</p> <p>4'b0100: Illegal configuration read</p> <p>4'b0101: Illegal configuration write</p> <p>4'b0110: Configuration write data partial byte enable error</p> <p>4'b0111: Configuration write data parity error or poison error</p> <p>4'b1000: BRESP error</p> <p>4'b1001: Poison error</p> <p>4'b1010: BRESP error and poison error</p> <p>4'b1011: Illegal MPU access</p> <p>NOTE: For configuration write data, BRESP, and poison errors, <code>por_hni_errmisc_NS.SRCID</code> is the only valid field. For other error types, all fields are valid.</p>	RW	4'b0

`por_hni_pmu_event_sel`

Specifies the PMU event to be counted.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2000
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

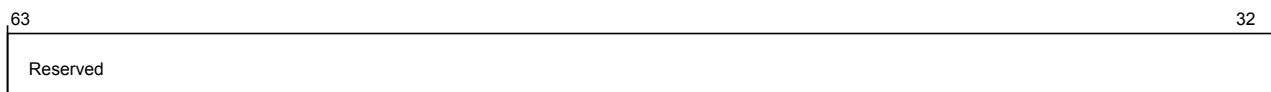


Figure 4-626 `por_hni_por_hni_pmu_event_sel` (high)

The following table shows the `por_hni_pmu_event_sel` higher register bit assignments.

Table 4-643 `por_hni_por_hni_pmu_event_sel` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

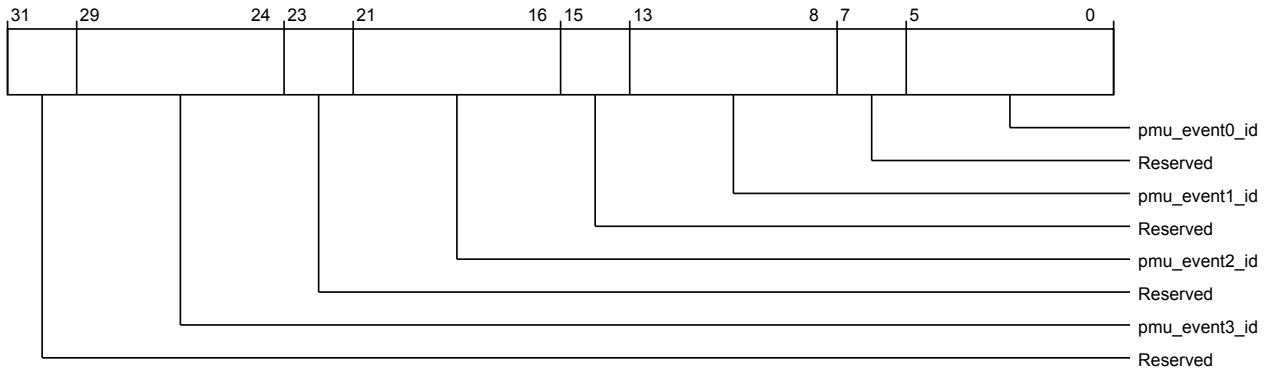


Figure 4-627 `por_hni_por_hni_pmu_event_sel` (low)

The following table shows the `por_hni_pmu_event_sel` lower register bit assignments.

Table 4-644 `por_hni_por_hni_pmu_event_sel` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>pmu_event3_id</code>	HN-I PMU Event 3 select; see <code>pmu_event0_id</code> for encodings	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	<code>pmu_event2_id</code>	HN-I PMU Event 2 select; see <code>pmu_event0_id</code> for encodings	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	<code>pmu_event1_id</code>	HN-I PMU Event 1 select; see <code>pmu_event0_id</code> for encodings	RW	6'b0

Table 4-644 por_hni_por_hni_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
7:6	Reserved	Reserved	RO	-
5:0	pmu_event0_id	<p>HN-I PMU Event 0 select</p> <p>6'h00: No event</p> <p>6'h20: RRT read occupancy count overflow</p> <p>6'h21: RRT write occupancy count overflow</p> <p>6'h22: RDT read occupancy count overflow</p> <p>6'h23: RDT write occupancy count overflow</p> <p>6'h24: WDB occupancy count overflow</p> <p>6'h25: RRT read allocation</p> <p>6'h26: RRT write allocation</p> <p>6'h27: RDT read allocation</p> <p>6'h28: RDT write allocation</p> <p>6'h29: WDB allocation</p> <p>6'h2A: RETRYACK TXRSP flit sent</p> <p>6'h2B: ARVALID set without ARREADY event</p> <p>6'h2C: ARREADY set without ARVALID event</p> <p>6'h2D: AWVALID set without AWREADY event</p> <p>6'h2E: AWREADY set without AWVALID event</p> <p>6'h2F: WVALID set without WREADY event</p> <p>6'h30: TXDAT stall (TXDAT valid but no link credit available)</p> <p>6'h31: Non-PCIe serialization event</p> <p>6'h32: PCIe serialization event</p> <p>NOTE: All other encodings are reserved.</p>	RW	6'b0

4.3.6 XP register descriptions

Lists the XP registers.

por_mxp_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

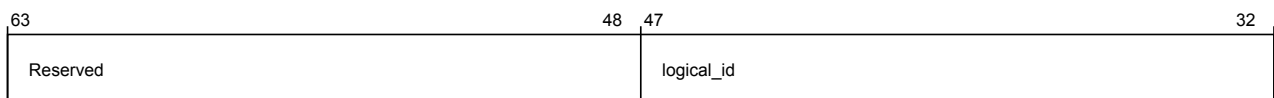


Figure 4-628 por_mxp_node_info (high)

The following table shows the por_mxp_node_info higher register bit assignments.

Table 4-645 por_mxp_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

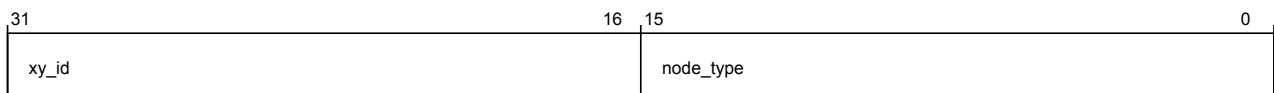


Figure 4-629 por_mxp_node_info (low)

The following table shows the por_mxp_node_info lower register bit assignments.

Table 4-646 por_mxp_por_mxp_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	xy_id	Identifies (X,Y) location of XP within the mesh NOTE: The (X,Y) location is specified following the node ID format as defined in Node ID mapping section, with the bottom 3 bits, corresponding to port ID and device ID, set to 0. Bits 31:11 must always be set to 0. The range of bits representing the (X,Y) location varies for different node ID formats.	RO	16'h0000
15:0	node_type	CMN-600AE node type identifier	RO	16'h0006

por_mxp_device_port_connect_info_p0

Contains device port connection information for port 0.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h8
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

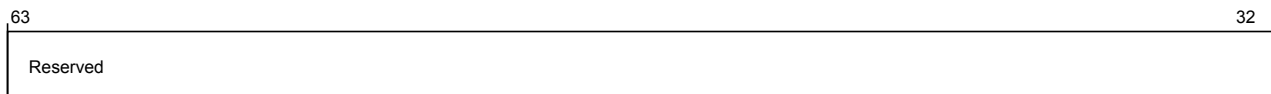


Figure 4-630 por_mxp_por_mxp_device_port_connect_info_p0 (high)

The following table shows the por_mxp_device_port_connect_info_p0 higher register bit assignments.

Table 4-647 por_mxp_por_mxp_device_port_connect_info_p0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

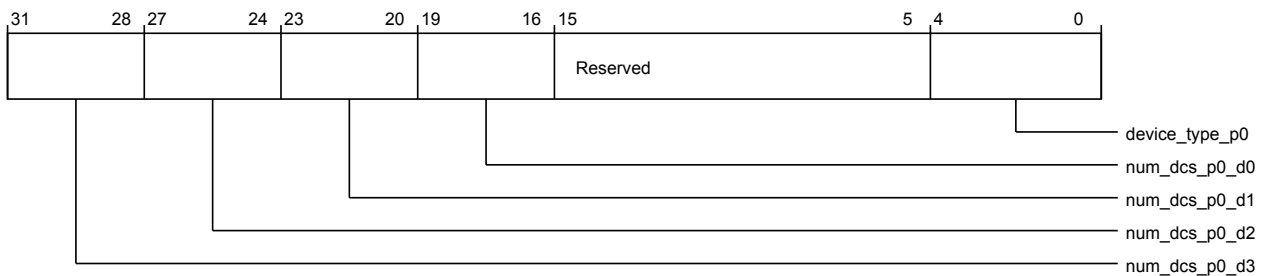


Figure 4-631 por_mxp_por_mxp_device_port_connect_info_p0 (low)

The following table shows the por_mxp_device_port_connect_info_p0 lower register bit assignments.

Table 4-648 por_mxp_por_mxp_device_port_connect_info_p0 (low)

Bits	Field name	Description	Type	Reset
31:28	num_dcs_p0_d3	Number of device credited slices connected to port 0 device 3 (Allowed values: 0-4)	RO	Configuration dependent
27:24	num_dcs_p0_d2	Number of device credited slices connected to port 0 device 2 (Allowed values: 0-4)	RO	Configuration dependent
23:20	num_dcs_p0_d1	Number of device credited slices connected to port 0 device 1 (Allowed values: 0-4)	RO	Configuration dependent
19:16	num_dcs_p0_d0	Number of device credited slices connected to port 0 device 0 (Allowed values: 0-4)	RO	Configuration dependent
15:5	Reserved	Reserved	RO	-
4:0	device_type_p0	Connected device type 5'b00000: Reserved 5'b00001: RN-I 5'b00010: RN-D 5'b00011: Reserved 5'b00100: RN-F_CHIB 5'b00101: RN-F_CHIB_ESAM 5'b00110: RN-F_CHIA 5'b00111: RN-F_CHIA_ESAM 5'b01000: HN-T 5'b01001: HN-I 5'b01010: HN-D 5'b01011: Reserved 5'b01100: SN-F 5'b01101: SBSX 5'b01110: HN-F 5'b01111: Reserved 5'b10000: Reserved 5'b10001: CXHA 5'b10010: CXRA 5'b10011: CXRH 5'b10100-5'b11111: Reserved	RO	Configuration dependent

por_mxp_device_port_connect_info_p1

Contains device port connection information for port 1.

Its characteristics are:

Type RO

Register width (Bits) 64
Address offset 14'h10
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

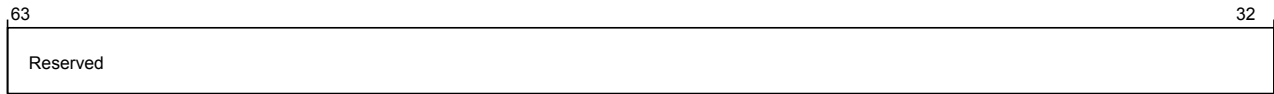


Figure 4-632 `por_mxp_por_mxp_device_port_connect_info_p1` (high)

The following table shows the `por_mxp_device_port_connect_info_p1` higher register bit assignments.

Table 4-649 `por_mxp_por_mxp_device_port_connect_info_p1` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

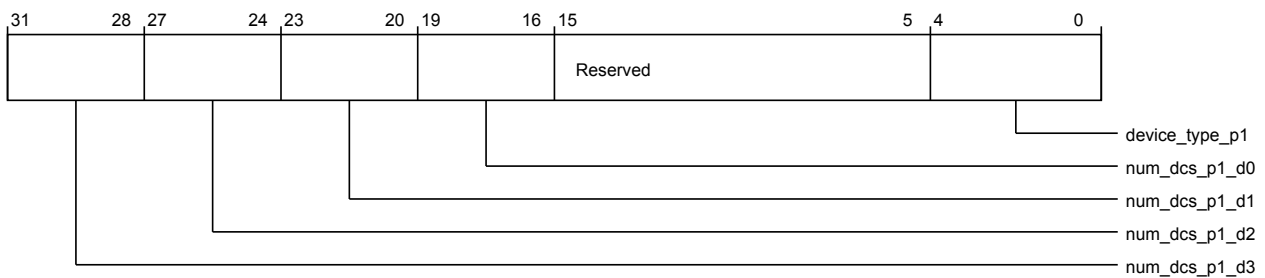


Figure 4-633 `por_mxp_por_mxp_device_port_connect_info_p1` (low)

The following table shows the `por_mxp_device_port_connect_info_p1` lower register bit assignments.

Table 4-650 `por_mxp_por_mxp_device_port_connect_info_p1` (low)

Bits	Field name	Description	Type	Reset
31:28	<code>num_dcs_p1_d3</code>	Number of device credited slices connected to port 1 device 3 (Allowed values: 0-4)	RO	Configuration dependent
27:24	<code>num_dcs_p1_d2</code>	Number of device credited slices connected to port 1 device 2 (Allowed values: 0-4)	RO	Configuration dependent
23:20	<code>num_dcs_p1_d1</code>	Number of device credited slices connected to port 1 device 1 (Allowed values: 0-4)	RO	Configuration dependent
19:16	<code>num_dcs_p1_d0</code>	Number of device credited slices connected to port 1 device 0 (Allowed values: 0-4)	RO	Configuration dependent

Table 4-650 por_mxp_por_mxp_device_port_connect_info_p1 (low) (continued)

Bits	Field name	Description	Type	Reset
15:5	Reserved	Reserved	RO	-
4:0	device_type_p1	<p>Connected device type</p> <p>5'b00000: Reserved</p> <p>5'b00001: RN-I</p> <p>5'b00010: RN-D</p> <p>5'b00011: Reserved</p> <p>5'b00100: RN-F CHIB</p> <p>5'b00101: RN-F CHIB ESAM</p> <p>5'b00110: RN-F CHIA</p> <p>5'b00111: RN-F CHIA ESAM</p> <p>5'b01000: HN-T</p> <p>5'b01001: HN-I</p> <p>5'b01010: HN-D</p> <p>5'b01011: Reserved</p> <p>5'b01100: SN-F</p> <p>5'b01101: SBSX</p> <p>5'b01110: HN-F</p> <p>5'b01111: Reserved</p> <p>5'b10000: Reserved</p> <p>5'b10001: CXHA</p> <p>5'b10010: CXRA</p> <p>5'b10011: CXRH</p> <p>5'b10100-5'b11111: Reserved</p>	RO	Configuration dependent

por_mxp_mesh_port_connect_info_east

Contains port connection information for East port.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h18
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

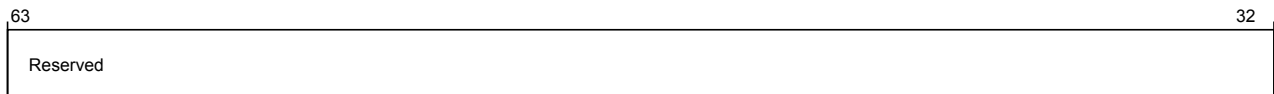


Figure 4-634 por_mxp_por_mxp_mesh_port_connect_info_east (high)

The following table shows the por_mxp_mesh_port_connect_info_east higher register bit assignments.

Table 4-651 por_mxp_por_mxp_mesh_port_connect_info_east (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

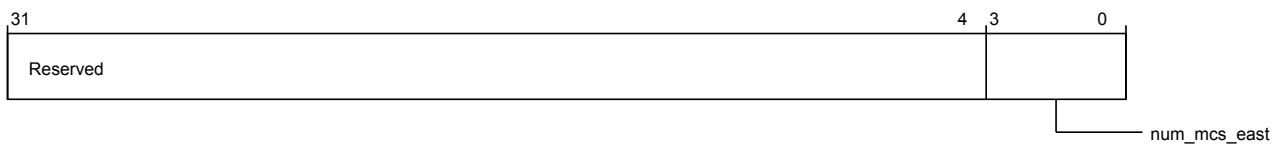


Figure 4-635 por_mxp_por_mxp_mesh_port_connect_info_east (low)

The following table shows the por_mxp_mesh_port_connect_info_east lower register bit assignments.

Table 4-652 por_mxp_por_mxp_mesh_port_connect_info_east (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	num_mcs_east	Number of mesh credited slices connected to East port (Allowed values: 0-4)	RO	Configuration dependent

por_mxp_mesh_port_connect_info_north

Contains port connection information for North port.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h20

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

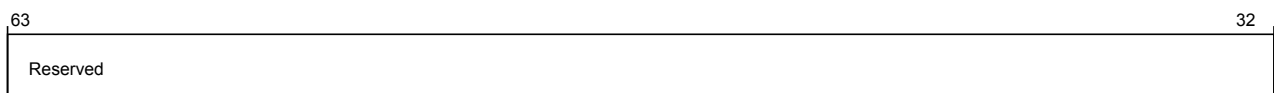


Figure 4-636 por_mxp_por_mxp_mesh_port_connect_info_north (high)

The following table shows the por_mxp_mesh_port_connect_info_north higher register bit assignments.

Table 4-653 por_mxp_por_mxp_mesh_port_connect_info_north (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

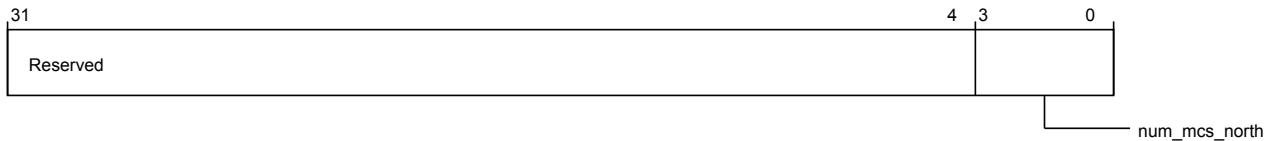


Figure 4-637 por_mxp_por_mxp_mesh_port_connect_info_north (low)

The following table shows the por_mxp_mesh_port_connect_info_north lower register bit assignments.

Table 4-654 por_mxp_por_mxp_mesh_port_connect_info_north (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	num_mcs_north	Number of mesh credited slices connected to North port (Allowed values: 0-4)	RO	Configuration dependent

por_mxp_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

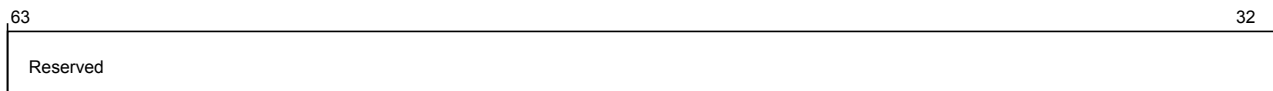


Figure 4-638 por_mxp_por_mxp_child_info (high)

The following table shows the por_mxp_child_info higher register bit assignments.

Table 4-655 por_mxp_por_mxp_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

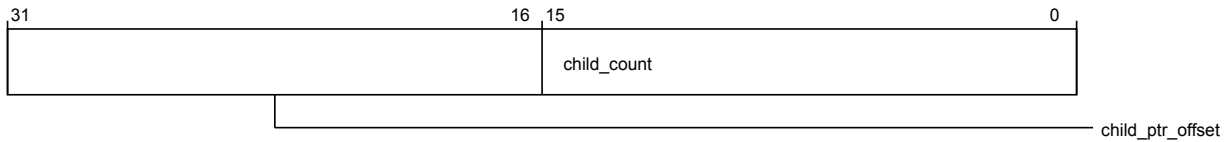


Figure 4-639 por_mxp_por_mxp_child_info (low)

The following table shows the por_mxp_child_info lower register bit assignments.

Table 4-656 por_mxp_por_mxp_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h100
15:0	child_count	Number of child nodes; used in discovery process	RO	Configuration dependent

por_mxp_child_pointer_0

Contains base address of the configuration slave for child 0.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h100
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

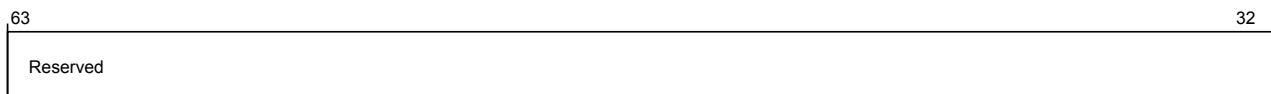


Figure 4-640 por_mxp_por_mxp_child_pointer_0 (high)

The following table shows the por_mxp_child_pointer_0 higher register bit assignments.

Table 4-657 por_mxp_por_mxp_child_pointer_0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

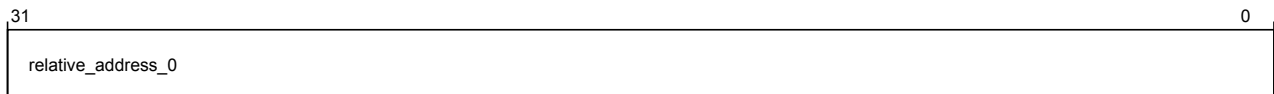


Figure 4-641 por_mxp_por_mxp_child_pointer_0 (low)

The following table shows the por_mxp_child_pointer_0 lower register bit assignments.

Table 4-658 por_mxp_por_mxp_child_pointer_0 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_0	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_1

Contains base address of the configuration slave for child 1.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h108
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-642 por_mxp_por_mxp_child_pointer_1 (high)

The following table shows the por_mxp_child_pointer_1 higher register bit assignments.

Table 4-659 por_mxp_por_mxp_child_pointer_1 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

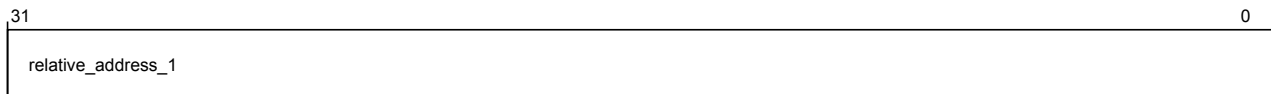


Figure 4-643 por_mxp_por_mxp_child_pointer_1 (low)

The following table shows the por_mxp_child_pointer_1 lower register bit assignments.

Table 4-660 por_mxp_por_mxp_child_pointer_1 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_1	<p>Bit [31]: External or internal child node</p> <p>1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE</p> <p>1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE</p> <p>Bits [30:28]: Set to 3'b000</p> <p>Bits [27:0]: Child node address offset relative to PERIPHBASE</p>	RO	32'b0

por_mxp_child_pointer_2

Contains base address of the configuration slave for child 2.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h110
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-644 por_mxp_por_mxp_child_pointer_2 (high)

The following table shows the por_mxp_child_pointer_2 higher register bit assignments.

Table 4-661 por_mxp_por_mxp_child_pointer_2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

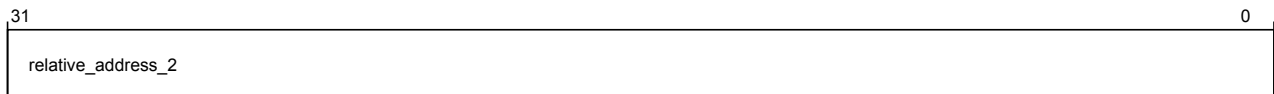


Figure 4-645 por_mxp_por_mxp_child_pointer_2 (low)

The following table shows the por_mxp_child_pointer_2 lower register bit assignments.

Table 4-662 por_mxp_por_mxp_child_pointer_2 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_2	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_3

Contains base address of the configuration slave for child 3.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h118
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-646 por_mxp_por_mxp_child_pointer_3 (high)

The following table shows the por_mxp_child_pointer_3 higher register bit assignments.

Table 4-663 por_mxp_por_mxp_child_pointer_3 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

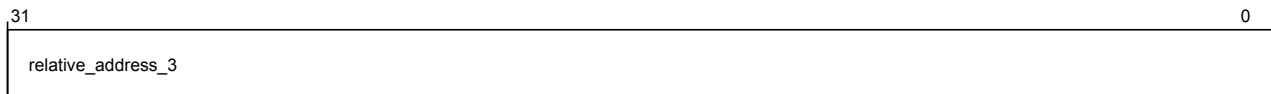


Figure 4-647 por_mxp_por_mxp_child_pointer_3 (low)

The following table shows the por_mxp_child_pointer_3 lower register bit assignments.

Table 4-664 por_mxp_por_mxp_child_pointer_3 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_3	<p>Bit [31]: External or internal child node</p> <p>1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE</p> <p>1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE</p> <p>Bits [30:28]: Set to 3'b000</p> <p>Bits [27:0]: Child node address offset relative to PERIPHBASE</p>	RO	32'b0

por_mxp_child_pointer_4

Contains base address of the configuration slave for child 4.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h120
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-648 por_mxp_por_mxp_child_pointer_4 (high)

The following table shows the por_mxp_child_pointer_4 higher register bit assignments.

Table 4-665 por_mxp_por_mxp_child_pointer_4 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

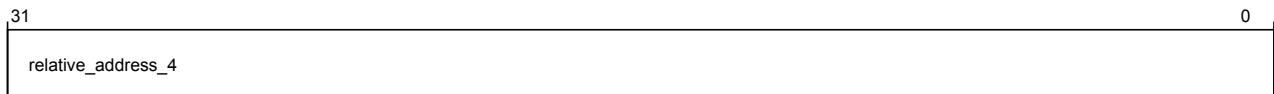


Figure 4-649 por_mxp_por_mxp_child_pointer_4 (low)

The following table shows the por_mxp_child_pointer_4 lower register bit assignments.

Table 4-666 por_mxp_por_mxp_child_pointer_4 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_4	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_5

Contains base address of the configuration slave for child 5.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h128
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-650 por_mxp_por_mxp_child_pointer_5 (high)

The following table shows the por_mxp_child_pointer_5 higher register bit assignments.

Table 4-667 por_mxp_por_mxp_child_pointer_5 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

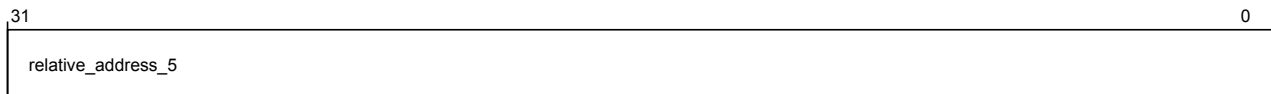


Figure 4-651 por_mxp_por_mxp_child_pointer_5 (low)

The following table shows the por_mxp_child_pointer_5 lower register bit assignments.

Table 4-668 por_mxp_por_mxp_child_pointer_5 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_5	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_6

Contains base address of the configuration slave for child 6.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h130
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-652 por_mxp_por_mxp_child_pointer_6 (high)

The following table shows the por_mxp_child_pointer_6 higher register bit assignments.

Table 4-669 por_mxp_por_mxp_child_pointer_6 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

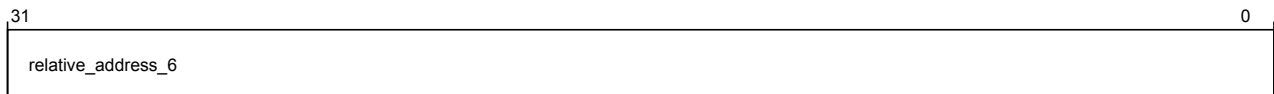


Figure 4-653 por_mxp_por_mxp_child_pointer_6 (low)

The following table shows the por_mxp_child_pointer_6 lower register bit assignments.

Table 4-670 por_mxp_por_mxp_child_pointer_6 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_6	<p>Bit [31]: External or internal child node</p> <p>1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE</p> <p>1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE</p> <p>Bits [30:28]: Set to 3'b000</p> <p>Bits [27:0]: Child node address offset relative to PERIPHBASE</p>	RO	32'b0

por_mxp_child_pointer_7

Contains base address of the configuration slave for child 7.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h138
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-654 por_mxp_por_mxp_child_pointer_7 (high)

The following table shows the por_mxp_child_pointer_7 higher register bit assignments.

Table 4-671 por_mxp_por_mxp_child_pointer_7 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

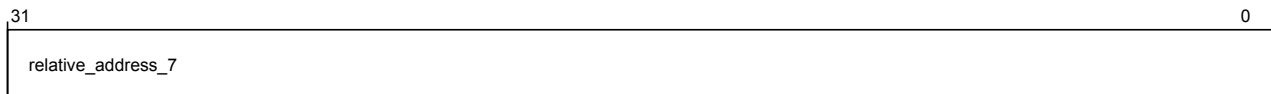


Figure 4-655 por_mxp_por_mxp_child_pointer_7 (low)

The following table shows the por_mxp_child_pointer_7 lower register bit assignments.

Table 4-672 por_mxp_por_mxp_child_pointer_7 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_7	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_8

Contains base address of the configuration slave for child 8.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h140
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-656 por_mxp_por_mxp_child_pointer_8 (high)

The following table shows the por_mxp_child_pointer_8 higher register bit assignments.

Table 4-673 por_mxp_por_mxp_child_pointer_8 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

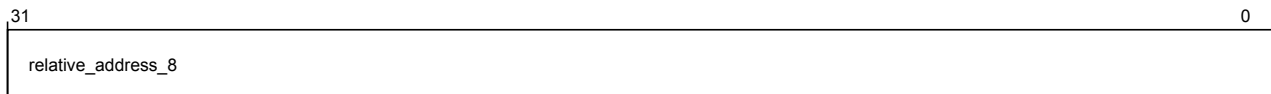


Figure 4-657 por_mxp_por_mxp_child_pointer_8 (low)

The following table shows the por_mxp_child_pointer_8 lower register bit assignments.

Table 4-674 por_mxp_por_mxp_child_pointer_8 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_8	<p>Bit [31]: External or internal child node</p> <p>1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE</p> <p>1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE</p> <p>Bits [30:28]: Set to 3'b000</p> <p>Bits [27:0]: Child node address offset relative to PERIPHBASE</p>	RO	32'b0

por_mxp_child_pointer_9

Contains base address of the configuration slave for child 9.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h148
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-658 por_mxp_por_mxp_child_pointer_9 (high)

The following table shows the por_mxp_child_pointer_9 higher register bit assignments.

Table 4-675 por_mxp_por_mxp_child_pointer_9 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

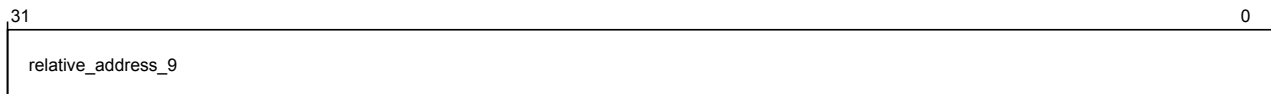


Figure 4-659 por_mxp_por_mxp_child_pointer_9 (low)

The following table shows the por_mxp_child_pointer_9 lower register bit assignments.

Table 4-676 por_mxp_por_mxp_child_pointer_9 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_9	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_10

Contains base address of the configuration slave for child 10.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h150
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-660 por_mxp_por_mxp_child_pointer_10 (high)

The following table shows the por_mxp_child_pointer_10 higher register bit assignments.

Table 4-677 por_mxp_por_mxp_child_pointer_10 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

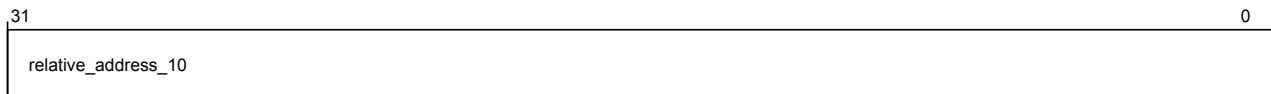


Figure 4-661 por_mxp_por_mxp_child_pointer_10 (low)

The following table shows the por_mxp_child_pointer_10 lower register bit assignments.

Table 4-678 por_mxp_por_mxp_child_pointer_10 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_10	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPBASE	RO	32'b0

por_mxp_child_pointer_11

Contains base address of the configuration slave for child 11.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h158
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-662 por_mxp_por_mxp_child_pointer_11 (high)

The following table shows the por_mxp_child_pointer_11 higher register bit assignments.

Table 4-679 por_mxp_por_mxp_child_pointer_11 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

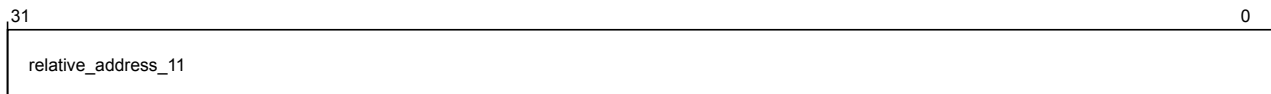


Figure 4-663 por_mxp_por_mxp_child_pointer_11 (low)

The following table shows the por_mxp_child_pointer_11 lower register bit assignments.

Table 4-680 por_mxp_por_mxp_child_pointer_11 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_11	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPBASE	RO	32'b0

por_mxp_child_pointer_12

Contains base address of the configuration slave for child 12.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h160
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-664 por_mxp_por_mxp_child_pointer_12 (high)

The following table shows the por_mxp_child_pointer_12 higher register bit assignments.

Table 4-681 por_mxp_por_mxp_child_pointer_12 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

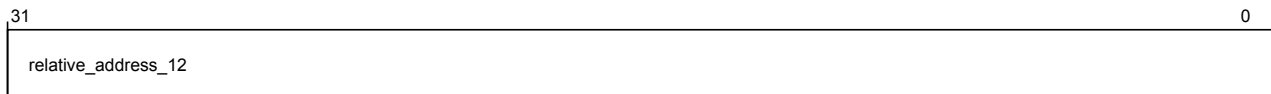


Figure 4-665 por_mxp_por_mxp_child_pointer_12 (low)

The following table shows the por_mxp_child_pointer_12 lower register bit assignments.

Table 4-682 por_mxp_por_mxp_child_pointer_12 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_12	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPBASE	RO	32'b0

por_mxp_child_pointer_13

Contains base address of the configuration slave for child 13.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h168
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-666 por_mxp_por_mxp_child_pointer_13 (high)

The following table shows the por_mxp_child_pointer_13 higher register bit assignments.

Table 4-683 por_mxp_por_mxp_child_pointer_13 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

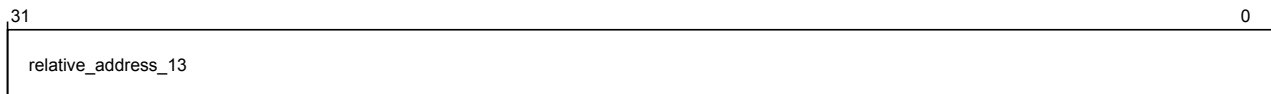


Figure 4-667 por_mxp_por_mxp_child_pointer_13 (low)

The following table shows the por_mxp_child_pointer_13 lower register bit assignments.

Table 4-684 por_mxp_por_mxp_child_pointer_13 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_13	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_14

Contains base address of the configuration slave for child 14.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h170
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-668 por_mxp_por_mxp_child_pointer_14 (high)

The following table shows the por_mxp_child_pointer_14 higher register bit assignments.

Table 4-685 por_mxp_por_mxp_child_pointer_14 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

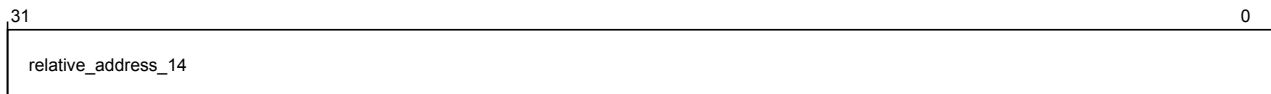


Figure 4-669 por_mxp_por_mxp_child_pointer_14 (low)

The following table shows the por_mxp_child_pointer_14 lower register bit assignments.

Table 4-686 por_mxp_por_mxp_child_pointer_14 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_14	<p>Bit [31]: External or internal child node</p> <p>1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE</p> <p>1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE</p> <p>Bits [30:28]: Set to 3'b000</p> <p>Bits [27:0]: Child node address offset relative to PERIPBASE</p>	RO	32'b0

por_mxp_child_pointer_15

Contains base address of the configuration slave for child 15.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h178
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-670 por_mxp_por_mxp_child_pointer_15 (high)

The following table shows the por_mxp_child_pointer_15 higher register bit assignments.

Table 4-687 por_mxp_por_mxp_child_pointer_15 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

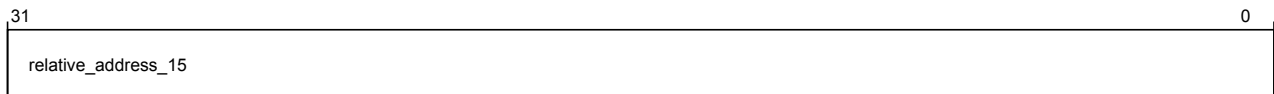


Figure 4-671 por_mxp_por_mxp_child_pointer_15 (low)

The following table shows the por_mxp_child_pointer_15 lower register bit assignments.

Table 4-688 por_mxp_por_mxp_child_pointer_15 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_15	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600AE 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600AE Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPBASE	RO	32'b0

por_mxp_p0_info

Provides component identification information for XP port 0.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h900
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-672 por_mxp_por_mxp_p0_info (high)

The following table shows the por_mxp_p0_info higher register bit assignments.

Table 4-689 por_mxp_por_mxp_p0_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

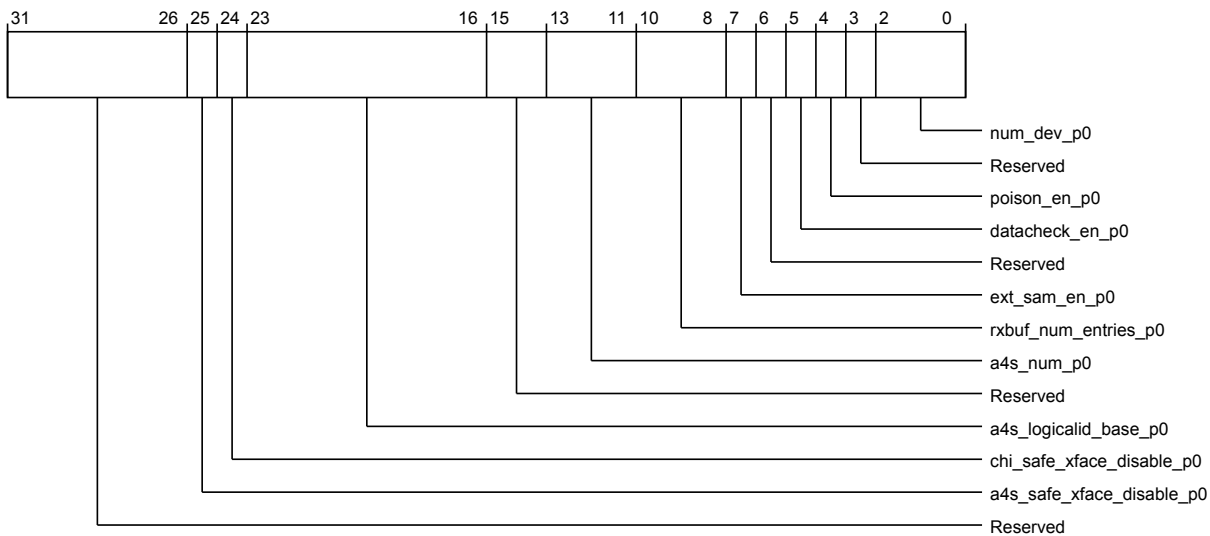


Figure 4-673 por_mxp_por_mxp_p0_info (low)

The following table shows the por_mxp_p0_info lower register bit assignments.

Table 4-690 por_mxp_por_mxp_p0_info (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25	a4s_safe_xface_disable_p0	AXI4Stream safe interface disable	RO	Configuration dependent
24	chi_safe_xface_disable_p0	CHI safe interface disable	RO	Configuration dependent
23:16	a4s_logicalid_base_p0	AXI4Stream interfaces logical ID base at this port (0 or 1)	RO	Configuration dependent
15:14	Reserved	Reserved	RO	-
13:11	a4s_num_p0	Total number of RN-F AXI4Stream interfaces at this port (0 to 4)	RO	Configuration dependent
10:8	rxbuf_num_entries_p0	Number of input buffers for each device at this port (2 to 4)	RO	Configuration dependent
7	ext_sam_en_p0	ESAM enable	RO	Configuration dependent
6	Reserved	Reserved	RO	-
5	datacheck_en_p0	Datacheck enable	RO	Configuration dependent
4	poison_en_p0	Poison enable	RO	Configuration dependent
3	Reserved	Reserved	RO	-
2:0	num_dev_p0	Number of devices connected to this port (0 to 4)	RO	Configuration dependent

por_mxp_p1_info

Provides component identification information for XP port 1.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h908
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-674 por_mxp_por_mxp_p1_info (high)

The following table shows the por_mxp_p1_info higher register bit assignments.

Table 4-691 por_mxp_por_mxp_p1_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

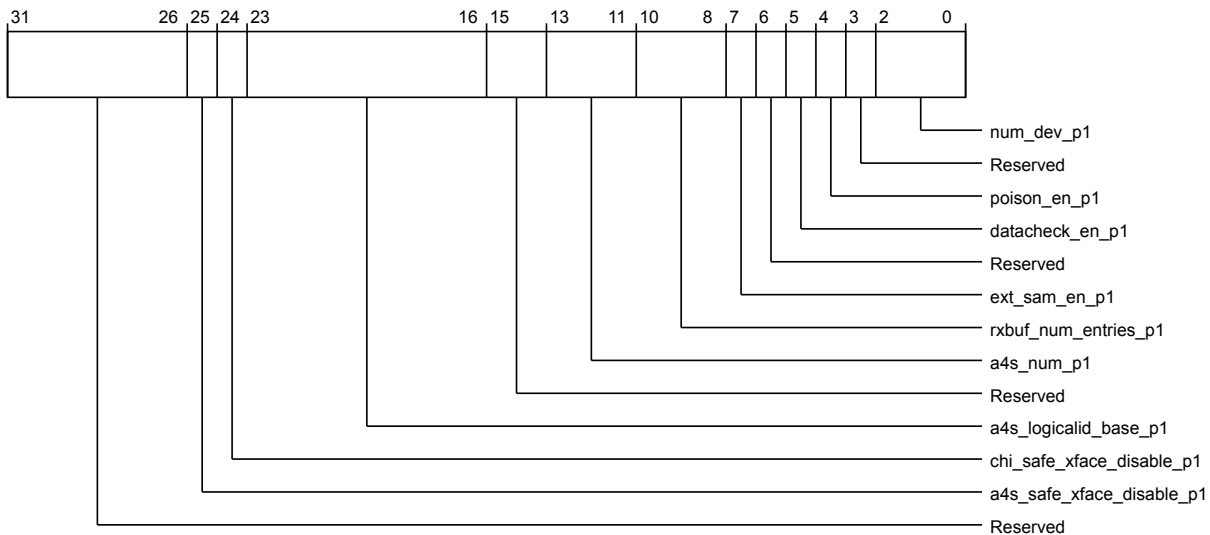


Figure 4-675 por_mxp_por_mxp_p1_info (low)

The following table shows the por_mxp_p1_info lower register bit assignments.

Table 4-692 por_mxp_por_mxp_p1_info (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25	a4s_safe_xface_disable_p1	AXI4Stream safe interface disable	RO	Configuration dependent
24	chi_safe_xface_disable_p1	CHI safe interface disable	RO	Configuration dependent

Table 4-692 por_mxp_por_mxp_p1_info (low) (continued)

Bits	Field name	Description	Type	Reset
23:16	a4s_logicalid_base_p1	AXI4Stream interfaces logical ID base at this port (0 or 1)	RO	Configuration dependent
15:14	Reserved	Reserved	RO	-
13:11	a4s_num_p1	Total number of RN-F AXI4Stream interfaces at this port (0 to 4)	RO	Configuration dependent
10:8	rxbuf_num_entries_p1	Number of input buffers at this port (2 to 4)	RO	Configuration dependent
7	ext_sam_en_p1	ESAM enable	RO	Configuration dependent
6	Reserved	Reserved	RO	-
5	datacheck_en_p1	Datacheck enable	RO	Configuration dependent
4	poison_en_p1	Poison enable	RO	Configuration dependent
3	Reserved	Reserved	RO	-
2:0	num_dev_p1	Number of devices connected to this port (0 to 4)	RO	Configuration dependent

por_mxp_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

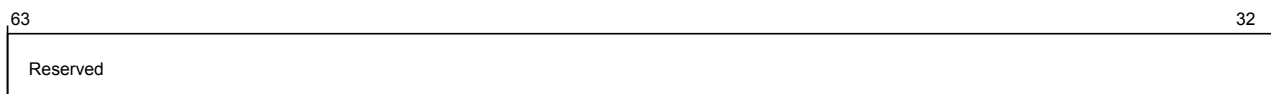


Figure 4-676 por_mxp_por_mxp_secure_register_groups_override (high)

The following table shows the por_mxp_secure_register_groups_override higher register bit assignments.

Table 4-693 por_mxp_por_mxp_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

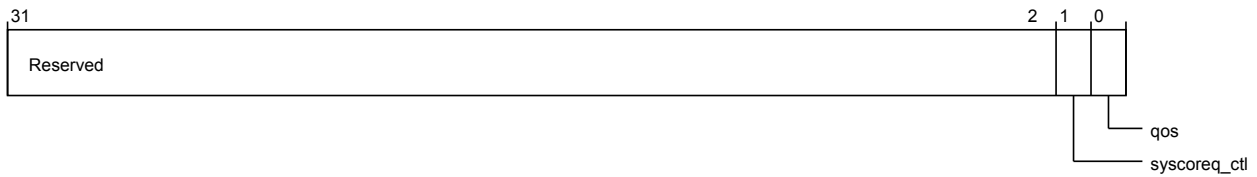


Figure 4-677 por_mxp_secure_register_groups_override (low)

The following table shows the por_mxp_secure_register_groups_override lower register bit assignments.

Table 4-694 por_mxp_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	syscoreq_ctl	Allows non-secure access to secure syscoreq_ctl registers	RW	1'b0
0	qos	Allows non-secure access to secure QoS registers	RW	1'b0

por_mxp_aux_ctl

Functions as the auxiliary control register for XP.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

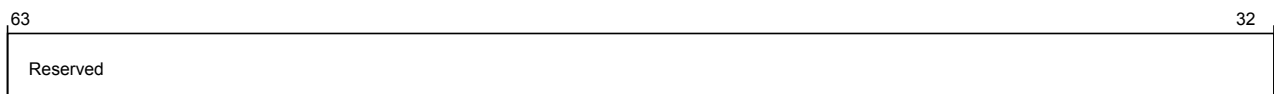


Figure 4-678 por_mxp_aux_ctl (high)

The following table shows the por_mxp_aux_ctl higher register bit assignments.

Table 4-695 por_mxp_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

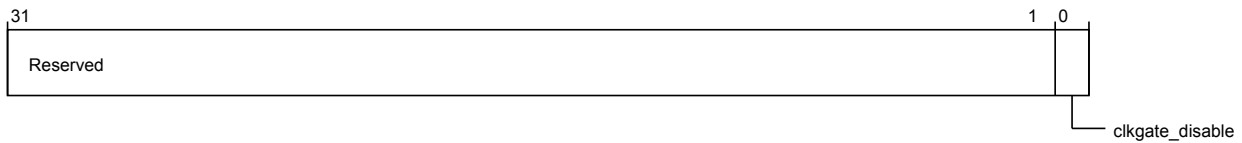


Figure 4-679 por_mxp_por_mxp_aux_ctl (low)

The following table shows the por_mxp_aux_ctl lower register bit assignments.

Table 4-696 por_mxp_por_mxp_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	clkgate_disable	Disables clock gating when set	RW	1'b0

por_mxp_p0_qos_control

Controls QoS settings for devices connected to port 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA80
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_mxp_secure_register_groups_override.qos

The following image shows the higher register bit assignments.

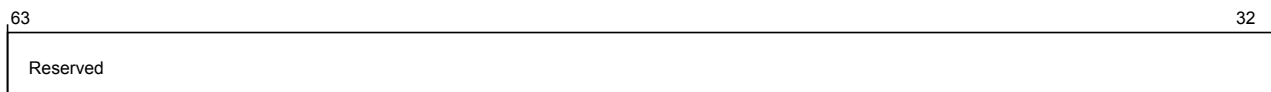


Figure 4-680 por_mxp_por_mxp_p0_qos_control (high)

The following table shows the por_mxp_p0_qos_control higher register bit assignments.

Table 4-697 por_mxp_por_mxp_p0_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

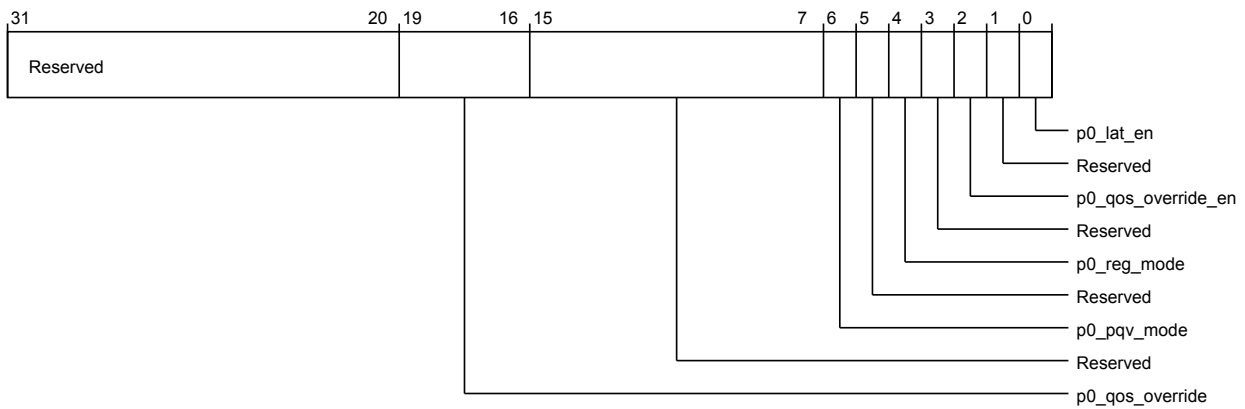


Figure 4-681 `por_mxp_por_mxp_p0_qos_control` (low)

The following table shows the `por_mxp_p0_qos_control` lower register bit assignments.

Table 4-698 `por_mxp_por_mxp_p0_qos_control` (low)

Bits	Field name	Description	Type	Reset
31:20	Reserved	Reserved	RO	-
19:16	<code>p0_qos_override</code>	QoS override value for port 0	RW	4'b0000
15:7	Reserved	Reserved	RO	-
6	<code>p0_pqv_mode</code>	Configures the QoS regulator mode during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	Reserved	Reserved	RO	-
4	<code>p0_reg_mode</code>	Configures the QoS regulator mode 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	Reserved	Reserved	RO	-
2	<code>p0_qos_override_en</code>	Enables port 0 QoS override; when set, allows QoS value on inbound transactions to be overridden	RW	1'b0
1	Reserved	Reserved	RO	-
0	<code>p0_lat_en</code>	Enables port 0 QoS regulation when set	RW	1'b0

`por_mxp_p0_qos_lat_tgt`

Controls QoS target latency/period (in cycles) for regulation of devices connected to port 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA88
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_mxp_secure_register_groups_override.qos

The following image shows the higher register bit assignments.



Figure 4-682 por_mxp_por_mxp_p0_qos_lat_tgt (high)

The following table shows the por_mxp_p0_qos_lat_tgt higher register bit assignments.

Table 4-699 por_mxp_por_mxp_p0_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

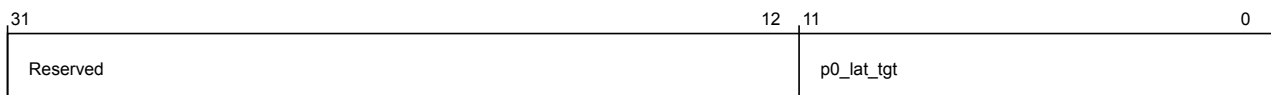


Figure 4-683 por_mxp_por_mxp_p0_qos_lat_tgt (low)

The following table shows the por_mxp_p0_qos_lat_tgt lower register bit assignments.

Table 4-700 por_mxp_por_mxp_p0_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:0	p0_lat_tgt	Port 0 transaction target latency/period; a value of 0 corresponds to no regulation	RW	12'h000

por_mxp_p0_qos_lat_scale

Controls the QoS target scale factor for devices connected to port 0. The scale factor is represented in powers of two from the range 2^{-3} to 2^{-10} .

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hA90
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

Secure group `por_mxp_secure_register_groups_override.qos` override

The following image shows the higher register bit assignments.



Figure 4-684 `por_mxp_por_mxp_p0_qos_lat_scale` (high)

The following table shows the `por_mxp_p0_qos_lat_scale` higher register bit assignments.

Table 4-701 `por_mxp_por_mxp_p0_qos_lat_scale` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

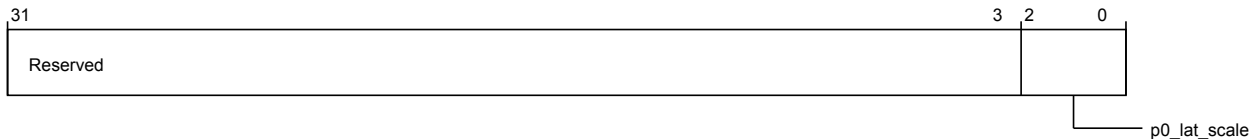


Figure 4-685 `por_mxp_por_mxp_p0_qos_lat_scale` (low)

The following table shows the `por_mxp_p0_qos_lat_scale` lower register bit assignments.

Table 4-702 `por_mxp_por_mxp_p0_qos_lat_scale` (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2:0	<code>p0_lat_scale</code>	Port 0 QoS scale factor 3'b000: $2^{(-3)}$ 3'b001: $2^{(-4)}$ 3'b010: $2^{(-5)}$ 3'b011: $2^{(-6)}$ 3'b100: $2^{(-7)}$ 3'b101: $2^{(-8)}$ 3'b110: $2^{(-9)}$ 3'b111: $2^{(-10)}$	RW	3'h0

`por_mxp_p0_qos_lat_range`

Controls the minimum and maximum QoS values generated by the QoS regulator for devices connected to port 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA98
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_mxp_secure_register_groups_override.qos

The following image shows the higher register bit assignments.

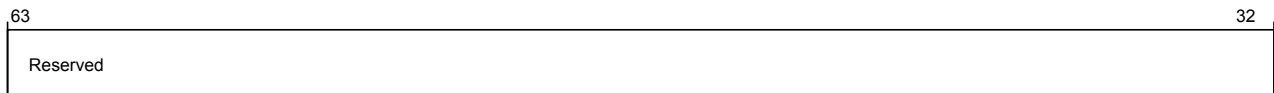


Figure 4-686 por_mxp_por_mxp_p0_qos_lat_range (high)

The following table shows the por_mxp_p0_qos_lat_range higher register bit assignments.

Table 4-703 por_mxp_por_mxp_p0_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

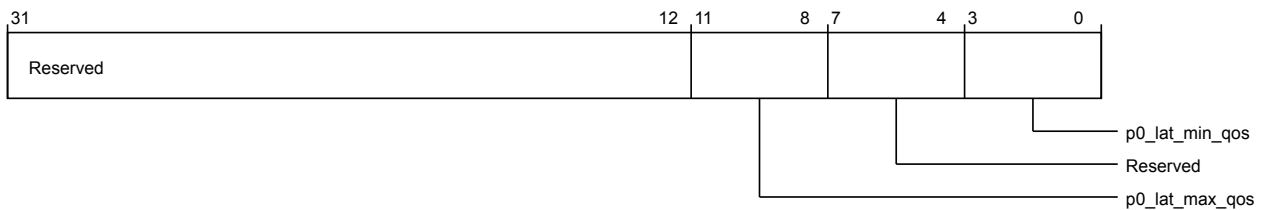


Figure 4-687 por_mxp_por_mxp_p0_qos_lat_range (low)

The following table shows the por_mxp_p0_qos_lat_range lower register bit assignments.

Table 4-704 por_mxp_por_mxp_p0_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	p0_lat_max_qos	Port 0 QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	p0_lat_min_qos	Port 0 QoS minimum value	RW	4'h0

por_mxp_p1_qos_control

Controls QoS settings for devices connected to port 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAA0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_mxp_secure_register_groups_override.qos

The following image shows the higher register bit assignments.

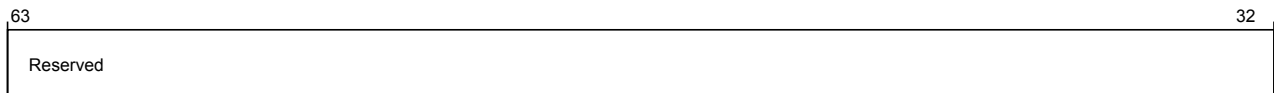


Figure 4-688 por_mxp_por_mxp_p1_qos_control (high)

The following table shows the por_mxp_p1_qos_control higher register bit assignments.

Table 4-705 por_mxp_por_mxp_p1_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

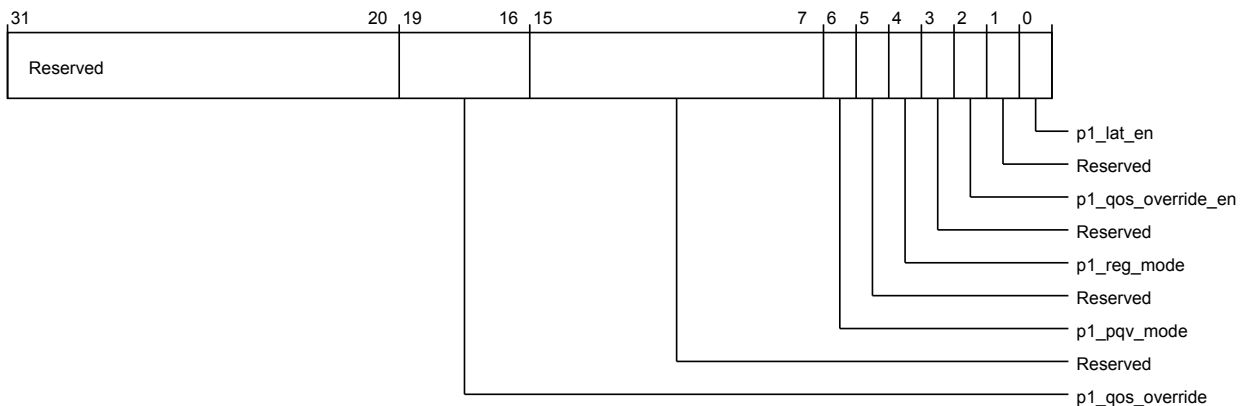


Figure 4-689 por_mxp_por_mxp_p1_qos_control (low)

The following table shows the por_mxp_p1_qos_control lower register bit assignments.

Table 4-706 por_mxp_por_mxp_p1_qos_control (low)

Bits	Field name	Description	Type	Reset
31:20	Reserved	Reserved	RO	-
19:16	p1_qos_override	QoS override value for port 1	RW	4'b0000
15:7	Reserved	Reserved	RO	-

Table 4-706 `por_mxp_por_mxp_p1_qos_control` (low) (continued)

Bits	Field name	Description	Type	Reset
6	<code>p1_pqv_mode</code>	Configures the QoS regulator mode during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	Reserved	Reserved	RO	-
4	<code>p1_reg_mode</code>	Configures the QoS regulator mode 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	Reserved	Reserved	RO	-
2	<code>p1_qos_override_en</code>	Enables port 1 QoS override; when set, allows QoS value on inbound transactions to be overridden	RW	1'b0
1	Reserved	Reserved	RO	-
0	<code>p1_lat_en</code>	Enables port 1 QoS regulation when set	RW	1'b0

`por_mxp_p1_qos_lat_tgt`

Controls QoS target latency/period (in cycles) for regulation of devices connected to port 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAA8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_mxp_secure_register_groups_override.qos</code>

The following image shows the higher register bit assignments.

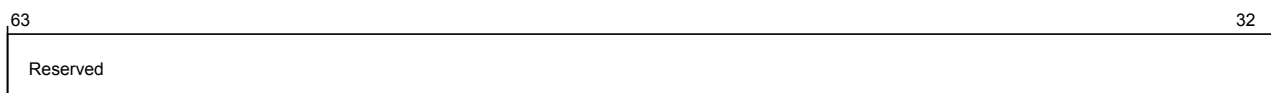


Figure 4-690 `por_mxp_por_mxp_p1_qos_lat_tgt` (high)

The following table shows the `por_mxp_p1_qos_lat_tgt` higher register bit assignments.

Table 4-707 `por_mxp_por_mxp_p1_qos_lat_tgt` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.



Figure 4-691 por_mxp_por_mxp_p1_qos_lat_tgt (low)

The following table shows the por_mxp_p1_qos_lat_tgt lower register bit assignments.

Table 4-708 por_mxp_por_mxp_p1_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:0	p1_lat_tgt	Port 1 transaction target latency/period; a value of 0 corresponds to no regulation	RW	12'h000

por_mxp_p1_qos_lat_scale

Controls the QoS target scale factor for devices connected to port 1. The scale factor is represented in powers of two from the range $2^{(-3)}$ to $2^{(-10)}$.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAB0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_mxp_secure_register_groups_override.qos

The following image shows the higher register bit assignments.

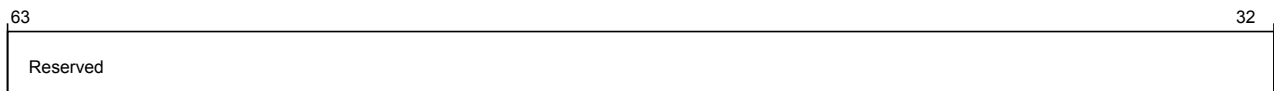


Figure 4-692 por_mxp_por_mxp_p1_qos_lat_scale (high)

The following table shows the por_mxp_p1_qos_lat_scale higher register bit assignments.

Table 4-709 por_mxp_por_mxp_p1_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

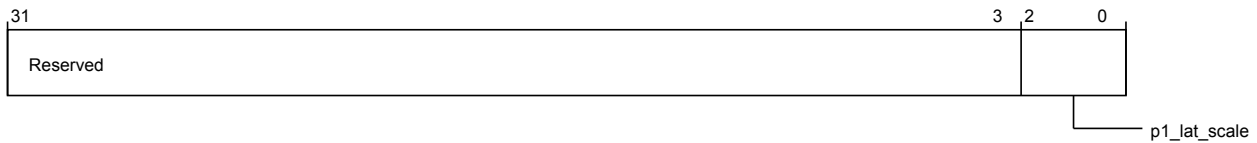


Figure 4-693 `por_mxp_por_mxp_p1_qos_lat_scale` (low)

The following table shows the `por_mxp_p1_qos_lat_scale` lower register bit assignments.

Table 4-710 `por_mxp_por_mxp_p1_qos_lat_scale` (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2:0	<code>p1_lat_scale</code>	Port 1 QoS scale factor 3'b000: $2^{(-3)}$ 3'b001: $2^{(-4)}$ 3'b010: $2^{(-5)}$ 3'b011: $2^{(-6)}$ 3'b100: $2^{(-7)}$ 3'b101: $2^{(-8)}$ 3'b110: $2^{(-9)}$ 3'b111: $2^{(-10)}$	RW	3'h0

`por_mxp_p1_qos_lat_range`

Controls the minimum and maximum QoS values generated by the QoS regulator for devices connected to port 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAB8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_mxp_secure_register_groups_override.qos</code>

The following image shows the higher register bit assignments.

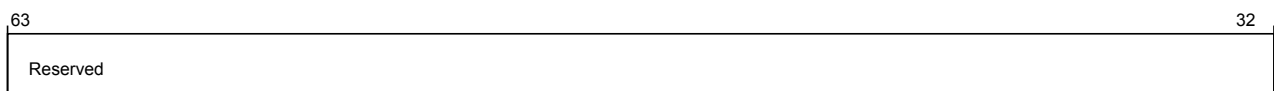


Figure 4-694 `por_mxp_por_mxp_p1_qos_lat_range` (high)

The following table shows the `por_mxp_p1_qos_lat_range` higher register bit assignments.

Table 4-711 `por_mxp_por_mxp_p1_qos_lat_range` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

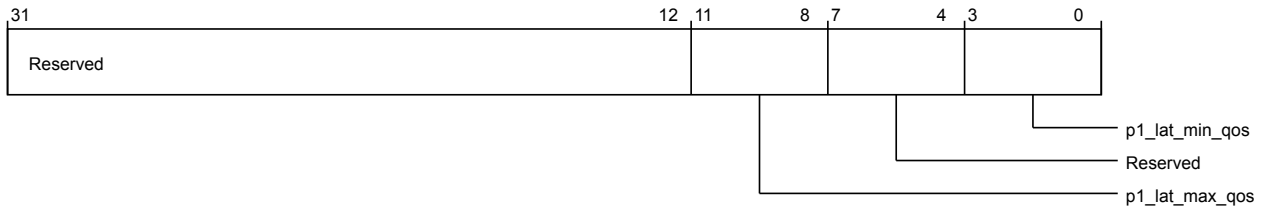


Figure 4-695 `por_mxp_por_mxp_p1_qos_lat_range` (low)

The following table shows the `por_mxp_p1_qos_lat_range` lower register bit assignments.

Table 4-712 `por_mxp_por_mxp_p1_qos_lat_range` (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	<code>p1_lat_max_qos</code>	Port 1 QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	<code>p1_lat_min_qos</code>	Port 1 QoS minimum value	RW	4'h0

`por_mxp_pmu_event_sel`

Specifies the PMU event to be counted.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2000

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

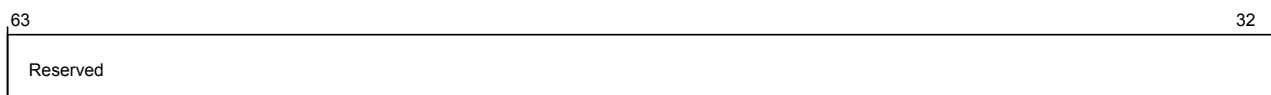


Figure 4-696 `por_mxp_por_mxp_pmu_event_sel` (high)

The following table shows the `por_mxp_pmu_event_sel` higher register bit assignments.

Table 4-713 `por_mxp_por_mxp_pmu_event_sel` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

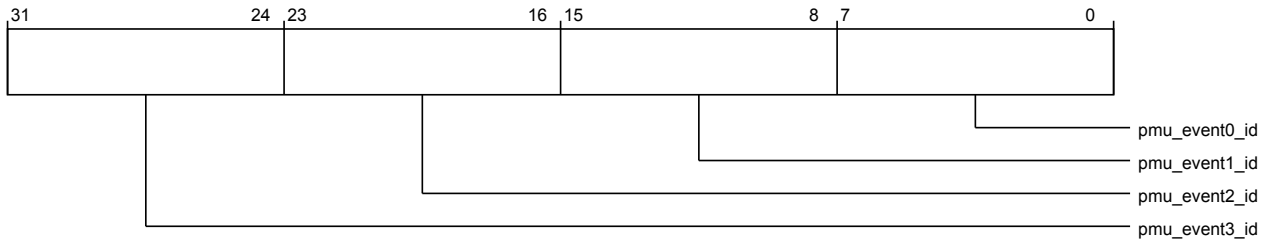


Figure 4-697 `por_mxp_por_mxp_pmu_event_sel` (low)

The following table shows the `por_mxp_pmu_event_sel` lower register bit assignments.

Table 4-714 `por_mxp_por_mxp_pmu_event_sel` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>pmu_event3_id</code>	XP PMU Event 3 ID; see <code>pmu_event0_id</code> for encodings	RW	8'b0
23:16	<code>pmu_event2_id</code>	XP PMU Event 2 ID; see <code>pmu_event0_id</code> for encodings	RW	8'b0
15:8	<code>pmu_event1_id</code>	XP PMU Event 1 ID; see <code>pmu_event0_id</code> for encodings	RW	8'b0
7:0	<code>pmu_event0_id</code>	XP PMU Event 0 ID Bits [7:5]: PC 3'b000: REQ 3'b001: RSP 3'b010: SNP 3'b011: DAT Bits [4:2]: Interface 3'b000: East 3'b001: West 3'b010: North 3'b011: South 3'b100: Device port 0 3'b101: Device port 1 Bits [1:0]: Event specifier 2'b00: No event 2'b01: TX flit valid; signaled when a flit is successfully transmitted 2'b10: TX flit stall; signaled when flit transmission is stalled and waiting on credits 2'b11: Partial DAT flit; signaled when 128-bit DAT flits could not be merged into a 256-bit DAT flit; only applicable on the DAT PC on RN-F CHIA and RN-F CHIA ESAM ports	RW	8'b0

por_mxp_errfr

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3000
Register reset	64'b0000010100101
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

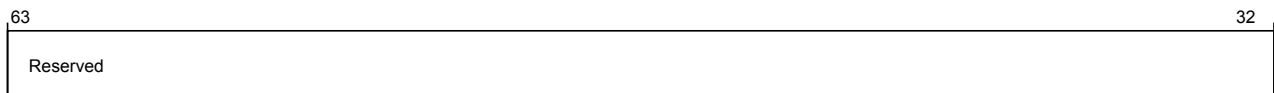


Figure 4-698 por_mxp_errfr (high)

The following table shows the por_mxp_errfr higher register bit assignments.

Table 4-715 por_mxp_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

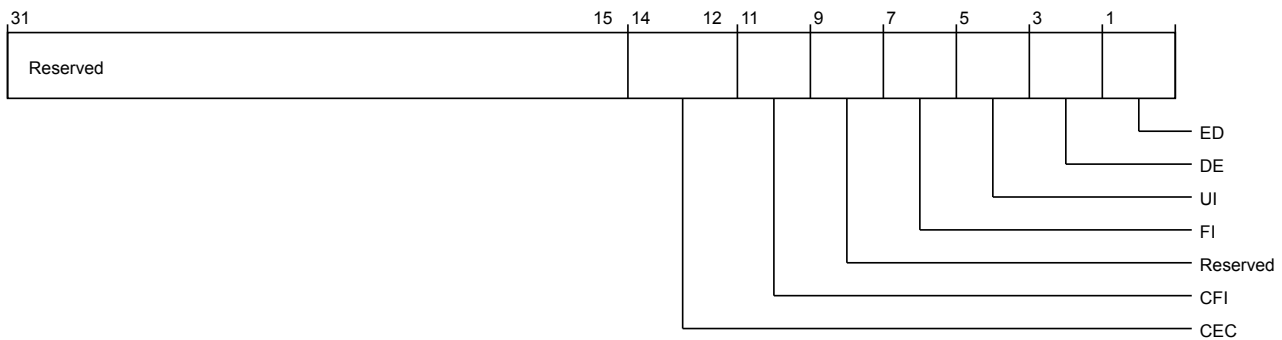


Figure 4-699 por_mxp_errfr (low)

The following table shows the por_mxp_errfr lower register bit assignments.

Table 4-716 por_mxp_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000

Table 4-716 por_mxp_por_mxp_errfr (low) (continued)

Bits	Field name	Description	Type	Reset
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_mxp_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3008
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

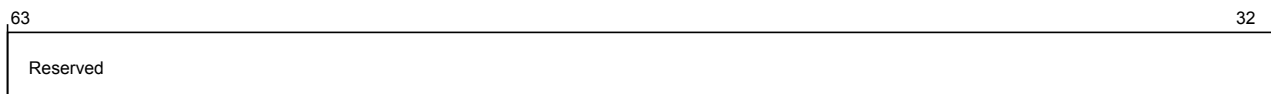


Figure 4-700 por_mxp_por_mxp_errctlr (high)

The following table shows the por_mxp_errctlr higher register bit assignments.

Table 4-717 por_mxp_por_mxp_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

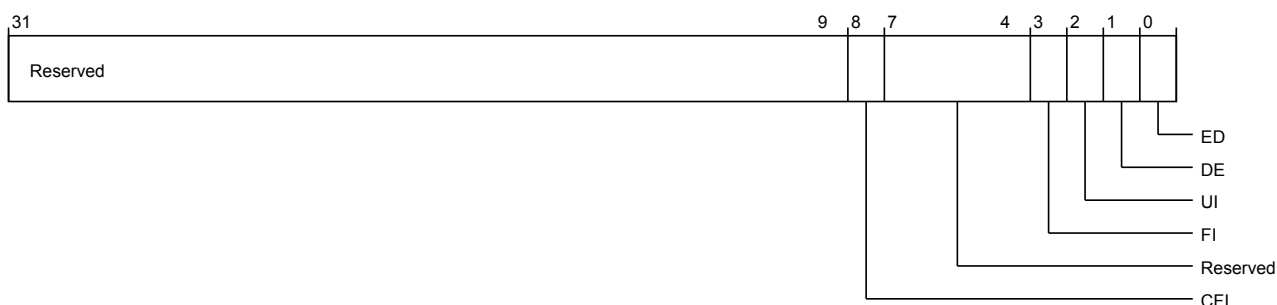


Figure 4-701 `por_mxp_errctlr (low)`

The following table shows the `por_mxp_errctlr` lower register bit assignments.

Table 4-718 `por_mxp_errctlr (low)`

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in <code>por_mxp_errfr.CFI</code>	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in <code>por_mxp_errfr.FI</code>	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in <code>por_mxp_errfr.UI</code>	RW	1'b0
1	DE	Enables error deferment as specified in <code>por_mxp_errfr.DE</code>	RW	1'b0
0	ED	Enables error detection as specified in <code>por_mxp_errfr.ED</code>	RW	1'b0

`por_mxp_errstatus`

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3010
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

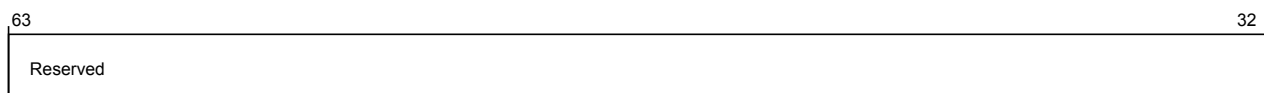


Figure 4-702 `por_mxp_errstatus (high)`

The following table shows the `por_mxp_errstatus` higher register bit assignments.

Table 4-719 por_mxp_por_mxp_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

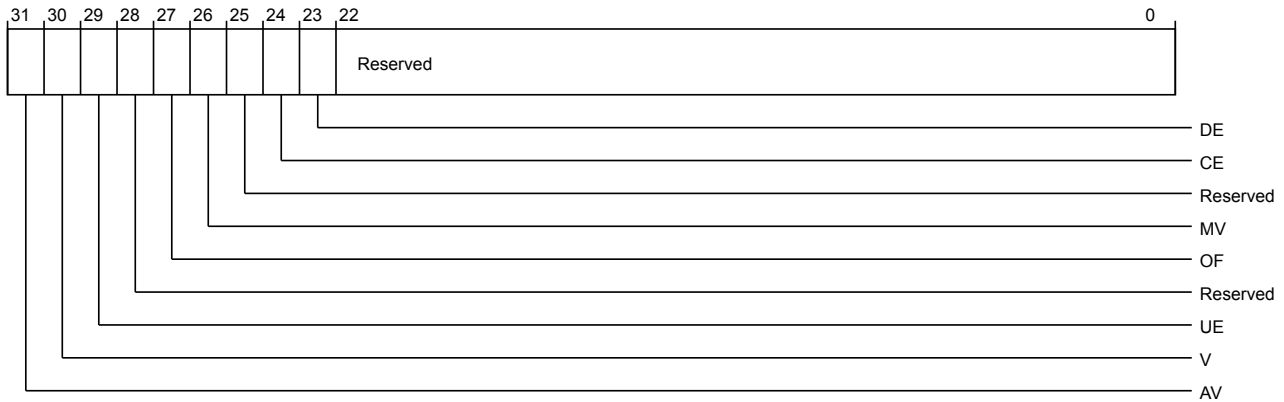


Figure 4-703 por_mxp_por_mxp_errstatus (low)

The following table shows the por_mxp_errstatus lower register bit assignments.

Table 4-720 por_mxp_por_mxp_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0

Table 4-720 por_mxp_por_mxp_errstatus (low) (continued)

Bits	Field name	Description	Type	Reset
26	MV	por_mxp_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_mxp_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3028

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

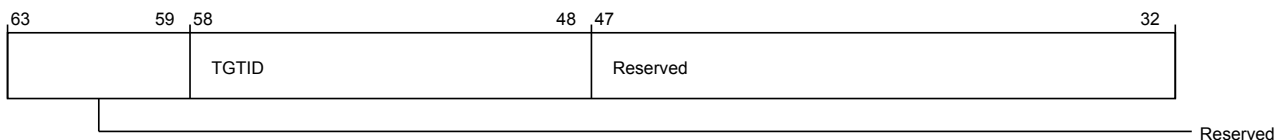


Figure 4-704 por_mxp_por_mxp_errmisc (high)

The following table shows the por_mxp_errmisc higher register bit assignments.

Table 4-721 por_mxp_por_mxp_errmisc (high)

Bits	Field name	Description	Type	Reset
63:59	Reserved	Reserved	RO	-
58:48	TGTID	Error flit target ID	RW	11'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

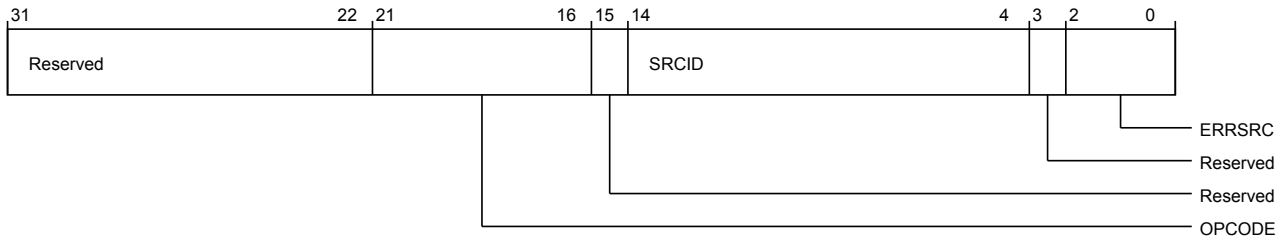


Figure 4-705 por_mxp_por_mxp_errmisc (low)

The following table shows the `por_mxp_errmisc` lower register bit assignments.

Table 4-722 por_mxp_por_mxp_errmisc (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21:16	OPCODE	Error flit opcode	RW	6'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error flit source ID	RW	11'b0
3	Reserved	Reserved	RO	-
2:0	ERRSRC	Error source Bits [2:1]: Transaction type 2'b00: REQ 2'b01: RSP 2'b10: SNP 2'b11: DAT Bit [0]: Port 1'b0: Port 0 1'b1: Port 1	RW	3'b0

por_mxp_p0_byte_par_err_inj

Functions as the byte parity error injection register for XP port 0.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 14'h3030
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

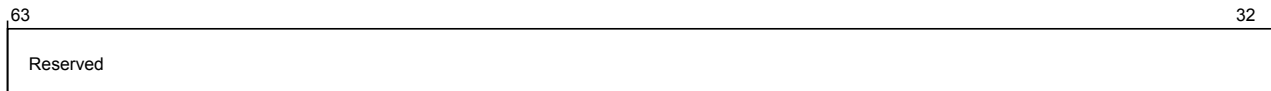


Figure 4-706 `por_mxp_por_mxp_p0_byte_par_err_inj` (high)

The following table shows the `por_mxp_p0_byte_par_err_inj` higher register bit assignments.

Table 4-723 `por_mxp_por_mxp_p0_byte_par_err_inj` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

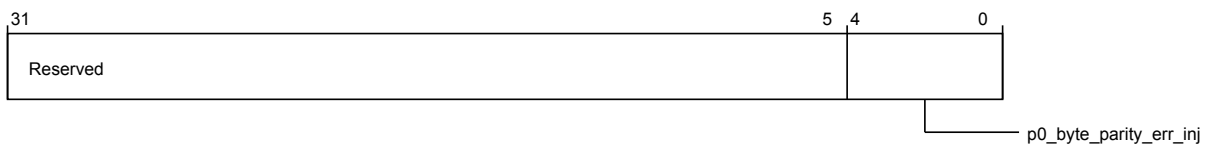


Figure 4-707 `por_mxp_por_mxp_p0_byte_par_err_inj` (low)

The following table shows the `por_mxp_p0_byte_par_err_inj` lower register bit assignments.

Table 4-724 `por_mxp_por_mxp_p0_byte_par_err_inj` (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4:0	<code>p0_byte_parity_err_inj</code>	Specifies a byte lane; once this register is written, a byte parity error is injected in the specified byte lane on the next DAT flit upload NOTE: Only applicable if an RN-F is attached to port 0. Byte parity error is only injected if the RN-F is configured to not support Datacheck.	WO	5'h00

`por_mxp_p1_byte_par_err_inj`

Functions as the byte parity error injection register for XP port 1.

Its characteristics are:

Type WO
Register width (Bits) 64

Address offset 14'h3038
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-708 `por_mxp_por_mxp_p1_byte_par_err_inj` (high)

The following table shows the `por_mxp_p1_byte_par_err_inj` higher register bit assignments.

Table 4-725 `por_mxp_por_mxp_p1_byte_par_err_inj` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

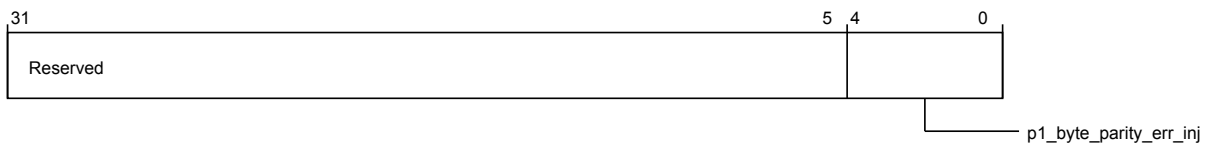


Figure 4-709 `por_mxp_por_mxp_p1_byte_par_err_inj` (low)

The following table shows the `por_mxp_p1_byte_par_err_inj` lower register bit assignments.

Table 4-726 `por_mxp_por_mxp_p1_byte_par_err_inj` (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4:0	<code>p1_byte_parity_err_inj</code>	Specifies a byte lane; once this register is written, a byte parity error is injected in the specified byte lane on the next DAT flit upload NOTE: Only applicable if an RN-F is attached to port 0. Byte parity error is only injected if the RN-F is configured to not support Datacheck.	WO	5'h00

`por_mxp_errfr_NS`

Functions as the non-secure error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3100
Register reset 64'b00000010100101
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-710 por_mxp_errfr_NS (high)

The following table shows the por_mxp_errfr_NS higher register bit assignments.

Table 4-727 por_mxp_errfr_NS (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

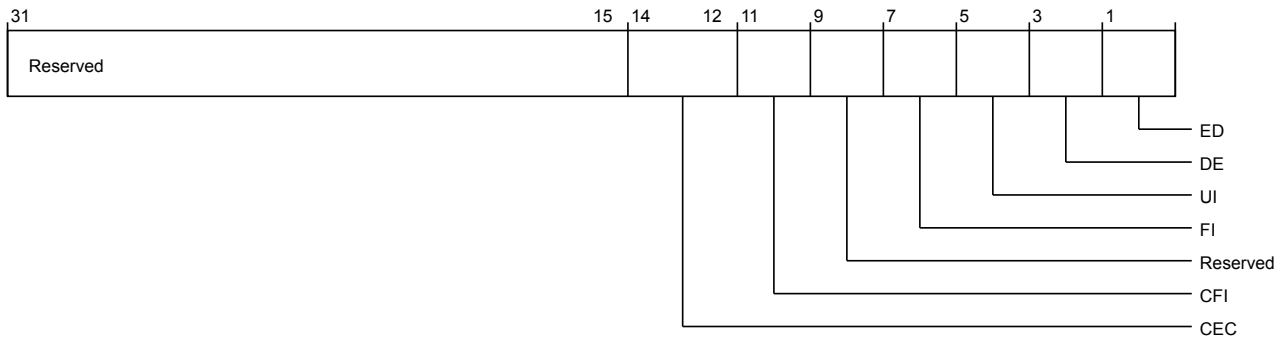


Figure 4-711 por_mxp_errfr_NS (low)

The following table shows the por_mxp_errfr_NS lower register bit assignments.

Table 4-728 por_mxp_errfr_NS (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_mxp_errctlr_NS

Functions as the non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3108
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

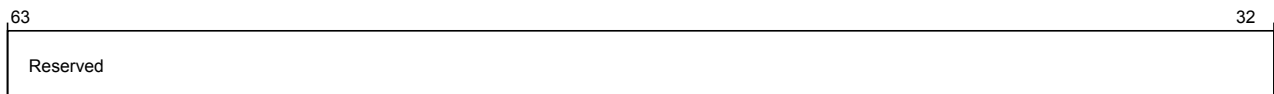


Figure 4-712 por_mxp_errctlr_ns (high)

The following table shows the por_mxp_errctlr_NS higher register bit assignments.

Table 4-729 por_mxp_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

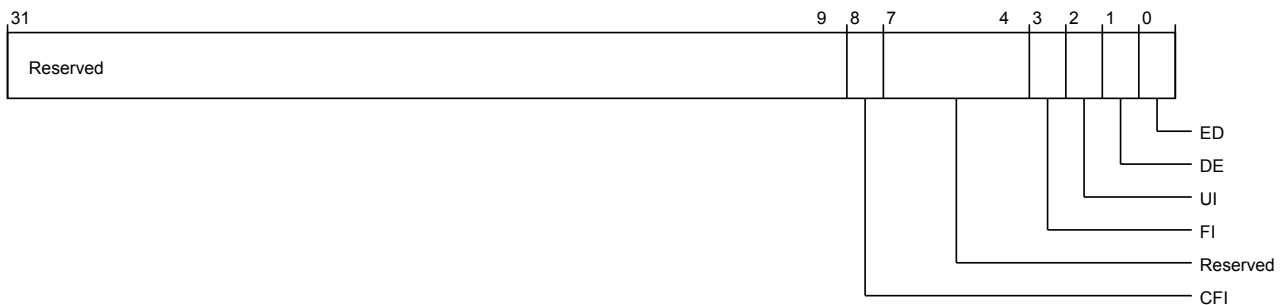


Figure 4-713 por_mxp_errctlr_ns (low)

The following table shows the por_mxp_errctlr_NS lower register bit assignments.

Table 4-730 por_mxp_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_mxp_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-

Table 4-730 `por_mxp_por_mxp_errctlr_ns` (low) (continued)

Bits	Field name	Description	Type	Reset
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in <code>por_mxp_errfr_NS.FI</code>	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in <code>por_mxp_errfr_NS.UI</code>	RW	1'b0
1	DE	Enables error deferment as specified in <code>por_mxp_errfr_NS.DE</code>	RW	1'b0
0	ED	Enables error detection as specified in <code>por_mxp_errfr_NS.ED</code>	RW	1'b0

`por_mxp_errstatus_NS`

Functions as the non-secure error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3110
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

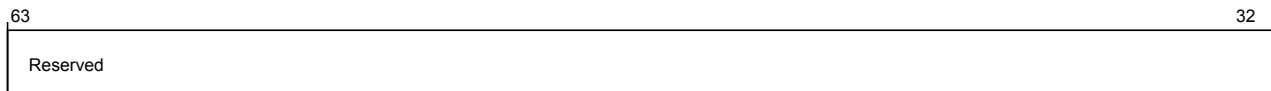


Figure 4-714 `por_mxp_por_mxp_errstatus_ns` (high)

The following table shows the `por_mxp_errstatus_NS` higher register bit assignments.

Table 4-731 `por_mxp_por_mxp_errstatus_ns` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.



Figure 4-715 `por_mxp_por_mxp_errstatus_ns` (low)

The following table shows the `por_mxp_errstatus_NS` lower register bit assignments.

Table 4-732 `por_mxp_por_mxp_errstatus_ns` (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	<code>por_mxp_errmisc_NS</code> valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 4-732 por_mxp_por_mxp_errstatus_ns (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_mxp_errmisc_NS

Functions as the non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3128

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

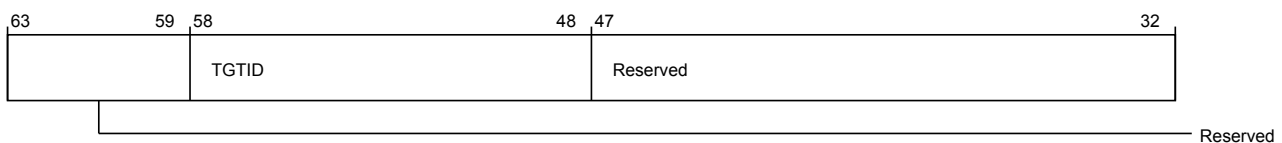


Figure 4-716 por_mxp_por_mxp_errmisc_ns (high)

The following table shows the por_mxp_errmisc_NS higher register bit assignments.

Table 4-733 por_mxp_por_mxp_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63:59	Reserved	Reserved	RO	-
58:48	TGTID	Error flit target ID	RW	11'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

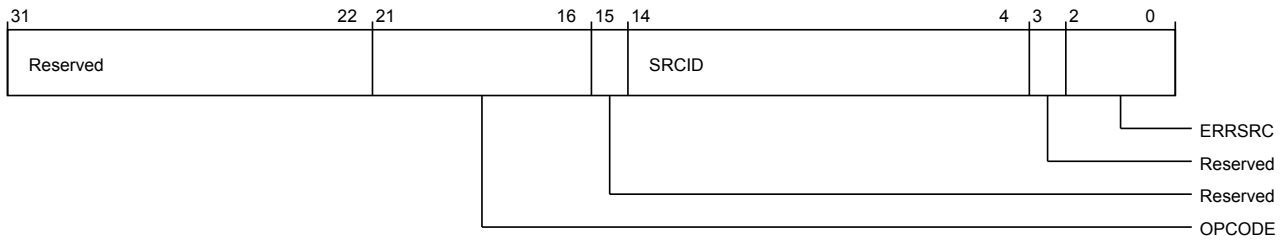


Figure 4-717 por_mxp_errmisc_NS (low)

The following table shows the por_mxp_errmisc_NS lower register bit assignments.

Table 4-734 por_mxp_errmisc_NS (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21:16	OPCODE	Error flit opcode	RW	6'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error flit source ID	RW	11'b0
3	Reserved	Reserved	RO	-
2:0	ERRSRC	Error source Bits [2:1]: Transaction type 2'b00: REQ 2'b01: RSP 2'b10: SNP 2'b11: DAT Bit [0]: Port 1'b0: Port 0 1'b1: Port 1	RW	3'b0

por_mxp_p0_syscoreq_ctl

Functions as the port 0 snoop and DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p0_syscoack_status. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1000
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

Secure group override

por_mxp_secure_register_groups_override.syscoreq_ctl

The following image shows the higher register bit assignments.

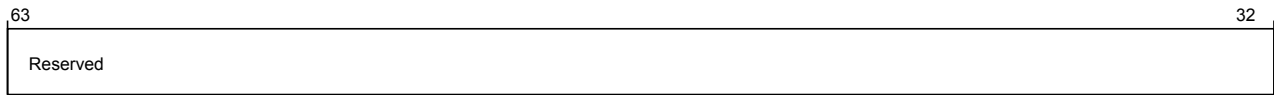


Figure 4-718 por_mxp_por_mxp_p0_syscoreq_ctl (high)

The following table shows the por_mxp_p0_syscoreq_ctl higher register bit assignments.

Table 4-735 por_mxp_por_mxp_p0_syscoreq_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

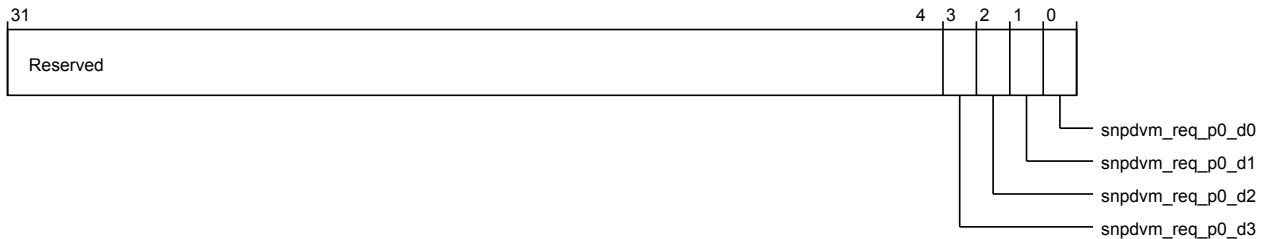


Figure 4-719 por_mxp_por_mxp_p0_syscoreq_ctl (low)

The following table shows the por_mxp_p0_syscoreq_ctl lower register bit assignments.

Table 4-736 por_mxp_por_mxp_p0_syscoreq_ctl (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	snpdvm_req_p0_d3	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 3 on port 0	RW	1'b0
2	snpdvm_req_p0_d2	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 2 on port 0	RW	1'b0
1	snpdvm_req_p0_d1	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 1 on port 0	RW	1'b0
0	snpdvm_req_p0_d0	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 0 on port 0	RW	1'b0

por_mxp_p1_syscoreq_ctl

Functions as the port 1 snoop and DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p1_syscoack_status. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1008
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_mxp_secure_register_groups_override.syscoreq_ctl

The following image shows the higher register bit assignments.

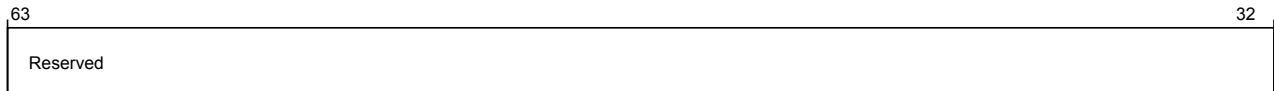


Figure 4-720 por_mxp_por_mxp_p1_syscoreq_ctl (high)

The following table shows the por_mxp_p1_syscoreq_ctl higher register bit assignments.

Table 4-737 por_mxp_por_mxp_p1_syscoreq_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

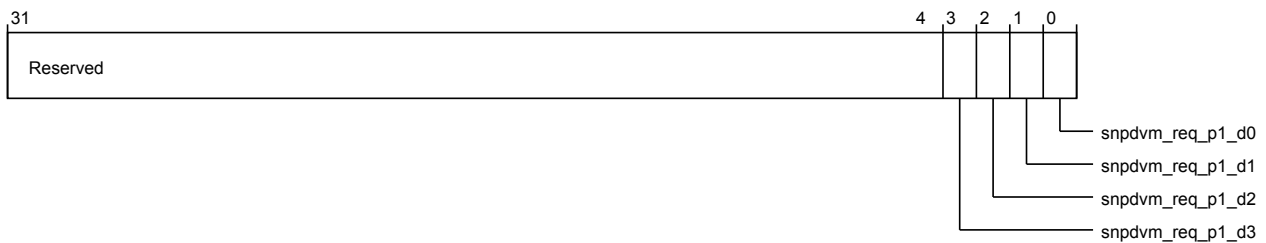


Figure 4-721 por_mxp_por_mxp_p1_syscoreq_ctl (low)

The following table shows the por_mxp_p1_syscoreq_ctl lower register bit assignments.

Table 4-738 por_mxp_por_mxp_p1_syscoreq_ctl (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	snpdvm_req_p1_d3	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 3 on port 1	RW	1'b0
2	snpdvm_req_p1_d2	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 2 on port 1	RW	1'b0

Table 4-738 `por_mxp_por_mxp_p1_syscoreq_ctl` (low) (continued)

Bits	Field name	Description	Type	Reset
1	<code>snpdvm_req_p1_d1</code>	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 1 on port 1	RW	1'b0
0	<code>snpdvm_req_p1_d0</code>	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 0 on port 1	RW	1'b0

`por_mxp_p0_syscoack_status`

Functions as the port 0 snoop and DVM domain status register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with `por_mxp_p0_syscoreq_ctl`. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h1010
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_mxp_secure_register_groups_override.syscoreq_ctl</code>

The following image shows the higher register bit assignments.



Figure 4-722 `por_mxp_por_mxp_p0_syscoack_status` (high)

The following table shows the `por_mxp_p0_syscoack_status` higher register bit assignments.

Table 4-739 `por_mxp_por_mxp_p0_syscoack_status` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

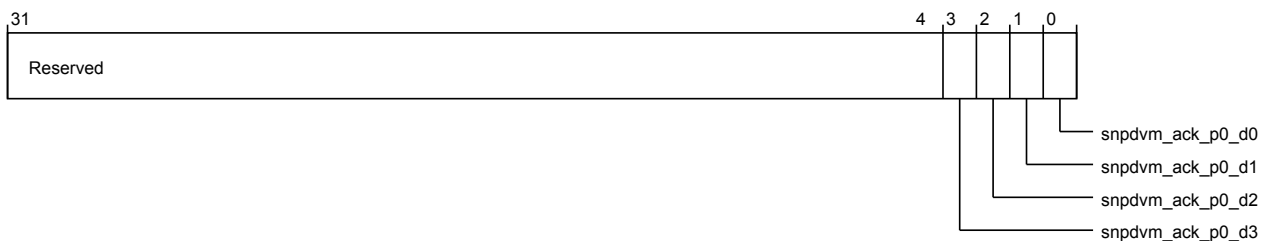


Figure 4-723 `por_mxp_por_mxp_p0_syscoack_status` (low)

The following table shows the `por_mxp_p0_syscoack_status` lower register bit assignments.

Table 4-740 `por_mxp_por_mxp_p0_syscoack_status` (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	<code>snpdvm_ack_p0_d3</code>	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 3 on port 0	RO	1'b0
2	<code>snpdvm_ack_p0_d2</code>	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 2 on port 0	RO	1'b0
1	<code>snpdvm_ack_p0_d1</code>	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 1 on port 0	RO	1'b0
0	<code>snpdvm_ack_p0_d0</code>	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 0 on port 0	RO	1'b0

`por_mxp_p1_syscoack_status`

Functions as the port 1 snoop and DVM domain status register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with `por_mxp_p1_syscoreq_ctl`. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h1018
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_mxp_secure_register_groups_override.syscoreq_ctl</code>

The following image shows the higher register bit assignments.

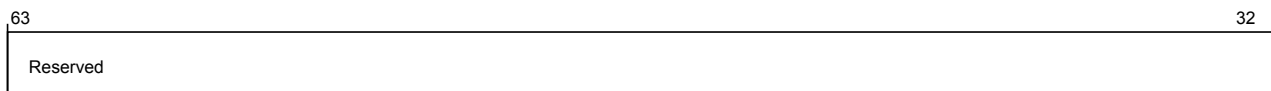


Figure 4-724 `por_mxp_por_mxp_p1_syscoack_status` (high)

The following table shows the `por_mxp_p1_syscoack_status` higher register bit assignments.

Table 4-741 `por_mxp_por_mxp_p1_syscoack_status` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

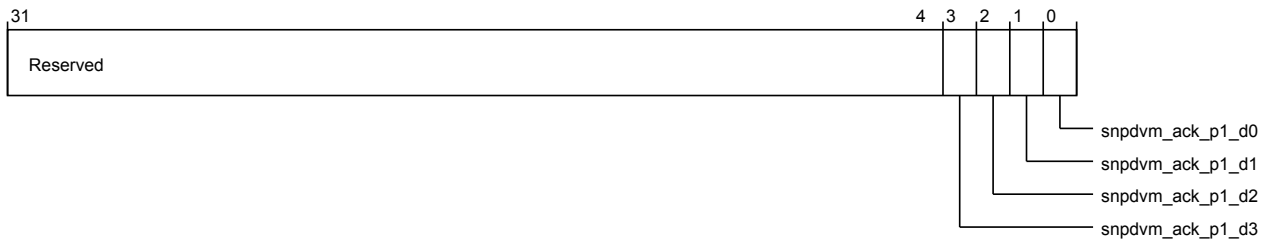


Figure 4-725 `por_mxp_por_mxp_p1_syscoack_status` (low)

The following table shows the `por_mxp_p1_syscoack_status` lower register bit assignments.

Table 4-742 `por_mxp_por_mxp_p1_syscoack_status` (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	<code>snpdvm_ack_p1_d3</code>	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 3 on port 1	RO	1'b0
2	<code>snpdvm_ack_p1_d2</code>	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 2 on port 1	RO	1'b0
1	<code>snpdvm_ack_p1_d1</code>	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 1 on port 1	RO	1'b0
0	<code>snpdvm_ack_p1_d0</code>	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 0 on port 1	RO	1'b0

`por_dtm_control`

Functions as the DTM control register.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2100

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

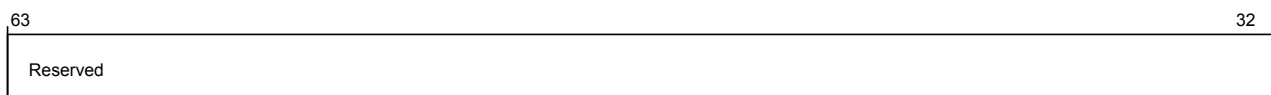


Figure 4-726 `por_mxp_por_dtm_control` (high)

The following table shows the `por_dtm_control` higher register bit assignments.

Table 4-743 por_mxp_por_dtm_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

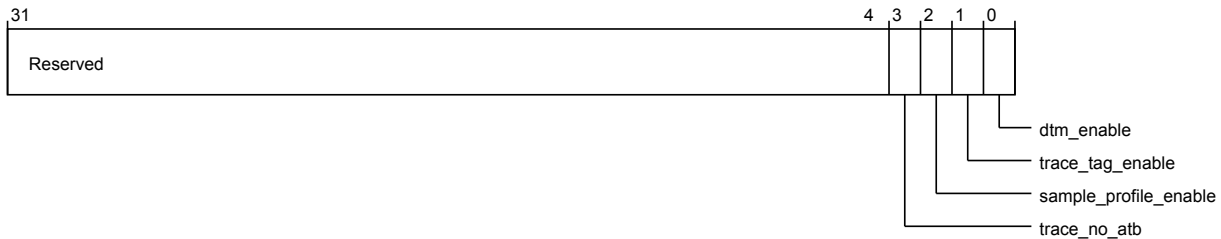


Figure 4-727 por_mxp_por_dtm_control (low)

The following table shows the por_dtm_control lower register bit assignments.

Table 4-744 por_mxp_por_dtm_control (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	trace_no_atb	When set, trace packet is not delivered out of ATB, and FIFO entry holds the first trace packet	RW	1'b0
2	sample_profile_enable	Enables sample profile function	RW	1'b0
1	trace_tag_enable	Watchpoint trace tag enable 1'b1: Trace tag enabled 1'b0: No trace tag	RW	1'b0
0	dtm_enable	Enables debug watchpoint and PMU function; prior to writing this bit, all other DT configuration registers must be programmed; once this bit is set, other DT configuration registers must not be modified	RW	1'b0

por_dtm_fifo_entry_ready

Controls status of DTM FIFO entries.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h2118
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

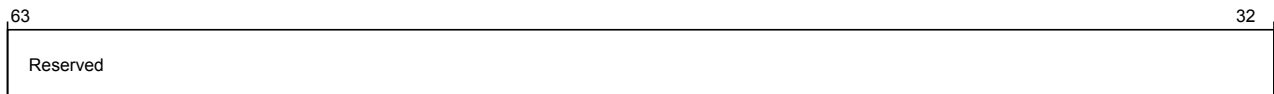


Figure 4-728 `por_mxp_por_dtm_fifo_entry_ready` (high)

The following table shows the `por_dtm_fifo_entry_ready` higher register bit assignments.

Table 4-745 `por_mxp_por_dtm_fifo_entry_ready` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

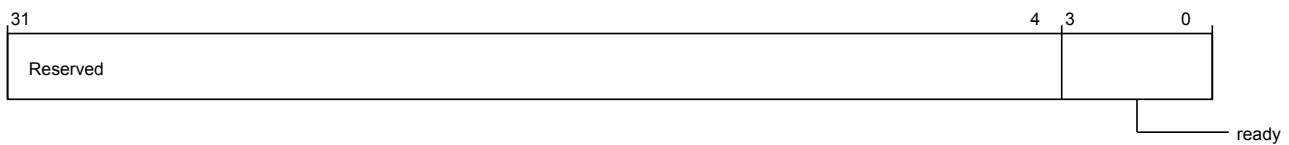


Figure 4-729 `por_mxp_por_dtm_fifo_entry_ready` (low)

The following table shows the `por_dtm_fifo_entry_ready` lower register bit assignments.

Table 4-746 `por_mxp_por_dtm_fifo_entry_ready` (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	ready	Indicates which DTM FIFO entries are ready; write a 1 to clear Bit [3]: Entry 3 ready when set Bit [2]: Entry 2 ready when set Bit [1]: Entry 1 ready when set Bit [0]: Entry 0 ready when set	W1C	4'b0

`por_dtm_fifo_entry0_0`

Contains DTM FIFO entry 0 data.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h2120

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

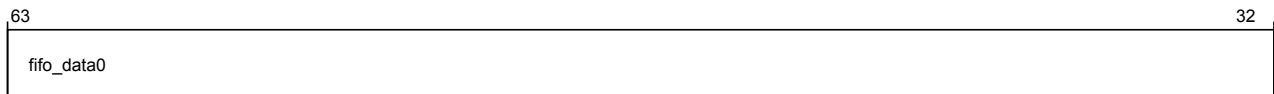


Figure 4-730 `por_mxp_por_dtm_fifo_entry0_0` (high)

The following table shows the `por_dtm_fifo_entry0_0` higher register bit assignments.

Table 4-747 `por_mxp_por_dtm_fifo_entry0_0` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>fifo_data0</code>	Entry data bit vector 63:0	RO	64'b0

The following image shows the lower register bit assignments.

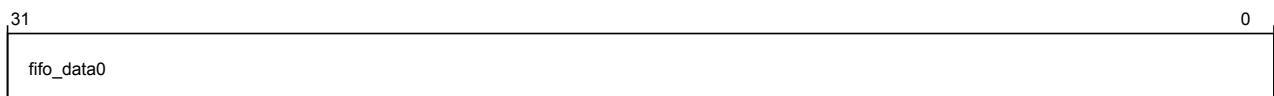


Figure 4-731 `por_mxp_por_dtm_fifo_entry0_0` (low)

The following table shows the `por_dtm_fifo_entry0_0` lower register bit assignments.

Table 4-748 `por_mxp_por_dtm_fifo_entry0_0` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>fifo_data0</code>	Entry data bit vector 63:0	RO	64'b0

`por_dtm_fifo_entry0_1`

Contains DTM FIFO entry 0 data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2128
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

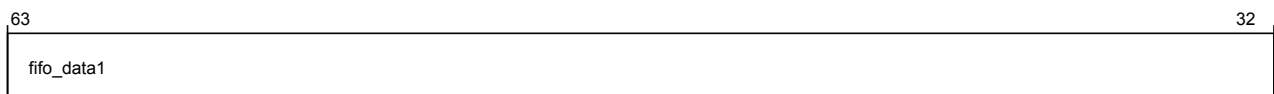


Figure 4-732 `por_mxp_por_dtm_fifo_entry0_1` (high)

The following table shows the `por_dtm_fifo_entry0_1` higher register bit assignments.

Table 4-749 por_mxp_por_dtm_fifo_entry0_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following image shows the lower register bit assignments.



Figure 4-733 por_mxp_por_dtm_fifo_entry0_1 (low)

The following table shows the por_dtm_fifo_entry0_1 lower register bit assignments.

Table 4-750 por_mxp_por_dtm_fifo_entry0_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

por_dtm_fifo_entry0_2

Contains DTM FIFO entry 0 data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2130
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

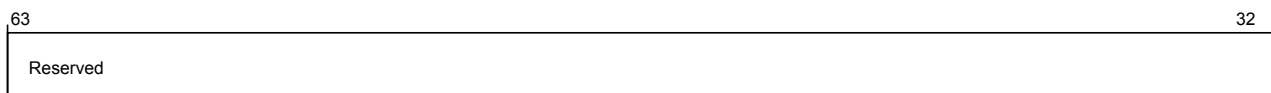


Figure 4-734 por_mxp_por_dtm_fifo_entry0_2 (high)

The following table shows the por_dtm_fifo_entry0_2 higher register bit assignments.

Table 4-751 por_mxp_por_dtm_fifo_entry0_2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

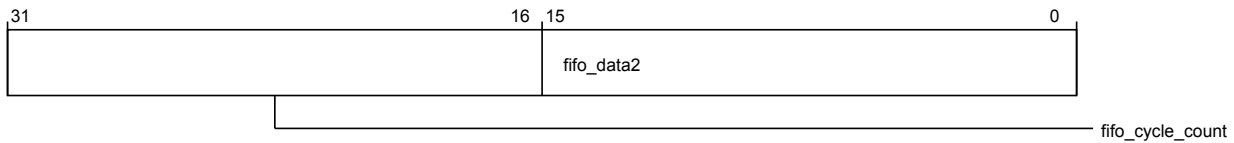


Figure 4-735 por_mxp_por_dtm_fifo_entry0_2 (low)

The following table shows the por_dtm_fifo_entry0_2 lower register bit assignments.

Table 4-752 por_mxp_por_dtm_fifo_entry0_2 (low)

Bits	Field name	Description	Type	Reset
31:16	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
15:0	fifo_data2	Entry data bit vector 143:128	RO	16'b0

por_dtm_fifo_entry1_0

Contains DTM FIFO entry 1 data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2138
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

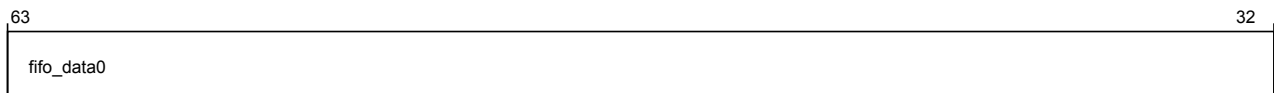


Figure 4-736 por_mxp_por_dtm_fifo_entry1_0 (high)

The following table shows the por_dtm_fifo_entry1_0 higher register bit assignments.

Table 4-753 por_mxp_por_dtm_fifo_entry1_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following image shows the lower register bit assignments.

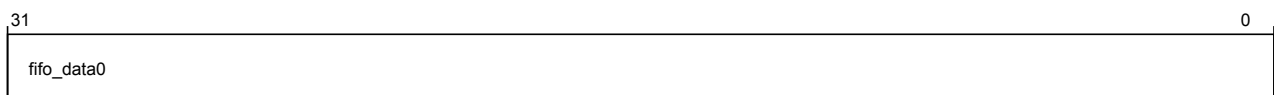


Figure 4-737 por_mxp_por_dtm_fifo_entry1_0 (low)

The following table shows the por_dtm_fifo_entry1_0 lower register bit assignments.

Table 4-754 por_mxp_por_dtm_fifo_entry1_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

por_dtm_fifo_entry1_1

Contains DTM FIFO entry 1 data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2140
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

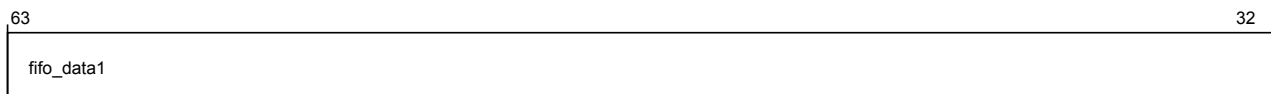


Figure 4-738 por_mxp_por_dtm_fifo_entry1_1 (high)

The following table shows the por_dtm_fifo_entry1_1 higher register bit assignments.

Table 4-755 por_mxp_por_dtm_fifo_entry1_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following image shows the lower register bit assignments.

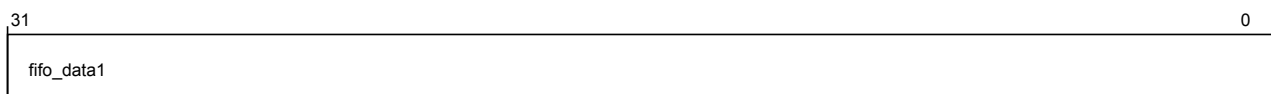


Figure 4-739 por_mxp_por_dtm_fifo_entry1_1 (low)

The following table shows the por_dtm_fifo_entry1_1 lower register bit assignments.

Table 4-756 por_mxp_por_dtm_fifo_entry1_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

por_dtm_fifo_entry1_2

Contains DTM FIFO entry 1 data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2148
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

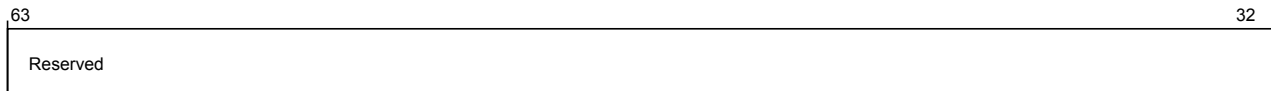


Figure 4-740 por_mxp_por_dtm_fifo_entry1_2 (high)

The following table shows the por_dtm_fifo_entry1_2 higher register bit assignments.

Table 4-757 por_mxp_por_dtm_fifo_entry1_2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

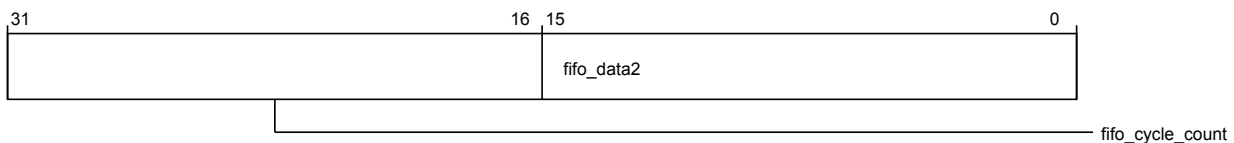


Figure 4-741 por_mxp_por_dtm_fifo_entry1_2 (low)

The following table shows the por_dtm_fifo_entry1_2 lower register bit assignments.

Table 4-758 por_mxp_por_dtm_fifo_entry1_2 (low)

Bits	Field name	Description	Type	Reset
31:16	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
15:0	fifo_data2	Entry data bit vector 143:128	RO	16'b0

por_dtm_fifo_entry2_0

Contains DTM FIFO entry 2 data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2150
Register reset	64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-742 por_mxp_por_dtm_fifo_entry2_0 (high)

The following table shows the por_dtm_fifo_entry2_0 higher register bit assignments.

Table 4-759 por_mxp_por_dtm_fifo_entry2_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following image shows the lower register bit assignments.

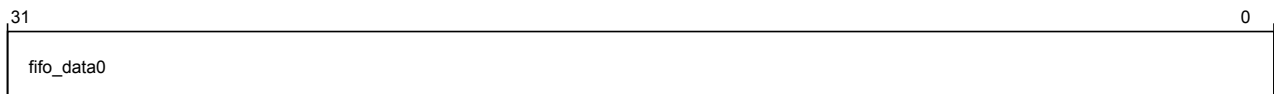


Figure 4-743 por_mxp_por_dtm_fifo_entry2_0 (low)

The following table shows the por_dtm_fifo_entry2_0 lower register bit assignments.

Table 4-760 por_mxp_por_dtm_fifo_entry2_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

por_dtm_fifo_entry2_1

Contains DTM FIFO entry 2 data.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h2158

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-744 por_mxp_por_dtm_fifo_entry2_1 (high)

The following table shows the por_dtm_fifo_entry2_1 higher register bit assignments.

Table 4-761 por_mxp_por_dtm_fifo_entry2_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following image shows the lower register bit assignments.

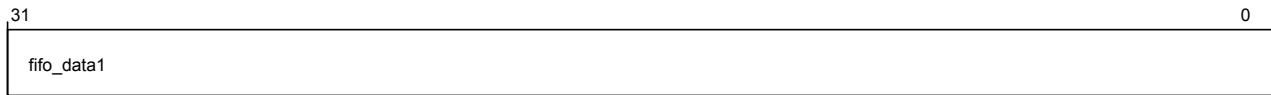


Figure 4-745 por_mxp_por_dtm_fifo_entry2_1 (low)

The following table shows the por_dtm_fifo_entry2_1 lower register bit assignments.

Table 4-762 por_mxp_por_dtm_fifo_entry2_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

por_dtm_fifo_entry2_2

Contains DTM FIFO entry 2 data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2160
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

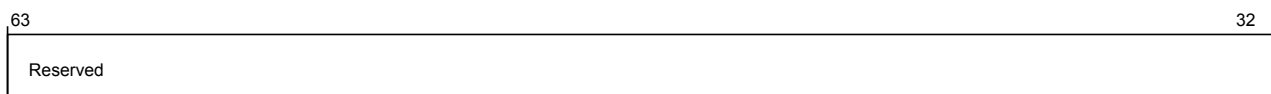


Figure 4-746 por_mxp_por_dtm_fifo_entry2_2 (high)

The following table shows the por_dtm_fifo_entry2_2 higher register bit assignments.

Table 4-763 por_mxp_por_dtm_fifo_entry2_2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

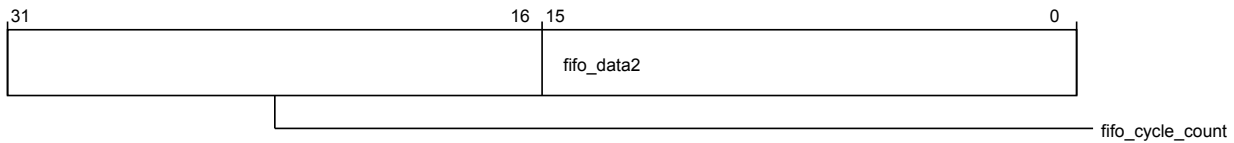


Figure 4-747 por_mxp_por_dtm_fifo_entry2_2 (low)

The following table shows the por_dtm_fifo_entry2_2 lower register bit assignments.

Table 4-764 por_mxp_por_dtm_fifo_entry2_2 (low)

Bits	Field name	Description	Type	Reset
31:16	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
15:0	fifo_data2	Entry data bit vector 143:128	RO	16'b0

por_dtm_fifo_entry3_0

Contains DTM FIFO entry 3 data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2168
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

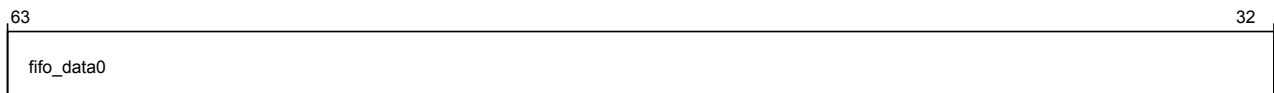


Figure 4-748 por_mxp_por_dtm_fifo_entry3_0 (high)

The following table shows the por_dtm_fifo_entry3_0 higher register bit assignments.

Table 4-765 por_mxp_por_dtm_fifo_entry3_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following image shows the lower register bit assignments.

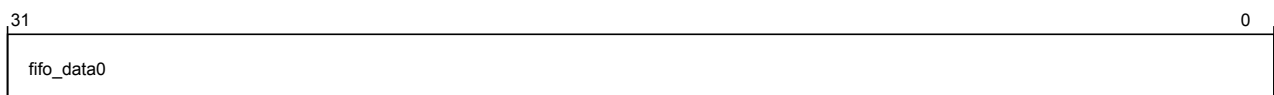


Figure 4-749 por_mxp_por_dtm_fifo_entry3_0 (low)

The following table shows the por_dtm_fifo_entry3_0 lower register bit assignments.

Table 4-766 por_mxp_por_dtm_fifo_entry3_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

por_dtm_fifo_entry3_1

Contains DTM FIFO entry 3 data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2170
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

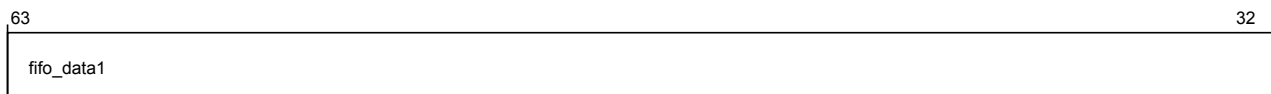


Figure 4-750 por_mxp_por_dtm_fifo_entry3_1 (high)

The following table shows the por_dtm_fifo_entry3_1 higher register bit assignments.

Table 4-767 por_mxp_por_dtm_fifo_entry3_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following image shows the lower register bit assignments.

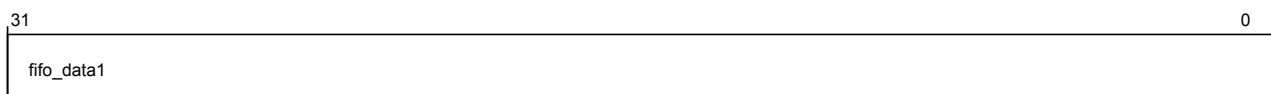


Figure 4-751 por_mxp_por_dtm_fifo_entry3_1 (low)

The following table shows the por_dtm_fifo_entry3_1 lower register bit assignments.

Table 4-768 por_mxp_por_dtm_fifo_entry3_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

por_dtm_fifo_entry3_2

Contains DTM FIFO entry 3 data.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h2178
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

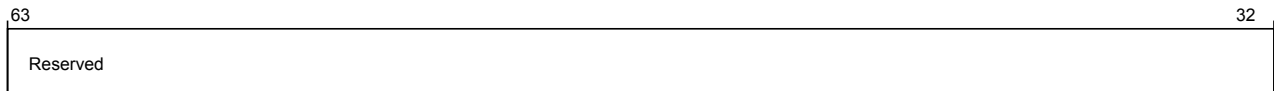


Figure 4-752 `por_mxp_por_dtm_fifo_entry3_2 (high)`

The following table shows the `por_dtm_fifo_entry3_2` higher register bit assignments.

Table 4-769 `por_mxp_por_dtm_fifo_entry3_2 (high)`

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

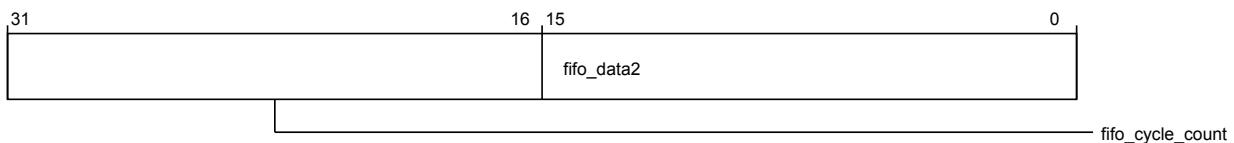


Figure 4-753 `por_mxp_por_dtm_fifo_entry3_2 (low)`

The following table shows the `por_dtm_fifo_entry3_2` lower register bit assignments.

Table 4-770 `por_mxp_por_dtm_fifo_entry3_2 (low)`

Bits	Field name	Description	Type	Reset
31:16	<code>fifo_cycle_count</code>	Entry cycle count bit vector 15:0	RO	16'b0
15:0	<code>fifo_data2</code>	Entry data bit vector 143:128	RO	16'b0

`por_dtm_wp0_config`

Configures watchpoint 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21A0
Register reset	64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-754 por_mxp_por_dtm_wp0_config (high)

The following table shows the por_dtm_wp0_config higher register bit assignments.

Table 4-771 por_mxp_por_dtm_wp0_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

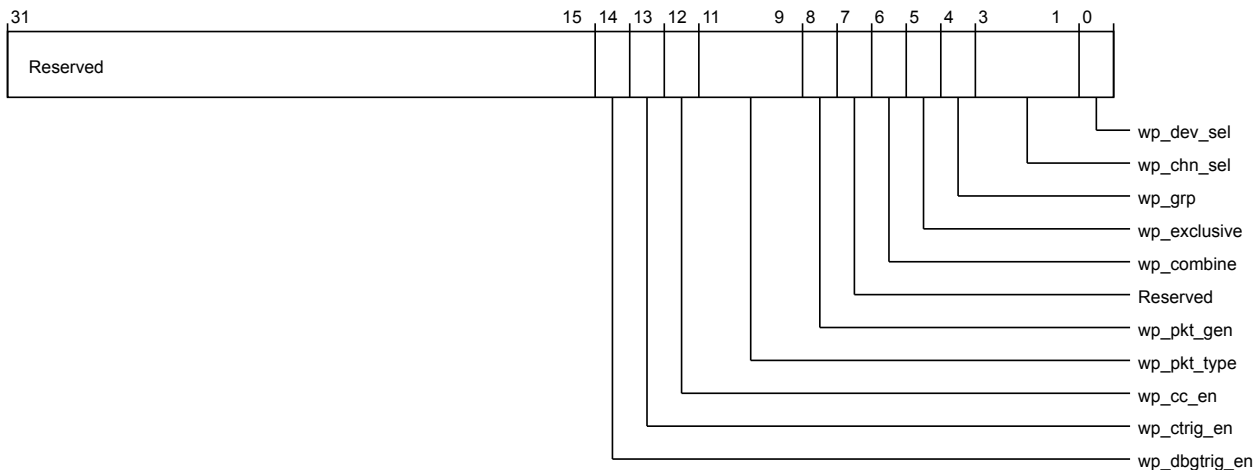


Figure 4-755 por_mxp_por_dtm_wp0_config (low)

The following table shows the por_dtm_wp0_config lower register bit assignments.

Table 4-772 por_mxp_por_dtm_wp0_config (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
13	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
12	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0

Table 4-772 por_mxp_por_dtm_wp0_config (low) (continued)

Bits	Field name	Description	Type	Reset
11:9	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: Reserved 3'b110: Reserved 3'b111: Reserved	RW	3'b000
8	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
7	Reserved	Reserved	RO	-
6	wp_combine	Enables combination of watchpoints 0 and 1	RW	1'b0
5	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
4	wp_grp	Watchpoint register format group 1'b0: Select primary group 1'b1: Select secondary group	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

por_dtm_wp0_val

Configures watchpoint 0 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21A8

Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-756 por_mxp_por_dtm_wp0_val (high)

The following table shows the por_dtm_wp0_val higher register bit assignments.

Table 4-773 por_mxp_por_dtm_wp0_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.



Figure 4-757 por_mxp_por_dtm_wp0_val (low)

The following table shows the por_dtm_wp0_val lower register bit assignments.

Table 4-774 por_mxp_por_dtm_wp0_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp0_mask

Configures watchpoint0 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21B0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

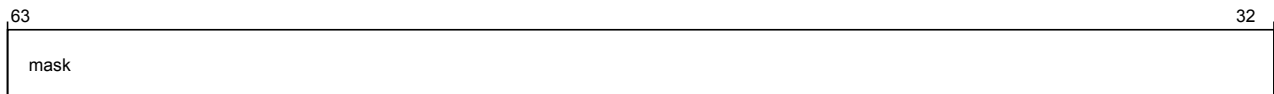


Figure 4-758 `por_mxp_por_dtm_wp0_mask` (high)

The following table shows the `por_dtm_wp0_mask` higher register bit assignments.

Table 4-775 `por_mxp_por_dtm_wp0_mask` (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

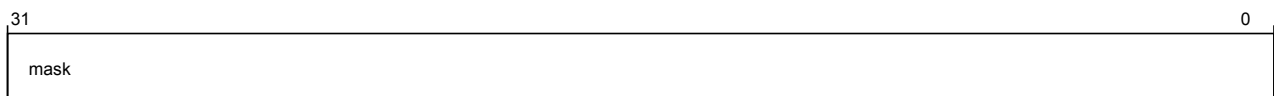


Figure 4-759 `por_mxp_por_dtm_wp0_mask` (low)

The following table shows the `por_dtm_wp0_mask` lower register bit assignments.

Table 4-776 `por_mxp_por_dtm_wp0_mask` (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

`por_dtm_wp1_config`

Configures watchpoint 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21B8
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

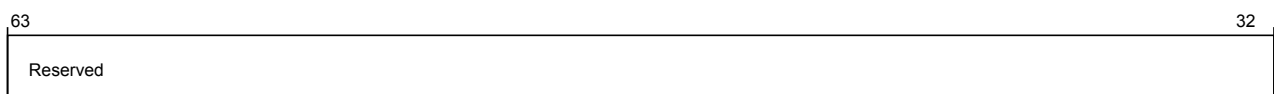


Figure 4-760 `por_mxp_por_dtm_wp1_config` (high)

The following table shows the `por_dtm_wp1_config` higher register bit assignments.

Table 4-777 por_mxp_por_dtm_wp1_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

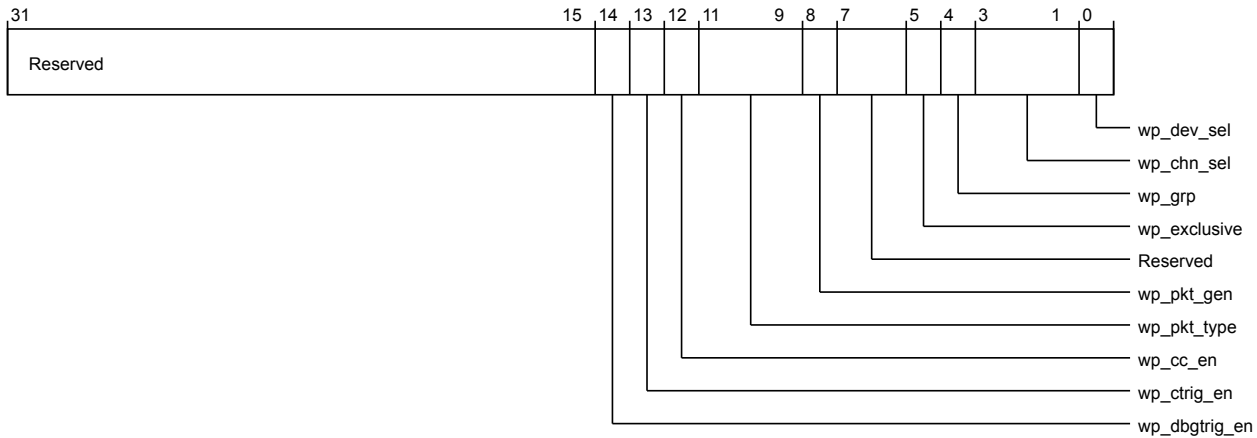


Figure 4-761 por_mxp_por_dtm_wp1_config (low)

The following table shows the por_dtm_wp1_config lower register bit assignments.

Table 4-778 por_mxp_por_dtm_wp1_config (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
13	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
12	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
11:9	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: Reserved 3'b110: Reserved 3'b111: Reserved	RW	3'b000
8	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
7:6	Reserved	Reserved	RO	-

Table 4-778 por_mxp_por_dtm_wp1_config (low) (continued)

Bits	Field name	Description	Type	Reset
5	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
4	wp_grp	Watchpoint register format group 1'b0: Select primary group 1'b1: Select secondary group	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

por_dtm_wp1_val

Configures watchpoint 1 comparison value.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21C0
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

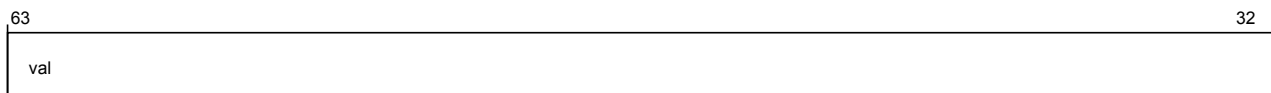


Figure 4-762 por_mxp_por_dtm_wp1_val (high)

The following table shows the por_dtm_wp1_val higher register bit assignments.

Table 4-779 por_mxp_por_dtm_wp1_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.



Figure 4-763 por_mxp_por_dtm_wp1_val (low)

The following table shows the por_dtm_wp1_val lower register bit assignments.

Table 4-780 por_mxp_por_dtm_wp1_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp1_mask

Configures watchpoint 1 comparison mask.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21C8
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

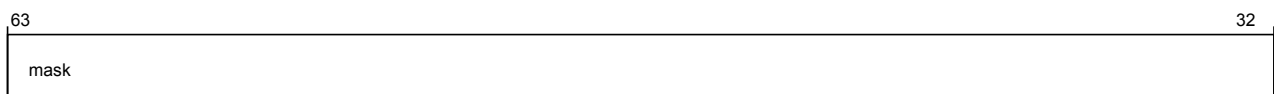


Figure 4-764 por_mxp_por_dtm_wp1_mask (high)

The following table shows the por_dtm_wp1_mask higher register bit assignments.

Table 4-781 por_mxp_por_dtm_wp1_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

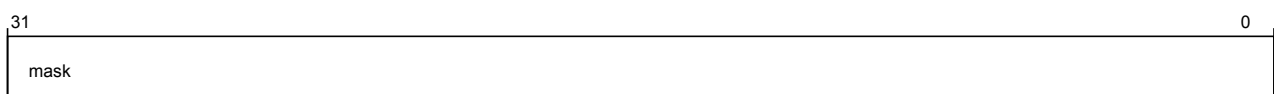


Figure 4-765 por_mxp_por_dtm_wp1_mask (low)

The following table shows the por_dtm_wp1_mask lower register bit assignments.

Table 4-782 `por_mxp_por_dtm_wp1_mask` (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

`por_dtm_wp2_config`

Configures watchpoint 2.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21D0
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

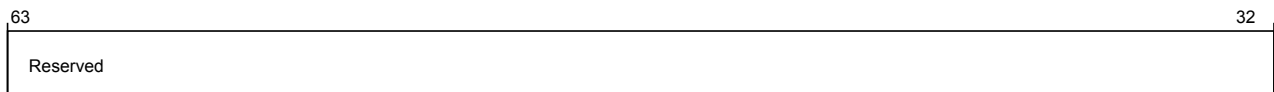


Figure 4-766 `por_mxp_por_dtm_wp2_config` (high)

The following table shows the `por_dtm_wp2_config` higher register bit assignments.

Table 4-783 `por_mxp_por_dtm_wp2_config` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

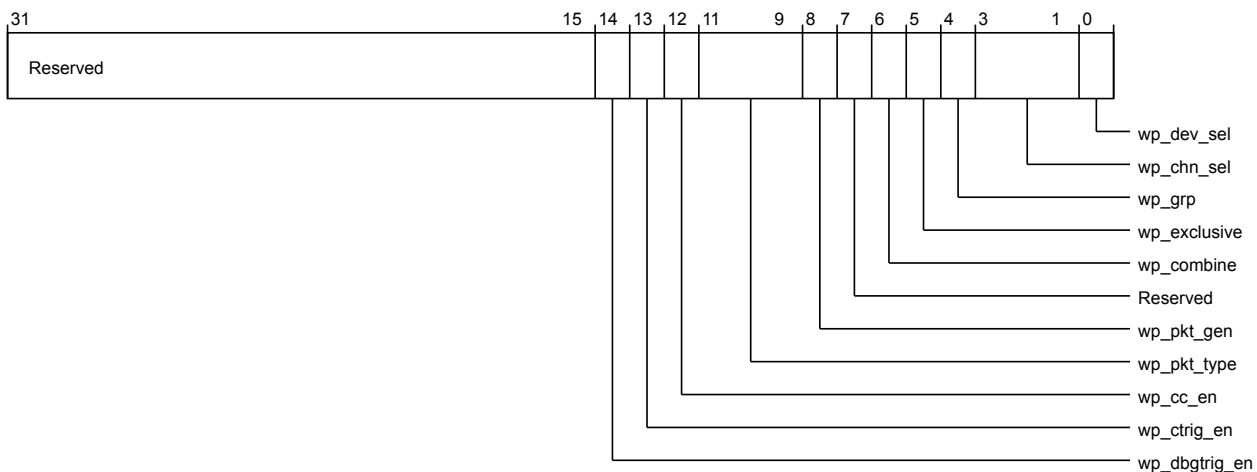


Figure 4-767 `por_mxp_por_dtm_wp2_config` (low)

The following table shows the `por_dtm_wp2_config` lower register bit assignments.

Table 4-784 por_mxp_por_dtm_wp2_config (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
13	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
12	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
11:9	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: Reserved 3'b110: Reserved 3'b111: Reserved	RW	3'b000
8	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
7	Reserved	Reserved	RO	-
6	wp_combine	Enables combination of watchpoints 2 and 3	RW	1'b0
5	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
4	wp_grp	Watchpoint register format group 1'b0: Select primary group 1'b1: Select secondary group	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

por_dtm_wp2_val

Configures watchpoint 2 comparison value.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21D8
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

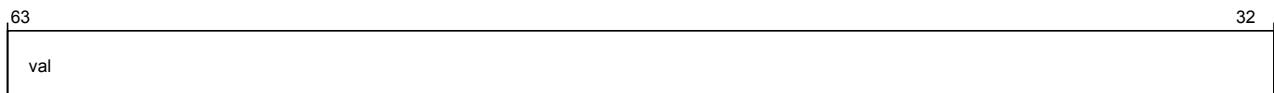


Figure 4-768 por_mxp_por_dtm_wp2_val (high)

The following table shows the por_dtm_wp2_val higher register bit assignments.

Table 4-785 por_mxp_por_dtm_wp2_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

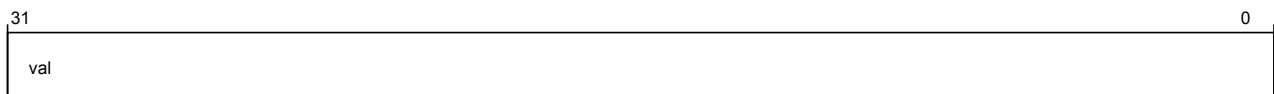


Figure 4-769 por_mxp_por_dtm_wp2_val (low)

The following table shows the por_dtm_wp2_val lower register bit assignments.

Table 4-786 por_mxp_por_dtm_wp2_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp2_mask

Configures watchpoint 2 comparison mask.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21E0
Register reset	64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-770 por_mxp_por_dtm_wp2_mask (high)

The following table shows the por_dtm_wp2_mask higher register bit assignments.

Table 4-787 por_mxp_por_dtm_wp2_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

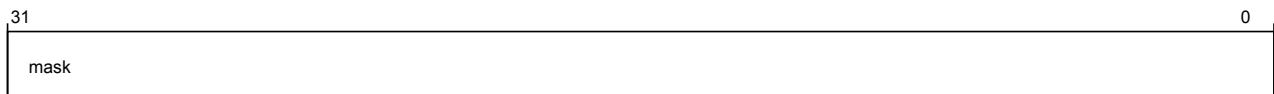


Figure 4-771 por_mxp_por_dtm_wp2_mask (low)

The following table shows the por_dtm_wp2_mask lower register bit assignments.

Table 4-788 por_mxp_por_dtm_wp2_mask (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp3_config

Configures watchpoint 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h21E8

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-772 por_mxp_por_dtm_wp3_config (high)

The following table shows the por_dtm_wp3_config higher register bit assignments.

Table 4-789 por_mxp_por_dtm_wp3_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

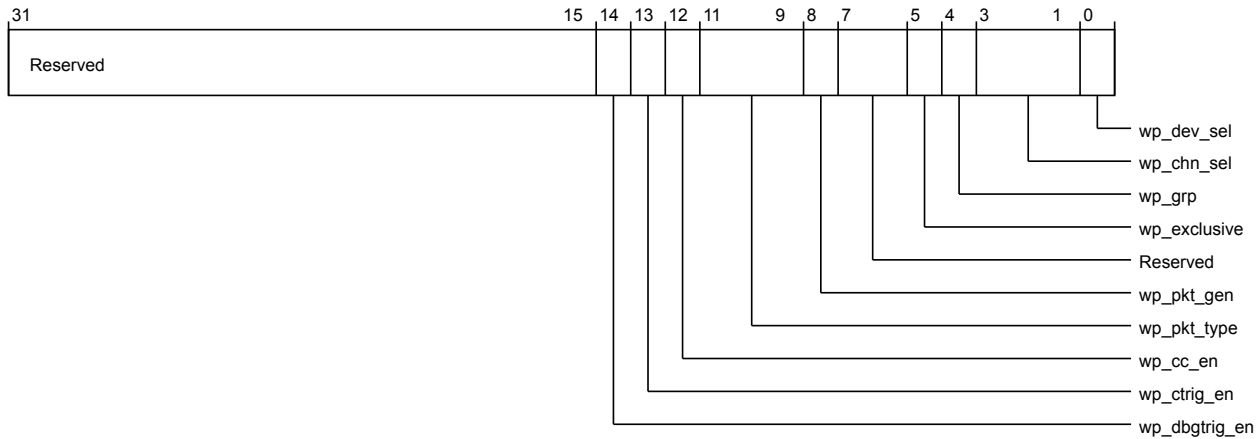


Figure 4-773 por_mxp_por_dtm_wp3_config (low)

The following table shows the por_dtm_wp3_config lower register bit assignments.

Table 4-790 por_mxp_por_dtm_wp3_config (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14	<code>wp_dbgtrig_en</code>	Enables watchpoint debug trigger packet generation	RW	1'b0
13	<code>wp_ctrig_en</code>	Enables watchpoint cross trigger packet generation	RW	1'b0
12	<code>wp_cc_en</code>	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
11:9	<code>wp_pkt_type</code>	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: Reserved 3'b110: Reserved 3'b111: Reserved	RW	3'b000
8	<code>wp_pkt_gen</code>	Enables watchpoint trace packet generation	RW	1'b0

Table 4-790 por_mxp_por_dtm_wp3_config (low) (continued)

Bits	Field name	Description	Type	Reset
7:6	Reserved	Reserved	RO	-
5	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
4	wp_grp	Watchpoint register format group 1'b0: Select primary group 1'b1: Select secondary group	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

por_dtm_wp3_val

Configures watchpoint 3 comparison value.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21F0
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

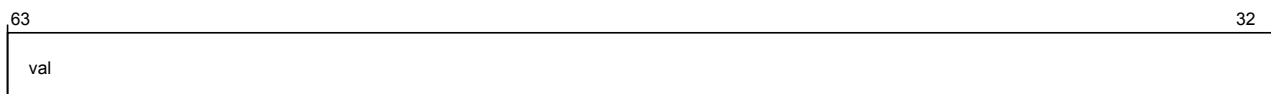


Figure 4-774 por_mxp_por_dtm_wp3_val (high)

The following table shows the por_dtm_wp3_val higher register bit assignments.

Table 4-791 por_mxp_por_dtm_wp3_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.



Figure 4-775 por_mxp_por_dtm_wp3_val (low)

The following table shows the por_dtm_wp3_val lower register bit assignments.

Table 4-792 por_mxp_por_dtm_wp3_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp3_mask

Configures watchpoint 3 comparison mask.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21F8
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

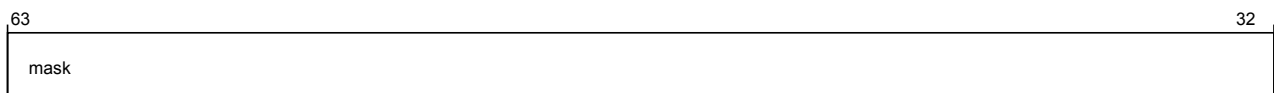


Figure 4-776 por_mxp_por_dtm_wp3_mask (high)

The following table shows the por_dtm_wp3_mask higher register bit assignments.

Table 4-793 por_mxp_por_dtm_wp3_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

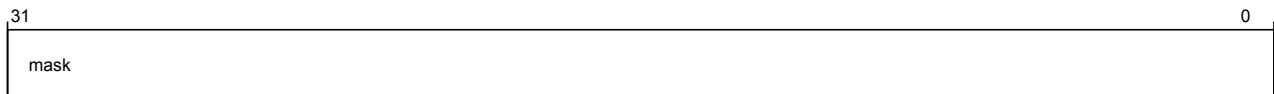


Figure 4-777 por_mxp_por_dtm_wp3_mask (low)

The following table shows the por_dtm_wp3_mask lower register bit assignments.

Table 4-794 por_mxp_por_dtm_wp3_mask (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_pmsicr

Functions as the sampling interval counter register.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2200
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

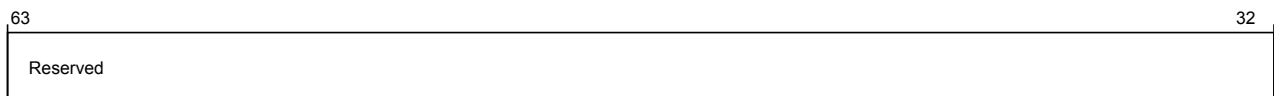


Figure 4-778 por_mxp_por_dtm_pmsicr (high)

The following table shows the por_dtm_pmsicr higher register bit assignments.

Table 4-795 por_mxp_por_dtm_pmsicr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

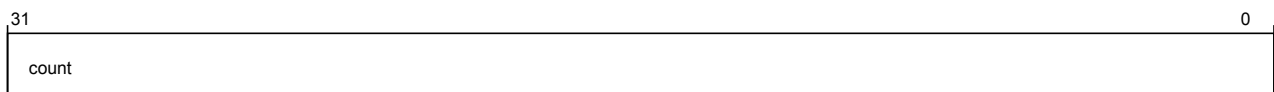


Figure 4-779 por_mxp_por_dtm_pmsicr (low)

The following table shows the por_dtm_pmsicr lower register bit assignments.

Table 4-796 por_mxp_por_dtm_pmsicr (low)

Bits	Field name	Description	Type	Reset
31:0	count	Current value of sample counter	RW	32'b0

por_dtm_pmsirr

Functions as the sampling interval reload register.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2208
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

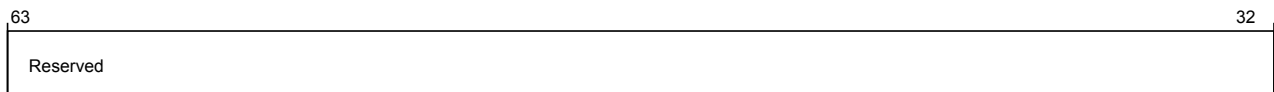


Figure 4-780 por_mxp_por_dtm_pmsirr (high)

The following table shows the por_dtm_pmsirr higher register bit assignments.

Table 4-797 por_mxp_por_dtm_pmsirr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

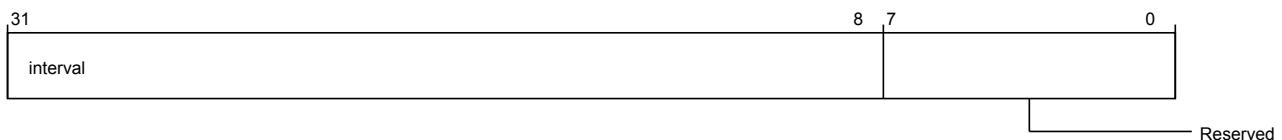


Figure 4-781 por_mxp_por_dtm_pmsirr (low)

The following table shows the por_dtm_pmsirr lower register bit assignments.

Table 4-798 por_mxp_por_dtm_pmsirr (low)

Bits	Field name	Description	Type	Reset
31:8	interval	Sampling interval to be reloaded	RW	24'b0
7:0	Reserved	Reserved	RO	-

por_dtm_pmu_config

Configures the DTM PMU.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2210
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

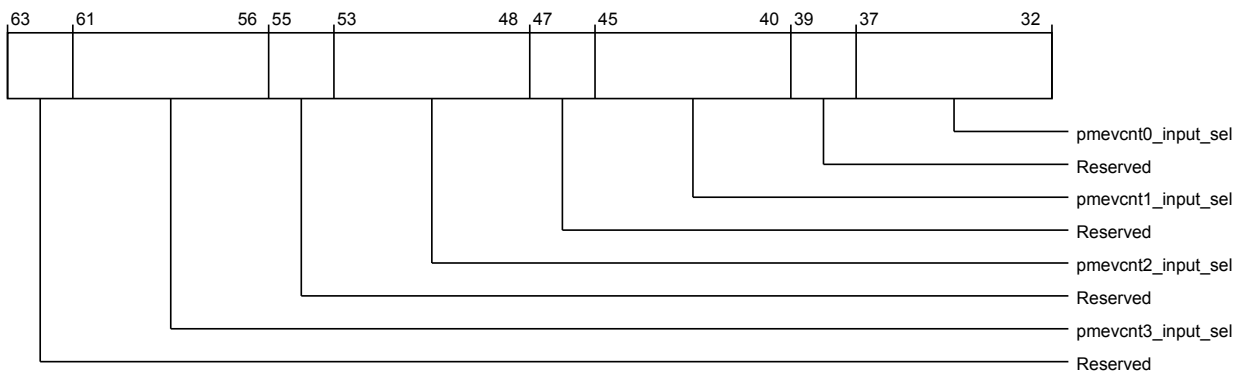


Figure 4-782 por_mxp_por_dtm_pmu_config (high)

The following table shows the por_dtm_pmu_config higher register bit assignments.

Table 4-799 por_mxp_por_dtm_pmu_config (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	pmevcnt3_input_sel	Source to be counted in PMU counter 3; see pmevcnt0_input_sel for encodings	RW	6'b0
55:54	Reserved	Reserved	RO	-
53:48	pmevcnt2_input_sel	Source to be counted in PMU counter 2; see pmevcnt0_input_sel for encodings	RW	6'b0
47:46	Reserved	Reserved	RO	-
45:40	pmevcnt1_input_sel	Source to be counted in PMU counter 1; see pmevcnt0_input_sel for encodings	RW	6'b0
39:38	Reserved	Reserved	RO	-

Table 4-799 por_mxp_por_dtm_pmu_config (high) (continued)

Bits	Field name	Description	Type	Reset
37:32	pmevnt0_input_sel	<p>Source to be counted in PMU counter 0</p> <p>6'h00: Watchpoint 0</p> <p>6'h01: Watchpoint 1</p> <p>6'h02: Watchpoint 2</p> <p>6'h03: Watchpoint 3</p> <p>6'h04: XP PMU Event 0</p> <p>6'h05: XP PMU Event 1</p> <p>6'h06: XP PMU Event 2</p> <p>6'h07: XP PMU Event 3</p> <p>6'h10: Port 0 Device 0 PMU Event 0</p> <p>6'h11: Port 0 Device 0 PMU Event 1</p> <p>6'h12: Port 0 Device 0 PMU Event 2</p> <p>6'h13: Port 0 Device 0 PMU Event 3</p> <p>6'h14: Port 0 Device 1 PMU Event 0</p> <p>6'h15: Port 0 Device 1 PMU Event 1</p> <p>6'h16: Port 0 Device 1 PMU Event 2</p> <p>6'h17: Port 0 Device 1 PMU Event 3</p> <p>6'h18: Port 0 Device 2 PMU Event 0</p> <p>6'h19: Port 0 Device 2 PMU Event 1</p> <p>6'h1A: Port 0 Device 2 PMU Event 2</p> <p>6'h1B: Port 0 Device 2 PMU Event 3</p> <p>6'h1C: Port 0 Device 3 PMU Event 0</p> <p>6'h1D: Port 0 Device 3 PMU Event 1</p> <p>6'h1E: Port 0 Device 3 PMU Event 2</p> <p>6'h1F: Port 0 Device 3 PMU Event 3</p> <p>6'h20: Port 1 Device 0 PMU Event 0</p> <p>6'h21: Port 1 Device 0 PMU Event 1</p> <p>6'h22: Port 1 Device 0 PMU Event 2</p> <p>6'h23: Port 1 Device 0 PMU Event 3</p> <p>6'h24: Port 1 Device 1 PMU Event 0</p> <p>6'h25: Port 1 Device 1 PMU Event 1</p> <p>6'h26: Port 1 Device 1 PMU Event 2</p> <p>6'h27: Port 1 Device 1 PMU Event 3</p> <p>6'h28: Port 1 Device 2 PMU Event 0</p> <p>6'h29: Port 1 Device 2 PMU Event 1</p>	RW	6'b0

Table 4-799 `por_mxp_por_dtm_pmu_config` (high) (continued)

Bits	Field name	Description	Type	Reset
37:32	<code>pmevcnt0_input_sel</code>	6'h2A: Port 1 Device 2 PMU Event 2 6'h2B: Port 1 Device 2 PMU Event 3 6'h2C: Port 1 Device 3 PMU Event 0 6'h2D: Port 1 Device 3 PMU Event 1 6'h2E: Port 1 Device 3 PMU Event 2 6'h2F: Port 1 Device 3 PMU Event 3	RW	6'b0

The following image shows the lower register bit assignments.

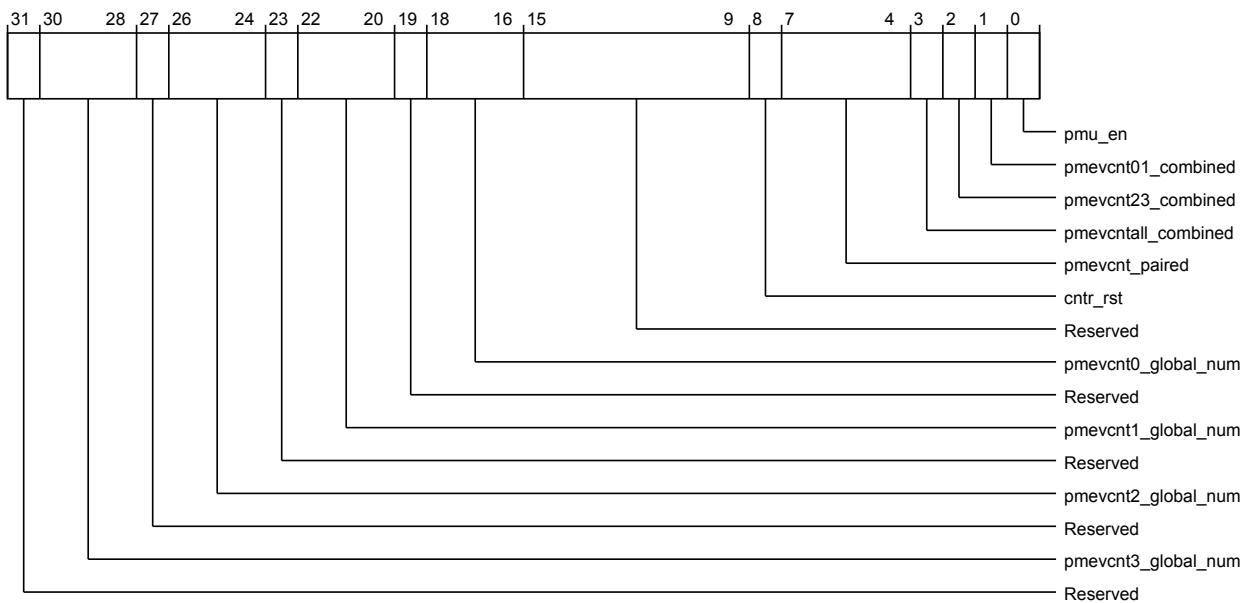


Figure 4-783 `por_mxp_por_dtm_pmu_config` (low)

The following table shows the `por_dtm_pmu_config` lower register bit assignments.

Table 4-800 `por_mxp_por_dtm_pmu_config` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	<code>pmevcnt3_global_num</code>	Global counter to pair with PMU counter 3; see <code>pmevcnt0_global_num</code> for encodings	RW	3'b0
27	Reserved	Reserved	RO	-
26:24	<code>pmevcnt2_global_num</code>	Global counter to pair with PMU counter 2; see <code>pmevcnt0_global_num</code> for encodings	RW	3'b0
23	Reserved	Reserved	RO	-
22:20	<code>pmevcnt1_global_num</code>	Global counter to pair with PMU counter 1; see <code>pmevcnt0_global_num</code> for encodings	RW	3'b0
19	Reserved	Reserved	RO	-

Table 4-800 por_mxp_por_dtm_pmu_config (low) (continued)

Bits	Field name	Description	Type	Reset
18:16	pmevcnt0_global_num	Global counter to pair with PMU counter 0 3'b000: Global PMU event counter A 3'b001: Global PMU event counter B 3'b010: Global PMU event counter C 3'b011: Global PMU event counter D 3'b100: Global PMU event counter E 3'b101: Global PMU event counter F 3'b110: Global PMU event counter G 3'b111: Global PMU event counter H	RW	3'b0
15:9	Reserved	Reserved	RO	-
8	cntr_rst	Enables clearing of live counters upon assertion of snapshot	RW	1'b0
7:4	pmevcnt_paired	PMU local counter paired with global counter	RW	4'b0
3	pmevcntall_combined	Enables combination of all PMU counters (0, 1, 2, 3) NOTE: When set, pmevcnt01_combined and pmevcnt23_combined have no effect.	RW	1'b0
2	pmevcnt23_combined	Enables combination of PMU counters 2 and 3	RW	1'b0
1	pmevcnt01_combined	Enables combination of PMU counters 0 and 1	RW	1'b0
0	pmu_en	DTM PMU enable NOTE: All other fields in this register are valid only if this bit is set.	RW	1'b0

por_dtm_pmevcnt

Contains all PMU event counters (0, 1, 2, 3).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2220

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

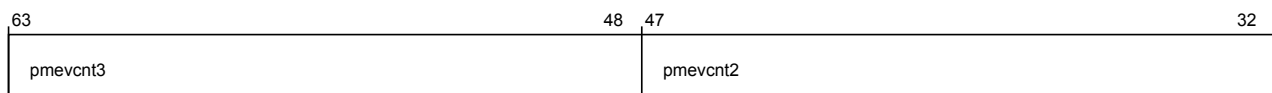


Figure 4-784 por_mxp_por_dtm_pmevcnt (high)

The following table shows the por_dtm_pmevcnt higher register bit assignments.

Table 4-801 por_mxp_por_dtm_pmevcnt (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcnt3	PMU event counter 3	RW	16'h0000
47:32	pmevcnt2	PMU event counter 2	RW	16'h0000

The following image shows the lower register bit assignments.

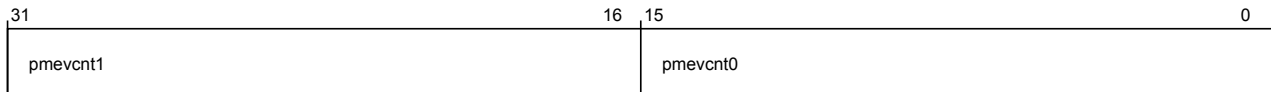


Figure 4-785 por_mxp_por_dtm_pmevcnt (low)

The following table shows the por_dtm_pmevcnt lower register bit assignments.

Table 4-802 por_mxp_por_dtm_pmevcnt (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcnt1	PMU event counter 1	RW	16'h0000
15:0	pmevcnt0	PMU event counter 0	RW	16'h0000

por_dtm_pmevcntsr

Functions as the PMU event counter shadow register for all counters (0, 1, 2, 3).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2240
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

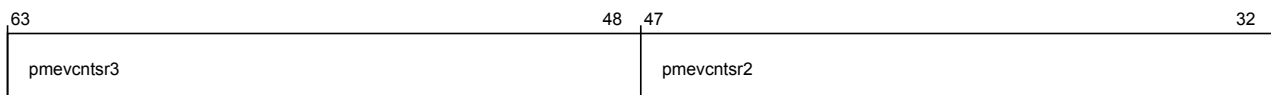


Figure 4-786 por_mxp_por_dtm_pmevcntsr (high)

The following table shows the por_dtm_pmevcntsr higher register bit assignments.

Table 4-803 por_mxp_por_dtm_pmevcntsr (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcntsr3	PMU event counter 3 shadow register	RW	16'h0000
47:32	pmevcntsr2	PMU event counter 2 shadow register	RW	16'h0000

The following image shows the lower register bit assignments.

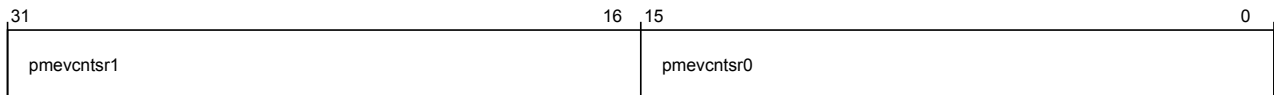


Figure 4-787 por_mxp_por_dtm_pmevcntsr (low)

The following table shows the por_dtm_pmevcntsr lower register bit assignments.

Table 4-804 por_mxp_por_dtm_pmevcntsr (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcntsr1	PMU event counter 1 shadow register	RW	16'h0000
15:0	pmevcntsr0	PMU event counter 0 shadow register	RW	16'h0000

4.3.7 RN-D register descriptions

Lists the RN-D registers.

por_rnd_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

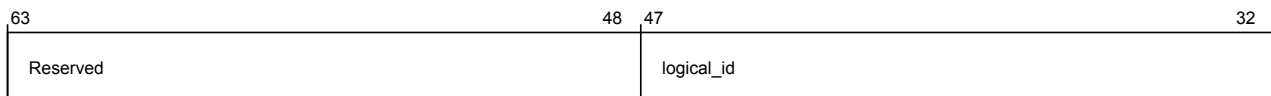


Figure 4-788 por_rnd_por_rnd_node_info (high)

The following table shows the por_rnd_node_info higher register bit assignments.

Table 4-805 por_rnd_por_rnd_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

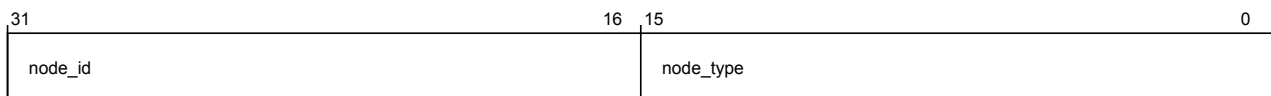


Figure 4-789 por_rnd_por_rnd_node_info (low)

The following table shows the por_rnd_node_info lower register bit assignments.

Table 4-806 por_rnd_por_rnd_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h000D

por_rnd_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

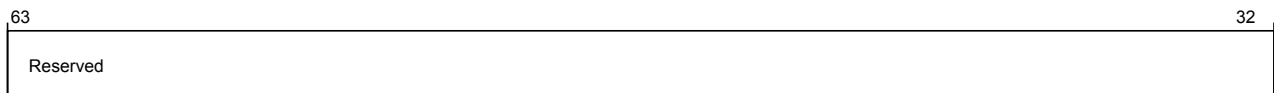


Figure 4-790 por_rnd_por_rnd_child_info (high)

The following table shows the por_rnd_child_info higher register bit assignments.

Table 4-807 por_rnd_por_rnd_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

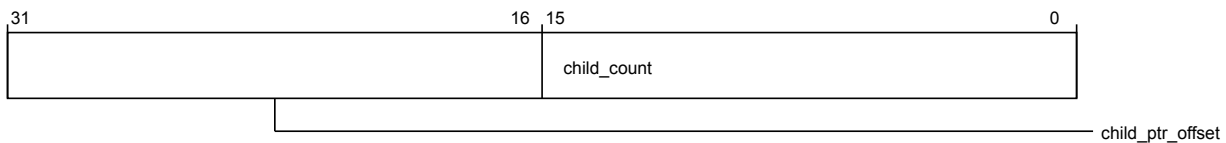


Figure 4-791 por_rnd_por_rnd_child_info (low)

The following table shows the por_rnd_child_info lower register bit assignments.

Table 4-808 por_rnd_por_rnd_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

por_rnd_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type	RW
Register width (Bits)	64

Address offset	14'h980
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

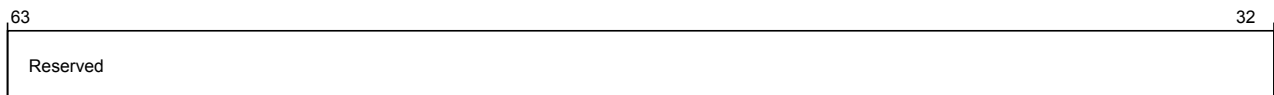


Figure 4-792 por_rnd_por_rnd_secure_register_groups_override (high)

The following table shows the por_rnd_secure_register_groups_override higher register bit assignments.

Table 4-809 por_rnd_por_rnd_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

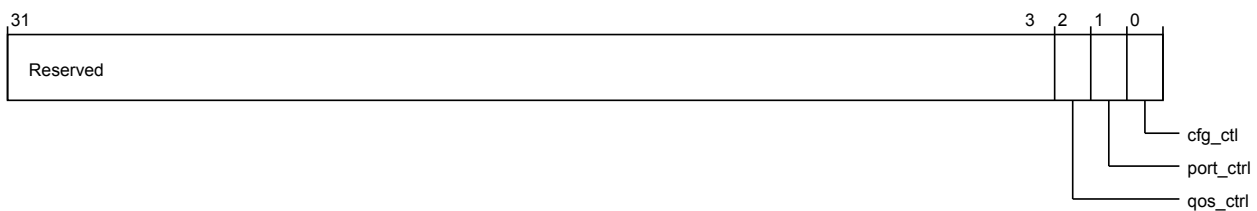


Figure 4-793 por_rnd_por_rnd_secure_register_groups_override (low)

The following table shows the por_rnd_secure_register_groups_override lower register bit assignments.

Table 4-810 por_rnd_por_rnd_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	qos_ctrl	Allows non-secure access to secure QoS control registers	RW	1'b0
1	port_ctrl	Allows non-secure access to secure AXI port control registers	RW	1'b0
0	cfg_ctl	Allows non-secure access to secure configuration control register	RW	1'b0

por_rnd_unit_info

Provides component identification information for RN-D.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

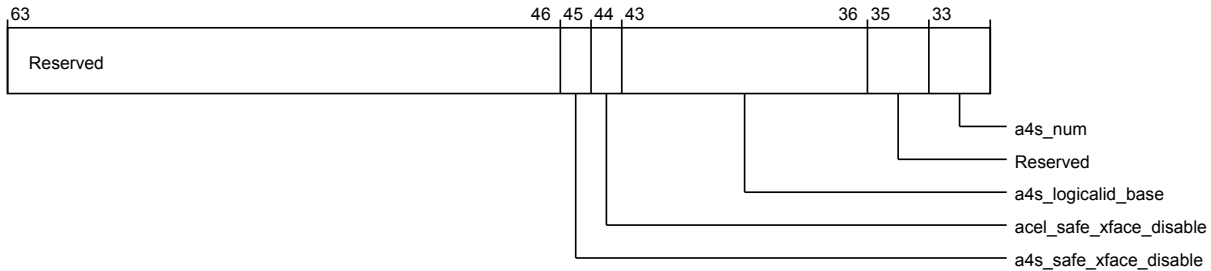


Figure 4-794 por_rnd_por_rnd_unit_info (high)

The following table shows the por_rnd_unit_info higher register bit assignments.

Table 4-811 por_rnd_por_rnd_unit_info (high)

Bits	Field name	Description	Type	Reset
63:46	Reserved	Reserved	RO	-
45	a4s_safe_xface_disable	AXI4Stream safe interface disable	RO	Configuration dependent
44	acel_safe_xface_disable	ACE-Lite/AXI4 safe interface disable	RO	Configuration dependent
43:36	a4s_logicalid_base	AXI4Stream interfaces logical ID base	RO	Configuration dependent
35:34	Reserved	Reserved	RO	-
33:32	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent

The following image shows the lower register bit assignments.

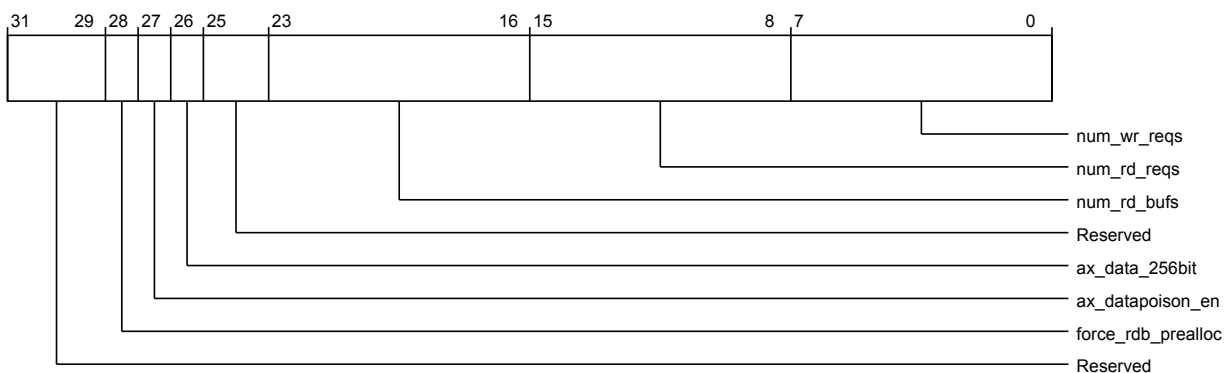


Figure 4-795 por_rnd_por_rnd_unit_info (low)

The following table shows the por_rnd_unit_info lower register bit assignments.

Table 4-812 por_rnd_por_rnd_unit_info (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28	force_rdb_prealloc	Force read data buffer preallocation 1'b1: yes 1'b0: no	RO	Configuration dependent
27	ax_datapoison_en	Data Poison enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
26	ax_data_256bit	AXI interface data width 1'b1: 256 bits 1'b0: 128 bits	RO	Configuration dependent
25:24	Reserved	Reserved	RO	-
23:16	num_rd_bufs	Number of read data buffers	RO	Configuration dependent
15:8	num_rd_reqs	Number of outstanding read requests	RO	Configuration dependent
7:0	num_wr_reqs	Number of outstanding write requests	RO	Configuration dependent

por_rnd_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA00
Register reset	Configuration dependent
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rnd_secure_register_groups_override.cfg_ctl

The following image shows the higher register bit assignments.

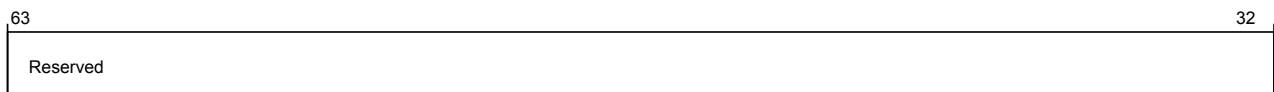


Figure 4-796 por_rnd_por_rnd_cfg_ctl (high)

The following table shows the por_rnd_cfg_ctl higher register bit assignments.

Table 4-813 por_rnd_por_rnd_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

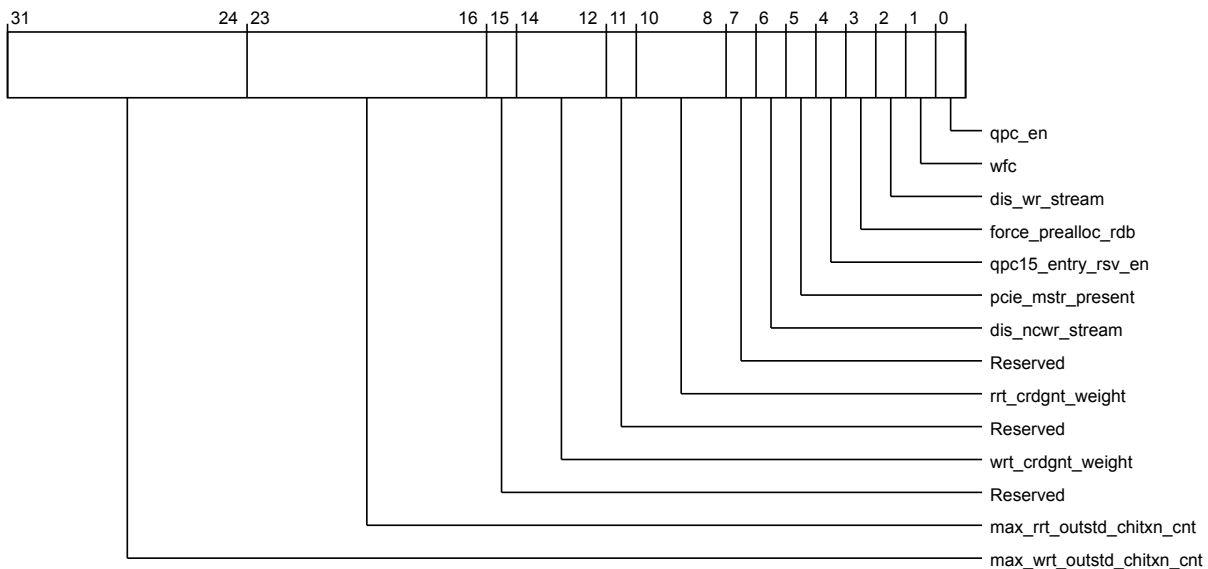


Figure 4-797 por_rnd_por_rnd_cfg_ctl (low)

The following table shows the `por_rnd_cfg_ctl` lower register bit assignments.

Table 4-814 por_rnd_por_rnd_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:24	<code>max_wrt_outstd_chitxn_cnt</code>	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent
23:16	<code>max_rrt_outstd_chitxn_cnt</code>	Maximum number of outstanding reads allowed on CHI-side	RW	Configuration dependent
15	Reserved	Reserved	RO	-
14:12	<code>wrt_crdgnt_weight</code>	Determines weight of credit grant allocated to retried writes in presence of pending retried reads	RW	3'b001
11	Reserved	Reserved	RO	-
10:8	<code>rrt_crdgnt_weight</code>	Determines weight of credit grant allocated to retried reads in presence of pending retried writes	RW	3'b100
7	Reserved	Reserved	RO	-
6	<code>dis_ncwr_stream</code>	Disables streaming of ordered non-cacheable writes when set	RW	1'b0
5	<code>pcie_mstr_present</code>	Indicates PCIe master is present; must be set if PCIe master is present upstream of RN-I or RN-D	RW	1'b0

Table 4-814 `por_rnd_por_rnd_cfg_ctl` (low) (continued)

Bits	Field name	Description	Type	Reset
4	<code>qpc15_entry_rsv_en</code>	Enables QPC15 entry reservation 1'b1: Reserves tracker entry for QoS15 requests 1'b0: Does not reserve tracker entry for QoS15 requests NOTE: Only valid and applicable when <code>por_rnd_qpc_en</code> is set	RW	1'b0
3	<code>force_prealloc_rdb</code>	When set, all reads from the RN-D are sent with a preallocated read data buffer	RW	Configuration dependent
2	<code>dis_wr_stream</code>	Disables streaming of ordered writes when set	RW	1'b0
1	<code>wfc</code>	When set, enables waiting for completion (COMP) before dispatching dependent transaction (TXN)	RW	1'b0
0	<code>qpc_en</code>	When set, enables QPC-based scheduling using two QoS priority classes (QoS15 and non-QoS15)	RW	1'b1

`por_rnd_aux_ctl`

Functions as the auxiliary control register for RN-D.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA08
Register reset	Configuration dependent
Usage constraints	Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

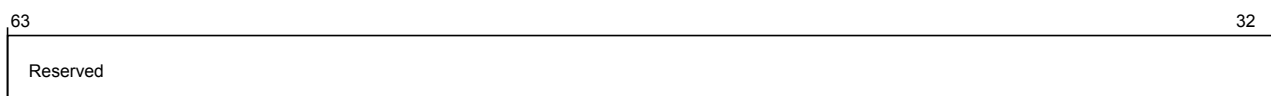


Figure 4-798 `por_rnd_por_rnd_aux_ctl` (high)

The following table shows the `por_rnd_aux_ctl` higher register bit assignments.

Table 4-815 `por_rnd_por_rnd_aux_ctl` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

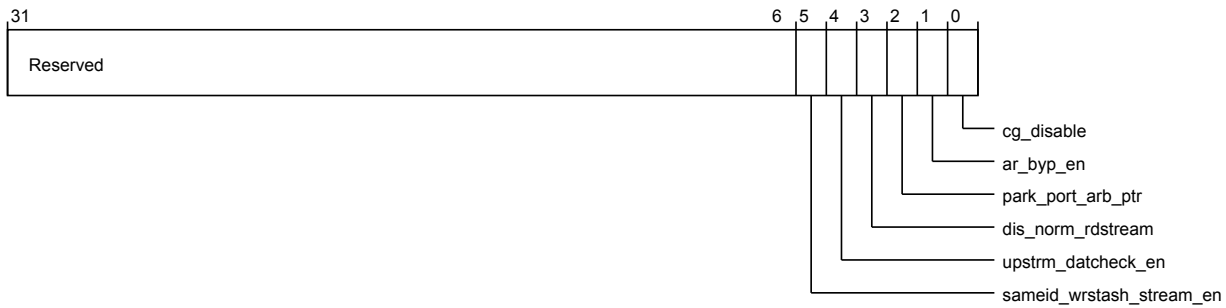


Figure 4-799 `por_rnd_por_rnd_aux_ctl` (low)

The following table shows the `por_rnd_aux_ctl` lower register bit assignments.

Table 4-816 `por_rnd_por_rnd_aux_ctl` (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5	<code>sameid_wrstash_stream_en</code>	Enables streaming of same-ID WrUniqStash	RW	Configuration dependent
4	<code>upstrm_datcheck_en</code>	Upstream supports Datacheck	RW	Configuration dependent
3	<code>dis_norm_rdstream</code>	Disables streaming of same ARID normal memory reads to different address	RW	1'b0
2	<code>park_port_arb_ptr</code>	Parks the AXI port arbitration pointer for Burst	RW	1'b0
1	<code>ar_byp_en</code>	AR bypass enable; enables bypass path in the AR pipeline	RW	1'b1
0	<code>cg_disable</code>	Disables clock gating when set	RW	1'b0

`por_rnd_s0_port_control`

Controls port S0 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_rnd_secure_register_groups_override.port_ctrl`

The following image shows the higher register bit assignments.

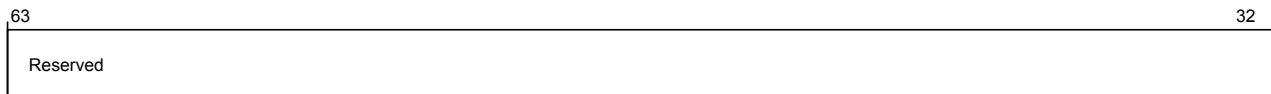


Figure 4-800 por_rnd_por_rnd_s0_port_control (high)

The following table shows the por_rnd_s0_port_control higher register bit assignments.

Table 4-817 por_rnd_por_rnd_s0_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

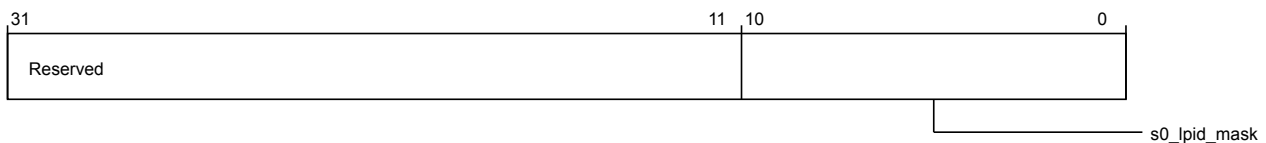


Figure 4-801 por_rnd_por_rnd_s0_port_control (low)

The following table shows the por_rnd_s0_port_control lower register bit assignments.

Table 4-818 por_rnd_por_rnd_s0_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s0_lpid_mask	Port S0 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rnd_s1_port_control

Controls port S1 AXI/ACE slave interface settings.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA18
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rnd_secure_register_groups_override.port_ctrl

The following image shows the higher register bit assignments.

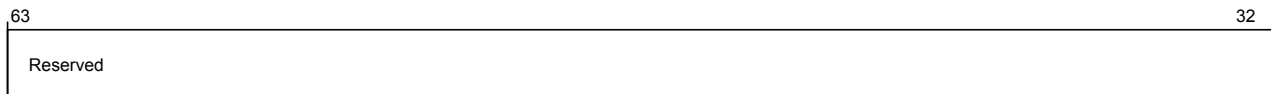


Figure 4-802 por_rnd_por_rnd_s1_port_control (high)

The following table shows the por_rnd_s1_port_control higher register bit assignments.

Table 4-819 por_rnd_por_rnd_s1_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

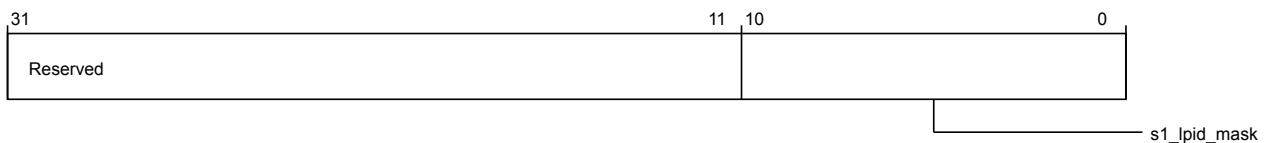


Figure 4-803 por_rnd_por_rnd_s1_port_control (low)

The following table shows the por_rnd_s1_port_control lower register bit assignments.

Table 4-820 por_rnd_por_rnd_s1_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s1_lpid_mask	Port S1 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rnd_s2_port_control

Controls port S2 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA20

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.port_ctrl

The following image shows the higher register bit assignments.

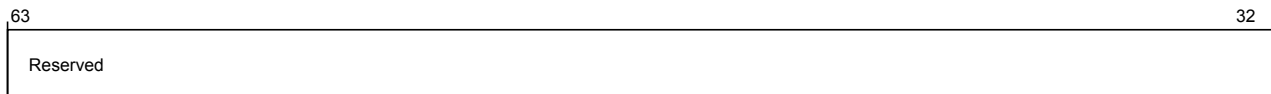


Figure 4-804 por_rnd_por_rnd_s2_port_control (high)

The following table shows the por_rnd_s2_port_control higher register bit assignments.

Table 4-821 por_rnd_por_rnd_s2_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

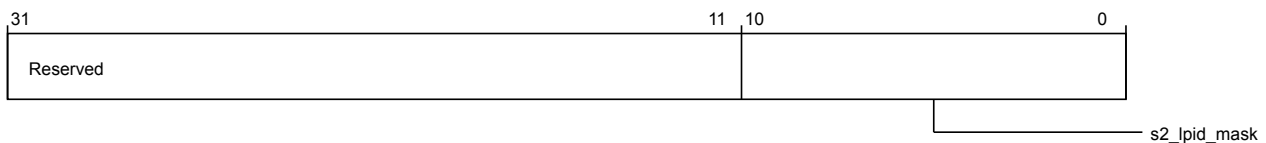


Figure 4-805 por_rnd_por_rnd_s2_port_control (low)

The following table shows the por_rnd_s2_port_control lower register bit assignments.

Table 4-822 por_rnd_por_rnd_s2_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s2_lpid_mask	Port S2 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rnd_s0_qos_control

Controls QoS settings for port S0 AXI/ACE slave interface.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

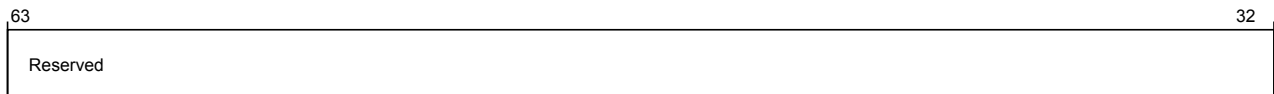


Figure 4-806 por_rnd_por_rnd_s0_qos_control (high)

The following table shows the por_rnd_s0_qos_control higher register bit assignments.

Table 4-823 por_rnd_por_rnd_s0_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

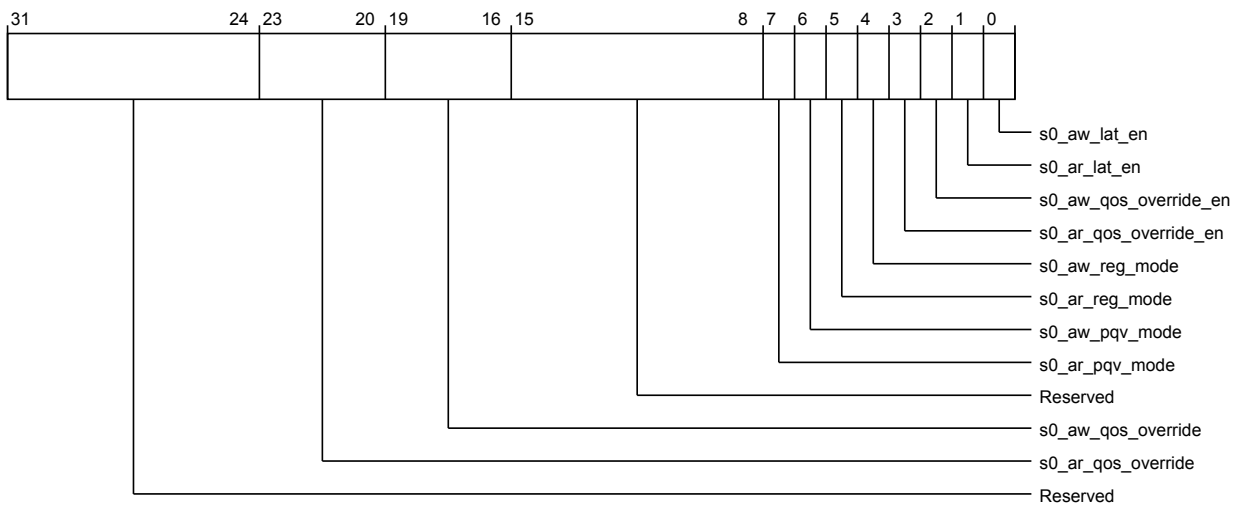


Figure 4-807 por_rnd_por_rnd_s0_qos_control (low)

The following table shows the por_rnd_s0_qos_control lower register bit assignments.

Table 4-824 por_rnd_por_rnd_s0_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s0_ar_qos_override	AR QoS override value for port S0	RW	4'b0000
19:16	s0_aw_qos_override	AW QoS override value for port S0	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s0_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0

Table 4-824 por_rnd_por_rnd_s0_qos_control (low) (continued)

Bits	Field name	Description	Type	Reset
6	s0_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s0_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s0_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s0_ar_qos_override_en	Enables port S0 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s0_aw_qos_override_en	Enables port S0 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s0_ar_lat_en	Enables port S0 AR QoS regulation when set	RW	1'b0
0	s0_aw_lat_en	Enables port S0 AW QoS regulation when set	RW	1'b0

por_rnd_s0_qos_lat_tgt

Controls QoS target latency (in cycles) for regulations of port S0 read and write transactions.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA88
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

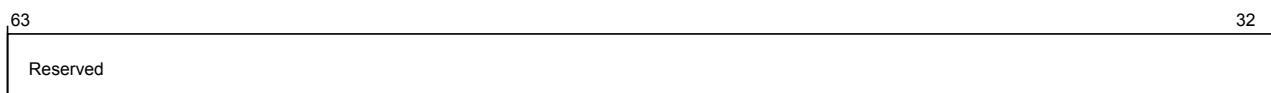


Figure 4-808 por_rnd_por_rnd_s0_qos_lat_tgt (high)

The following table shows the por_rnd_s0_qos_lat_tgt higher register bit assignments.

Table 4-825 `por_rnd_por_rnd_s0_qos_lat_tgt` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

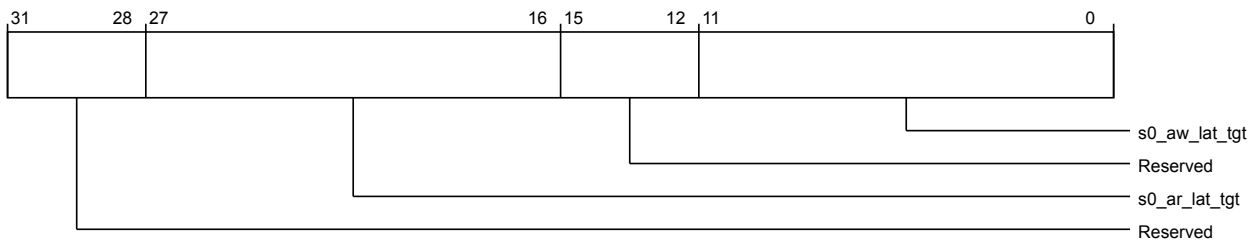


Figure 4-809 `por_rnd_por_rnd_s0_qos_lat_tgt` (low)

The following table shows the `por_rnd_s0_qos_lat_tgt` lower register bit assignments.

Table 4-826 `por_rnd_por_rnd_s0_qos_lat_tgt` (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	<code>s0_ar_lat_tgt</code>	Port S0 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	<code>s0_aw_lat_tgt</code>	Port S0 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

`por_rnd_s0_qos_lat_scale`

Controls the QoS target latency scale factor for port S0 read and write transactions. This register represents powers of two from the range $2^{(-5)}$ to $2^{(-12)}$; it is used to match a 16-bit integrator.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA90

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_rnd_secure_register_groups_override.qos_ctrl`

The following image shows the higher register bit assignments.

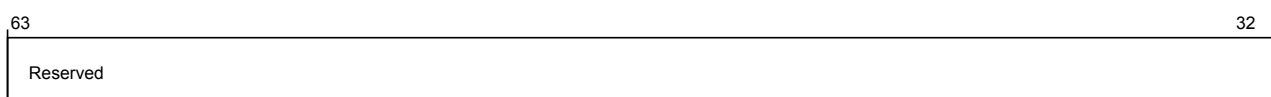


Figure 4-810 `por_rnd_por_rnd_s0_qos_lat_scale` (high)

The following table shows the por_rnd_s0_qos_lat_scale higher register bit assignments.

Table 4-827 por_rnd_por_rnd_s0_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

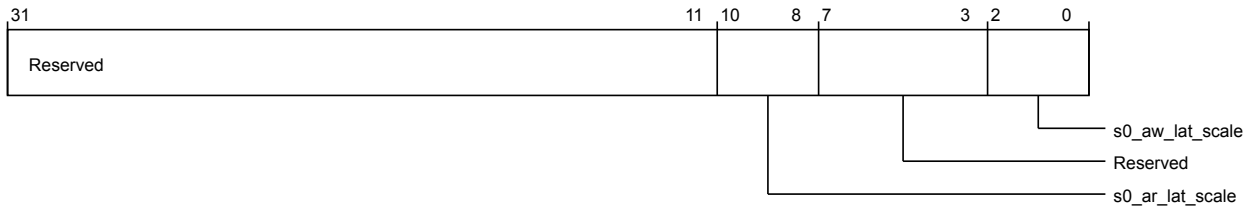


Figure 4-811 por_rnd_por_rnd_s0_qos_lat_scale (low)

The following table shows the por_rnd_s0_qos_lat_scale lower register bit assignments.

Table 4-828 por_rnd_por_rnd_s0_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s0_ar_lat_scale	Port S0 AR QoS scale factor 3'b000: 2 ⁽⁻⁵⁾ 3'b001: 2 ⁽⁻⁶⁾ 3'b010: 2 ⁽⁻⁷⁾ 3'b011: 2 ⁽⁻⁸⁾ 3'b100: 2 ⁽⁻⁹⁾ 3'b101: 2 ⁽⁻¹⁰⁾ 3'b110: 2 ⁽⁻¹¹⁾ 3'b111: 2 ⁽⁻¹²⁾	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	s0_aw_lat_scale	Port S0 AW QoS scale factor 3'b000: 2 ⁽⁻⁵⁾ 3'b001: 2 ⁽⁻⁶⁾ 3'b010: 2 ⁽⁻⁷⁾ 3'b011: 2 ⁽⁻⁸⁾ 3'b100: 2 ⁽⁻⁹⁾ 3'b101: 2 ⁽⁻¹⁰⁾ 3'b110: 2 ⁽⁻¹¹⁾ 3'b111: 2 ⁽⁻¹²⁾	RW	3'h0

por_rnd_s0_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S0 read and write transactions.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA98
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

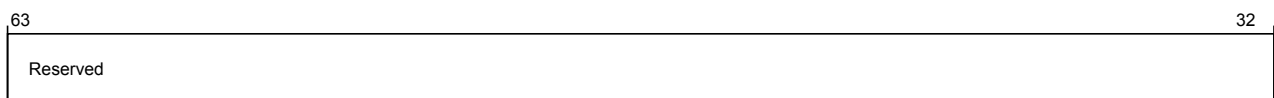


Figure 4-812 por_rnd_por_rnd_s0_qos_lat_range (high)

The following table shows the por_rnd_s0_qos_lat_range higher register bit assignments.

Table 4-829 por_rnd_por_rnd_s0_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

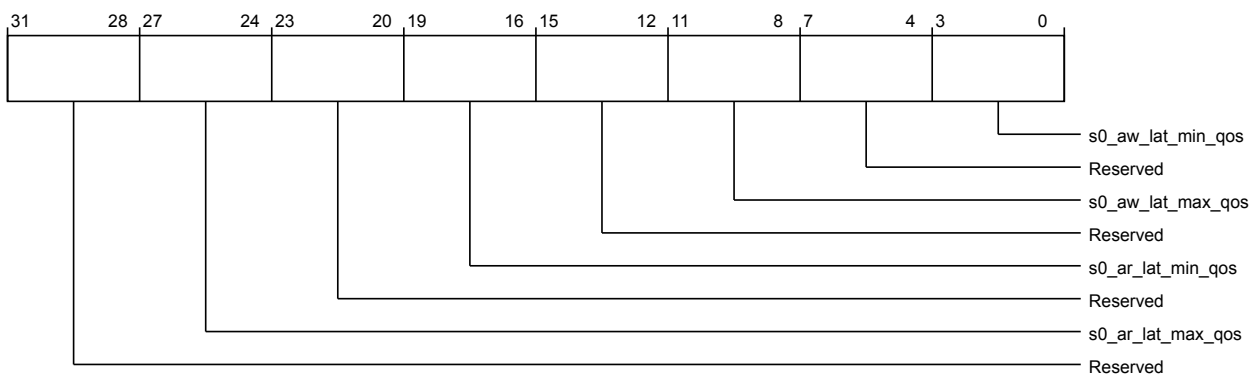


Figure 4-813 por_rnd_por_rnd_s0_qos_lat_range (low)

The following table shows the por_rnd_s0_qos_lat_range lower register bit assignments.

Table 4-830 `por_rnd_por_rnd_s0_qos_lat_range` (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	<code>s0_ar_lat_max_qos</code>	Port S0 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	<code>s0_ar_lat_min_qos</code>	Port S0 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	<code>s0_aw_lat_max_qos</code>	Port S0 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	<code>s0_aw_lat_min_qos</code>	Port S0 AW QoS minimum value	RW	4'h0

`por_rnd_s1_qos_control`

Controls QoS settings for port S1 AXI/ACE slave interface.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAA0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	<code>por_rnd_secure_register_groups_override.qos_ctrl</code>

The following image shows the higher register bit assignments.

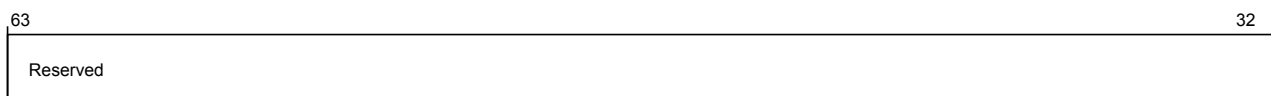


Figure 4-814 `por_rnd_por_rnd_s1_qos_control` (high)

The following table shows the `por_rnd_s1_qos_control` higher register bit assignments.

Table 4-831 `por_rnd_por_rnd_s1_qos_control` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

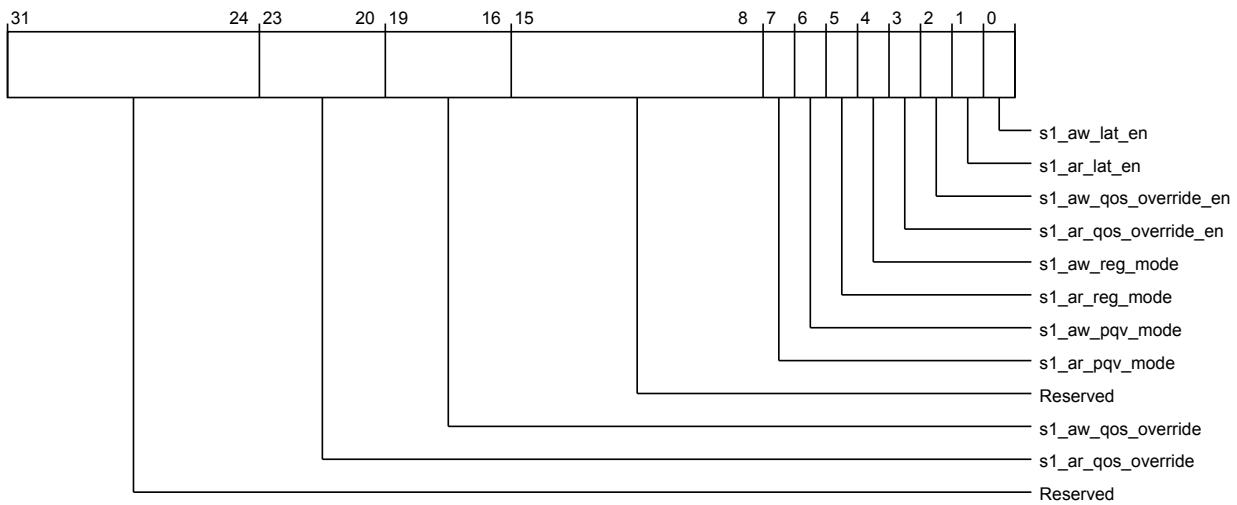


Figure 4-815 `por_rnd_por_rnd_s1_qos_control` (low)

The following table shows the `por_rnd_s1_qos_control` lower register bit assignments.

Table 4-832 `por_rnd_por_rnd_s1_qos_control` (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	<code>s1_ar_qos_override</code>	AR QoS override value for port S1	RW	4'b0000
19:16	<code>s1_aw_qos_override</code>	AW QoS override value for port S1	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	<code>s1_ar_pqv_mode</code>	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	<code>s1_aw_pqv_mode</code>	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	<code>s1_ar_reg_mode</code>	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	<code>s1_aw_reg_mode</code>	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	<code>s1_ar_qos_override_en</code>	Enables port S1 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0

Table 4-832 por_rnd_por_rnd_s1_qos_control (low) (continued)

Bits	Field name	Description	Type	Reset
2	s1_aw_qos_override_en	Enables port S1 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s1_ar_lat_en	Enables port S1 AR QoS regulation when set	RW	1'b0
0	s1_aw_lat_en	Enables port S1 AW QoS regulation when set	RW	1'b0

por_rnd_s1_qos_lat_tgt

Controls QoS target latency (in cycles) for regulation of port S1 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

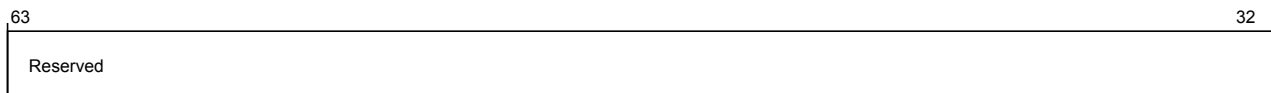


Figure 4-816 por_rnd_por_rnd_s1_qos_lat_tgt (high)

The following table shows the por_rnd_s1_qos_lat_tgt higher register bit assignments.

Table 4-833 por_rnd_por_rnd_s1_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

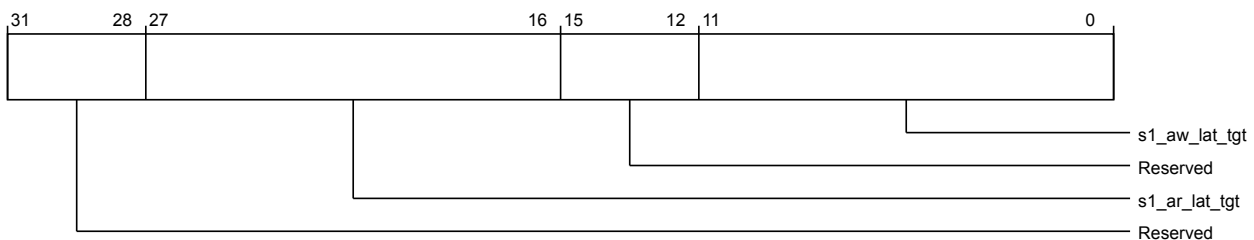


Figure 4-817 por_rnd_por_rnd_s1_qos_lat_tgt (low)

The following table shows the por_rnd_s1_qos_lat_tgt lower register bit assignments.

Table 4-834 `por_rnd_por_rnd_s1_qos_lat_tgt` (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	<code>s1_ar_lat_tgt</code>	Port S1 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	<code>s1_aw_lat_tgt</code>	Port S1 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

`por_rnd_s1_qos_lat_scale`

Controls the QoS target latency scale factor for port S1 read and write transactions. This register represents powers of two from the range $2^{(-5)}$ to $2^{(-12)}$; it is used to match a 16-bit integrator.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_rnd_secure_register_groups_override.qos_ctrl`

The following image shows the higher register bit assignments.

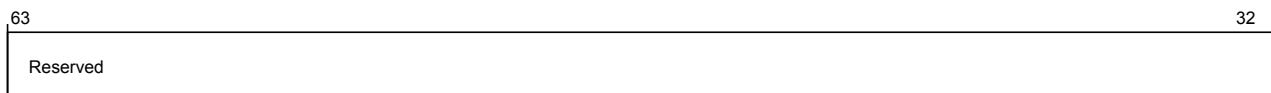


Figure 4-818 `por_rnd_por_rnd_s1_qos_lat_scale` (high)

The following table shows the `por_rnd_s1_qos_lat_scale` higher register bit assignments.

Table 4-835 `por_rnd_por_rnd_s1_qos_lat_scale` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

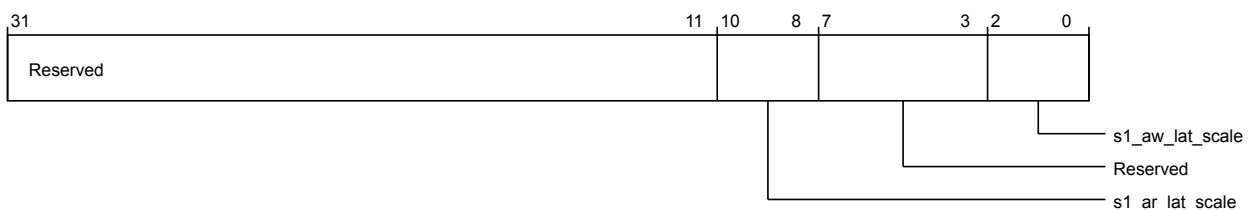


Figure 4-819 `por_rnd_por_rnd_s1_qos_lat_scale` (low)

The following table shows the `por_rnd_s1_qos_lat_scale` lower register bit assignments.

Table 4-836 `por_rnd_por_rnd_s1_qos_lat_scale` (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	<code>s1_ar_lat_scale</code>	Port S1 AR QoS scale factor 3'b000: 2 [^] (-5) 3'b001: 2 [^] (-6) 3'b010: 2 [^] (-7) 3'b011: 2 [^] (-8) 3'b100: 2 [^] (-9) 3'b101: 2 [^] (-10) 3'b110: 2 [^] (-11) 3'b111: 2 [^] (-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	<code>s1_aw_lat_scale</code>	Port S1 AW QoS scale factor 3'b000: 2 [^] (-5) 3'b001: 2 [^] (-6) 3'b010: 2 [^] (-7) 3'b011: 2 [^] (-8) 3'b100: 2 [^] (-9) 3'b101: 2 [^] (-10) 3'b110: 2 [^] (-11) 3'b111: 2 [^] (-12)	RW	3'h0

`por_rnd_s1_qos_lat_range`

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S1 read and write transactions.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAB8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	<code>por_rnd_secure_register_groups_override.qos_ctrl</code>

The following image shows the higher register bit assignments.

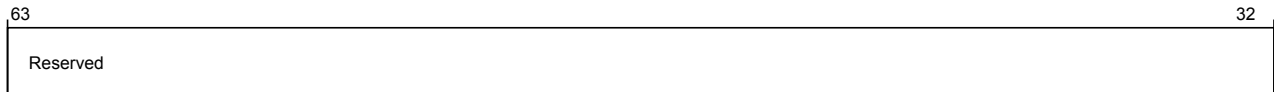


Figure 4-820 por_rnd_por_rnd_s1_qos_lat_range (high)

The following table shows the por_rnd_s1_qos_lat_range higher register bit assignments.

Table 4-837 por_rnd_por_rnd_s1_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

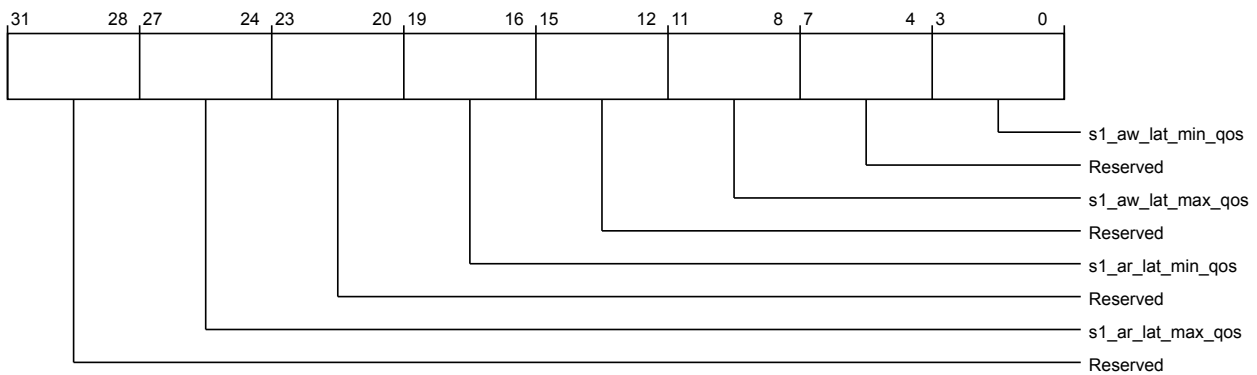


Figure 4-821 por_rnd_por_rnd_s1_qos_lat_range (low)

The following table shows the por_rnd_s1_qos_lat_range lower register bit assignments.

Table 4-838 por_rnd_por_rnd_s1_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s1_ar_lat_max_qos	Port S1 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s1_ar_lat_min_qos	Port S1 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s1_aw_lat_max_qos	Port S1 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s1_aw_lat_min_qos	Port S1 AW QoS minimum value	RW	4'h0

por_rnd_s2_qos_control

Controls QoS settings for port S2 AXI/ACE slave interface.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAC0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

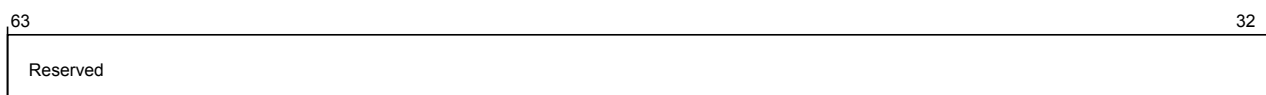


Figure 4-822 por_rnd_por_rnd_s2_qos_control (high)

The following table shows the por_rnd_s2_qos_control higher register bit assignments.

Table 4-839 por_rnd_por_rnd_s2_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

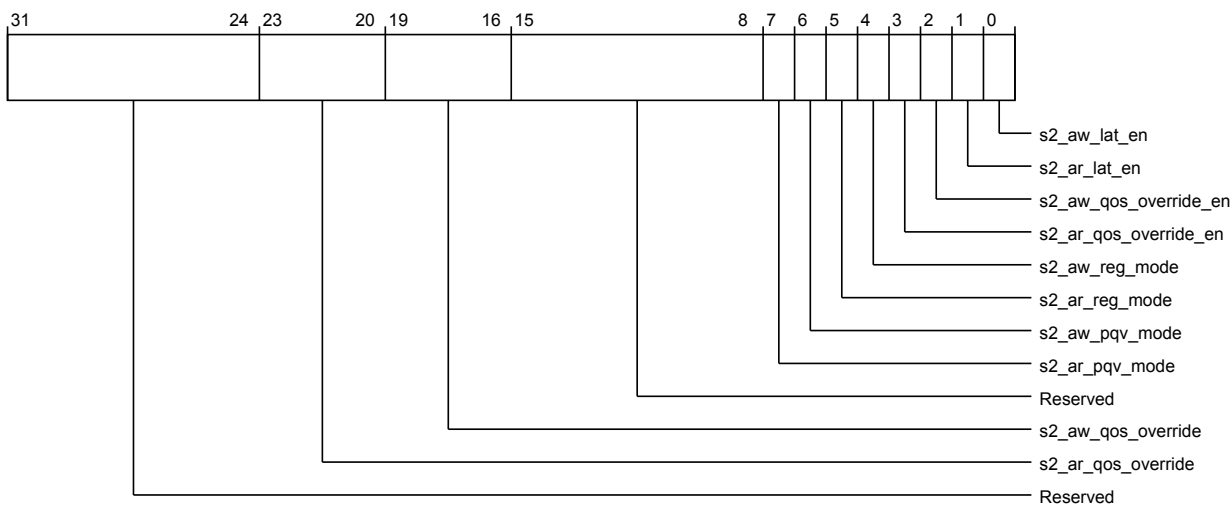


Figure 4-823 por_rnd_por_rnd_s2_qos_control (low)

The following table shows the por_rnd_s2_qos_control lower register bit assignments.

Table 4-840 `por_rnd_por_rnd_s2_qos_control` (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	<code>s2_ar_qos_override</code>	AR QoS override value for port S2	RW	4'b0000
19:16	<code>s2_aw_qos_override</code>	AW QoS override value for port S2	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	<code>s2_ar_pqv_mode</code>	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	<code>s2_aw_pqv_mode</code>	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	<code>s2_ar_reg_mode</code>	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	<code>s2_aw_reg_mode</code>	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	<code>s2_ar_qos_override_en</code>	Enables port S2 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	<code>s2_aw_qos_override_en</code>	Enables port S2 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	<code>s2_ar_lat_en</code>	Enables port S2 AR QoS regulation when set	RW	1'b0
0	<code>s2_aw_lat_en</code>	Enables port S2 AW QoS regulation when set	RW	1'b0

`por_rnd_s2_qos_lat_tgt`

Controls QoS target latency (in cycles) for regulation of port S2 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group `por_rnd_secure_register_groups_override.qos_ctrl`
override

The following image shows the higher register bit assignments.



Figure 4-824 `por_rnd_por_rnd_s2_qos_lat_tgt` (high)

The following table shows the `por_rnd_s2_qos_lat_tgt` higher register bit assignments.

Table 4-841 `por_rnd_por_rnd_s2_qos_lat_tgt` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

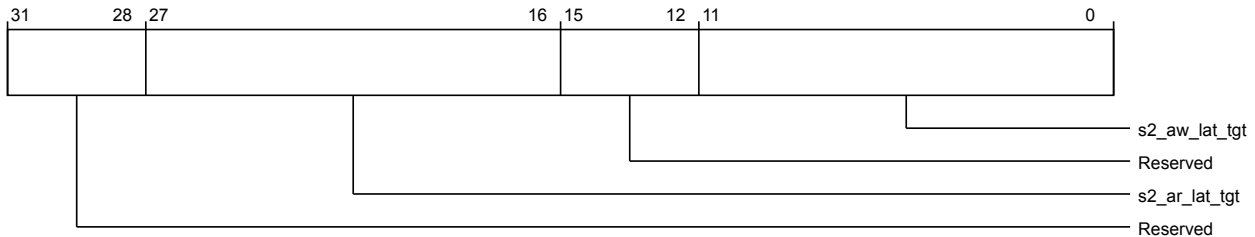


Figure 4-825 `por_rnd_por_rnd_s2_qos_lat_tgt` (low)

The following table shows the `por_rnd_s2_qos_lat_tgt` lower register bit assignments.

Table 4-842 `por_rnd_por_rnd_s2_qos_lat_tgt` (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	<code>s2_ar_lat_tgt</code>	Port S2 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	<code>s2_aw_lat_tgt</code>	Port S2 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

`por_rnd_s2_qos_lat_scale`

Controls the QoS target latency scale factor for port S2 read and write transactions. This register represents powers of two from the range $2^{(-5)}$ to $2^{(-12)}$; it is used to match a 16-bit integrator.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hAD0
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

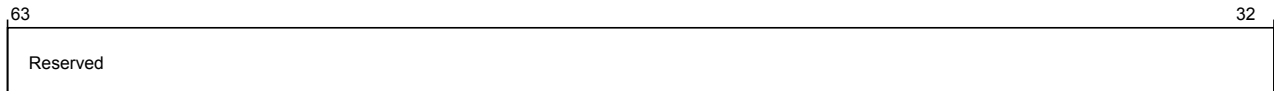


Figure 4-826 por_rnd_por_rnd_s2_qos_lat_scale (high)

The following table shows the por_rnd_s2_qos_lat_scale higher register bit assignments.

Table 4-843 por_rnd_por_rnd_s2_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

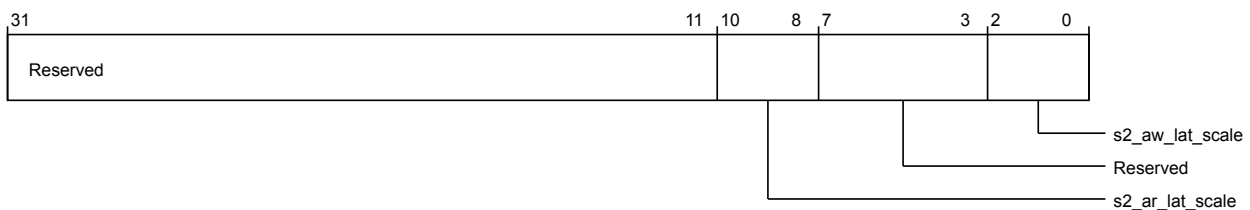


Figure 4-827 por_rnd_por_rnd_s2_qos_lat_scale (low)

The following table shows the por_rnd_s2_qos_lat_scale lower register bit assignments.

Table 4-844 por_rnd_por_rnd_s2_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s2_ar_lat_scale	Port S2 AR QoS scale factor 3'b000: 2 [^] (-5) 3'b001: 2 [^] (-6) 3'b010: 2 [^] (-7) 3'b011: 2 [^] (-8) 3'b100: 2 [^] (-9) 3'b101: 2 [^] (-10) 3'b110: 2 [^] (-11) 3'b111: 2 [^] (-12)	RW	3'h0

Table 4-844 `por_rnd_por_rnd_s2_qos_lat_scale` (low) (continued)

Bits	Field name	Description	Type	Reset
7:3	Reserved	Reserved	RO	-
2:0	<code>s2_aw_lat_scale</code>	Port S2 AW QoS scale factor 3'b000: $2^{(-5)}$ 3'b001: $2^{(-6)}$ 3'b010: $2^{(-7)}$ 3'b011: $2^{(-8)}$ 3'b100: $2^{(-9)}$ 3'b101: $2^{(-10)}$ 3'b110: $2^{(-11)}$ 3'b111: $2^{(-12)}$	RW	3'h0

`por_rnd_s2_qos_lat_range`

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S2 read and write transactions.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAD8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	<code>por_rnd_secure_register_groups_override.qos_ctrl</code>

The following image shows the higher register bit assignments.

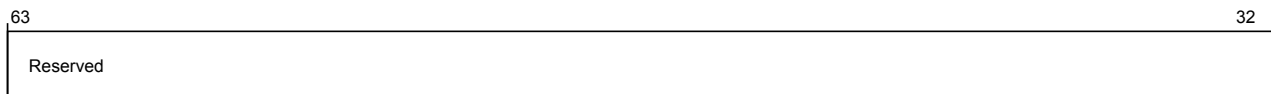


Figure 4-828 `por_rnd_por_rnd_s2_qos_lat_range` (high)

The following table shows the `por_rnd_s2_qos_lat_range` higher register bit assignments.

Table 4-845 `por_rnd_por_rnd_s2_qos_lat_range` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

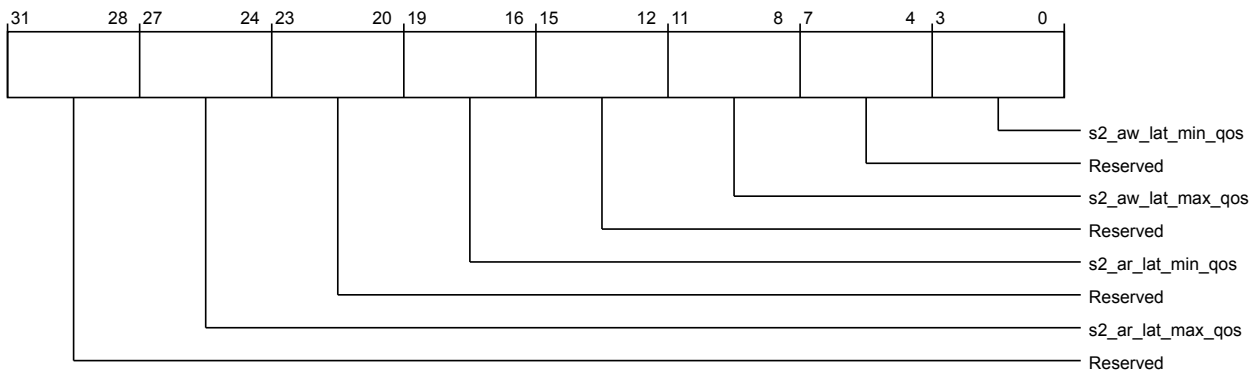


Figure 4-829 `por_rnd_por_rnd_s2_qos_lat_range` (low)

The following table shows the `por_rnd_s2_qos_lat_range` lower register bit assignments.

Table 4-846 `por_rnd_por_rnd_s2_qos_lat_range` (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	<code>s2_ar_lat_max_qos</code>	Port S2 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	<code>s2_ar_lat_min_qos</code>	Port S2 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	<code>s2_aw_lat_max_qos</code>	Port S2 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	<code>s2_aw_lat_min_qos</code>	Port S2 AW QoS minimum value	RW	4'h0

`por_rnd_pmu_event_sel`

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

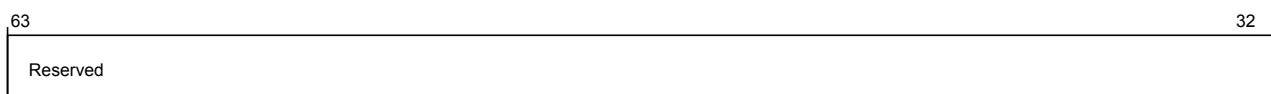


Figure 4-830 `por_rnd_por_rnd_pmu_event_sel` (high)

The following table shows the `por_rnd_pmu_event_sel` higher register bit assignments.

Table 4-847 `por_rnd_por_rnd_pmu_event_sel` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

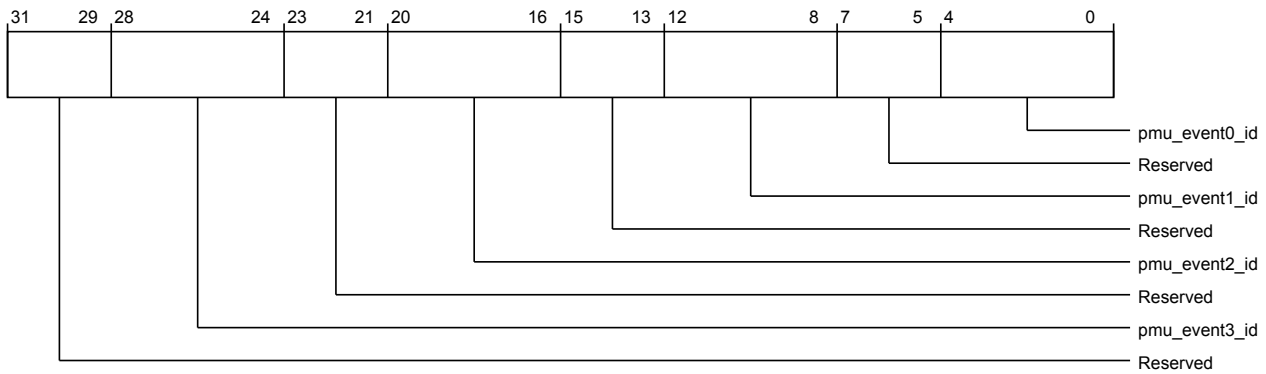


Figure 4-831 `por_rnd_por_rnd_pmu_event_sel` (low)

The following table shows the `por_rnd_pmu_event_sel` lower register bit assignments.

Table 4-848 `por_rnd_por_rnd_pmu_event_sel` (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	<code>pmu_event3_id</code>	RN-D PMU Event 3 ID; see <code>pmu_event0_id</code> for encodings	RW	5'b0
23:21	Reserved	Reserved	RO	-
20:16	<code>pmu_event2_id</code>	RN-D PMU Event 2 ID; see <code>pmu_event0_id</code> for encodings	RW	5'b0
15:13	Reserved	Reserved	RO	-
12:8	<code>pmu_event1_id</code>	RN-D PMU Event 1 ID; see <code>pmu_event0_id</code> for encodings	RW	5'b0

Table 4-848 `por_rnd_por_rnd_pmu_event_sel` (low) (continued)

Bits	Field name	Description	Type	Reset
7:5	Reserved	Reserved	RO	-
4:0	<code>pmu_event0_id</code>	RN-D PMU Event 0 ID 5'h00: No event 5'h01: Port S0 RDataBeats 5'h02: Port S1 RDataBeats 5'h03: Port S2 RDataBeats 5'h04: RXDAT flits received 5'h05: TXDAT flits sent 5'h06: Total TXREQ flits sent 5'h07: Retried TXREQ flits sent 5'h08: RRT occupancy count overflow 5'h09: WRT occupancy count overflow 5'h0A: Replayed TXREQ flits 5'h0B: WriteCancel sent 5'h0C: Port S0 WDataBeats 5'h0D: Port S1 WDataBeats 5'h0E: Port S2 WDataBeats 5'h0F: RRT allocation 5'h10: WRT allocation 5'h11: RDB pool state is all unordered 5'h12: RDB pool state is replay 5'h13: RDB pool state is hybrid 5'h14: RDB pool state is all ordered	RW	5'b0

`por_rnd_syscoreq_ctl`

Functions as the RN-D DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with `por_rnd_syscoack_status`.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1000
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

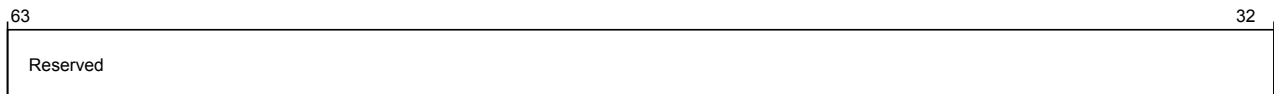


Figure 4-832 por_rnd_por_rnd_syscoreq_ctl (high)

The following table shows the por_rnd_syscoreq_ctl higher register bit assignments.

Table 4-849 por_rnd_por_rnd_syscoreq_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

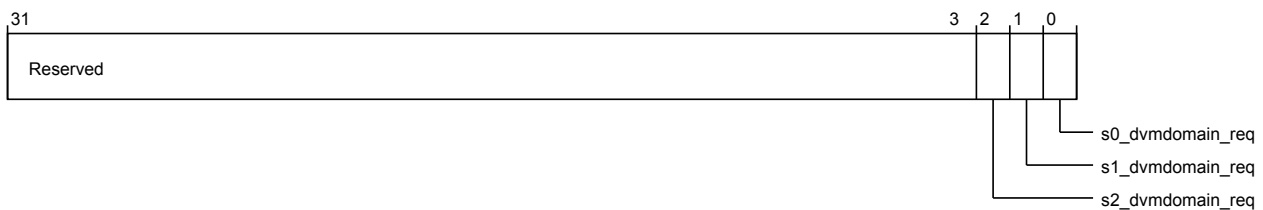


Figure 4-833 por_rnd_por_rnd_syscoreq_ctl (low)

The following table shows the por_rnd_syscoreq_ctl lower register bit assignments.

Table 4-850 por_rnd_por_rnd_syscoreq_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	s2_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S2	RW	1'b0
1	s1_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S1	RW	1'b0
0	s0_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S0	RW	1'b0

por_rnd_syscoack_status

Functions as the RN-D DVM domain status register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_rnd_syscoreq_ctl.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h1008
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

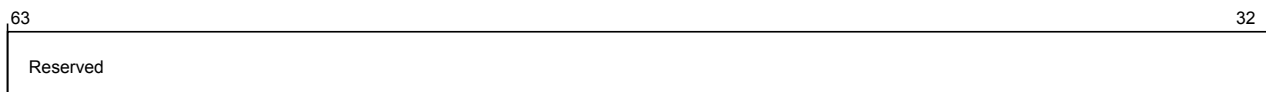


Figure 4-834 `por_rnd_por_rnd_syscoack_status` (high)

The following table shows the `por_rnd_syscoack_status` higher register bit assignments.

Table 4-851 `por_rnd_por_rnd_syscoack_status` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

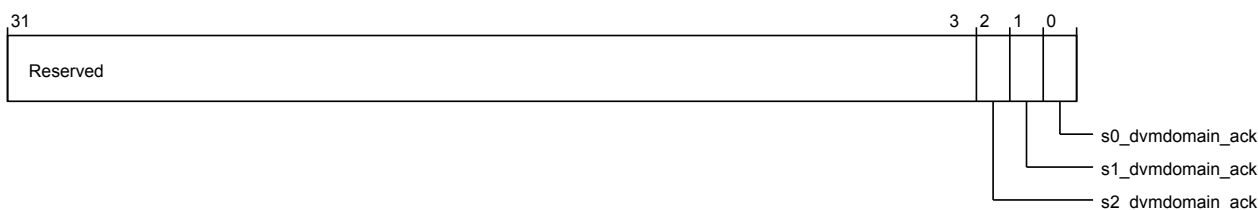


Figure 4-835 `por_rnd_por_rnd_syscoack_status` (low)

The following table shows the `por_rnd_syscoack_status` lower register bit assignments.

Table 4-852 `por_rnd_por_rnd_syscoack_status` (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	<code>s2_dvmdomain_ack</code>	Provides DVM domain status (SYSCOACK) for port S2	RO	1'b0
1	<code>s1_dvmdomain_ack</code>	Provides DVM domain status (SYSCOACK) for port S1	RO	1'b0
0	<code>s0_dvmdomain_ack</code>	Provides DVM domain status (SYSCOACK) for port S0	RO	1'b0

4.3.8 RN-I register descriptions

Lists the RN-I registers.

por_rni_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

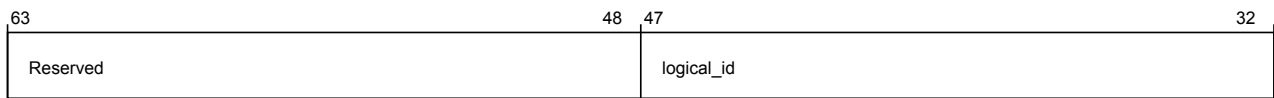


Figure 4-836 por_rni_node_info (high)

The following table shows the por_rni_node_info higher register bit assignments.

Table 4-853 por_rni_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

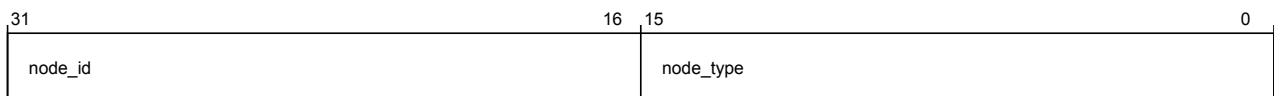


Figure 4-837 por_rni_node_info (low)

The following table shows the por_rni_node_info lower register bit assignments.

Table 4-854 por_rni_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h000A

por_rni_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

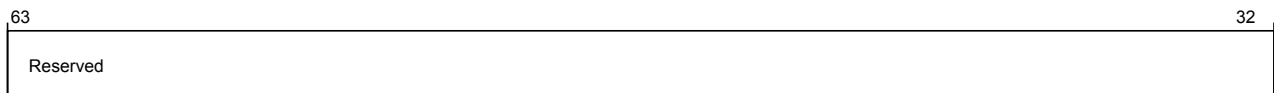


Figure 4-838 por_rni_por_rni_child_info (high)

The following table shows the por_rni_child_info higher register bit assignments.

Table 4-855 por_rni_por_rni_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

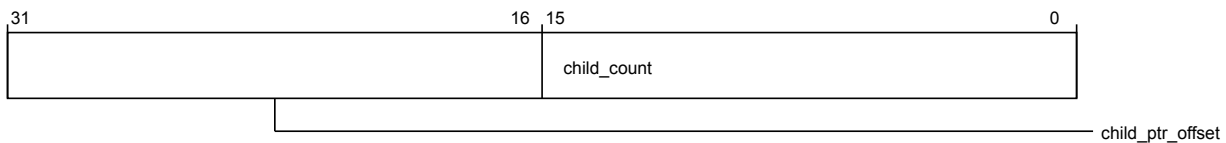


Figure 4-839 por_rni_por_rni_child_info (low)

The following table shows the por_rni_child_info lower register bit assignments.

Table 4-856 por_rni_por_rni_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

por_rni_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type	RW
Register width (Bits)	64

Address offset	14'h980
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

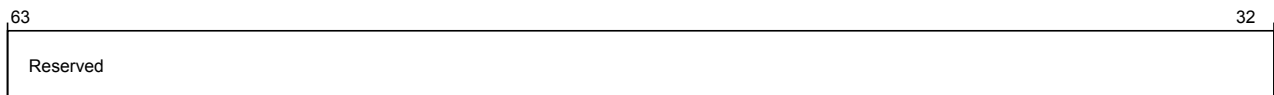


Figure 4-840 por_rni_secure_register_groups_override (high)

The following table shows the por_rni_secure_register_groups_override higher register bit assignments.

Table 4-857 por_rni_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

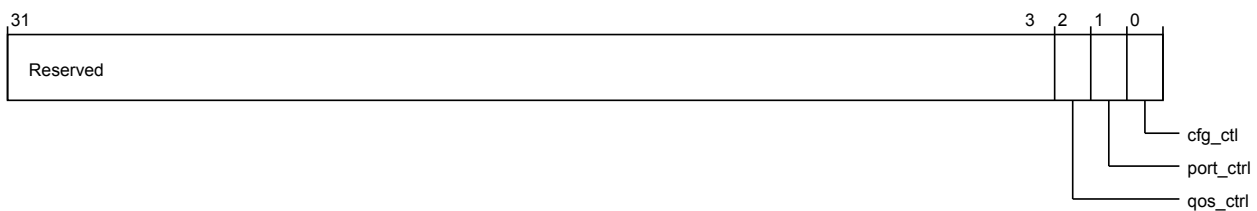


Figure 4-841 por_rni_secure_register_groups_override (low)

The following table shows the por_rni_secure_register_groups_override lower register bit assignments.

Table 4-858 por_rni_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	qos_ctrl	Allows non-secure access to secure QoS control registers	RW	1'b0
1	port_ctrl	Allows non-secure access to secure AXI port control registers	RW	1'b0
0	cfg_ctl	Allows non-secure access to secure configuration control register	RW	1'b0

por_rni_unit_info

Provides component identification information for RN-I.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

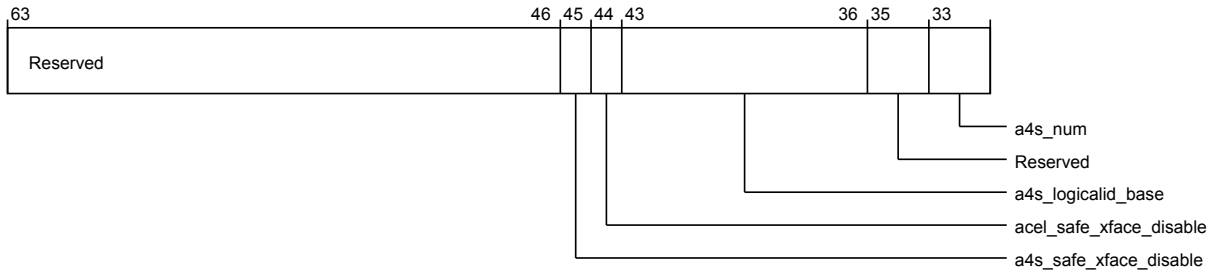


Figure 4-842 por_rni_por_rni_unit_info (high)

The following table shows the por_rni_unit_info higher register bit assignments.

Table 4-859 por_rni_por_rni_unit_info (high)

Bits	Field name	Description	Type	Reset
63:46	Reserved	Reserved	RO	-
45	a4s_safe_xface_disable	AXI4Stream safe interface disable	RO	Configuration dependent
44	acel_safe_xface_disable	ACE-Lite/AXI4 safe interface disable	RO	Configuration dependent
43:36	a4s_logicalid_base	AXI4Stream interfaces logical ID base	RO	Configuration dependent
35:34	Reserved	Reserved	RO	-
33:32	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent

The following image shows the lower register bit assignments.

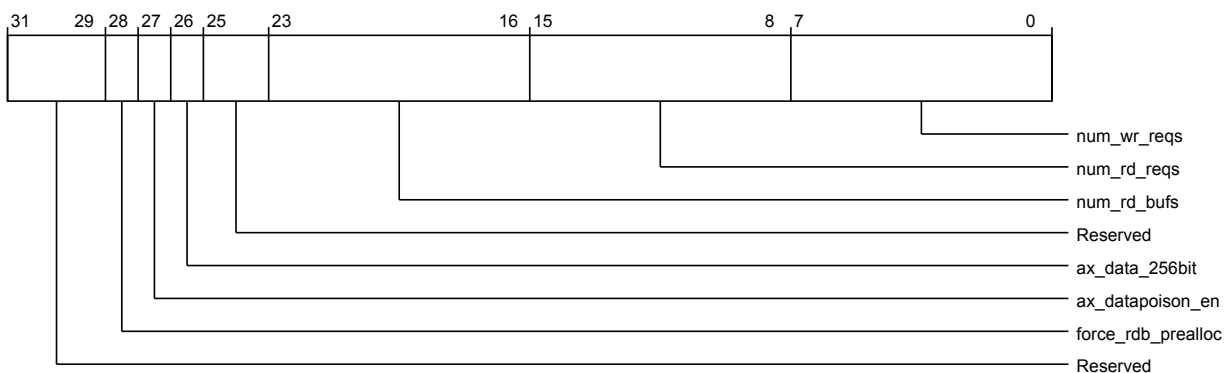


Figure 4-843 por_rni_por_rni_unit_info (low)

The following table shows the por_rni_unit_info lower register bit assignments.

Table 4-860 por_rni_por_rni_unit_info (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28	force_rdb_prealloc	Force read data buffer preallocation l'b1: yes l'b0: no	RO	Configuration dependent
27	ax_datapoison_en	Data poison enable on ACE-Lite/AXI4 interface l'b1: Enabled l'b0: Not enabled	RO	Configuration dependent
26	ax_data_256bit	AXI interface data width l'b1: 256 bits l'b0: 128 bits	RO	Configuration dependent
25:24	Reserved	Reserved	RO	-
23:16	num_rd_bufs	Number of read data buffers	RO	Configuration dependent
15:8	num_rd_reqs	Number of outstanding read requests	RO	Configuration dependent
7:0	num_wr_reqs	Number of outstanding write requests	RO	Configuration dependent

por_rni_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA00
Register reset	Configuration dependent
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rni_secure_register_groups_override.cfg_ctl

The following image shows the higher register bit assignments.

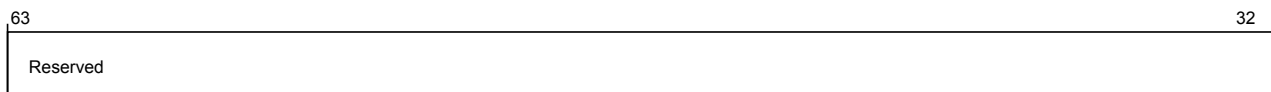


Figure 4-844 por_rni_por_rni_cfg_ctl (high)

The following table shows the por_rni_cfg_ctl higher register bit assignments.

Table 4-861 por_rni_por_rni_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

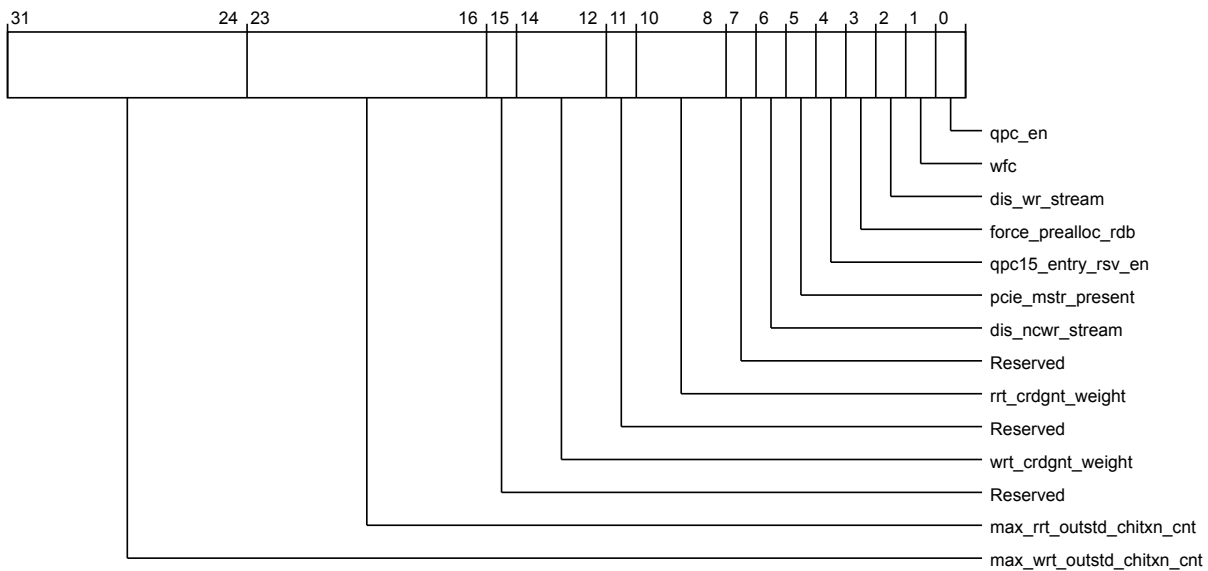


Figure 4-845 por_rni_por_rni_cfg_ctl (low)

The following table shows the `por_rni_cfg_ctl` lower register bit assignments.

Table 4-862 por_rni_por_rni_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:24	<code>max_wrt_outstd_chitxn_cnt</code>	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent
23:16	<code>max_rrt_outstd_chitxn_cnt</code>	Maximum number of outstanding reads allowed on CHI-side	RW	Configuration dependent
15	Reserved	Reserved	RO	-
14:12	<code>wrt_crdgnt_weight</code>	Determines weight of credit grant allocated to retried writes in presence of pending retried reads	RW	3'b001
11	Reserved	Reserved	RO	-
10:8	<code>rrt_crdgnt_weight</code>	Determines weight of credit grant allocated to retried reads in presence of pending retried writes	RW	3'b100
7	Reserved	Reserved	RO	-
6	<code>dis_ncwr_stream</code>	Disables streaming of ordered non-cacheable writes when set	RW	1'b0
5	<code>pcie_mstr_present</code>	Indicates PCIe master is present; must be set if PCIe master is present upstream of RN-I or RN-D	RW	1'b0

Table 4-862 por_rni_por_rni_cfg_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
4	qpc15_entry_rsv_en	Enables QPC15 entry reservation 1'b1: Reserves tracker entry for QoS15 requests 1'b0: Does not reserve tracker entry for QoS15 requests NOTE: Only valid and applicable when por_rni_qpc_en is set	RW	1'b0
3	force_prealloc_rdb	When set, all reads from the RN-I are sent with a preallocated read data buffer	RW	Configuration dependent
2	dis_wr_stream	Disables streaming of ordered writes when set	RW	1'b0
1	wfc	When set, enables waiting for completion (COMP) before dispatching dependent transaction (TXN)	RW	1'b0
0	qpc_en	When set, enables QPC-based scheduling using two QoS priority classes (QoS15 and non-QoS15)	RW	1'b1

por_rni_aux_ctl

Functions as the auxiliary control register for RN-I.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA08
Register reset	Configuration dependent
Usage constraints	Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

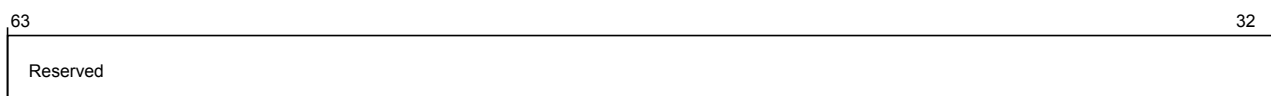


Figure 4-846 por_rni_por_rni_aux_ctl (high)

The following table shows the por_rni_aux_ctl higher register bit assignments.

Table 4-863 por_rni_por_rni_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

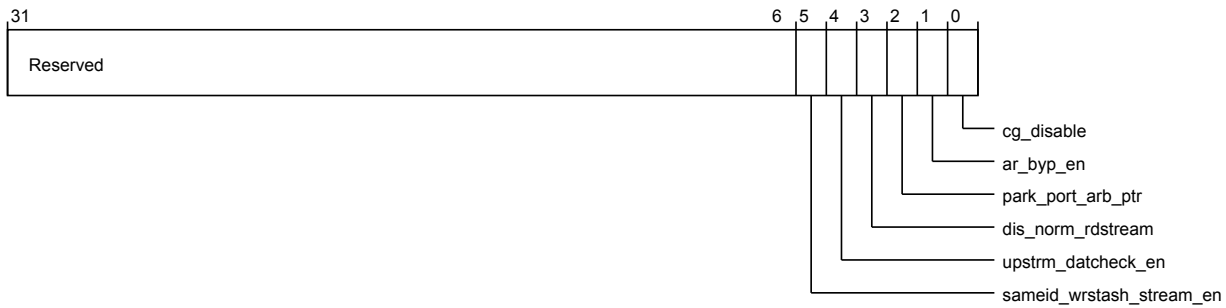


Figure 4-847 `por_rni_por_rni_aux_ctl` (low)

The following table shows the `por_rni_aux_ctl` lower register bit assignments.

Table 4-864 `por_rni_por_rni_aux_ctl` (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5	<code>sameid_wrstash_stream_en</code>	Enables streaming of same-ID WrUniqStash	RW	Configuration dependent
4	<code>upstrm_datcheck_en</code>	Upstream supports Datacheck	RW	Configuration dependent
3	<code>dis_norm_rdstream</code>	Disables streaming of same ARID normal memory reads to different address	RW	1'b0
2	<code>park_port_arb_ptr</code>	Parks the AXI port arbitration pointer for Burst	RW	1'b0
1	<code>ar_byp_en</code>	AR bypass enable; enables bypass path in the AR pipeline	RW	1'b1
0	<code>cg_disable</code>	Disables clock gating when set	RW	1'b0

`por_rni_s0_port_control`

Controls port S0 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_rni_secure_register_groups_override.port_ctrl`

The following image shows the higher register bit assignments.

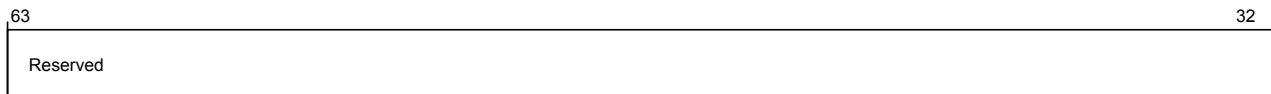


Figure 4-848 por_rni_por_rni_s0_port_control (high)

The following table shows the por_rni_s0_port_control higher register bit assignments.

Table 4-865 por_rni_por_rni_s0_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

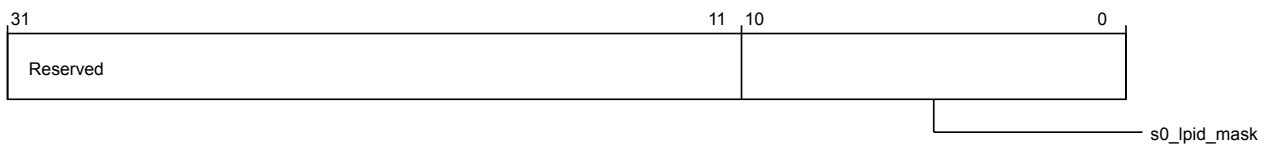


Figure 4-849 por_rni_por_rni_s0_port_control (low)

The following table shows the por_rni_s0_port_control lower register bit assignments.

Table 4-866 por_rni_por_rni_s0_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s0_lpid_mask	Port S0 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rni_s1_port_control

Controls port S1 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA18

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.port_ctrl

The following image shows the higher register bit assignments.

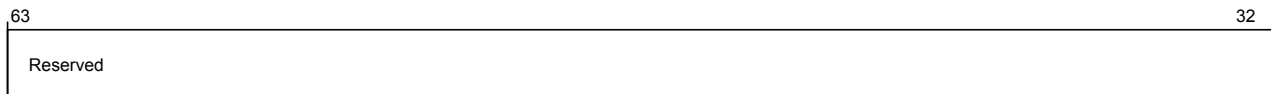


Figure 4-850 por_rni_por_rni_s1_port_control (high)

The following table shows the por_rni_s1_port_control higher register bit assignments.

Table 4-867 por_rni_por_rni_s1_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

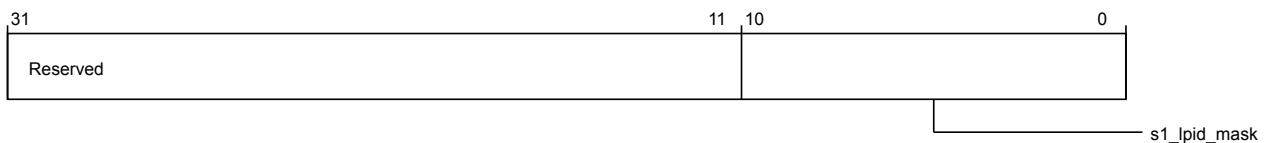


Figure 4-851 por_rni_por_rni_s1_port_control (low)

The following table shows the por_rni_s1_port_control lower register bit assignments.

Table 4-868 por_rni_por_rni_s1_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s1_lpid_mask	Port S1 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rni_s2_port_control

Controls port S2 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA20

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.port_ctrl

The following image shows the higher register bit assignments.

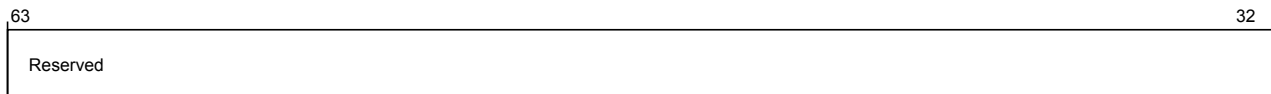


Figure 4-852 por_rni_por_rni_s2_port_control (high)

The following table shows the por_rni_s2_port_control higher register bit assignments.

Table 4-869 por_rni_por_rni_s2_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

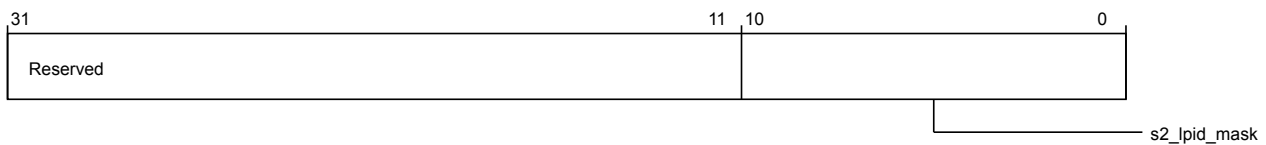


Figure 4-853 por_rni_por_rni_s2_port_control (low)

The following table shows the por_rni_s2_port_control lower register bit assignments.

Table 4-870 por_rni_por_rni_s2_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s2_lpid_mask	Port S2 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rni_s0_qos_control

Controls QoS settings for port S0 AXI/ACE slave interface.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA80
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

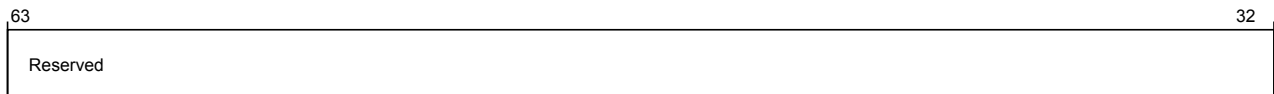


Figure 4-854 por_rni_por_rni_s0_qos_control (high)

The following table shows the por_rni_s0_qos_control higher register bit assignments.

Table 4-871 por_rni_por_rni_s0_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

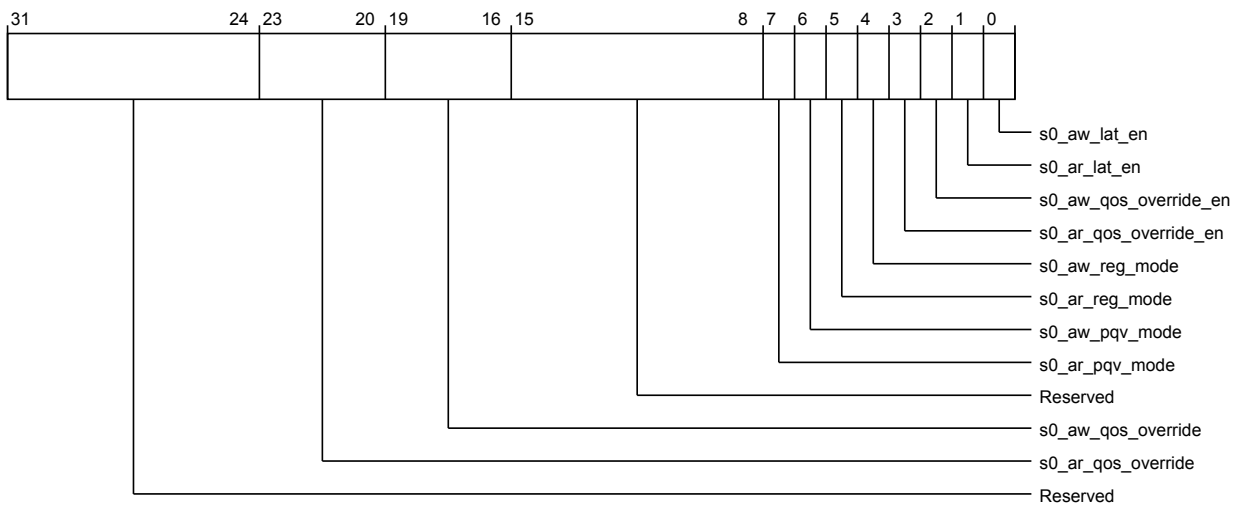


Figure 4-855 por_rni_por_rni_s0_qos_control (low)

The following table shows the por_rni_s0_qos_control lower register bit assignments.

Table 4-872 por_rni_por_rni_s0_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s0_ar_qos_override	AR QoS override value for port S0	RW	4'b0000
19:16	s0_aw_qos_override	AW QoS override value for port S0	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s0_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0

Table 4-872 `por_rni_por_rni_s0_qos_control` (low) (continued)

Bits	Field name	Description	Type	Reset
6	<code>s0_aw_pqv_mode</code>	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	<code>s0_ar_reg_mode</code>	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	<code>s0_aw_reg_mode</code>	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	<code>s0_ar_qos_override_en</code>	Enables port S0 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	<code>s0_aw_qos_override_en</code>	Enables port S0 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	<code>s0_ar_lat_en</code>	Enables port S0 AR QoS regulation when set	RW	1'b0
0	<code>s0_aw_lat_en</code>	Enables port S0 AW QoS regulation when set	RW	1'b0

`por_rni_s0_qos_lat_tgt`

Controls QoS target latency (in cycles) for regulations of port S0 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA88

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_rni_secure_register_groups_override.qos_ctrl`

The following image shows the higher register bit assignments.

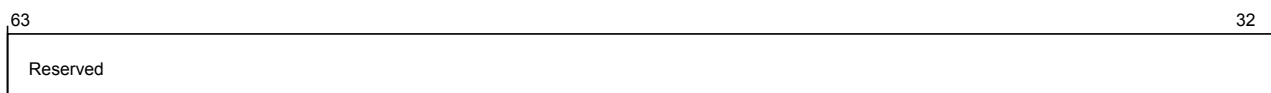


Figure 4-856 `por_rni_por_rni_s0_qos_lat_tgt` (high)

The following table shows the `por_rni_s0_qos_lat_tgt` higher register bit assignments.

Table 4-873 `por_rni_por_rni_s0_qos_lat_tgt` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

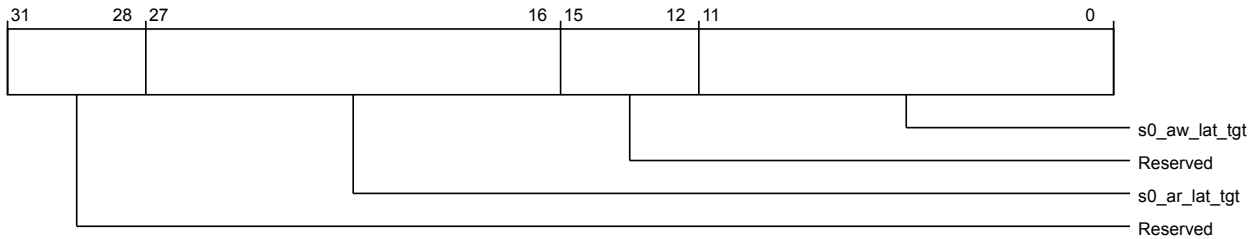


Figure 4-857 `por_rni_por_rni_s0_qos_lat_tgt` (low)

The following table shows the `por_rni_s0_qos_lat_tgt` lower register bit assignments.

Table 4-874 `por_rni_por_rni_s0_qos_lat_tgt` (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	<code>s0_ar_lat_tgt</code>	Port S0 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	<code>s0_aw_lat_tgt</code>	Port S0 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

`por_rni_s0_qos_lat_scale`

Controls the QoS target latency scale factor for port S0 read and write transactions. This register represents powers of two from the range $2^{(-5)}$ to $2^{(-12)}$; it is used to match a 16-bit integrator.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA90

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_rni_secure_register_groups_override.qos_ctrl`

The following image shows the higher register bit assignments.

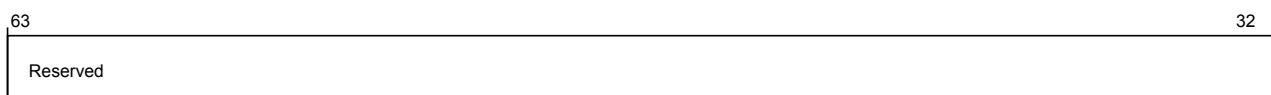


Figure 4-858 `por_rni_por_rni_s0_qos_lat_scale` (high)

The following table shows the por_rni_s0_qos_lat_scale higher register bit assignments.

Table 4-875 por_rni_por_rni_s0_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

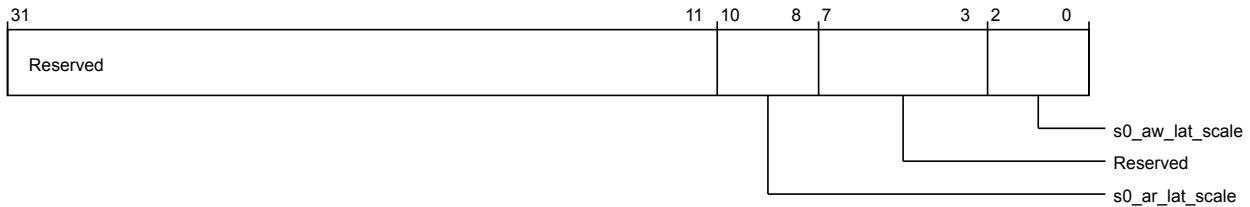


Figure 4-859 por_rni_por_rni_s0_qos_lat_scale (low)

The following table shows the por_rni_s0_qos_lat_scale lower register bit assignments.

Table 4-876 por_rni_por_rni_s0_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s0_ar_lat_scale	Port S0 AR QoS scale factor 3'b000: 2 [^] (-5) 3'b001: 2 [^] (-6) 3'b010: 2 [^] (-7) 3'b011: 2 [^] (-8) 3'b100: 2 [^] (-9) 3'b101: 2 [^] (-10) 3'b110: 2 [^] (-11) 3'b111: 2 [^] (-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	s0_aw_lat_scale	Port S0 AW QoS scale factor 3'b000: 2 [^] (-5) 3'b001: 2 [^] (-6) 3'b010: 2 [^] (-7) 3'b011: 2 [^] (-8) 3'b100: 2 [^] (-9) 3'b101: 2 [^] (-10) 3'b110: 2 [^] (-11) 3'b111: 2 [^] (-12)	RW	3'h0

por_rni_s0_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S0 read and write transactions.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA98
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rni_secure_register_groups_override.qos_ctl

The following image shows the higher register bit assignments.

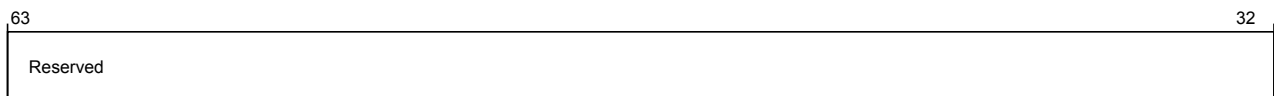


Figure 4-860 por_rni_por_rni_s0_qos_lat_range (high)

The following table shows the por_rni_s0_qos_lat_range higher register bit assignments.

Table 4-877 por_rni_por_rni_s0_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

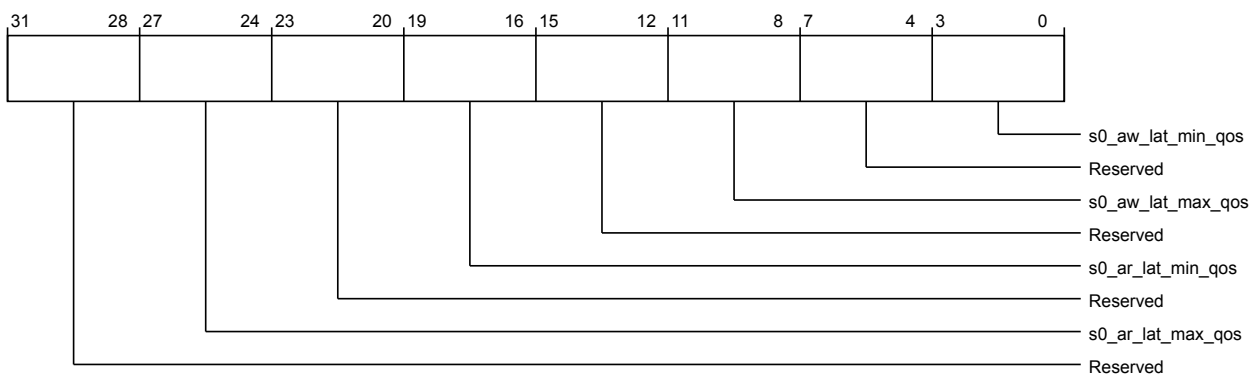


Figure 4-861 por_rni_por_rni_s0_qos_lat_range (low)

The following table shows the por_rni_s0_qos_lat_range lower register bit assignments.

Table 4-878 por_rni_por_rni_s0_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s0_ar_lat_max_qos	Port S0 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s0_ar_lat_min_qos	Port S0 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s0_aw_lat_max_qos	Port S0 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s0_aw_lat_min_qos	Port S0 AW QoS minimum value	RW	4'h0

por_rni_s1_qos_control

Controls QoS settings for port S1 AXI/ACE slave interface.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAA0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

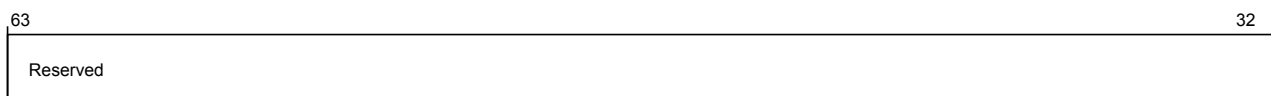


Figure 4-862 por_rni_por_rni_s1_qos_control (high)

The following table shows the por_rni_s1_qos_control higher register bit assignments.

Table 4-879 por_rni_por_rni_s1_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

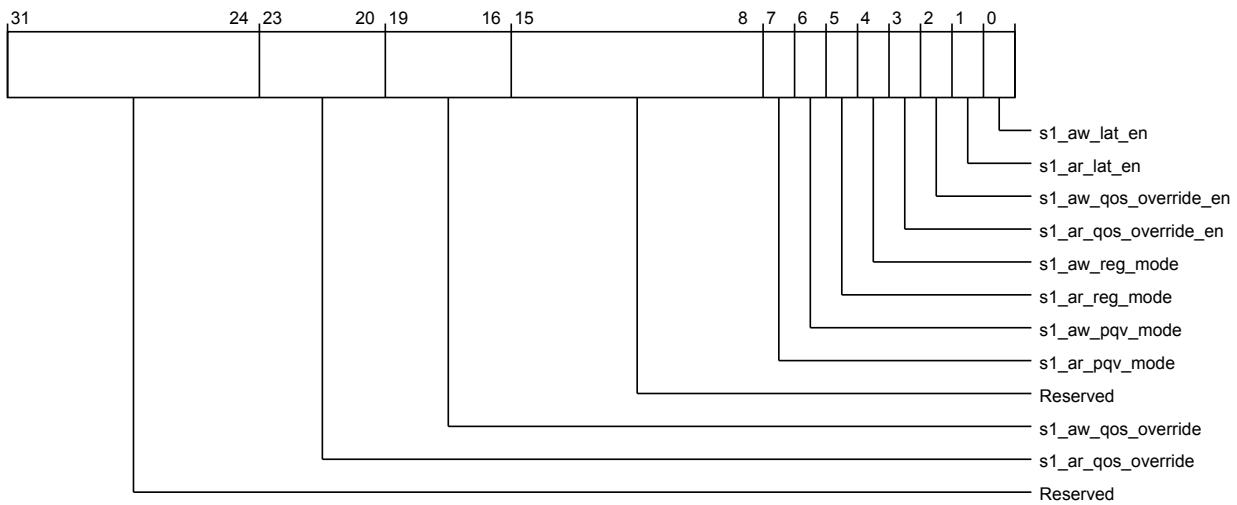


Figure 4-863 `por_rni_por_rni_s1_qos_control` (low)

The following table shows the `por_rni_s1_qos_control` lower register bit assignments.

Table 4-880 `por_rni_por_rni_s1_qos_control` (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	<code>s1_ar_qos_override</code>	AR QoS override value for port S1	RW	4'b0000
19:16	<code>s1_aw_qos_override</code>	AW QoS override value for port S1	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	<code>s1_ar_pqv_mode</code>	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	<code>s1_aw_pqv_mode</code>	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	<code>s1_ar_reg_mode</code>	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	<code>s1_aw_reg_mode</code>	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	<code>s1_ar_qos_override_en</code>	Enables port S1 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0

Table 4-880 `por_rni_por_rni_s1_qos_control` (low) (continued)

Bits	Field name	Description	Type	Reset
2	<code>s1_aw_qos_override_en</code>	Enables port S1 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	<code>s1_ar_lat_en</code>	Enables port S1 AR QoS regulation when set	RW	1'b0
0	<code>s1_aw_lat_en</code>	Enables port S1 AW QoS regulation when set	RW	1'b0

`por_rni_s1_qos_lat_tgt`

Controls QoS target latency (in cycles) for regulation of port S1 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_rni_secure_register_groups_override.qos_ctrl`

The following image shows the higher register bit assignments.

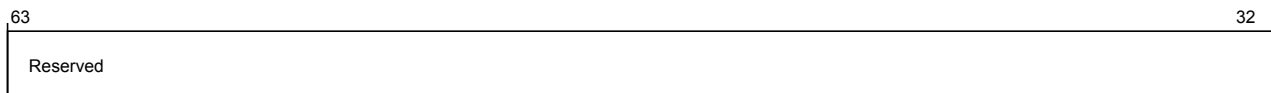


Figure 4-864 `por_rni_por_rni_s1_qos_lat_tgt` (high)

The following table shows the `por_rni_s1_qos_lat_tgt` higher register bit assignments.

Table 4-881 `por_rni_por_rni_s1_qos_lat_tgt` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

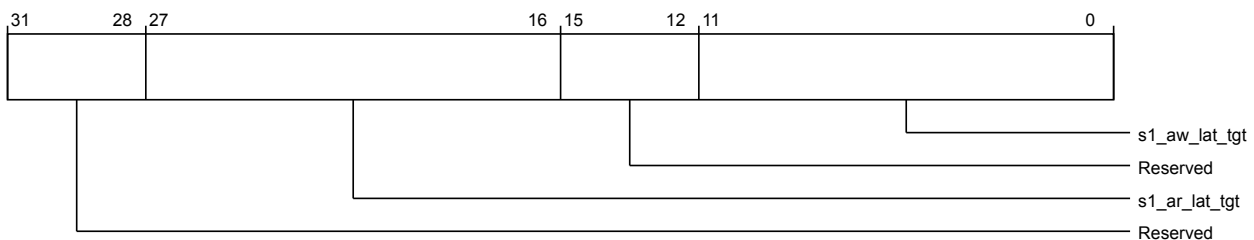


Figure 4-865 `por_rni_por_rni_s1_qos_lat_tgt` (low)

The following table shows the `por_rni_s1_qos_lat_tgt` lower register bit assignments.

Table 4-882 `por_rni_por_rni_s1_qos_lat_tgt` (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	<code>s1_ar_lat_tgt</code>	Port S1 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	<code>s1_aw_lat_tgt</code>	Port S1 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

`por_rni_s1_qos_lat_scale`

Controls the QoS target latency scale factor for port S1 read and write transactions. This register represents powers of two from the range $2^{(-5)}$ to $2^{(-12)}$; it is used to match a 16-bit integrator.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override `por_rni_secure_register_groups_override.qos_ctrl`

The following image shows the higher register bit assignments.

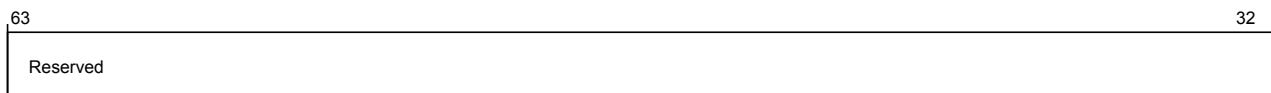


Figure 4-866 `por_rni_por_rni_s1_qos_lat_scale` (high)

The following table shows the `por_rni_s1_qos_lat_scale` higher register bit assignments.

Table 4-883 `por_rni_por_rni_s1_qos_lat_scale` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

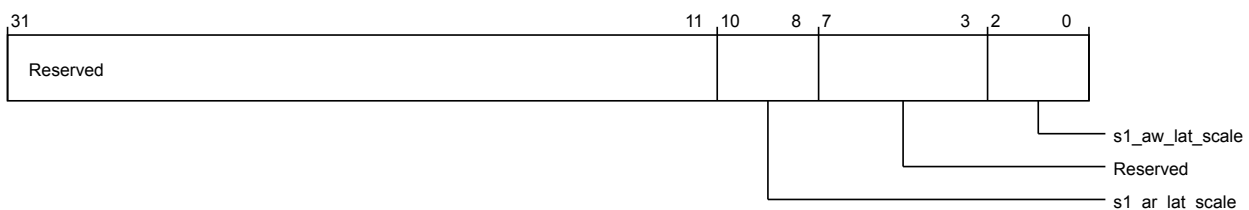


Figure 4-867 `por_rni_por_rni_s1_qos_lat_scale` (low)

The following table shows the `por_rni_s1_qos_lat_scale` lower register bit assignments.

Table 4-884 `por_rni_por_rni_s1_qos_lat_scale` (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	<code>s1_ar_lat_scale</code>	Port S1 AR QoS scale factor 3'b000: $2^{(-5)}$ 3'b001: $2^{(-6)}$ 3'b010: $2^{(-7)}$ 3'b011: $2^{(-8)}$ 3'b100: $2^{(-9)}$ 3'b101: $2^{(-10)}$ 3'b110: $2^{(-11)}$ 3'b111: $2^{(-12)}$	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	<code>s1_aw_lat_scale</code>	Port S1 AW QoS scale factor 3'b000: $2^{(-5)}$ 3'b001: $2^{(-6)}$ 3'b010: $2^{(-7)}$ 3'b011: $2^{(-8)}$ 3'b100: $2^{(-9)}$ 3'b101: $2^{(-10)}$ 3'b110: $2^{(-11)}$ 3'b111: $2^{(-12)}$	RW	3'h0

`por_rni_s1_qos_lat_range`

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S1 read and write transactions.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAB8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	<code>por_rni_secure_register_groups_override.qos_ctrl</code>

The following image shows the higher register bit assignments.

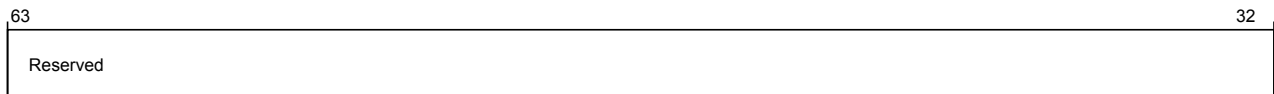


Figure 4-868 por_rni_por_rni_s1_qos_lat_range (high)

The following table shows the por_rni_s1_qos_lat_range higher register bit assignments.

Table 4-885 por_rni_por_rni_s1_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

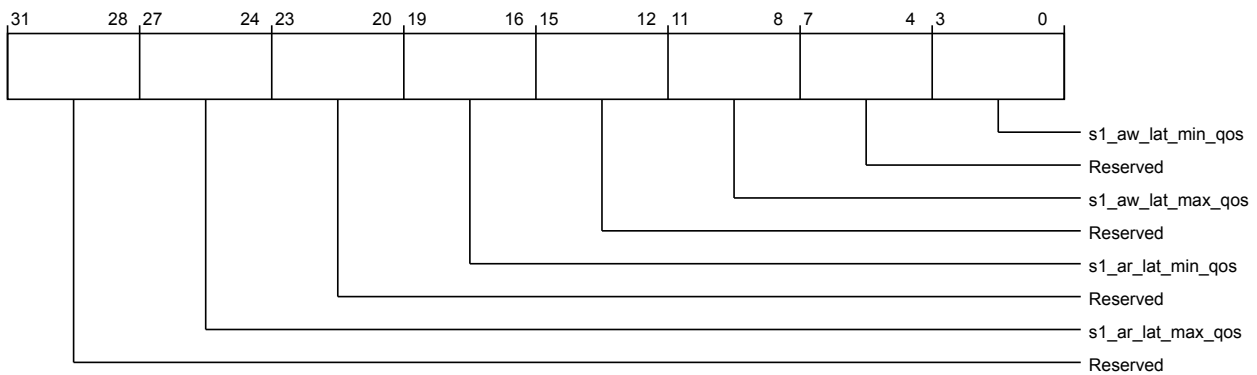


Figure 4-869 por_rni_por_rni_s1_qos_lat_range (low)

The following table shows the por_rni_s1_qos_lat_range lower register bit assignments.

Table 4-886 por_rni_por_rni_s1_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s1_ar_lat_max_qos	Port S1 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s1_ar_lat_min_qos	Port S1 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s1_aw_lat_max_qos	Port S1 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s1_aw_lat_min_qos	Port S1 AW QoS minimum value	RW	4'h0

por_rni_s2_qos_control

Controls QoS settings for port S2 AXI/ACE slave interface.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAC0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

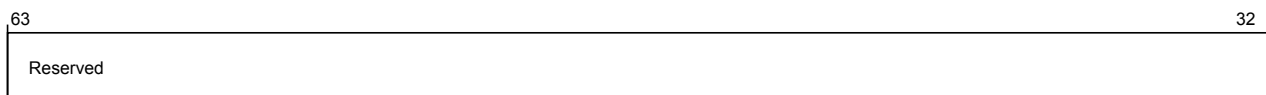


Figure 4-870 por_rni_por_rni_s2_qos_control (high)

The following table shows the por_rni_s2_qos_control higher register bit assignments.

Table 4-887 por_rni_por_rni_s2_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

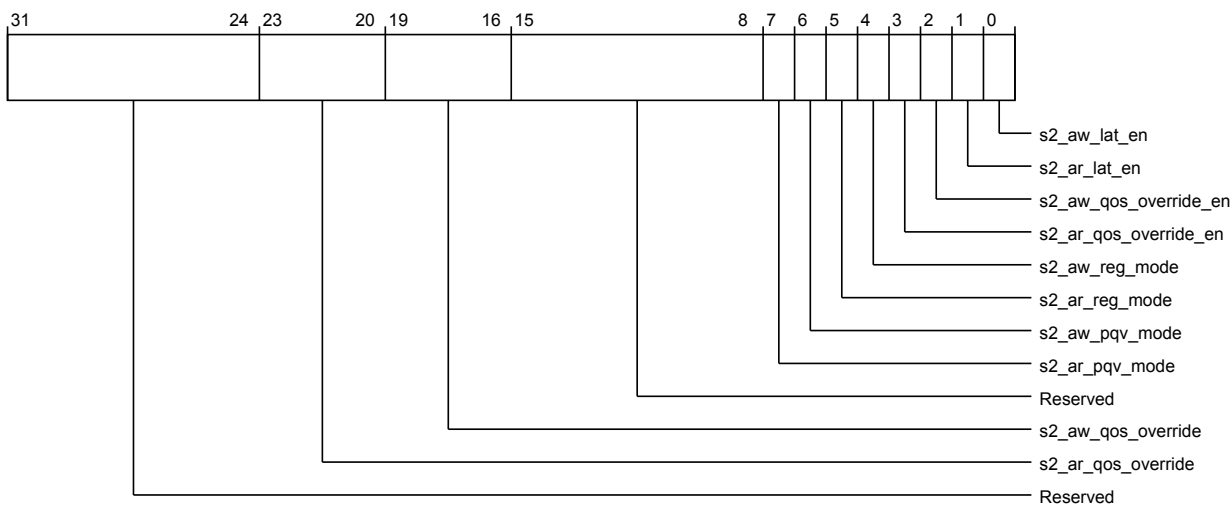


Figure 4-871 por_rni_por_rni_s2_qos_control (low)

The following table shows the por_rni_s2_qos_control lower register bit assignments.

Table 4-888 por_rni_por_rni_s2_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s2_ar_qos_override	AR QoS override value for port S2	RW	4'b0000
19:16	s2_aw_qos_override	AW QoS override value for port S2	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s2_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s2_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s2_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s2_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s2_ar_qos_override_en	Enables port S2 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s2_aw_qos_override_en	Enables port S2 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s2_ar_lat_en	Enables port S2 AR QoS regulation when set	RW	1'b0
0	s2_aw_lat_en	Enables port S2 AW QoS regulation when set	RW	1'b0

por_rni_s2_qos_lat_tgt

Controls QoS target latency (in cycles) for regulation of port S2 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group `por_rni_secure_register_groups_override.qos_ctrl`
override

The following image shows the higher register bit assignments.



Figure 4-872 `por_rni_por_rni_s2_qos_lat_tgt` (high)

The following table shows the `por_rni_s2_qos_lat_tgt` higher register bit assignments.

Table 4-889 `por_rni_por_rni_s2_qos_lat_tgt` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

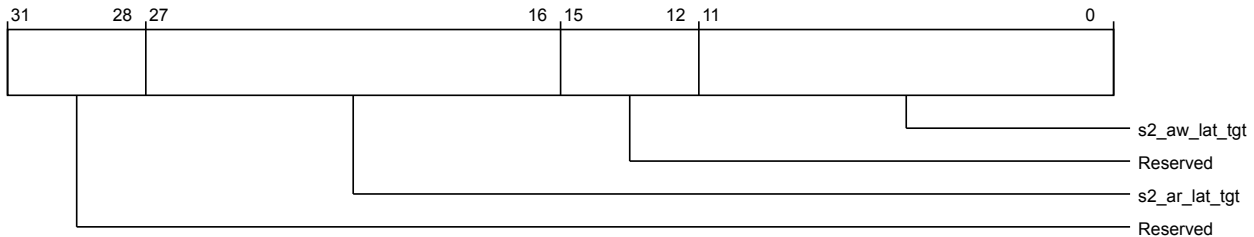


Figure 4-873 `por_rni_por_rni_s2_qos_lat_tgt` (low)

The following table shows the `por_rni_s2_qos_lat_tgt` lower register bit assignments.

Table 4-890 `por_rni_por_rni_s2_qos_lat_tgt` (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	<code>s2_ar_lat_tgt</code>	Port S2 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	<code>s2_aw_lat_tgt</code>	Port S2 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

`por_rni_s2_qos_lat_scale`

Controls the QoS target latency scale factor for port S2 read and write transactions. This register represents powers of two from the range $2^{(-5)}$ to $2^{(-12)}$; it is used to match a 16-bit integrator.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hAD0
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.



Figure 4-874 por_rni_por_rni_s2_qos_lat_scale (high)

The following table shows the por_rni_s2_qos_lat_scale higher register bit assignments.

Table 4-891 por_rni_por_rni_s2_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

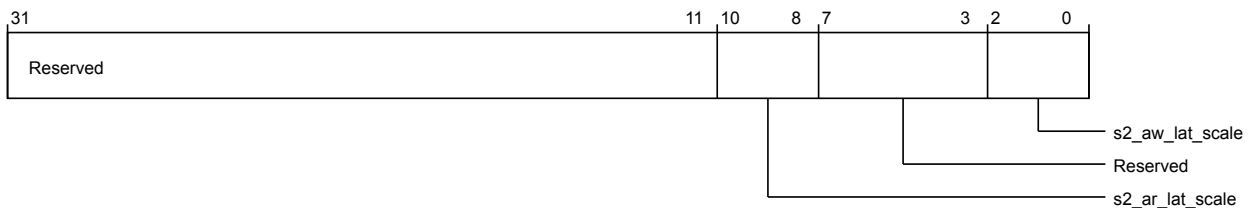


Figure 4-875 por_rni_por_rni_s2_qos_lat_scale (low)

The following table shows the por_rni_s2_qos_lat_scale lower register bit assignments.

Table 4-892 por_rni_por_rni_s2_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s2_ar_lat_scale	Port S2 AR QoS scale factor 3'b000: 2 [^] (-5) 3'b001: 2 [^] (-6) 3'b010: 2 [^] (-7) 3'b011: 2 [^] (-8) 3'b100: 2 [^] (-9) 3'b101: 2 [^] (-10) 3'b110: 2 [^] (-11) 3'b111: 2 [^] (-12)	RW	3'h0

Table 4-892 por_rni_por_rni_s2_qos_lat_scale (low) (continued)

Bits	Field name	Description	Type	Reset
7:3	Reserved	Reserved	RO	-
2:0	s2_aw_lat_scale	Port S2 AW QoS scale factor 3'b000: 2 [^] (-5) 3'b001: 2 [^] (-6) 3'b010: 2 [^] (-7) 3'b011: 2 [^] (-8) 3'b100: 2 [^] (-9) 3'b101: 2 [^] (-10) 3'b110: 2 [^] (-11) 3'b111: 2 [^] (-12)	RW	3'h0

por_rni_s2_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S2 read and write transactions.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAD8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

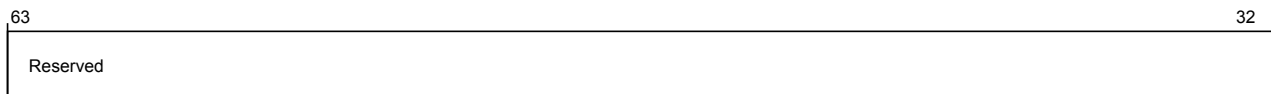


Figure 4-876 por_rni_por_rni_s2_qos_lat_range (high)

The following table shows the por_rni_s2_qos_lat_range higher register bit assignments.

Table 4-893 por_rni_por_rni_s2_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

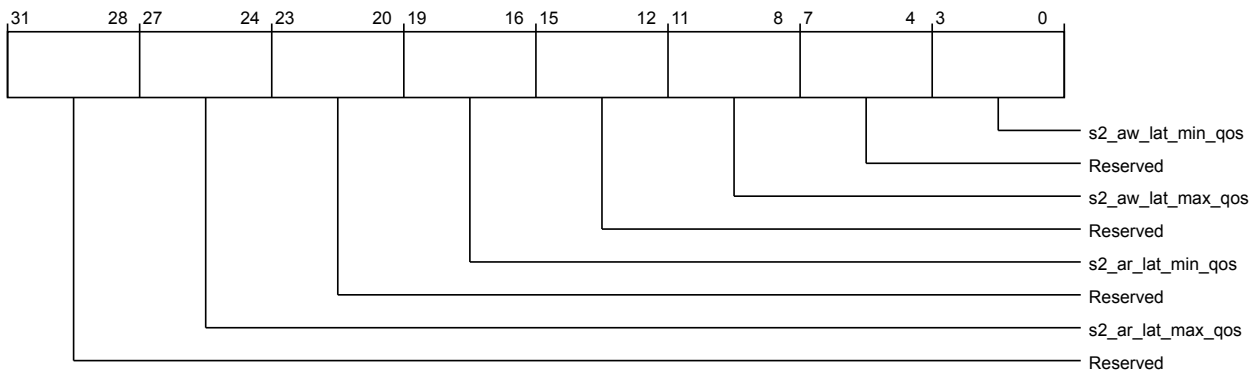


Figure 4-877 `por_rni_por_rni_s2_qos_lat_range` (low)

The following table shows the `por_rni_s2_qos_lat_range` lower register bit assignments.

Table 4-894 `por_rni_por_rni_s2_qos_lat_range` (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	<code>s2_ar_lat_max_qos</code>	Port S2 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	<code>s2_ar_lat_min_qos</code>	Port S2 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	<code>s2_aw_lat_max_qos</code>	Port S2 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	<code>s2_aw_lat_min_qos</code>	Port S2 AW QoS minimum value	RW	4'h0

`por_rni_pmu_event_sel`

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

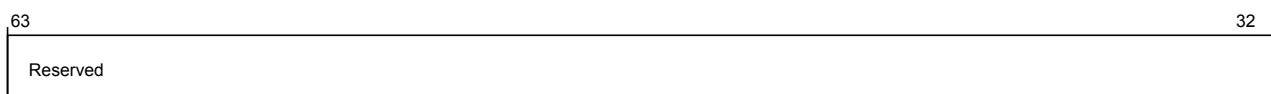


Figure 4-878 `por_rni_por_rni_pmu_event_sel` (high)

The following table shows the por_rni_pmu_event_sel higher register bit assignments.

Table 4-895 por_rni_por_rni_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

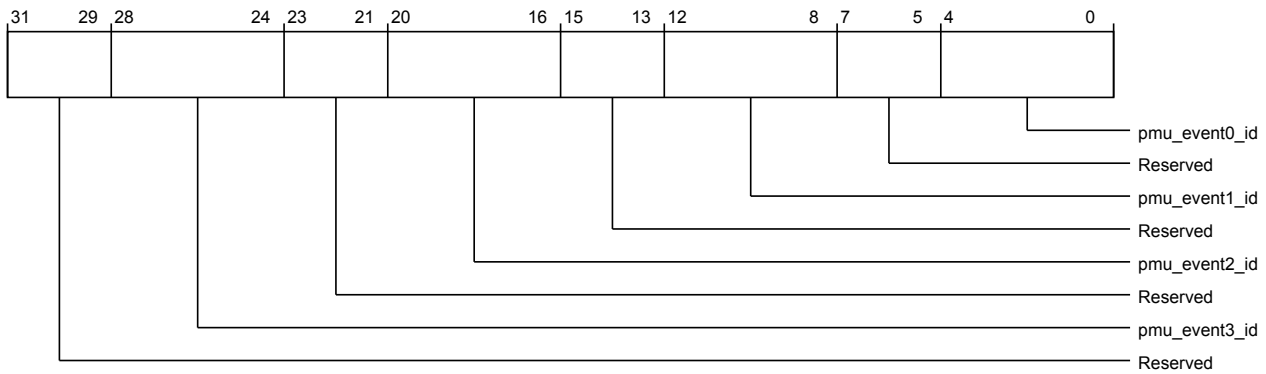


Figure 4-879 por_rni_por_rni_pmu_event_sel (low)

The following table shows the por_rni_pmu_event_sel lower register bit assignments.

Table 4-896 por_rni_por_rni_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	pmu_event3_id	RN-I PMU Event 3 ID; see pmu_event0_id for encodings	RW	5'b0
23:21	Reserved	Reserved	RO	-
20:16	pmu_event2_id	RN-I PMU Event 2 ID; see pmu_event0_id for encodings	RW	5'b0
15:13	Reserved	Reserved	RO	-
12:8	pmu_event1_id	RN-I PMU Event 1 ID; see pmu_event0_id for encodings	RW	5'b0

Table 4-896 `por_rni_por_rni_pmu_event_sel` (low) (continued)

Bits	Field name	Description	Type	Reset
7:5	Reserved	Reserved	RO	-
4:0	<code>pmu_event0_id</code>	RN-I PMU Event 0 ID 5'h00: No event 5'h01: Port S0 RDataBeats 5'h02: Port S1 RDataBeats 5'h03: Port S2 RDataBeats 5'h04: RXDAT flits received 5'h05: TXDAT flits sent 5'h06: Total TXREQ flits sent 5'h07: Retried TXREQ flits sent 5'h08: RRT occupancy count overflow 5'h09: WRT occupancy count overflow 5'h0A: Replayed TXREQ flits 5'h0B: WriteCancel sent 5'h0C: Port S0 WDataBeats 5'h0D: Port S1 WDataBeats 5'h0E: Port S2 WDataBeats 5'h0F: RRT allocation 5'h10: WRT allocation 5'h11: RDB pool state is all unordered 5'h12: RDB pool state is replay 5'h13: RDB pool state is hybrid 5'h14: RDB pool state is all ordered	RW	5'b0

4.3.9 RN SAM register descriptions

Lists the RN SAM registers.

por_rnsam_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

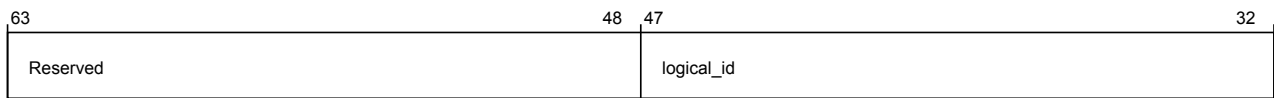


Figure 4-880 por_rnsam_por_rnsam_node_info (high)

The following table shows the por_rnsam_node_info higher register bit assignments.

Table 4-897 por_rnsam_por_rnsam_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID NOTE: RN SAM logical ID is always set to 16'b0.	RO	16'h0

The following image shows the lower register bit assignments.

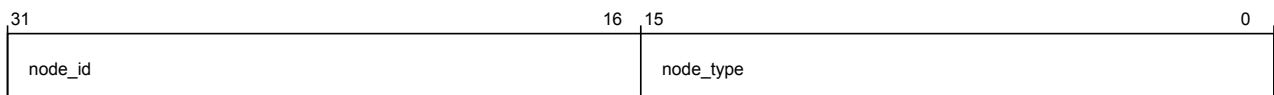


Figure 4-881 por_rnsam_por_rnsam_node_info (low)

The following table shows the por_rnsam_node_info lower register bit assignments.

Table 4-898 por_rnsam_por_rnsam_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h000F

por_rnsam_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-882 por_rnsam_por_rnsam_child_info (high)

The following table shows the por_rnsam_child_info higher register bit assignments.

Table 4-899 por_rnsam_por_rnsam_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

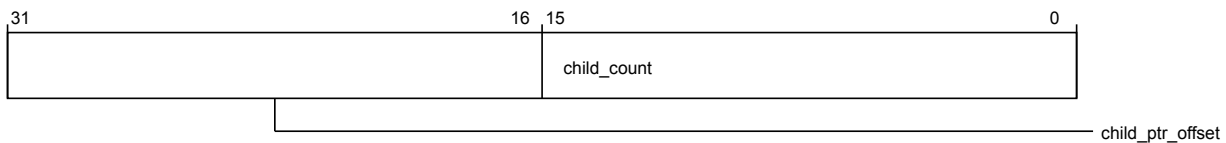


Figure 4-883 por_rnsam_por_rnsam_child_info (low)

The following table shows the por_rnsam_child_info lower register bit assignments.

Table 4-900 por_rnsam_por_rnsam_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_rnsam_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type	RW
Register width (Bits)	64

Address offset	14'h980
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

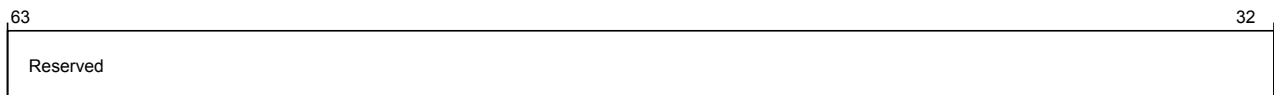


Figure 4-884 por_rnsam_secure_register_groups_override (high)

The following table shows the por_rnsam_secure_register_groups_override higher register bit assignments.

Table 4-901 por_rnsam_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

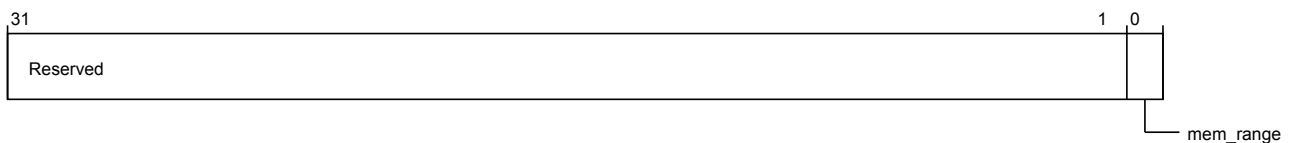


Figure 4-885 por_rnsam_secure_register_groups_override (low)

The following table shows the por_rnsam_secure_register_groups_override lower register bit assignments.

Table 4-902 por_rnsam_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	mem_range	Allows non-secure access to secure mem_ranges registers	RW	1'b0

por_rnsam_unit_info

Provides component identification information for RN SAM.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h900
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

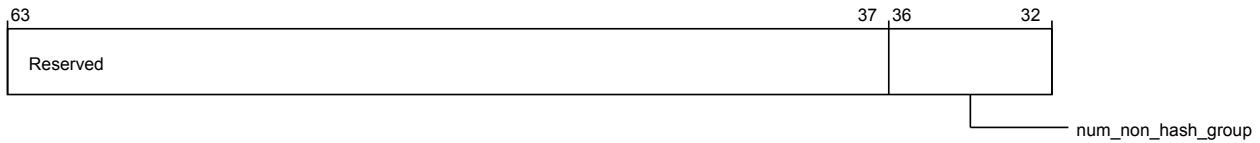


Figure 4-886 `por_rnsam_por_rnsam_unit_info` (high)

The following table shows the `por_rnsam_unit_info` higher register bit assignments.

Table 4-903 `por_rnsam_por_rnsam_unit_info` (high)

Bits	Field name	Description	Type	Reset
63:37	Reserved	Reserved	RO	-
36:32	<code>num_non_hash_group</code>	Number of non-hashed groups supported	RO	Configuration dependent

The following image shows the lower register bit assignments.

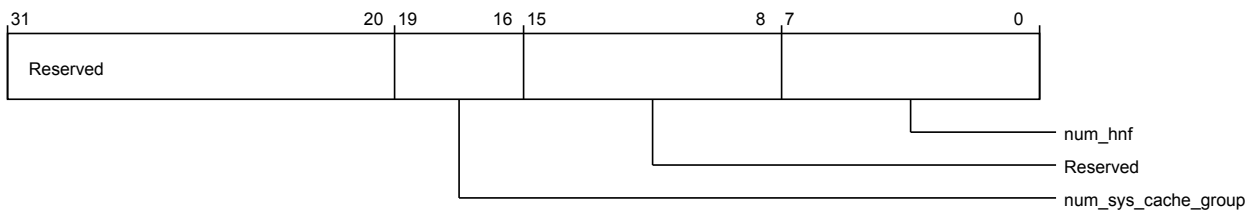


Figure 4-887 `por_rnsam_por_rnsam_unit_info` (low)

The following table shows the `por_rnsam_unit_info` lower register bit assignments.

Table 4-904 `por_rnsam_por_rnsam_unit_info` (low)

Bits	Field name	Description	Type	Reset
31:20	Reserved	Reserved	RO	-
19:16	<code>num_sys_cache_group</code>	Number of system cache groups supported	RO	Configuration dependent
15:8	Reserved	Reserved	RO	-
7:0	<code>num_hnf</code>	Number of hashed targets supported	RO	Configuration dependent

rnsam_status

Functions as the default and programming mode status register.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC00
Register reset	64'b01

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

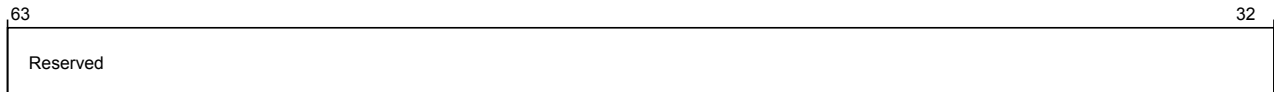


Figure 4-888 por_rnsam_rnsam_status (high)

The following table shows the rnsam_status higher register bit assignments.

Table 4-905 por_rnsam_rnsam_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

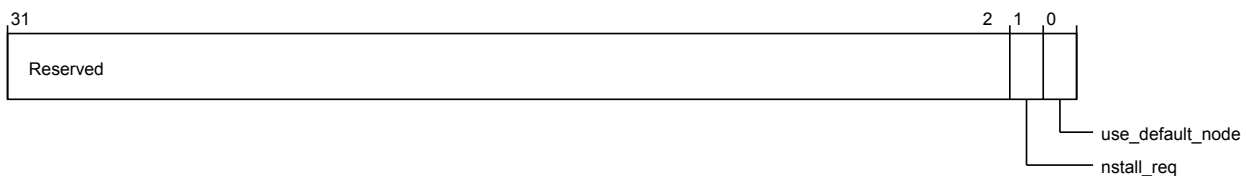


Figure 4-889 por_rnsam_rnsam_status (low)

The following table shows the rnsam_status lower register bit assignments.

Table 4-906 por_rnsam_rnsam_status (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	ninstall_req	Indicates RN SAM is programmed and ready 1'b0: STALL requests 1'b1: UNSTALL requests	RW	1'b0
0	use_default_node	Indicates target ID selection mode 1'b0: Enables RN SAM to hash address bits and generate target ID 1'b1: Uses default target ID	RW	1'b1

non_hash_mem_region_reg0

Configures non-hashed memory regions 0 and 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset	14'hC08
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

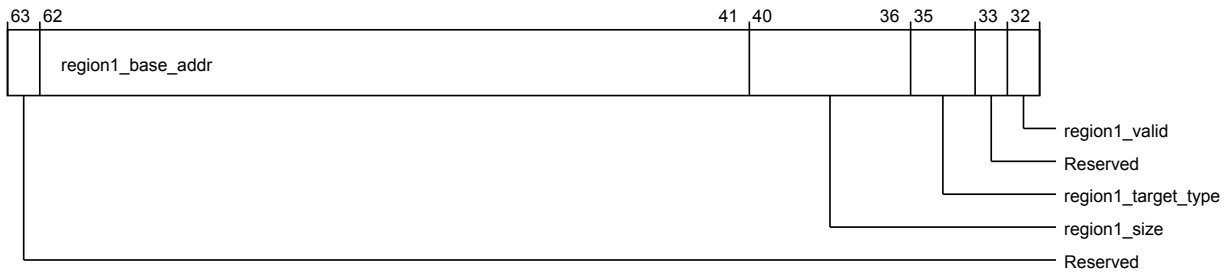


Figure 4-890 `por_rnsam_non_hash_mem_region_reg0 (high)`

The following table shows the `non_hash_mem_region_reg0` higher register bit assignments.

Table 4-907 `por_rnsam_non_hash_mem_region_reg0 (high)`

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	<code>region1_base_addr</code>	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	22'b000000000000000000000000
40:36	<code>region1_size</code>	Memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	5'b00000
35:34	<code>region1_target_type</code>	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	<code>region1_valid</code>	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

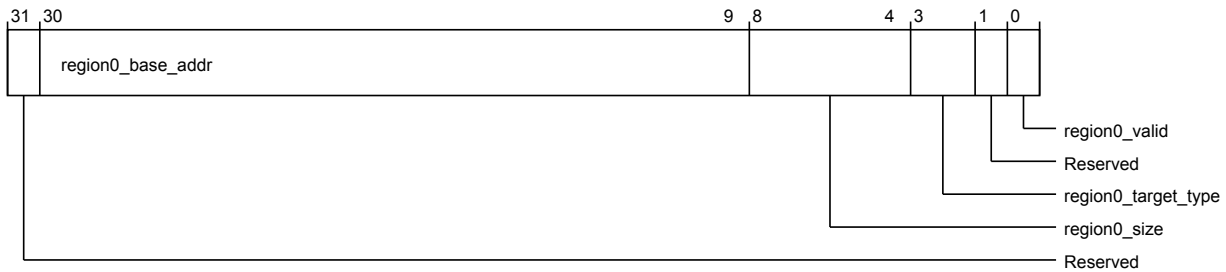


Figure 4-891 por_rnsam_non_hash_mem_region_reg0 (low)

The following table shows the non_hash_mem_region_reg0 lower register bit assignments.

Table 4-908 por_rnsam_non_hash_mem_region_reg0 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region0_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	22'b000000000000000000000000
8:4	region0_size	Memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region0_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region0_valid	Memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg1

Configures non-hashed memory regions 2 and 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC10
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

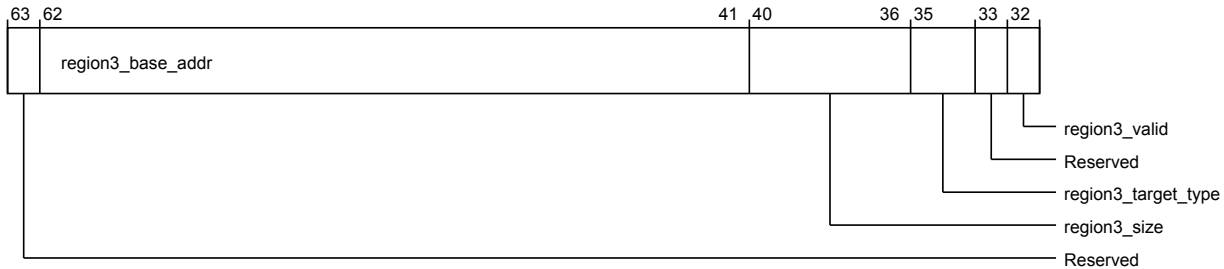


Figure 4-892 por_rnsam_non_hash_mem_region_reg1 (high)

The following table shows the non_hash_mem_region_reg1 higher register bit assignments.

Table 4-909 por_rnsam_non_hash_mem_region_reg1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region3_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	22'b000000000000000000000000
40:36	region3_size	Memory region 3 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2 ^{address width}).	RW	5'b00000
35:34	region3_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region3_valid	Memory region 3 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

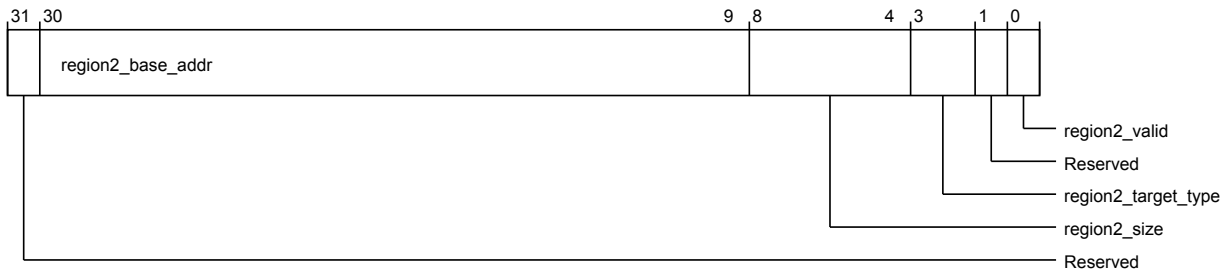


Figure 4-893 por_rnsam_non_hash_mem_region_reg1 (low)

The following table shows the non_hash_mem_region_reg1 lower register bit assignments.

Table 4-910 por_rnsam_non_hash_mem_region_reg1 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region2_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	22'b000000000000000000000000
8:4	region2_size	Memory region 2 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region2_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region2_valid	Memory region 2 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg2

Configures non-hashed memory regions 4 and 5.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC18
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

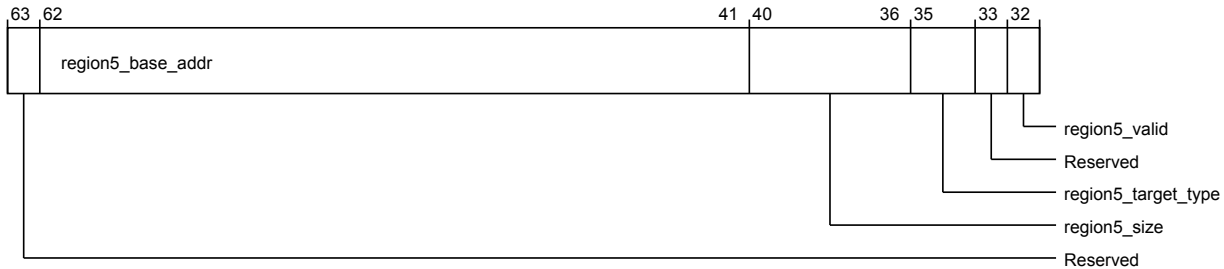


Figure 4-894 por_rnsam_non_hash_mem_region_reg2 (high)

The following table shows the non_hash_mem_region_reg2 higher register bit assignments.

Table 4-911 por_rnsam_non_hash_mem_region_reg2 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region5_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 5 size	RW	22'b000000000000000000000000
40:36	region5_size	Memory region 5 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2 ^{address width}).	RW	5'b00000
35:34	region5_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region5_valid	Memory region 5 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.



Figure 4-895 por_rnsam_non_hash_mem_region_reg2 (low)

The following table shows the non_hash_mem_region_reg2 lower register bit assignments.

Table 4-912 por_rnsam_non_hash_mem_region_reg2 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region4_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 4 size	RW	22'b000000000000000000000000
8:4	region4_size	Memory region 4 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region4_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region4_valid	Memory region 4 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg3

Configures non-hashed memory regions 6 and 7.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC20
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

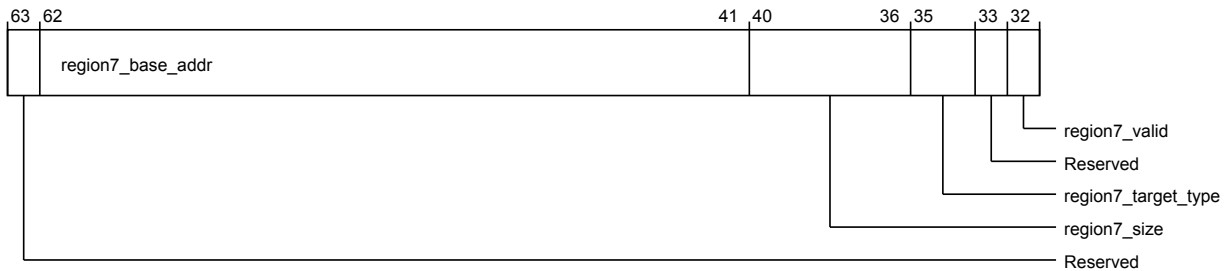


Figure 4-896 por_rnsam_non_hash_mem_region_reg3 (high)

The following table shows the non_hash_mem_region_reg3 higher register bit assignments.

Table 4-913 por_rnsam_non_hash_mem_region_reg3 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region7_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 7 size	RW	22'b000000000000000000000000
40:36	region7_size	Memory region 7 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2 ^{address width}).	RW	5'b00000
35:34	region7_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region7_valid	Memory region 7 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

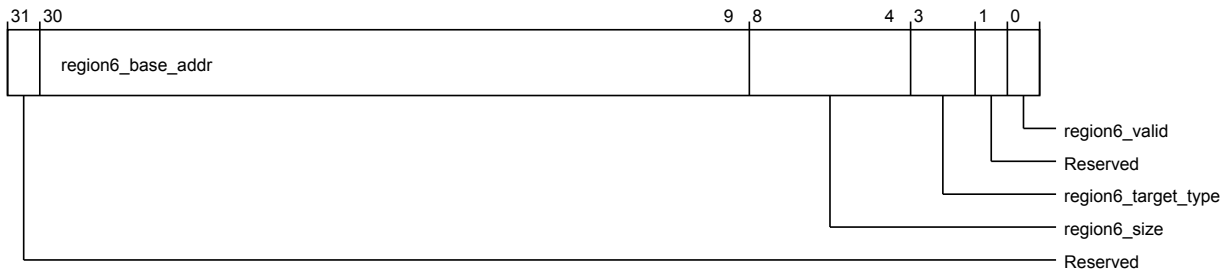


Figure 4-897 por_rnsam_non_hash_mem_region_reg3 (low)

The following table shows the non_hash_mem_region_reg3 lower register bit assignments.

Table 4-914 por_rnsam_non_hash_mem_region_reg3 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region6_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 6 size	RW	22'b0000000000000000000000
8:4	region6_size	Memory region 6 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region6_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region6_valid	Memory region 6 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_tgt_nodeid0

Configures non-hashed target node IDs 0 to 3.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC30
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

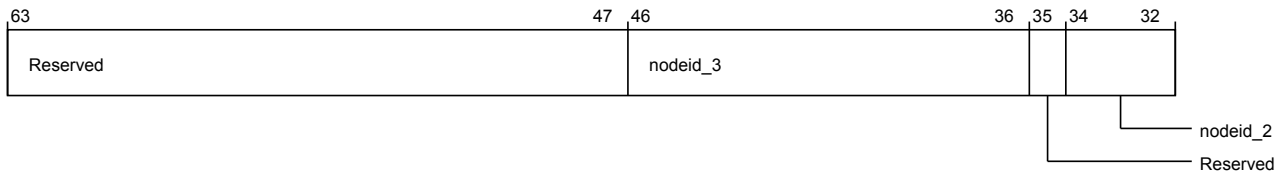


Figure 4-898 `por_rnsam_non_hash_tgt_nodeid0` (high)

The following table shows the `non_hash_tgt_nodeid0` higher register bit assignments.

Table 4-915 `por_rnsam_non_hash_tgt_nodeid0` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	<code>nodeid_3</code>	Non-hashed target node ID 3	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	<code>nodeid_2</code>	Non-hashed target node ID 2	RW	11'b000000000000

The following image shows the lower register bit assignments.

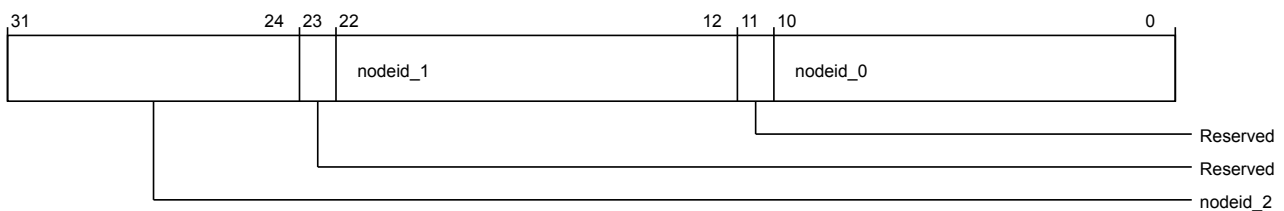


Figure 4-899 `por_rnsam_non_hash_tgt_nodeid0` (low)

The following table shows the `non_hash_tgt_nodeid0` lower register bit assignments.

Table 4-916 `por_rnsam_non_hash_tgt_nodeid0` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>nodeid_2</code>	Non-hashed target node ID 2	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	<code>nodeid_1</code>	Non-hashed target node ID 1	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	<code>nodeid_0</code>	Non-hashed target node ID 0	RW	11'b000000000000

non_hash_tgt_nodeid1

Configures non-hashed target node IDs 4 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC38

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

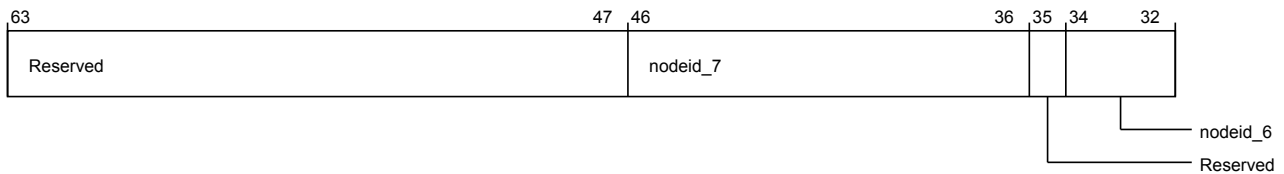


Figure 4-900 por_rnsam_non_hash_tgt_nodeid1 (high)

The following table shows the non_hash_tgt_nodeid1 higher register bit assignments.

Table 4-917 por_rnsam_non_hash_tgt_nodeid1 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_7	Non-hashed target node ID 7	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_6	Non-hashed target node ID 6	RW	11'b000000000000

The following image shows the lower register bit assignments.

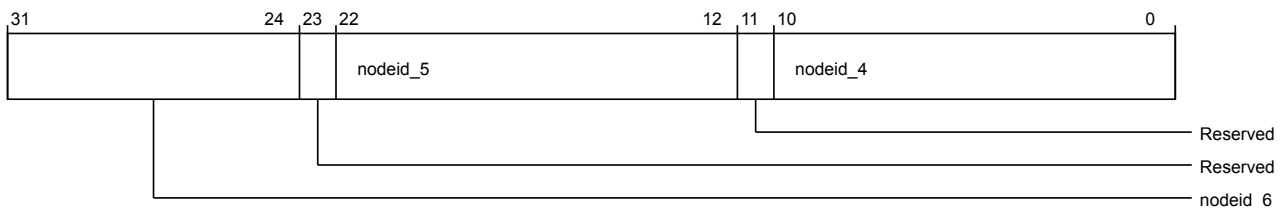


Figure 4-901 por_rnsam_non_hash_tgt_nodeid1 (low)

The following table shows the non_hash_tgt_nodeid1 lower register bit assignments.

Table 4-918 por_rnsam_non_hash_tgt_nodeid1 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_6	Non-hashed target node ID 6	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_5	Non-hashed target node ID 5	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_4	Non-hashed target node ID 4	RW	11'b000000000000

non_hash_tgt_nodeid2

Configures non-hashed target node IDs 8 to 9.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC40

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

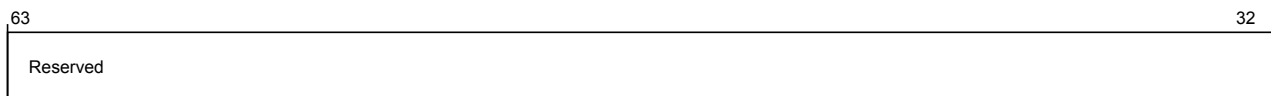


Figure 4-902 por_rnsam_non_hash_tgt_nodeid2 (high)

The following table shows the non_hash_tgt_nodeid2 higher register bit assignments.

Table 4-919 por_rnsam_non_hash_tgt_nodeid2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

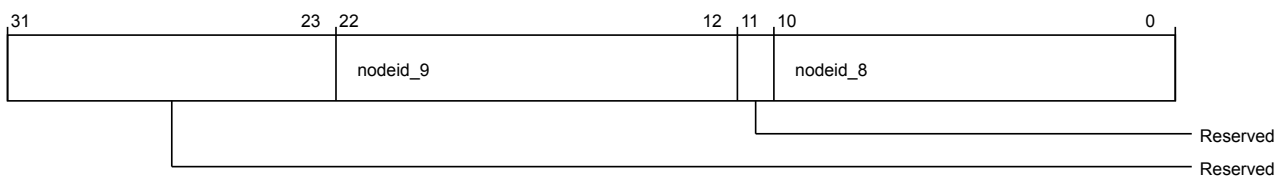


Figure 4-903 por_rnsam_non_hash_tgt_nodeid2 (low)

The following table shows the non_hash_tgt_nodeid2 lower register bit assignments.

Table 4-920 por_rnsam_non_hash_tgt_nodeid2 (low)

Bits	Field name	Description	Type	Reset
31:23	Reserved	Reserved	RO	-
22:12	nodeid_9	Non-hashed target node ID 9	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_8	Non-hashed target node ID 8	RW	11'b000000000000

sys_cache_grp_region0

Configures hashed memory regions 0 and 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC48

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

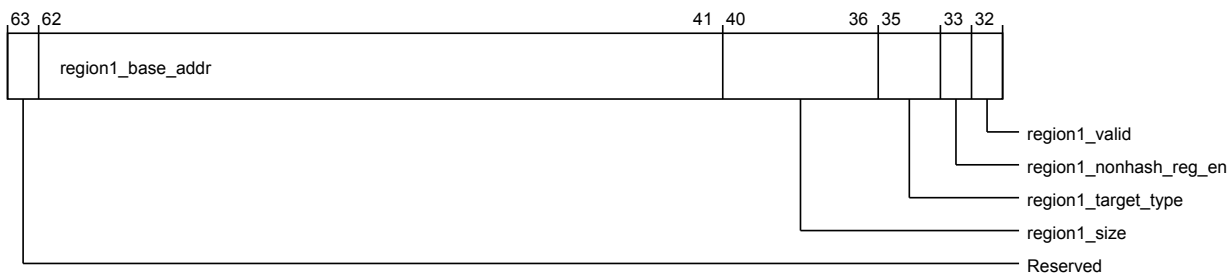


Figure 4-904 por_rnsam_sys_cache_grp_region0 (high)

The following table shows the sys_cache_grp_region0 higher register bit assignments.

Table 4-921 por_rnsam_sys_cache_grp_region0 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region1_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	22'b000000000000000000000000

Table 4-921 por_rnsam_sys_cache_grp_region0 (high) (continued)

Bits	Field name	Description	Type	Reset
40:36	region1_size	Memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	5'b00000
35:34	region1_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	region1_nonhash_reg_en	Enables hashed region 1 to select non-hashed node	RW	1'b0
32	region1_valid	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

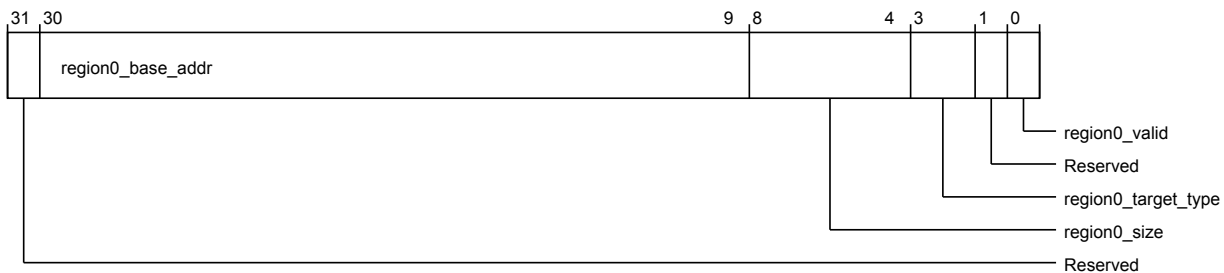


Figure 4-905 por_rnsam_sys_cache_grp_region0 (low)

The following table shows the sys_cache_grp_region0 lower register bit assignments.

Table 4-922 por_rnsam_sys_cache_grp_region0 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region0_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	22'b0000000000000000000000
8:4	region0_size	Memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	5'b00000

Table 4-922 por_rnsam_sys_cache_grp_region0 (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	region0_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region0_valid	Memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

sys_cache_grp_region1

Configures hashed memory regions 2 and 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC50

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

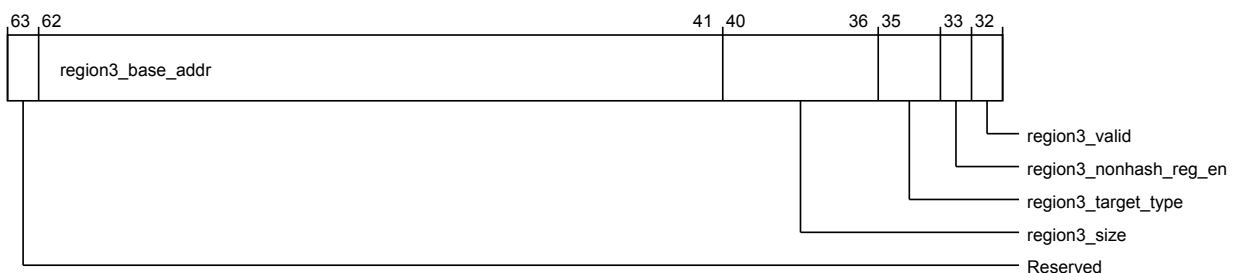


Figure 4-906 por_rnsam_sys_cache_grp_region1 (high)

The following table shows the sys_cache_grp_region1 higher register bit assignments.

Table 4-923 por_rnsam_sys_cache_grp_region1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region3_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	22'b0000000000000000000000
40:36	region3_size	Memory region 3 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region3_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	region3_nonhash_reg_en	Enables hashed region 3 to select non-hashed node	RW	1'b0
32	region3_valid	Memory region 3 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

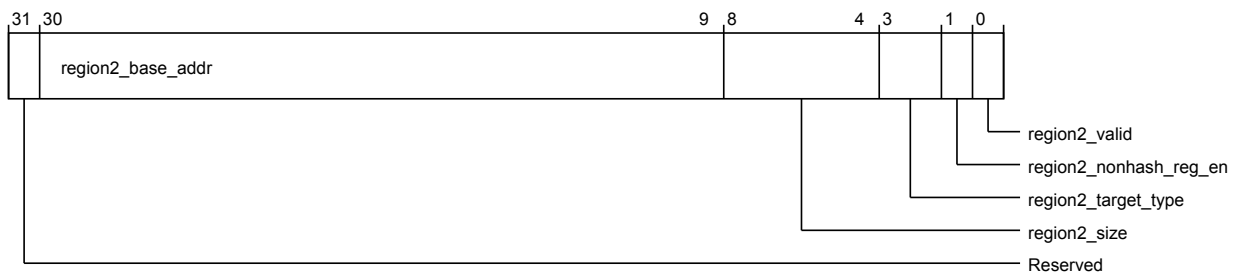


Figure 4-907 por_rnsam_sys_cache_grp_region1 (low)

The following table shows the sys_cache_grp_region1 lower register bit assignments.

Table 4-924 por_rnsam_sys_cache_grp_region1 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region2_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	22'b000000000000000000000000
8:4	region2_size	Memory region 2 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region2_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	region2_nonhash_reg_en	Enables hashed region 2 to select non-hashed node	RW	1'b0
0	region2_valid	Memory region 2 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

sys_cache_grp_hn_nodeid_reg0

Configures hashed node IDs for system cache groups. Controls target HN node IDs 0 to 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC58

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

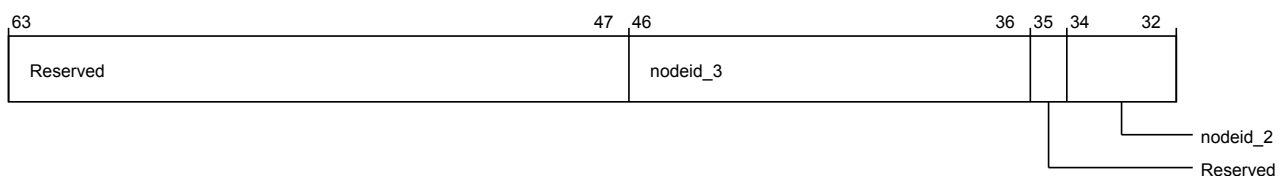


Figure 4-908 por_rnsam_sys_cache_grp_hn_nodeid_reg0 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg0 higher register bit assignments.

Table 4-925 por_rnsam_sys_cache_grp_hn_nodeid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_3	Hashed target node ID 3	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_2	Hashed target node ID 2	RW	11'b000000000000

The following image shows the lower register bit assignments.

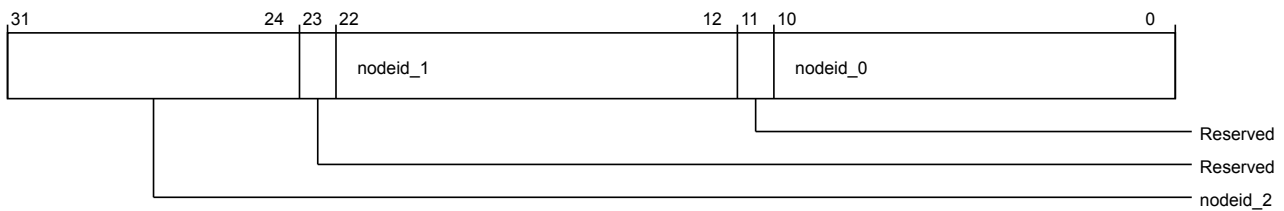


Figure 4-909 por_rnsam_sys_cache_grp_hn_nodeid_reg0 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg0 lower register bit assignments.

Table 4-926 por_rnsam_sys_cache_grp_hn_nodeid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_2	Hashed target node ID 2	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_1	Hashed target node ID 1	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_0	Hashed target node ID 0	RW	11'b000000000000

sys_cache_grp_hn_nodeid_reg1

Configures hashed node IDs for system cache groups. Controls target HN node IDs 4 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC60

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

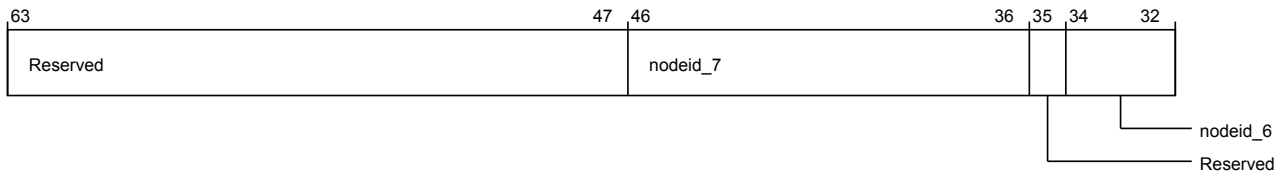


Figure 4-910 `por_rnsam_sys_cache_grp_hn_nodeid_reg1` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg1` higher register bit assignments.

Table 4-927 `por_rnsam_sys_cache_grp_hn_nodeid_reg1` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	<code>nodeid_7</code>	Hashed target node ID 7	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	<code>nodeid_6</code>	Hashed target node ID 6	RW	11'b000000000000

The following image shows the lower register bit assignments.

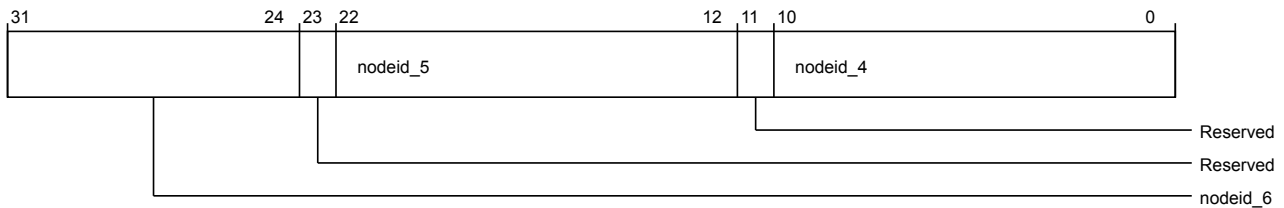


Figure 4-911 `por_rnsam_sys_cache_grp_hn_nodeid_reg1` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg1` lower register bit assignments.

Table 4-928 `por_rnsam_sys_cache_grp_hn_nodeid_reg1` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>nodeid_6</code>	Hashed target node ID 6	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	<code>nodeid_5</code>	Hashed target node ID 5	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	<code>nodeid_4</code>	Hashed target node ID 4	RW	11'b000000000000

`sys_cache_grp_hn_nodeid_reg2`

Configures hashed node IDs for system cache groups. Controls target HN node IDs 8 to 11.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC68
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

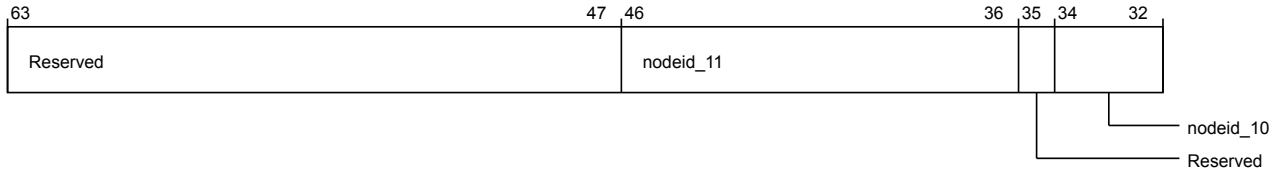


Figure 4-912 `por_rnsam_sys_cache_grp_hn_nodeid_reg2` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg2` higher register bit assignments.

Table 4-929 `por_rnsam_sys_cache_grp_hn_nodeid_reg2` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	<code>nodeid_11</code>	Hashed target node ID 11	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	<code>nodeid_10</code>	Hashed target node ID 10	RW	11'b000000000000

The following image shows the lower register bit assignments.

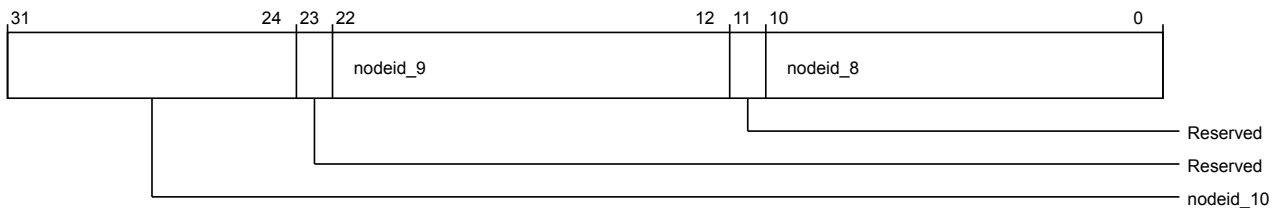


Figure 4-913 `por_rnsam_sys_cache_grp_hn_nodeid_reg2` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg2` lower register bit assignments.

Table 4-930 `por_rnsam_sys_cache_grp_hn_nodeid_reg2` (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_10	Hashed target node ID 10	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_9	Hashed target node ID 9	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_8	Hashed target node ID 8	RW	11'b000000000000

sys_cache_grp_hn_nodeid_reg3

Configures hashed node IDs for system cache groups. Controls target HN node IDs 12 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC70

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

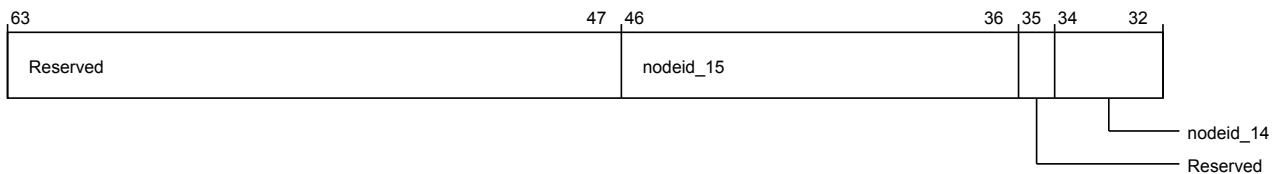


Figure 4-914 `por_rnsam_sys_cache_grp_hn_nodeid_reg3` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg3` higher register bit assignments.

Table 4-931 `por_rnsam_sys_cache_grp_hn_nodeid_reg3` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_15	Hashed target node ID 15	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_14	Hashed target node ID 14	RW	11'b000000000000

The following image shows the lower register bit assignments.

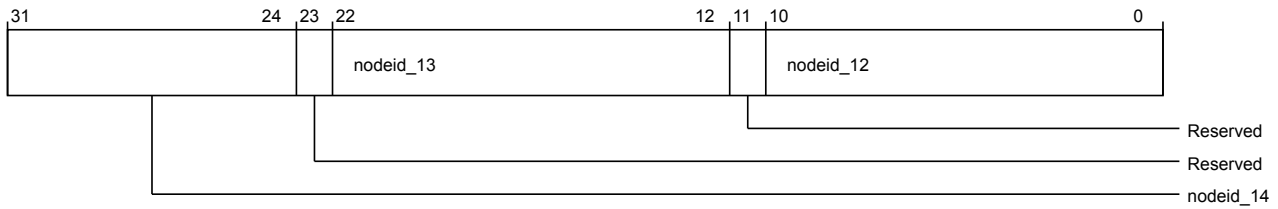


Figure 4-915 `por_rnsam_sys_cache_grp_hn_nodeid_reg3` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg3` lower register bit assignments.

Table 4-932 `por_rnsam_sys_cache_grp_hn_nodeid_reg3` (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_14	Hashed target node ID 14	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_13	Hashed target node ID 13	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_12	Hashed target node ID 12	RW	11'b000000000000

`sys_cache_grp_hn_nodeid_reg4`

Configures hashed node IDs for system cache groups. Controls target HN node IDs 16 to 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC78

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

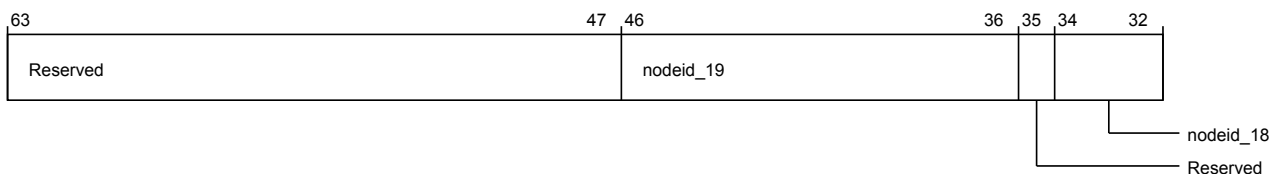


Figure 4-916 `por_rnsam_sys_cache_grp_hn_nodeid_reg4` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg4` higher register bit assignments.

Table 4-933 `por_rnsam_sys_cache_grp_hn_nodeid_reg4` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_19	Hashed target node ID 19	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_18	Hashed target node ID 18	RW	11'b000000000000

The following image shows the lower register bit assignments.

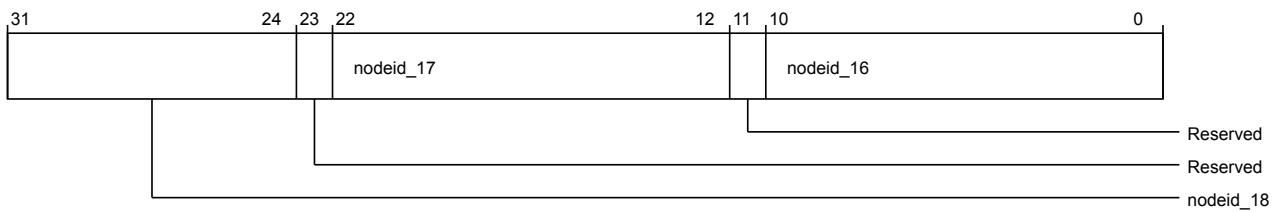


Figure 4-917 `por_rnsam_sys_cache_grp_hn_nodeid_reg4` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg4` lower register bit assignments.

Table 4-934 `por_rnsam_sys_cache_grp_hn_nodeid_reg4` (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_18	Hashed target node ID 18	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_17	Hashed target node ID 17	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_16	Hashed target node ID 16	RW	11'b000000000000

`sys_cache_grp_hn_nodeid_reg5`

Configures hashed node IDs for system cache groups. Controls target HN node IDs 20 to 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

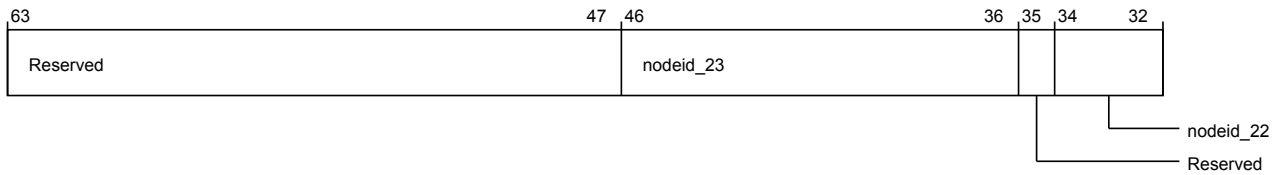


Figure 4-918 por_rnsam_sys_cache_grp_hn_nodeid_reg5 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg5 higher register bit assignments.

Table 4-935 por_rnsam_sys_cache_grp_hn_nodeid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_23	Hashed target node ID 23	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_22	Hashed target node ID 22	RW	11'b000000000000

The following image shows the lower register bit assignments.

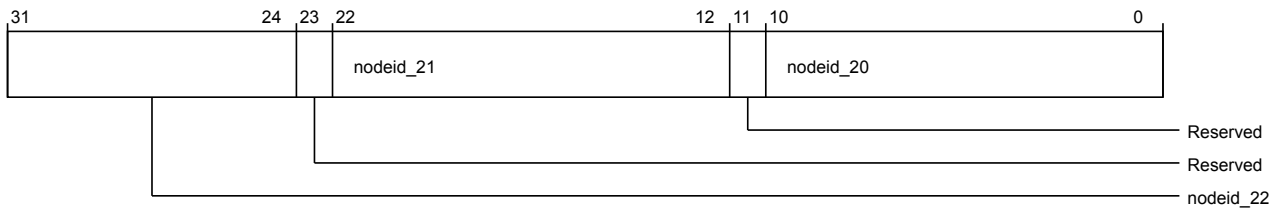


Figure 4-919 por_rnsam_sys_cache_grp_hn_nodeid_reg5 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg5 lower register bit assignments.

Table 4-936 por_rnsam_sys_cache_grp_hn_nodeid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_22	Hashed target node ID 22	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_21	Hashed target node ID 21	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_20	Hashed target node ID 20	RW	11'b000000000000

sys_cache_grp_hn_nodeid_reg6

Configures hashed node IDs for system cache groups. Controls target HN node IDs 24 to 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC88
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

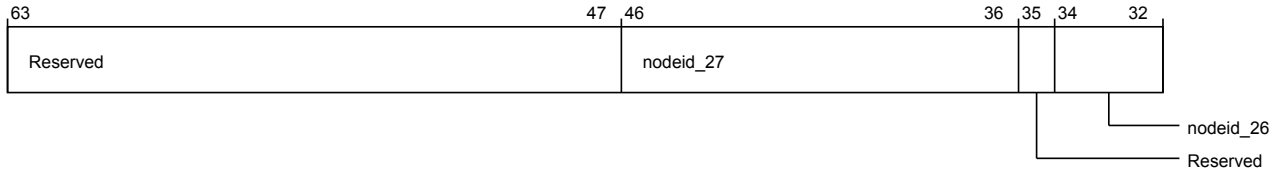


Figure 4-920 `por_rnsam_sys_cache_grp_hn_nodeid_reg6` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg6` higher register bit assignments.

Table 4-937 `por_rnsam_sys_cache_grp_hn_nodeid_reg6` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	<code>nodeid_27</code>	Hashed target node ID 27	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	<code>nodeid_26</code>	Hashed target node ID 26	RW	11'b000000000000

The following image shows the lower register bit assignments.

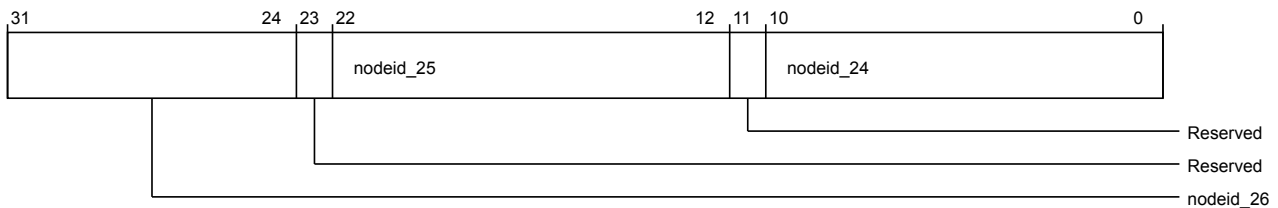


Figure 4-921 `por_rnsam_sys_cache_grp_hn_nodeid_reg6` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg6` lower register bit assignments.

Table 4-938 `por_rnsam_sys_cache_grp_hn_nodeid_reg6` (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_26	Hashed target node ID 26	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_25	Hashed target node ID 25	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_24	Hashed target node ID 24	RW	11'b000000000000

sys_cache_grp_hn_nodeid_reg7

Configures hashed node IDs for system cache groups. Controls target HN node IDs 28 to 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC90

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

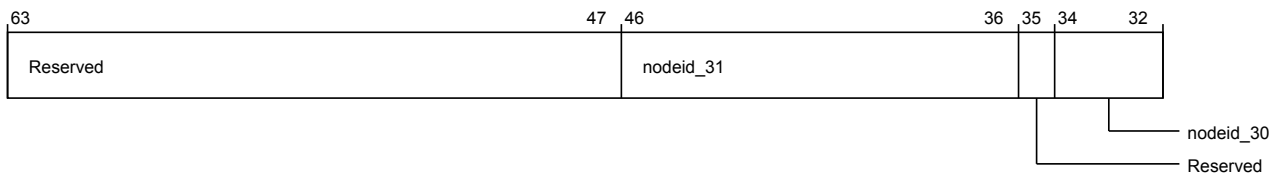


Figure 4-922 `por_rnsam_sys_cache_grp_hn_nodeid_reg7` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg7` higher register bit assignments.

Table 4-939 `por_rnsam_sys_cache_grp_hn_nodeid_reg7` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_31	Hashed target node ID 31	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_30	Hashed target node ID 30	RW	11'b000000000000

The following image shows the lower register bit assignments.

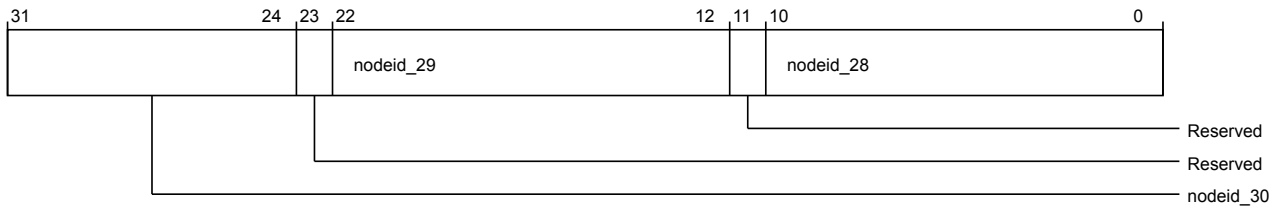


Figure 4-923 `por_rnsam_sys_cache_grp_hn_nodeid_reg7` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg7` lower register bit assignments.

Table 4-940 `por_rnsam_sys_cache_grp_hn_nodeid_reg7` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>nodeid_30</code>	Hashed target node ID 30	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	<code>nodeid_29</code>	Hashed target node ID 29	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	<code>nodeid_28</code>	Hashed target node ID 28	RW	11'b000000000000

`sys_cache_grp_nonhash_nodeid`

Configures non-hashed node IDs for system cache groups 1 to 3. NOTE: Only applicable in the non-hashed mode.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC98
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

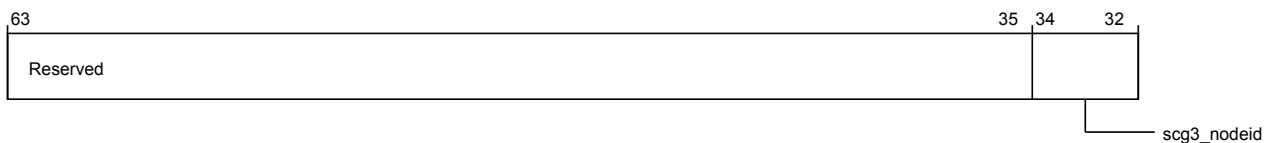


Figure 4-924 `por_rnsam_sys_cache_grp_nonhash_nodeid` (high)

The following table shows the `sys_cache_grp_nonhash_nodeid` higher register bit assignments.

Table 4-941 por_rnsam_sys_cache_grp_nonhash_nodeid (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	scg3_nodeid	Non-hashed node ID for system cache group 3	RW	11'b000000000000

The following image shows the lower register bit assignments.

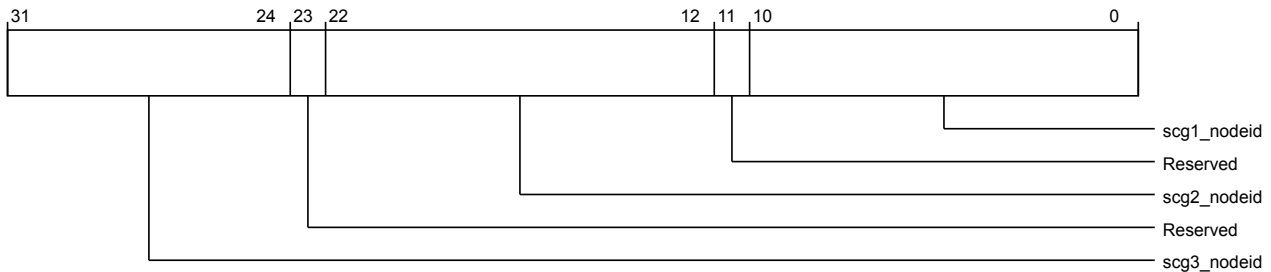


Figure 4-925 por_rnsam_sys_cache_grp_nonhash_nodeid (low)

The following table shows the sys_cache_grp_nonhash_nodeid lower register bit assignments.

Table 4-942 por_rnsam_sys_cache_grp_nonhash_nodeid (low)

Bits	Field name	Description	Type	Reset
31:24	scg3_nodeid	Non-hashed node ID for system cache group 3	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	scg2_nodeid	Non-hashed node ID for system cache group 2	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	scg1_nodeid	Non-hashed node ID for system cache group 1	RW	11'b000000000000

sys_cache_group_hn_count

Indicates number of HN-Fs in system cache groups 0 to 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD00

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

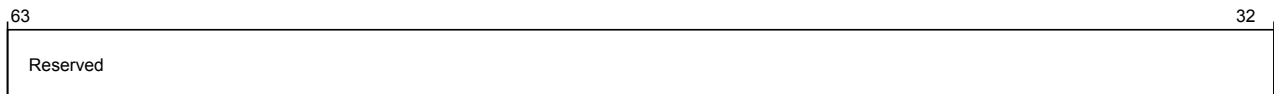


Figure 4-926 `por_rnsam_sys_cache_group_hn_count` (high)

The following table shows the `sys_cache_group_hn_count` higher register bit assignments.

Table 4-943 `por_rnsam_sys_cache_group_hn_count` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

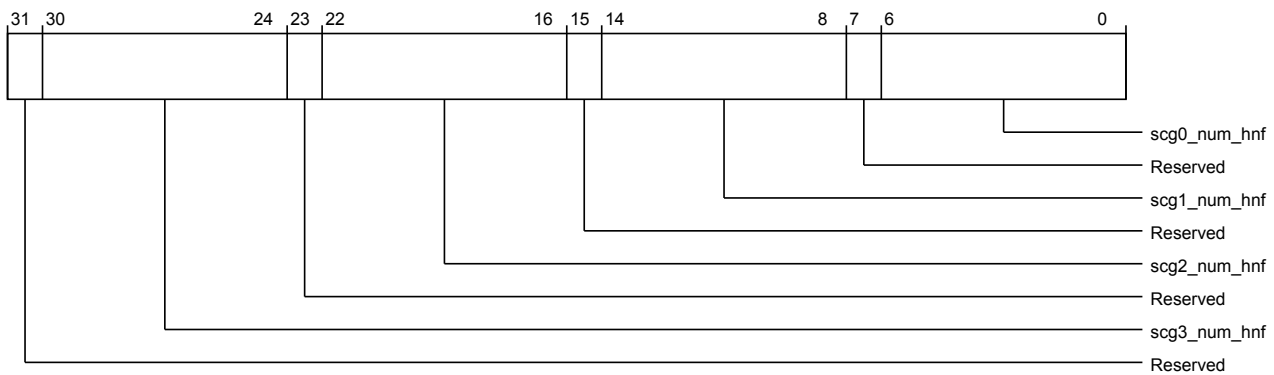


Figure 4-927 `por_rnsam_sys_cache_group_hn_count` (low)

The following table shows the `sys_cache_group_hn_count` lower register bit assignments.

Table 4-944 `por_rnsam_sys_cache_group_hn_count` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:24	<code>scg3_num_hnf</code>	HN-F count for system cache group 3	RW	7'b000000
23	Reserved	Reserved	RO	-
22:16	<code>scg2_num_hnf</code>	HN-F count for system cache group 2	RW	7'b000000
15	Reserved	Reserved	RO	-
14:8	<code>scg1_num_hnf</code>	HN-F count for system cache group 1	RW	7'b000000
7	Reserved	Reserved	RO	-
6:0	<code>scg0_num_hnf</code>	HN-F count for system cache group 0	RW	7'b000000

`sys_cache_grp_sn_nodeid_reg0`

Configures hashed node IDs for system cache groups. Controls target SN node IDs 0 to 3.

Its characteristics are:

Type	RW
------	----

Register width (Bits) 64

Address offset	14'hD08
-----------------------	---------

Register reset	64'b0
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Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
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The following image shows the higher register bit assignments.

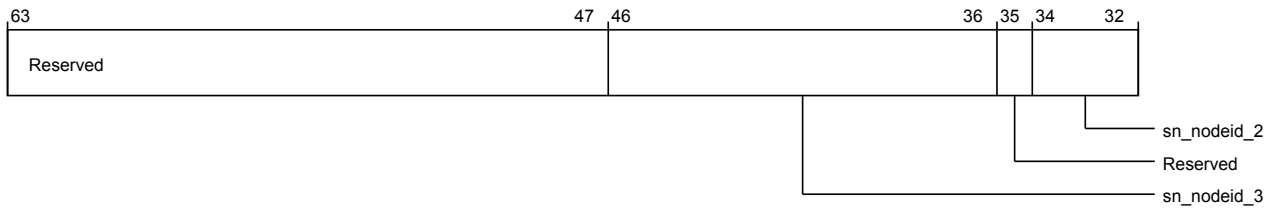


Figure 4-928 `por_rnsam_sys_cache_grp_sn_nodeid_reg0` (high)

The following table shows the sys_cache_grp_sn_nodeid_reg0 higher register bit assignments.

Table 4-945 `por_rnsam_sys_cache_grp_sn_nodeid_reg0` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_3	Hashed target SN node ID 3	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_2	Hashed target SN node ID 2	RW	11'b000000000000

The following image shows the lower register bit assignments.

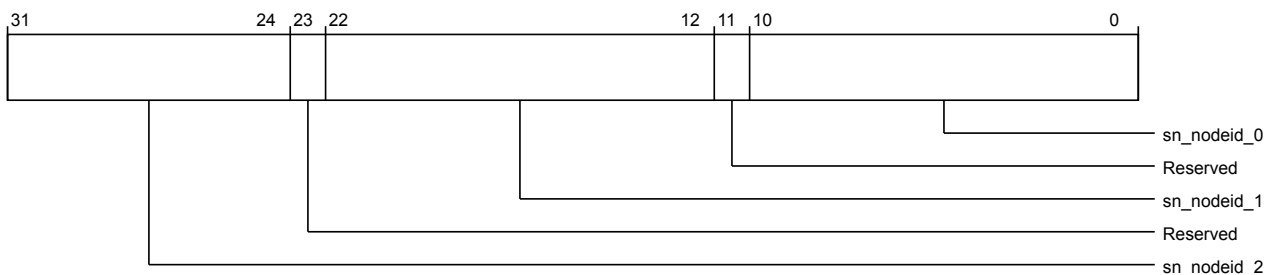


Figure 4-929 `por_rnsam_sys_cache_grp_sn_nodeid_reg0` (low)

The following table shows the sys_cache_grp sn nodeid reg0 lower register bit assignments.

Table 4-946 `por_rnsam_sys_cache_grp_sn_nodeid_reg0` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>sn_nodeid_2</code>	Hashed target SN node ID 2	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	<code>sn_nodeid_1</code>	Hashed target SN node ID 1	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	<code>sn_nodeid_0</code>	Hashed target SN node ID 0	RW	11'b000000000000

`sys_cache_grp_sn_nodeid_reg1`

Configures hashed node IDs for system cache groups. Controls target SN node IDs 4 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

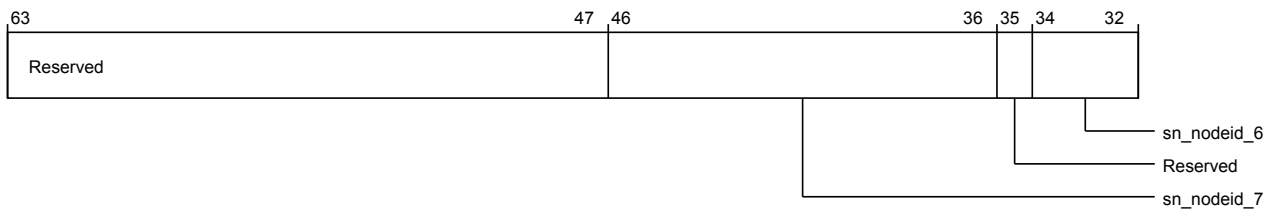


Figure 4-930 `por_rnsam_sys_cache_grp_sn_nodeid_reg1` (high)

The following table shows the `sys_cache_grp_sn_nodeid_reg1` higher register bit assignments.

Table 4-947 `por_rnsam_sys_cache_grp_sn_nodeid_reg1` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	<code>sn_nodeid_7</code>	Hashed target SN node ID 7	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	<code>sn_nodeid_6</code>	Hashed target SN node ID 6	RW	11'b000000000000

The following image shows the lower register bit assignments.

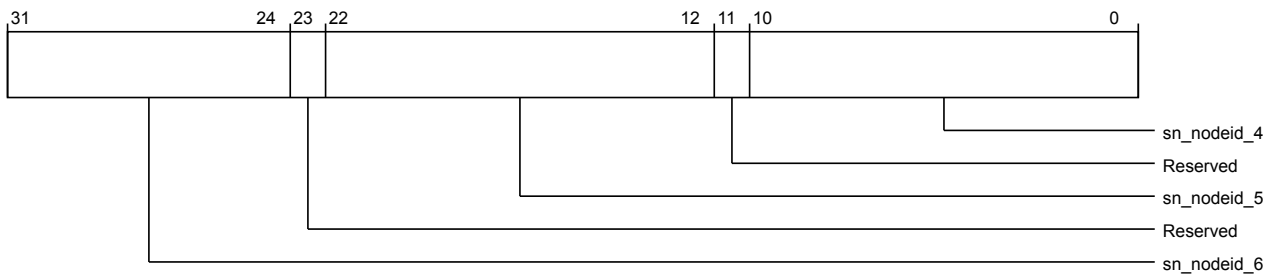


Figure 4-931 por_rnsam_sys_cache_grp_sn_nodeid_reg1 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg1 lower register bit assignments.

Table 4-948 por_rnsam_sys_cache_grp_sn_nodeid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_6	Hashed target SN node ID 6	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_5	Hashed target SN node ID 5	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_4	Hashed target SN node ID 4	RW	11'b000000000000

sys_cache_grp_sn_nodeid_reg2

Configures hashed node IDs for system cache groups. Controls target SN node IDs 8 to 11.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD18
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

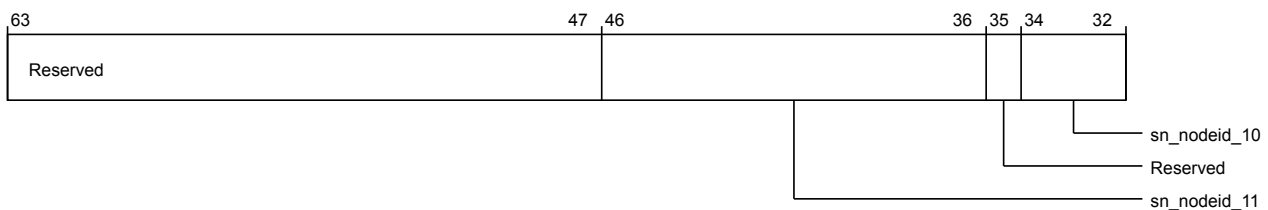


Figure 4-932 por_rnsam_sys_cache_grp_sn_nodeid_reg2 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg2 higher register bit assignments.

Table 4-949 `por_rnsam_sys_cache_grp_sn_nodeid_reg2` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	<code>sn_nodeid_11</code>	Hashed target SN node ID 11	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	<code>sn_nodeid_10</code>	Hashed target SN node ID 10	RW	11'b000000000000

The following image shows the lower register bit assignments.

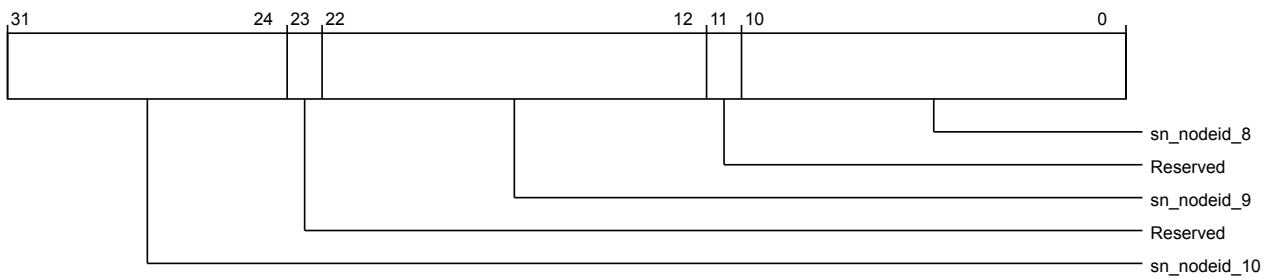


Figure 4-933 `por_rnsam_sys_cache_grp_sn_nodeid_reg2` (low)

The following table shows the `sys_cache_grp_sn_nodeid_reg2` lower register bit assignments.

Table 4-950 `por_rnsam_sys_cache_grp_sn_nodeid_reg2` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>sn_nodeid_10</code>	Hashed target SN node ID 10	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	<code>sn_nodeid_9</code>	Hashed target SN node ID 9	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	<code>sn_nodeid_8</code>	Hashed target SN node ID 8	RW	11'b000000000000

`sys_cache_grp_sn_nodeid_reg3`

Configures hashed node IDs for system cache groups. Controls target SN node IDs 12 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD20

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

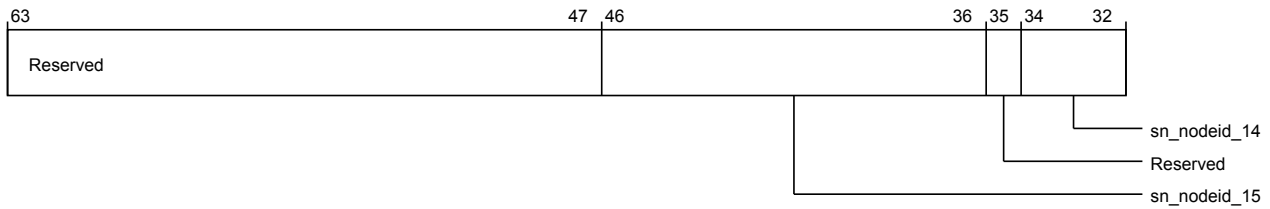


Figure 4-934 por_rnsam_sys_cache_grp_sn_nodeid_reg3 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg3 higher register bit assignments.

Table 4-951 por_rnsam_sys_cache_grp_sn_nodeid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_15	Hashed target SN node ID 15	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_14	Hashed target SN node ID 14	RW	11'b000000000000

The following image shows the lower register bit assignments.

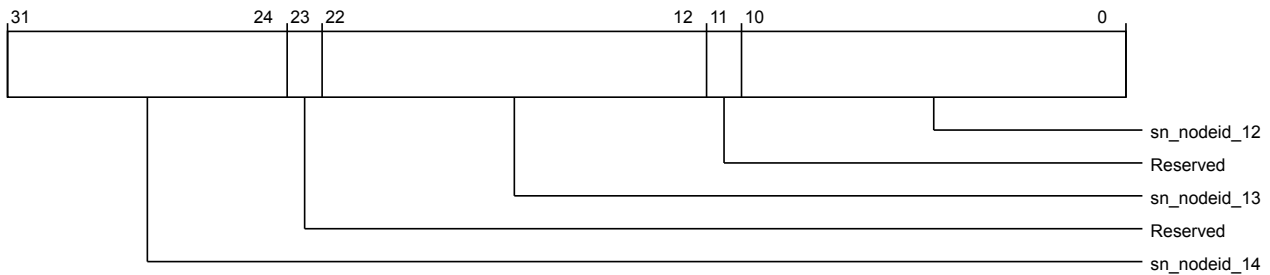


Figure 4-935 por_rnsam_sys_cache_grp_sn_nodeid_reg3 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg3 lower register bit assignments.

Table 4-952 por_rnsam_sys_cache_grp_sn_nodeid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_14	Hashed target SN node ID 14	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_13	Hashed target SN node ID 13	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_12	Hashed target SN node ID 12	RW	11'b000000000000

sys_cache_grp_sn_nodeid_reg4

Configures hashed node IDs for system cache groups. Controls target SN node IDs 16 to 19.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD28
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

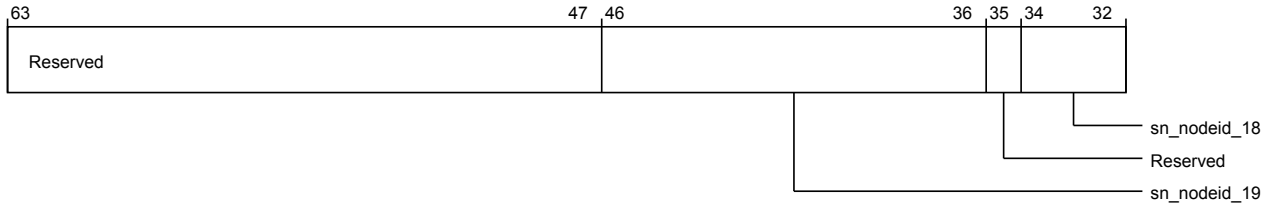


Figure 4-936 por_rnsam_sys_cache_grp_sn_nodeid_reg4 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg4 higher register bit assignments.

Table 4-953 por_rnsam_sys_cache_grp_sn_nodeid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_19	Hashed target SN node ID 19	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_18	Hashed target SN node ID 18	RW	11'b000000000000

The following image shows the lower register bit assignments.

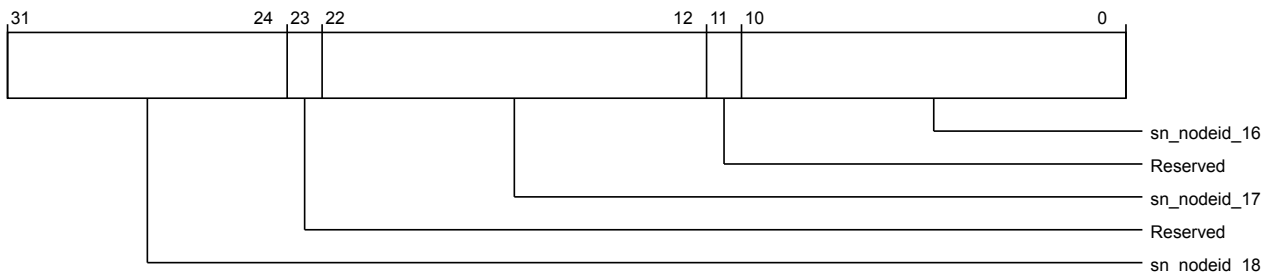


Figure 4-937 por_rnsam_sys_cache_grp_sn_nodeid_reg4 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg4 lower register bit assignments.

Table 4-954 `por_rnsam_sys_cache_grp_sn_nodeid_reg4` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>sn_nodeid_18</code>	Hashed target SN node ID 18	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	<code>sn_nodeid_17</code>	Hashed target SN node ID 17	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	<code>sn_nodeid_16</code>	Hashed target SN node ID 16	RW	11'b000000000000

`sys_cache_grp_sn_nodeid_reg5`

Configures hashed node IDs for system cache groups. Controls target SN node IDs 20 to 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD30

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

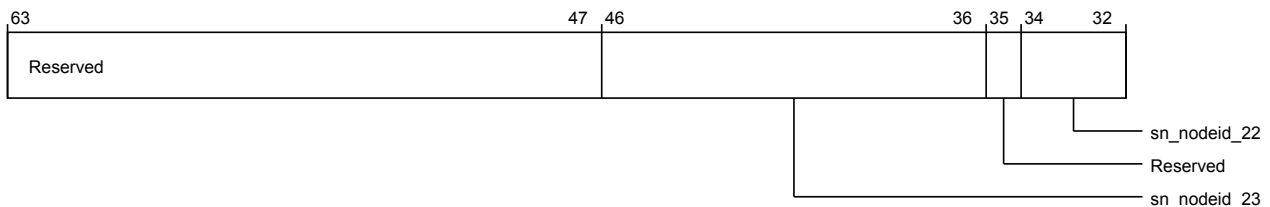


Figure 4-938 `por_rnsam_sys_cache_grp_sn_nodeid_reg5` (high)

The following table shows the `sys_cache_grp_sn_nodeid_reg5` higher register bit assignments.

Table 4-955 `por_rnsam_sys_cache_grp_sn_nodeid_reg5` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	<code>sn_nodeid_23</code>	Hashed target SN node ID 23	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	<code>sn_nodeid_22</code>	Hashed target SN node ID 22	RW	11'b000000000000

The following image shows the lower register bit assignments.

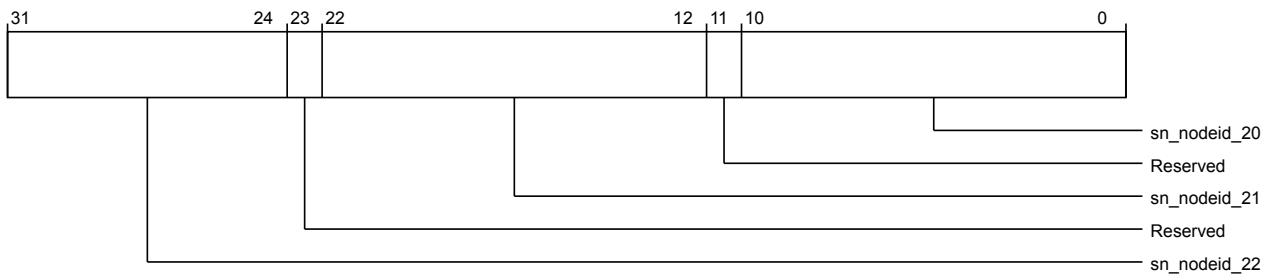


Figure 4-939 por_rnsam_sys_cache_grp_sn_nodeid_reg5 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg5 lower register bit assignments.

Table 4-956 por_rnsam_sys_cache_grp_sn_nodeid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_22	Hashed target SN node ID 22	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_21	Hashed target SN node ID 21	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_20	Hashed target SN node ID 20	RW	11'b000000000000

sys_cache_grp_sn_nodeid_reg6

Configures hashed node IDs for system cache groups. Controls target SN node IDs 24 to 27.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD38

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

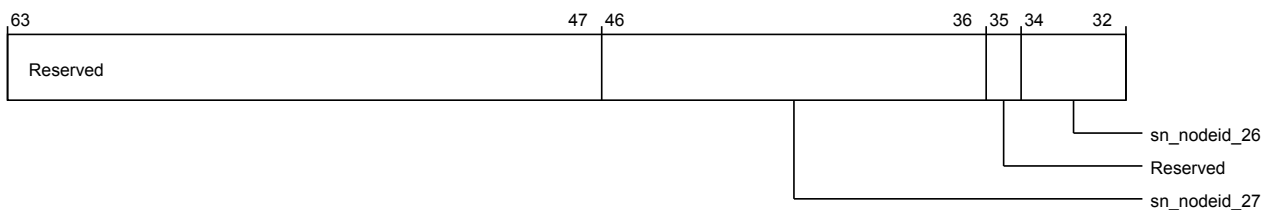


Figure 4-940 por_rnsam_sys_cache_grp_sn_nodeid_reg6 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg6 higher register bit assignments.

Table 4-957 `por_rnsam_sys_cache_grp_sn_nodeid_reg6` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	<code>sn_nodeid_27</code>	Hashed target SN node ID 27	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	<code>sn_nodeid_26</code>	Hashed target SN node ID 26	RW	11'b000000000000

The following image shows the lower register bit assignments.

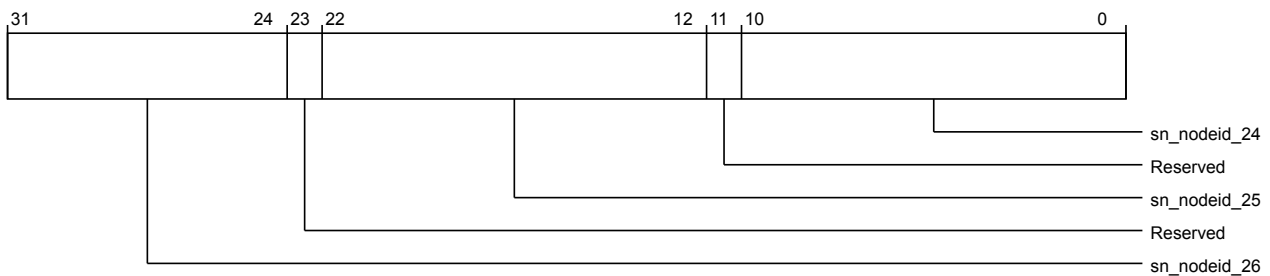


Figure 4-941 `por_rnsam_sys_cache_grp_sn_nodeid_reg6` (low)

The following table shows the `sys_cache_grp_sn_nodeid_reg6` lower register bit assignments.

Table 4-958 `por_rnsam_sys_cache_grp_sn_nodeid_reg6` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>sn_nodeid_26</code>	Hashed target SN node ID 26	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	<code>sn_nodeid_25</code>	Hashed target SN node ID 25	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	<code>sn_nodeid_24</code>	Hashed target SN node ID 24	RW	11'b000000000000

`sys_cache_grp_sn_nodeid_reg7`

Configures hashed node IDs for system cache groups. Controls target SN node IDs 28 to 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD40

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

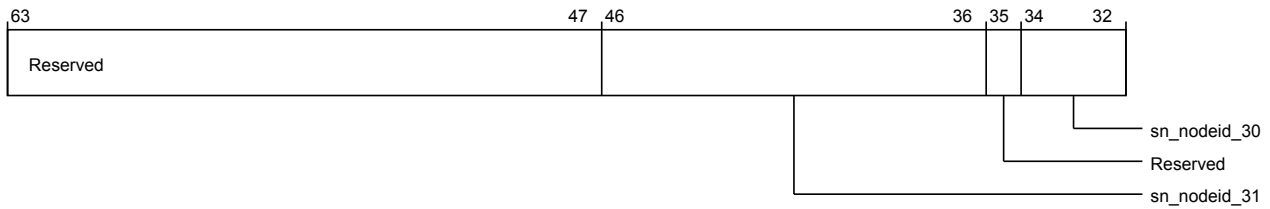


Figure 4-942 por_rnsam_sys_cache_grp_sn_nodeid_reg7 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg7 higher register bit assignments.

Table 4-959 por_rnsam_sys_cache_grp_sn_nodeid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_31	Hashed target SN node ID 31	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_30	Hashed target SN node ID 30	RW	11'b000000000000

The following image shows the lower register bit assignments.

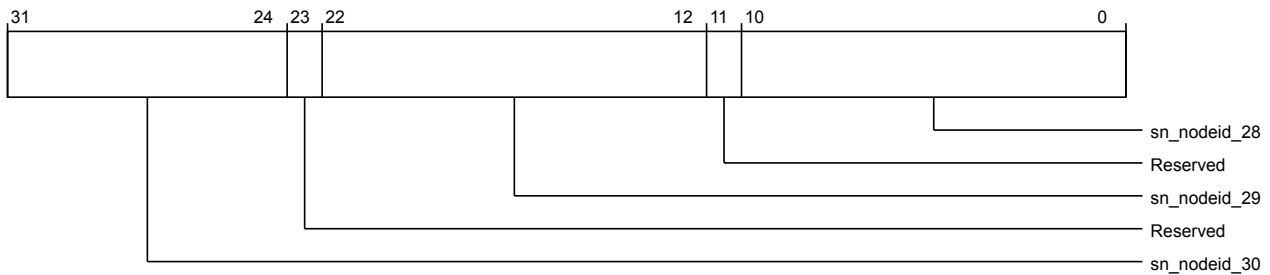


Figure 4-943 por_rnsam_sys_cache_grp_sn_nodeid_reg7 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg7 lower register bit assignments.

Table 4-960 por_rnsam_sys_cache_grp_sn_nodeid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_30	Hashed target SN node ID 30	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_29	Hashed target SN node ID 29	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_28	Hashed target SN node ID 28	RW	11'b000000000000

sys_cache_grp_sn_sam_cfg0

Configures top address bits for SN SAM system cache groups 0 and 1. All top_address_bit fields must be between bits 47 and 28. top_address_bit2 > top_address_bit1 > top_address_bit0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD48
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

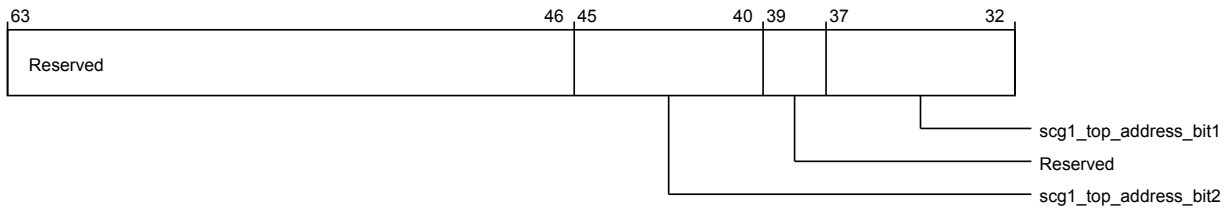


Figure 4-944 por_rnsam_sys_cache_grp_sn_sam_cfg0 (high)

The following table shows the sys_cache_grp_sn_sam_cfg0 higher register bit assignments.

Table 4-961 por_rnsam_sys_cache_grp_sn_sam_cfg0 (high)

Bits	Field name	Description	Type	Reset
63:46	Reserved	Reserved	RO	-
45:40	scg1_top_address_bit2	Top address bit 2 for system cache group 1	RW	6'h00
39:38	Reserved	Reserved	RO	-
37:32	scg1_top_address_bit1	Top address bit 1 for system cache group 1	RW	6'h00

The following image shows the lower register bit assignments.

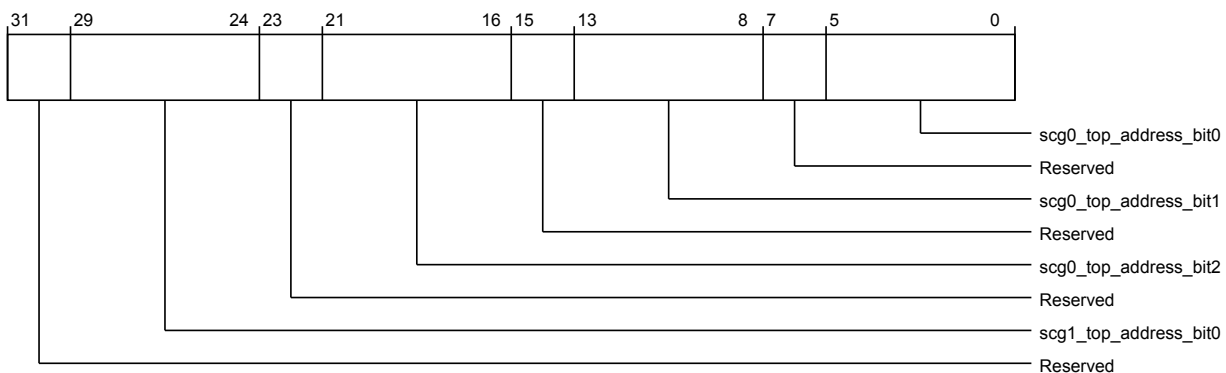


Figure 4-945 por_rnsam_sys_cache_grp_sn_sam_cfg0 (low)

The following table shows the sys_cache_grp_sn_sam_cfg0 lower register bit assignments.

Table 4-962 `por_rnsam_sys_cache_grp_sn_sam_cfg0` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>scg1_top_address_bit0</code>	Top address bit 0 for system cache group 1	RW	6'h00
23:22	Reserved	Reserved	RO	-
21:16	<code>scg0_top_address_bit2</code>	Top address bit 2 for system cache group 0	RW	6'h00
15:14	Reserved	Reserved	RO	-
13:8	<code>scg0_top_address_bit1</code>	Top address bit 1 for system cache group 0	RW	6'h00
7:6	Reserved	Reserved	RO	-
5:0	<code>scg0_top_address_bit0</code>	Top address bit 0 for system cache group 0	RW	6'h00

`sys_cache_grp_sn_sam_cfg1`

Configures top address bits for SN SAM system cache groups 2 and 3. All `top_address_bit` fields must be between bits 47 and 28. `top_address_bit2` andgt; `top_address_bit1` andgt; `top_address_bit0`.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD50

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

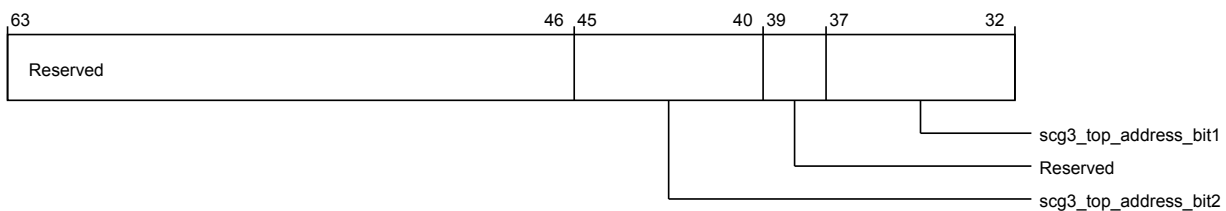


Figure 4-946 `por_rnsam_sys_cache_grp_sn_sam_cfg1` (high)

The following table shows the `sys_cache_grp_sn_sam_cfg1` higher register bit assignments.

Table 4-963 `por_rnsam_sys_cache_grp_sn_sam_cfg1` (high)

Bits	Field name	Description	Type	Reset
63:46	Reserved	Reserved	RO	-
45:40	<code>scg3_top_address_bit2</code>	Top address bit 2 for system cache group 3	RW	6'h00

Table 4-963 `por_rnsam_sys_cache_grp_sn_sam_cfg1` (high) (continued)

Bits	Field name	Description	Type	Reset
39:38	Reserved	Reserved	RO	-
37:32	<code>scg3_top_address_bit1</code>	Top address bit 1 for system cache group 3	RW	6'h00

The following image shows the lower register bit assignments.

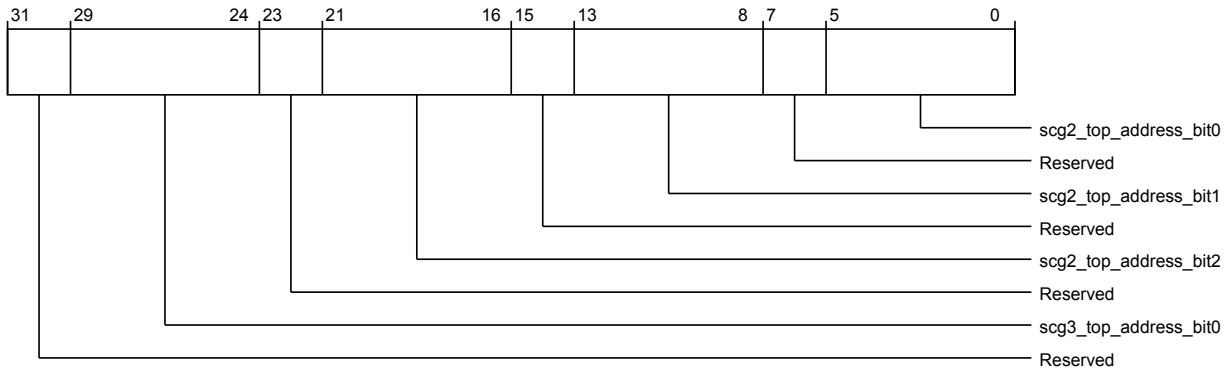


Figure 4-947 `por_rnsam_sys_cache_grp_sn_sam_cfg1` (low)

The following table shows the `sys_cache_grp_sn_sam_cfg1` lower register bit assignments.

Table 4-964 `por_rnsam_sys_cache_grp_sn_sam_cfg1` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>scg3_top_address_bit0</code>	Top address bit 0 for system cache group 3	RW	6'h00
23:22	Reserved	Reserved	RO	-
21:16	<code>scg2_top_address_bit2</code>	Top address bit 2 for system cache group 2	RW	6'h00
15:14	Reserved	Reserved	RO	-
13:8	<code>scg2_top_address_bit1</code>	Top address bit 1 for system cache group 2	RW	6'h00
7:6	Reserved	Reserved	RO	-
5:0	<code>scg2_top_address_bit0</code>	Top address bit 0 for system cache group 2	RW	6'h00

`gic_mem_region_reg`

Configures GIC memory region.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD58
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

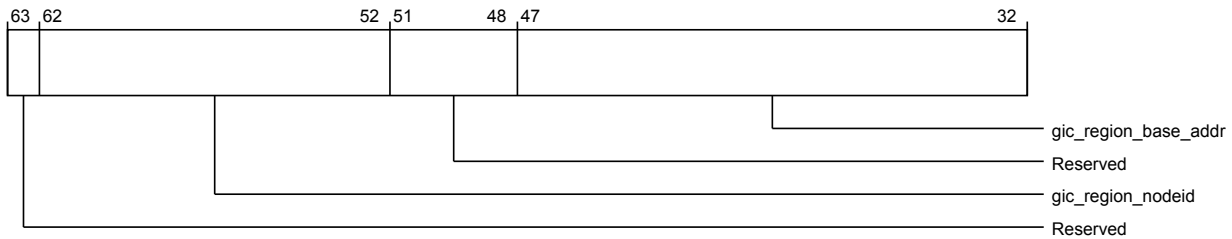


Figure 4-948 por_rnsam_gic_mem_region_reg (high)

The following table shows the gic_mem_region_reg higher register bit assignments.

Table 4-965 por_rnsam_gic_mem_region_reg (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:52	gic_region_nodeid	GIC node ID 30	RW	11'b000000000000
51:48	Reserved	Reserved	RO	-
47:32	gic_region_base_addr	Base address of the GIC memory region CONSTRAINT: Must be an integer multiple of region size	RW	32'h00000000

The following image shows the lower register bit assignments.

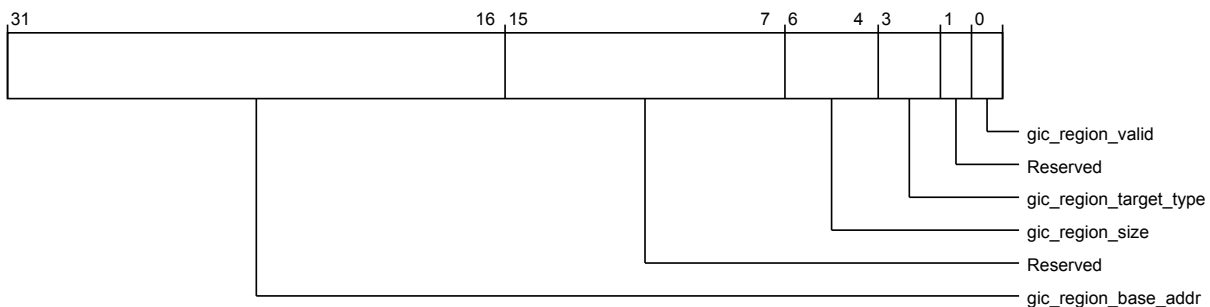


Figure 4-949 por_rnsam_gic_mem_region_reg (low)

The following table shows the gic_mem_region_reg lower register bit assignments.

Table 4-966 `por_rnsam_gic_mem_region_reg` (low)

Bits	Field name	Description	Type	Reset
31:16	<code>gic_region_base_addr</code>	Base address of the GIC memory region CONSTRAINT: Must be an integer multiple of region size	RW	32'h00000000
15:7	Reserved	Reserved	RO	-
6:4	<code>gic_region_size</code>	GIC memory region size 3'b000: 64KB 3'b001: 128KB 3'b010: 256KB 3'b011: 512KB CONSTRAINT: Memory region must be a power of 2.	RW	3'b000
3:2	<code>gic_region_target_type</code>	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	<code>gic_region_valid</code>	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

sys_cache_grp_sn_attr

Configures attributes for SN node IDs for system cache groups.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD60

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

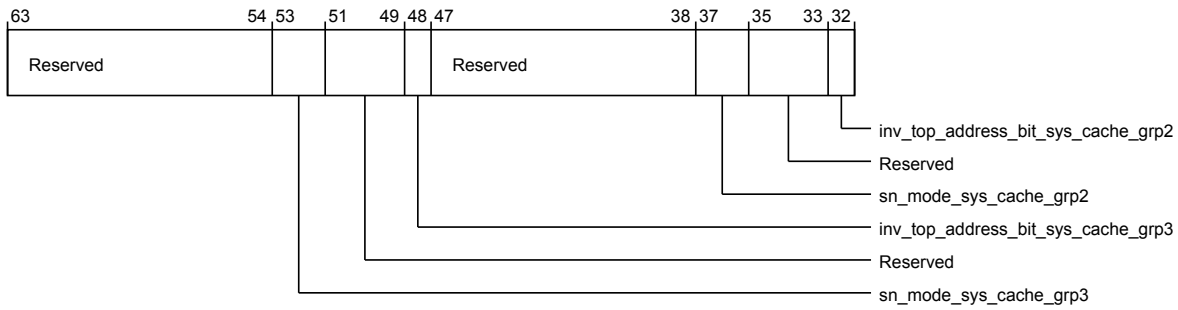


Figure 4-950 por_rnsam_sys_cache_grp_sn_attr (high)

The following table shows the sys_cache_grp_sn_attr higher register bit assignments.

Table 4-967 por_rnsam_sys_cache_grp_sn_attr (high)

Bits	Field name	Description	Type	Reset
63:54	Reserved	Reserved	RO	-
53:52	sn_mode_sys_cache_grp3	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b0
51:49	Reserved	Reserved	RO	-
48	inv_top_address_bit_sys_cache_grp3	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
47:38	Reserved	Reserved	RO	-
37:36	sn_mode_sys_cache_grp2	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b00
35:33	Reserved	Reserved	RO	-
32	inv_top_address_bit_sys_cache_grp2	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0

The following image shows the lower register bit assignments.

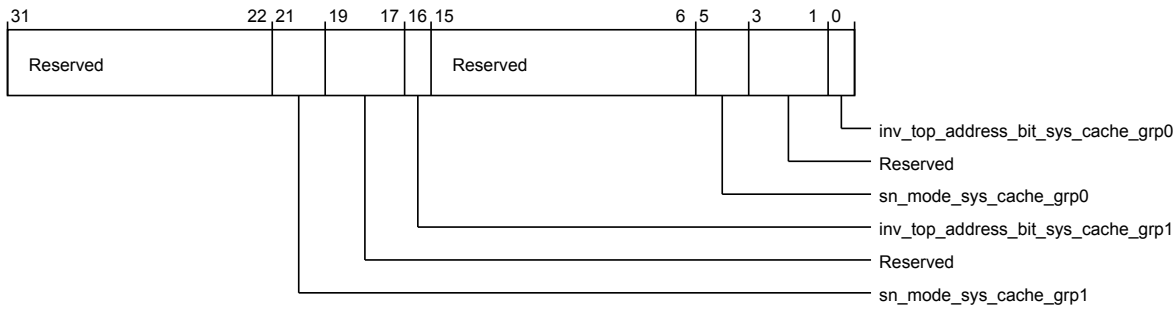


Figure 4-951 `por_rnsam_sys_cache_grp_sn_attr` (low)

The following table shows the `sys_cache_grp_sn_attr` lower register bit assignments.

Table 4-968 `por_rnsam_sys_cache_grp_sn_attr` (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21:20	<code>sn_mode_sys_cache_grp1</code>	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b0
19:17	Reserved	Reserved	RO	-
16	<code>inv_top_address_bit_sys_cache_grp1</code>	Inverts the top address bit (<code>top_address_bit1</code> if 3-SN, <code>top_address_bit2</code> if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
15:6	Reserved	Reserved	RO	-
5:4	<code>sn_mode_sys_cache_grp0</code>	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b0
3:1	Reserved	Reserved	RO	-
0	<code>inv_top_address_bit_sys_cache_grp0</code>	Inverts the top address bit (<code>top_address_bit1</code> if 3-SN, <code>top_address_bit2</code> if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0

`sys_cache_grp_hn_cpa_en_reg`

Configures CCIX port aggregation mode for hashed HN node IDs

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD68
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

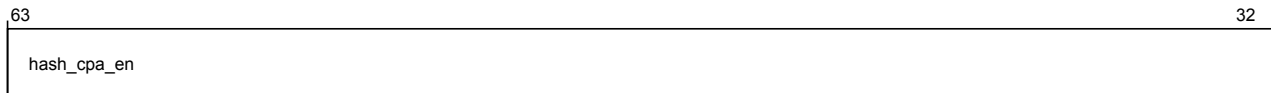


Figure 4-952 por_rnsam_sys_cache_grp_hn_cpa_en_reg (high)

The following table shows the sys_cache_grp_hn_cpa_en_reg higher register bit assignments.

Table 4-969 por_rnsam_sys_cache_grp_hn_cpa_en_reg (high)

Bits	Field name	Description	Type	Reset
63:32	hash_cpa_en	Enable CPA for each hashed node ID	RW	64'h0000000000000000

The following image shows the lower register bit assignments.

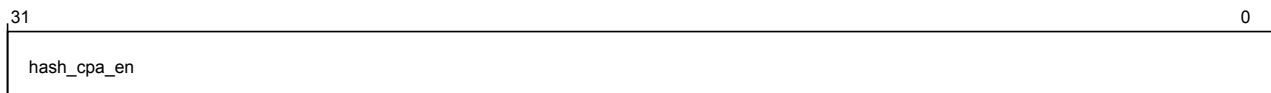


Figure 4-953 por_rnsam_sys_cache_grp_hn_cpa_en_reg (low)

The following table shows the sys_cache_grp_hn_cpa_en_reg lower register bit assignments.

Table 4-970 por_rnsam_sys_cache_grp_hn_cpa_en_reg (low)

Bits	Field name	Description	Type	Reset
31:0	hash_cpa_en	Enable CPA for each hashed node ID	RW	64'h0000000000000000

sys_cache_grp_hn_cpa_grp_reg

Configures CCIX port aggregation group ID for each System Cache Group

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD70
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

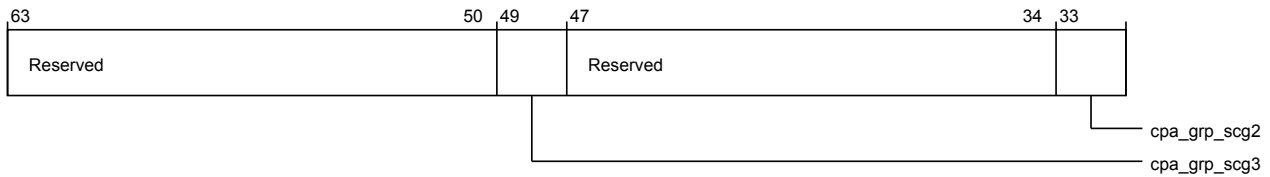


Figure 4-954 `por_rnsam_sys_cache_grp_hn_cpa_grp_reg` (high)

The following table shows the `sys_cache_grp_hn_cpa_grp_reg` higher register bit assignments.

Table 4-971 `por_rnsam_sys_cache_grp_hn_cpa_grp_reg` (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	<code>cpa_grp_scg3</code>	Specifies CCIX port aggregation group ID for System Cache Group 3 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'b00
47:34	Reserved	Reserved	RO	-
33:32	<code>cpa_grp_scg2</code>	Specifies CCIX port aggregation group ID for System Cache Group 2 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'b00

The following image shows the lower register bit assignments.

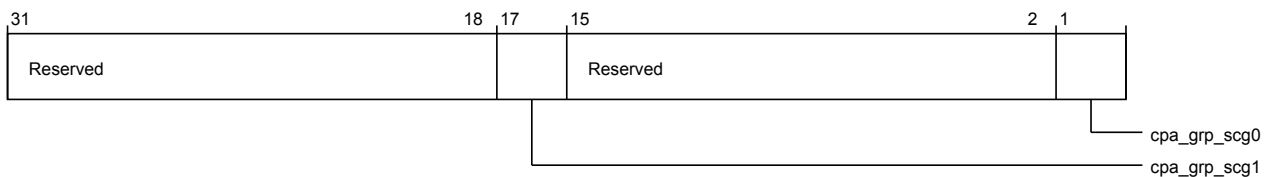


Figure 4-955 `por_rnsam_sys_cache_grp_hn_cpa_grp_reg` (low)

The following table shows the `sys_cache_grp_hn_cpa_grp_reg` lower register bit assignments.

Table 4-972 por_rnsam_sys_cache_grp_hn_cpa_grp_reg (low)

Bits	Field name	Description	Type	Reset
31:18	Reserved	Reserved	RO	-
17:16	cpa_grp_scg1	Specifies CCIX port aggregation group ID for System Cache Group 1 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'b00
15:2	Reserved	Reserved	RO	-
1:0	cpa_grp_scg0	Specifies CCIX port aggregation group ID for System Cache Group 0 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'b00

cml_port_aggr_mode_ctrl_reg

Configures the CCIX port aggregation modes for all non-hashed memory regions.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

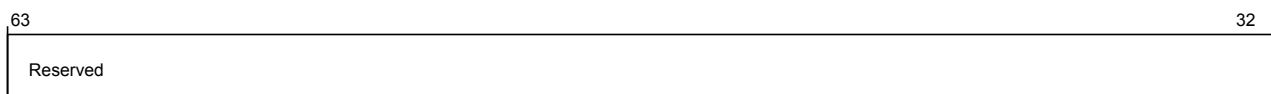


Figure 4-956 por_rnsam_cml_port_aggr_mode_ctrl_reg (high)

The following table shows the cml_port_aggr_mode_ctrl_reg higher register bit assignments.

Table 4-973 por_rnsam_cml_port_aggr_mode_ctrl_reg (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

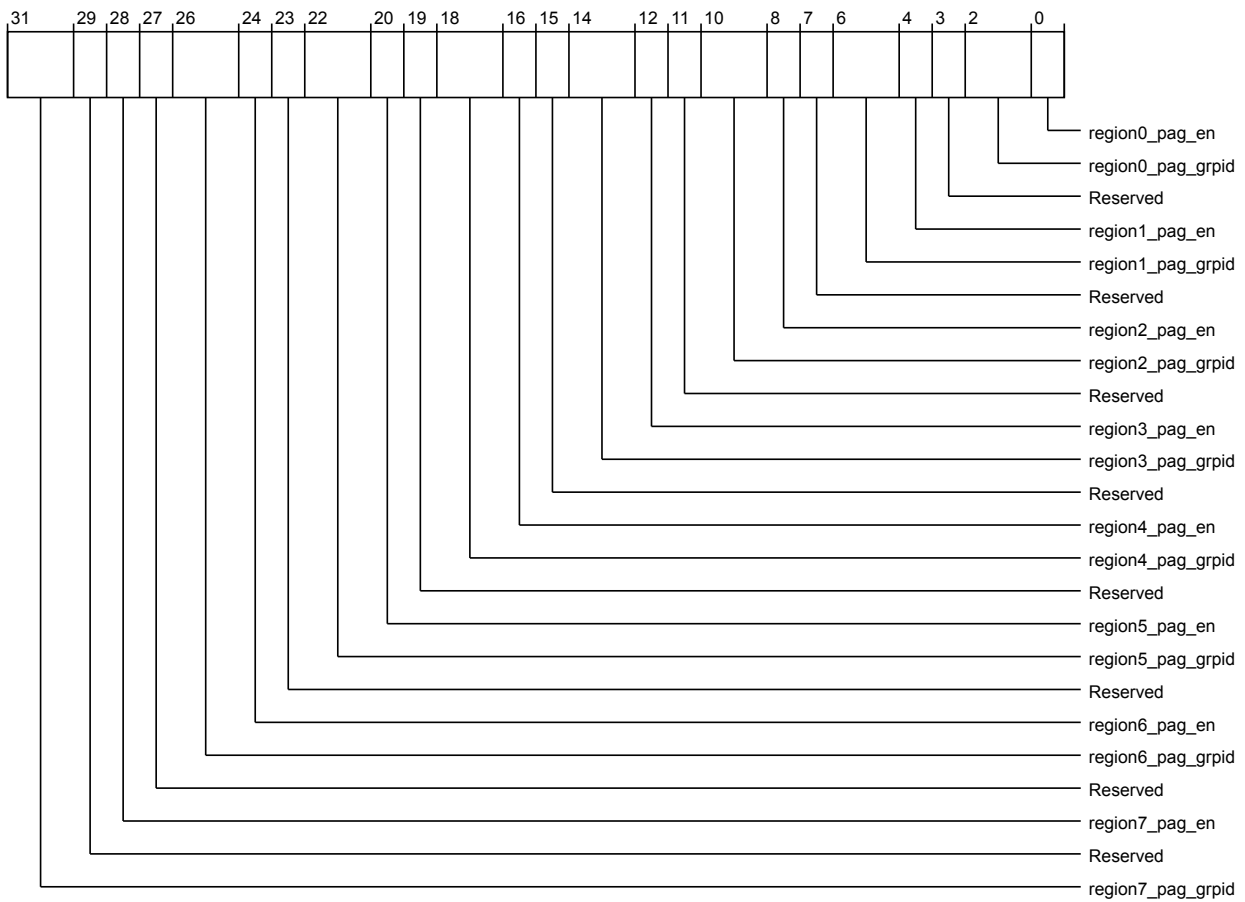


Figure 4-957 por_rnsam_cml_port_aggr_mode_ctrl_reg (low)

The following table shows the cml_port_aggr_mode_ctrl_reg lower register bit assignments.

Table 4-974 por_rnsam_cml_port_aggr_mode_ctrl_reg (low)

Bits	Field name	Description	Type	Reset
31:30	region7_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved7	RW	2'b0
29	Reserved	Reserved	RO	-
28	region7_pag_en	Enables the CPA mode for non-hashed memory region 7	RW	1'b0
27	Reserved	Reserved	RO	-

Table 4-974 por_rnsam_cml_port_aggr_mode_ctrl_reg (low) (continued)

Bits	Field name	Description	Type	Reset
26:25	region6_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved6	RW	2'b0
24	region6_pag_en	Enables the CPA mode for non-hashed memory region 6	RW	1'b0
23	Reserved	Reserved	RO	-
22:21	region5_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved5	RW	2'b0
20	region5_pag_en	Enables the CPA mode for non-hashed memory region 5	RW	1'b0
19	Reserved	Reserved	RO	-
18:17	region4_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved4	RW	2'b0
16	region4_pag_en	Enables the CPA mode for non-hashed memory region 4	RW	1'b0
15	Reserved	Reserved	RO	-
14:13	region3_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved3	RW	2'b0
12	region3_pag_en	Enables the CPA mode for non-hashed memory region 3	RW	1'b0
11	Reserved	Reserved	RO	-

Table 4-974 por_rnsam_cml_port_aggr_mode_ctrl_reg (low) (continued)

Bits	Field name	Description	Type	Reset
10:9	region2_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved2	RW	2'b0
8	region2_pag_en	Enables the CPA mode for non-hashed memory region 2	RW	1'b0
7	Reserved	Reserved	RO	-
6:5	region1_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved1	RW	2'b0
4	region1_pag_en	Enables the CPA mode for non-hashed memory region 1	RW	1'b0
3	Reserved	Reserved	RO	-
2:1	region0_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved0	RW	2'b0
0	region0_pag_en	Enables the CPA mode for non-hashed memory region 0	RW	1'b0

cml_port_aggr_grp0_add_mask

Configures the CCIX port aggregation address mask for group 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE08

Register reset 64'b1

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

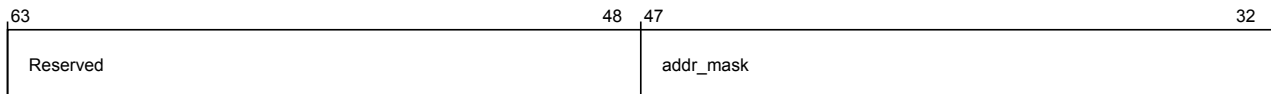


Figure 4-958 por_rnsam_cml_port_aggr_grp0_add_mask (high)

The following table shows the cml_port_aggr_grp0_add_mask higher register bit assignments.

Table 4-975 por_rnsam_cml_port_aggr_grp0_add_mask (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask to be applied before hashing	RW	42'b1

The following image shows the lower register bit assignments.

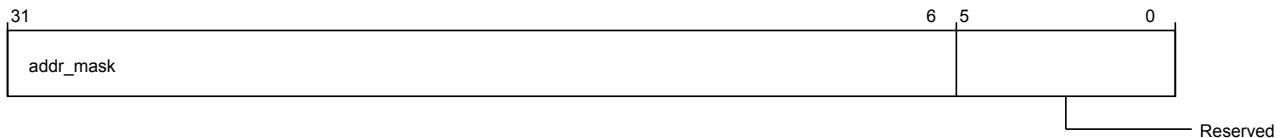


Figure 4-959 por_rnsam_cml_port_aggr_grp0_add_mask (low)

The following table shows the cml_port_aggr_grp0_add_mask lower register bit assignments.

Table 4-976 por_rnsam_cml_port_aggr_grp0_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	42'b1
5:0	Reserved	Reserved	RO	-

cml_port_aggr_grp1_add_mask

Configures the CCIX port aggregation address mask for group 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE10
Register reset	64'b1
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

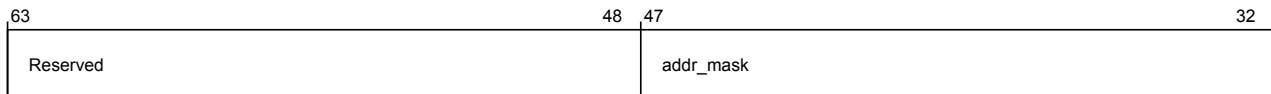


Figure 4-960 por_rnsam_cml_port_aggr_grp1_add_mask (high)

The following table shows the cml_port_aggr_grp1_add_mask higher register bit assignments.

Table 4-977 por_rnsam_cml_port_aggr_grp1_add_mask (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask to be applied before hashing	RW	42'b1

The following image shows the lower register bit assignments.

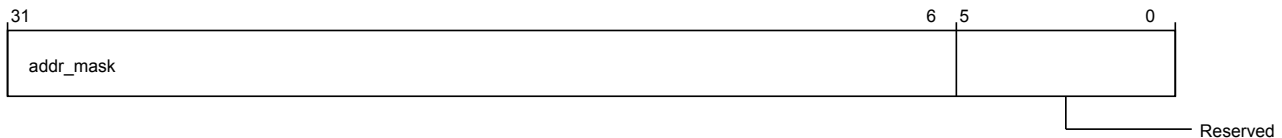


Figure 4-961 por_rnsam_cml_port_aggr_grp1_add_mask (low)

The following table shows the cml_port_aggr_grp1_add_mask lower register bit assignments.

Table 4-978 por_rnsam_cml_port_aggr_grp1_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	42'b1
5:0	Reserved	Reserved	RO	-

cml_port_aggr_grp0_reg

Configures the CCIX port aggregation port IDs for group 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE40
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

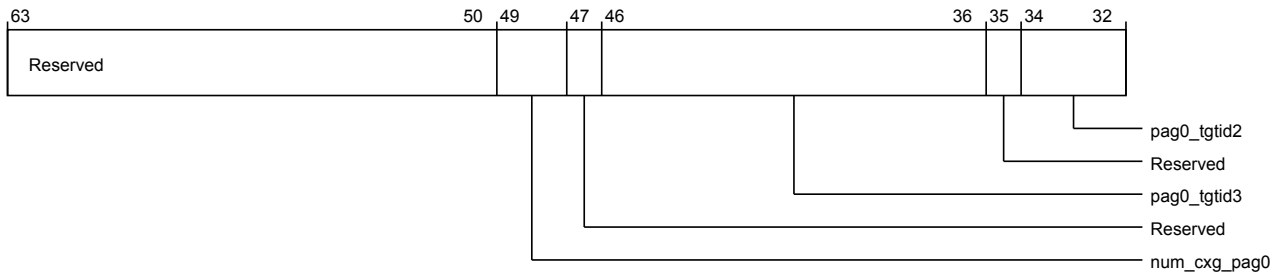


Figure 4-962 por_rnsam_cml_port_aggr_grp0_reg (high)

The following table shows the cml_port_aggr_grp0_reg higher register bit assignments.

Table 4-979 por_rnsam_cml_port_aggr_grp0_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	num_cxg_pag0	Specifies the number of CXRAs in CPAG 0 2'b00: 1 port used 2'b01: 2 ports used 2'b10: 4 ports used 2'b11: Reserved	RW	2'b0
47	Reserved	Reserved	RO	-
46:36	pag0_tgtid3	Specifies target ID 3 for CPAG 0	RW	11'b0
35	Reserved	Reserved	RO	-
34:32	pag0_tgtid2	Specifies target ID 2 for CPAG 0	RW	11'b0

The following image shows the lower register bit assignments.

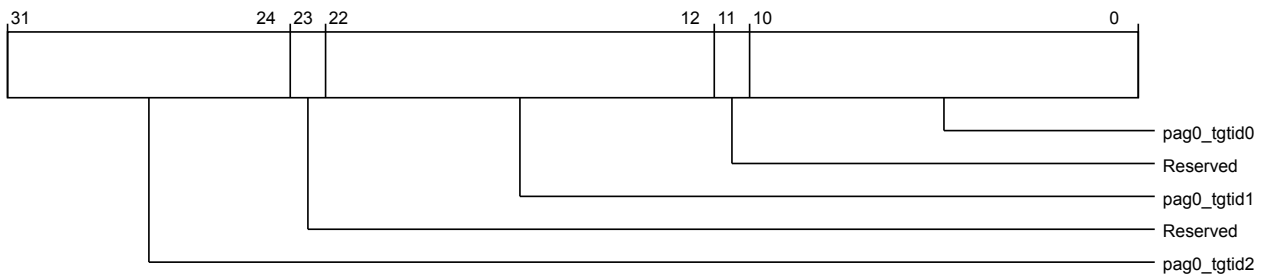


Figure 4-963 por_rnsam_cml_port_aggr_grp0_reg (low)

The following table shows the cml_port_aggr_grp0_reg lower register bit assignments.

Table 4-980 por_rnsam_cml_port_aggr_grp0_reg (low)

Bits	Field name	Description	Type	Reset
31:24	pag0_tgtid2	Specifies target ID 2 for CPAG 0	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag0_tgtid1	Specifies target ID 1 for CPAG 0	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	pag0_tgtid0	Specifies target ID 0 for CPAG 0	RW	11'b0

cml_port_aggr_grp1_reg

Configures the CCIX port aggregation port IDs for group 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE48

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

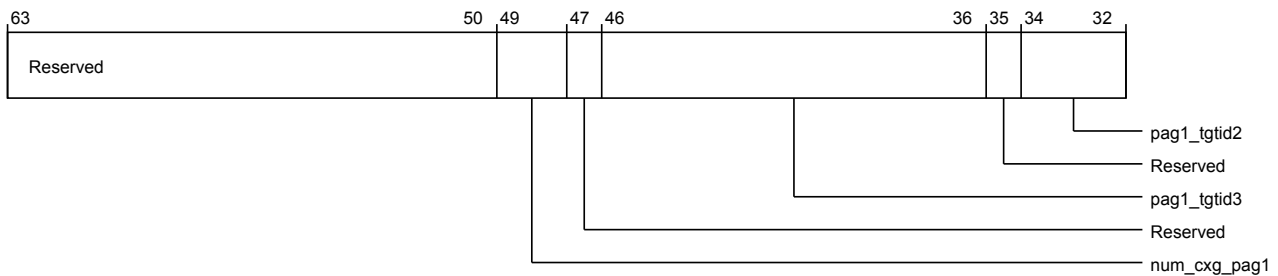


Figure 4-964 por_rnsam_cml_port_aggr_grp1_reg (high)

The following table shows the cml_port_aggr_grp1_reg higher register bit assignments.

Table 4-981 por_rnsam_cml_port_aggr_grp1_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	num_cxg_pag1	Specifies the number of CXRAs in CPAG 1	RW	2'b0
47	Reserved	Reserved	RO	-
46:36	pag1_tgtid3	Specifies target ID 3 for CPAG 1	RW	11'b0

Table 4-981 `por_rnsam_cml_port_aggr_grp1_reg` (high) (continued)

Bits	Field name	Description	Type	Reset
35	Reserved	Reserved	RO	-
34:32	<code>pag1_tgtid2</code>	Specifies target ID 2 for CPAG 1	RW	11'b0

The following image shows the lower register bit assignments.

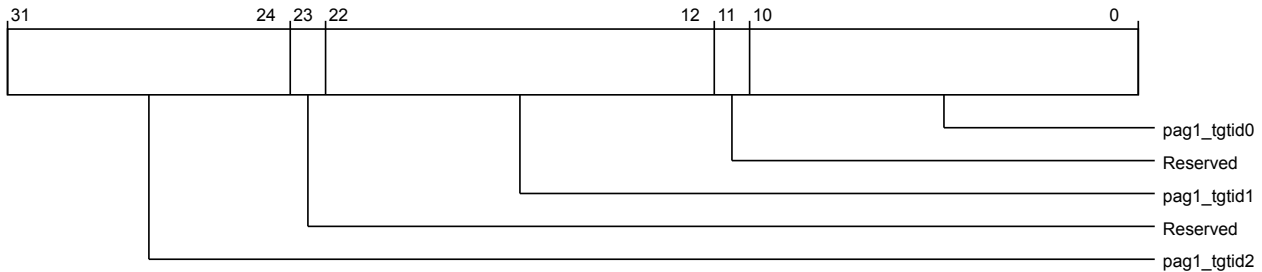


Figure 4-965 `por_rnsam_cml_port_aggr_grp1_reg` (low)

The following table shows the `cml_port_aggr_grp1_reg` lower register bit assignments.

Table 4-982 `por_rnsam_cml_port_aggr_grp1_reg` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>pag1_tgtid2</code>	Specifies target ID 2 for CPAG 1	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	<code>pag1_tgtid1</code>	Specifies target ID 1 for CPAG 1	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	<code>pag1_tgtid0</code>	Specifies target ID 0 for CPAG 1	RW	11'b0

`sys_cache_grp_secondary_reg0`

Configures secondary hashed memory regions 0 and 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF00

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

Secure group override `por_rnsam_secure_register_groups_override.mem_range`

The following image shows the higher register bit assignments.

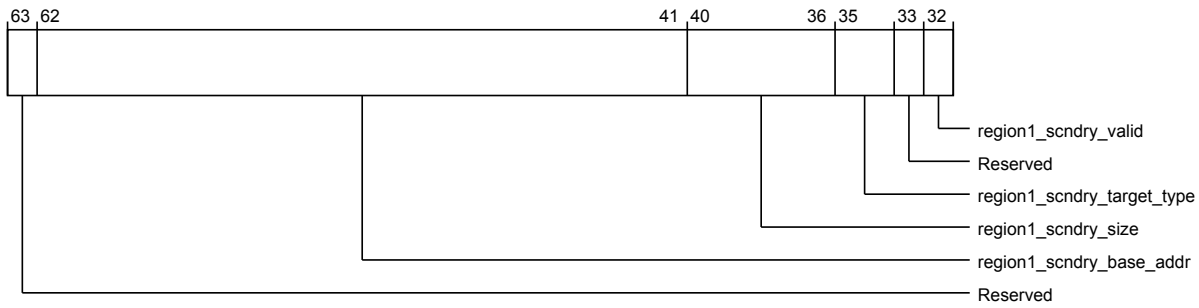


Figure 4-966 `por_rnsam_sys_cache_grp_secondary_reg0` (high)

The following table shows the `sys_cache_grp_secondary_reg0` higher register bit assignments.

Table 4-983 `por_rnsam_sys_cache_grp_secondary_reg0` (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	<code>region1_scndry_base_addr</code>	Bits [47:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	22'b000000000000000000000000
40:36	<code>region1_scndry_size</code>	Secondary memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	<code>region1_scndry_target_type</code>	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	<code>region1_scndry_valid</code>	Secondary memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

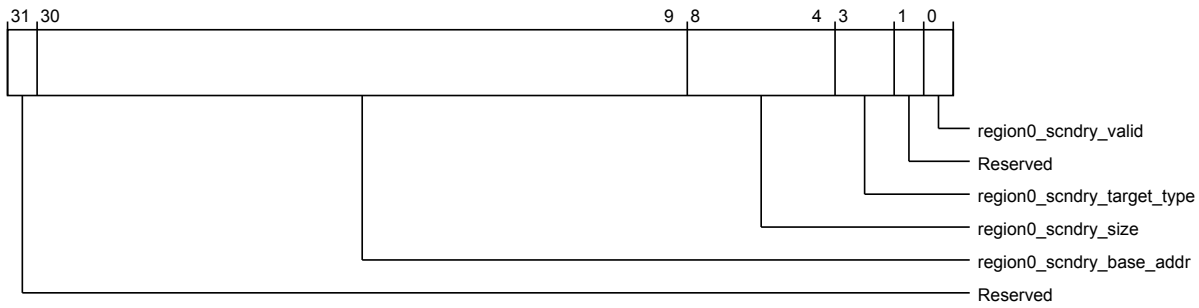


Figure 4-967 por_rnsam_sys_cache_grp_secondary_reg0 (low)

The following table shows the sys_cache_grp_secondary_reg0 lower register bit assignments.

Table 4-984 por_rnsam_sys_cache_grp_secondary_reg0 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region0_scndry_base_addr	Bits [47:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	22'b0000000000000000000000
8:4	region0_scndry_size	Secondary memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2 ^{address width}).	RW	5'b00000
3:2	region0_scndry_target_type	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region0_scndry_valid	Secondary memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

sys_cache_grp_secondary_reg1

Configures secondary hashed memory regions 2 and 3.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF08
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

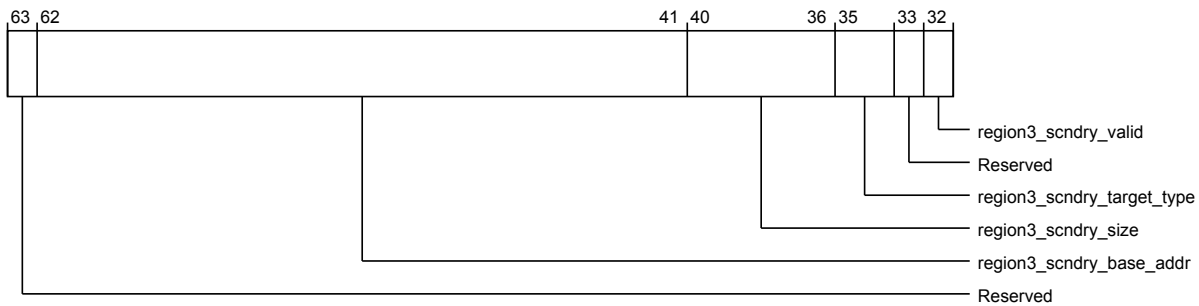


Figure 4-968 por_rnsam_sys_cache_grp_secondary_reg1 (high)

The following table shows the sys_cache_grp_secondary_reg1 higher register bit assignments.

Table 4-985 por_rnsam_sys_cache_grp_secondary_reg1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region3_scndry_base_addr	Bits [47:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	22'b000000000000000000000000
40:36	region3_scndry_size	Secondary memory region 3 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2 ^{address width}).	RW	5'b00000
35:34	region3_scndry_target_type	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region3_scndry_valid	Secondary memory region 3 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

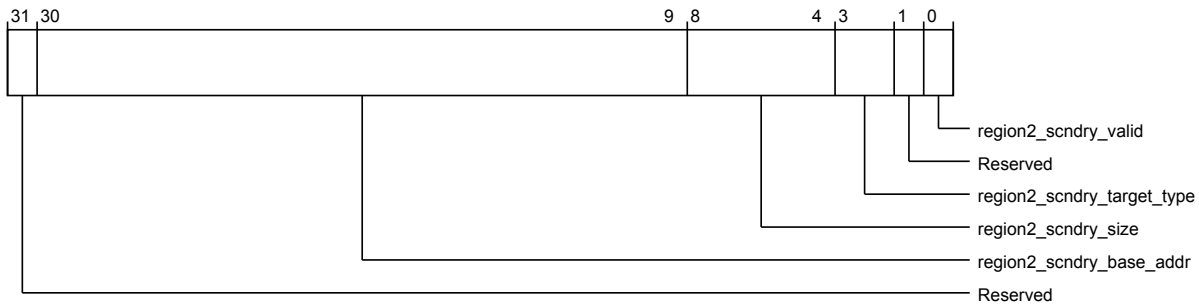


Figure 4-969 `por_rnsam_sys_cache_grp_secondary_reg1` (low)

The following table shows the `sys_cache_grp_secondary_reg1` lower register bit assignments.

Table 4-986 `por_rnsam_sys_cache_grp_secondary_reg1` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	<code>region2_scndry_base_addr</code>	Bits [47:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	22'b000000000000000000000000
8:4	<code>region2_scndry_size</code>	Secondary memory region 2 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2 ^{address width}).	RW	5'b00000
3:2	<code>region2_scndry_target_type</code>	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	<code>region2_scndry_valid</code>	Secondary memory region 2 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

`sys_cache_grp_cal_mode_reg`

Configures the HN-F CAL mode support for all system cache groups.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF10
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

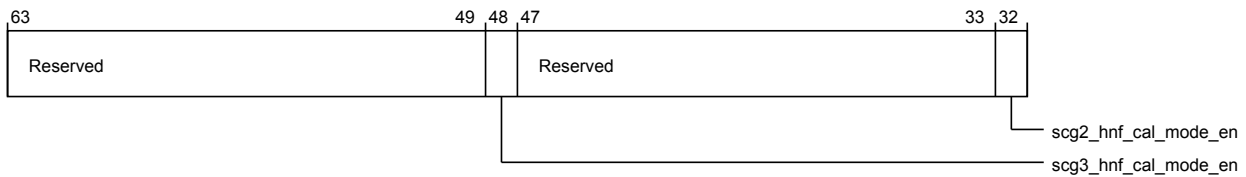


Figure 4-970 por_rnsam_sys_cache_grp_cal_mode_reg (high)

The following table shows the sys_cache_grp_cal_mode_reg higher register bit assignments.

Table 4-987 por_rnsam_sys_cache_grp_cal_mode_reg (high)

Bits	Field name	Description	Type	Reset
63:49	Reserved	Reserved	RO	-
48	scg3_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 3	RW	1'b0
47:33	Reserved	Reserved	RO	-
32	scg2_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 2	RW	1'b0

The following image shows the lower register bit assignments.

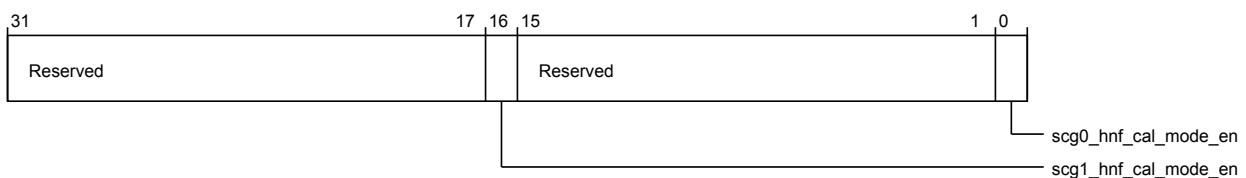


Figure 4-971 por_rnsam_sys_cache_grp_cal_mode_reg (low)

The following table shows the sys_cache_grp_cal_mode_reg lower register bit assignments.

Table 4-988 por_rnsam_sys_cache_grp_cal_mode_reg (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	scg1_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 1	RW	1'b0
15:1	Reserved	Reserved	RO	-
0	scg0_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 0	RW	1'b0

rnsam_hash_addr_mask_reg

Configures the address mask that is applied before hashing the address bits.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF18

[illegible]

Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.
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The following image shows the higher register bit assignments.

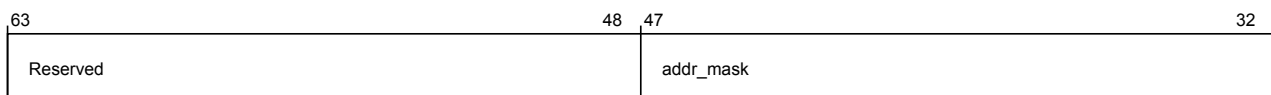


Figure 4-972 `por_rnsam_rnsam_hash_addr_mask_reg` (high)

The following table shows the `rnsam` `hash` `addr` `mask` `reg` higher register bit assignments.

Table 4-989 `por_rnsam_rnsam_hash_addr_mask_reg` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask applied before hashing	RW	42'h3FFFFFFFFF

The following image shows the lower register bit assignments.

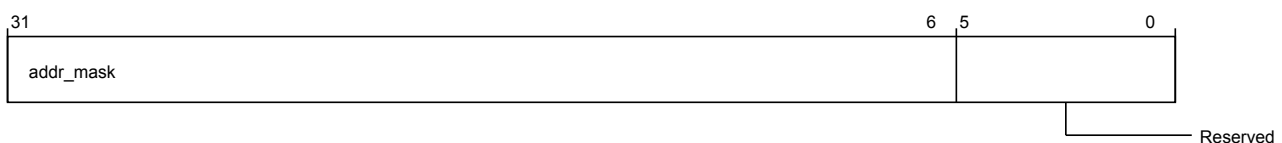


Figure 4-973 `por_rnsam_rnsam_hash_addr_mask_reg` (low)

The following table shows the `rnsam` `hash` `addr` `mask` `reg` lower register bit assignments.

Table 4-990 `por_rnsam_rnsam_hash_addr_mask_reg` (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask applied before hashing	RW	42'h3FFFFFFFFF
5:0	Reserved	Reserved	RO	-

rnsam_region_cmp_addr_mask_reg

Configures the address mask that is applied before region compare.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF20
Register reset	64'b11111111111111111111111111111111
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

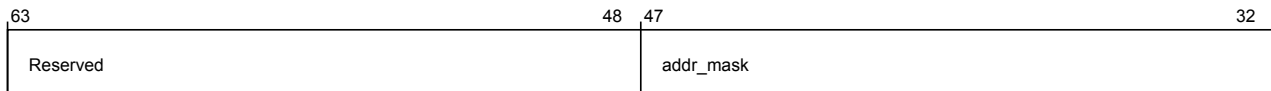


Figure 4-974 por_rnsam_rnsam_region_cmp_addr_mask_reg (high)

The following table shows the rnsam_region_cmp_addr_mask_reg higher register bit assignments.

Table 4-991 por_rnsam_rnsam_region_cmp_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask applied before memory region compare	RW	32'hFFFFFFFF

The following image shows the lower register bit assignments.

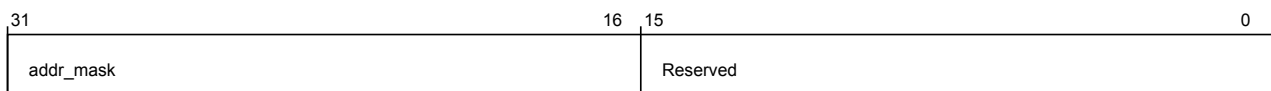


Figure 4-975 por_rnsam_rnsam_region_cmp_addr_mask_reg (low)

The following table shows the rnsam_region_cmp_addr_mask_reg lower register bit assignments.

Table 4-992 por_rnsam_rnsam_region_cmp_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:16	addr_mask	Address mask applied before memory region compare	RW	32'hFFFFFFFF
15:0	Reserved	Reserved	RO	-

sys_cache_grp_hn_nodeid_reg8

Configures hashed node IDs for system cache groups. Controls target HN node IDs 32 to 35.

Its characteristics are:

Type	RW
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Register width (Bits) 64
Address offset 14'hF58
Register reset 64'b0
Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

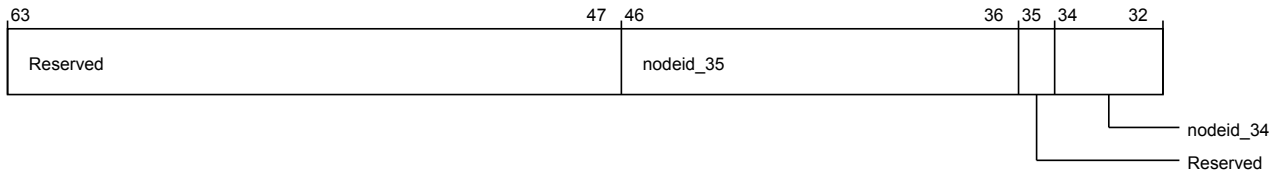


Figure 4-976 `por_rnsam_sys_cache_grp_hn_nodeid_reg8` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg8` higher register bit assignments.

Table 4-993 `por_rnsam_sys_cache_grp_hn_nodeid_reg8` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	<code>nodeid_35</code>	Hashed target node ID 35	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	<code>nodeid_34</code>	Hashed target node ID 34	RW	11'b000000000000

The following image shows the lower register bit assignments.

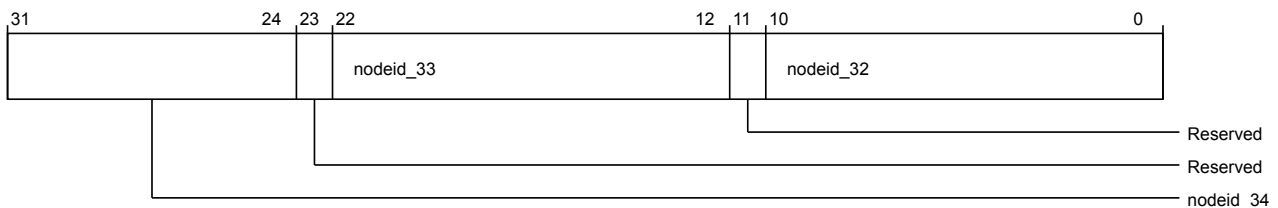


Figure 4-977 `por_rnsam_sys_cache_grp_hn_nodeid_reg8` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg8` lower register bit assignments.

Table 4-994 `por_rnsam_sys_cache_grp_hn_nodeid_reg8` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>nodeid_34</code>	Hashed target node ID 34	RW	11'b000000000000
23	Reserved	Reserved	RO	-

Table 4-994 por_rnsam_sys_cache_grp_hn_nodeid_reg8 (low) (continued)

Bits	Field name	Description	Type	Reset
22:12	nodeid_33	Hashed target node ID 33	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_32	Hashed target node ID 32	RW	11'b000000000000

sys_cache_grp_hn_nodeid_reg9

Configures hashed node IDs for system cache groups. Controls target HN node IDs 36 to 39.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF60

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

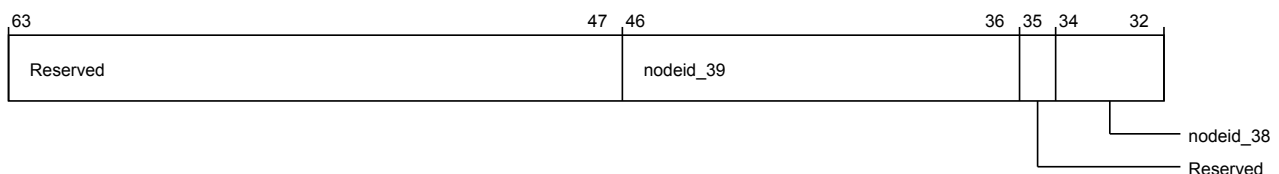


Figure 4-978 por_rnsam_sys_cache_grp_hn_nodeid_reg9 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg9 higher register bit assignments.

Table 4-995 por_rnsam_sys_cache_grp_hn_nodeid_reg9 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_39	Hashed target node ID 39	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_38	Hashed target node ID 38	RW	11'b000000000000

The following image shows the lower register bit assignments.

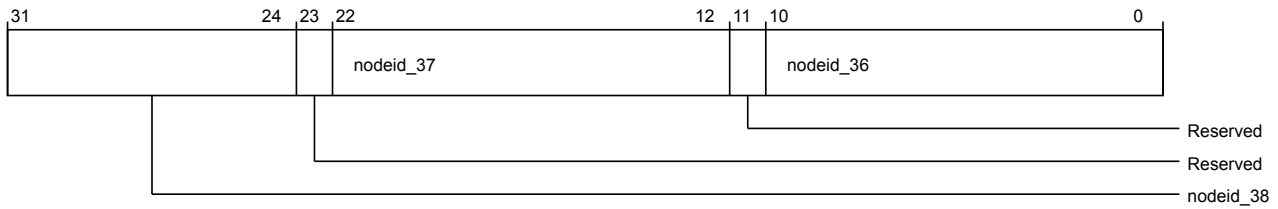


Figure 4-979 `por_rnsam_sys_cache_grp_hn_nodeid_reg9` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg9` lower register bit assignments.

Table 4-996 `por_rnsam_sys_cache_grp_hn_nodeid_reg9` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>nodeid_38</code>	Hashed target node ID 38	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	<code>nodeid_37</code>	Hashed target node ID 37	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	<code>nodeid_36</code>	Hashed target node ID 36	RW	11'b000000000000

`sys_cache_grp_hn_nodeid_reg10`

Configures hashed node IDs for system cache groups. Controls target HN node IDs 40 to 43.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF68
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

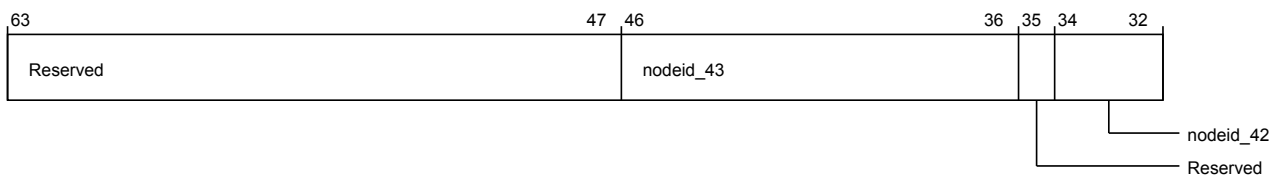


Figure 4-980 `por_rnsam_sys_cache_grp_hn_nodeid_reg10` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg10` higher register bit assignments.

Table 4-997 `por_rnsam_sys_cache_grp_hn_nodeid_reg10` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_43	Hashed target node ID 43	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_42	Hashed target node ID 42	RW	11'b000000000000

The following image shows the lower register bit assignments.

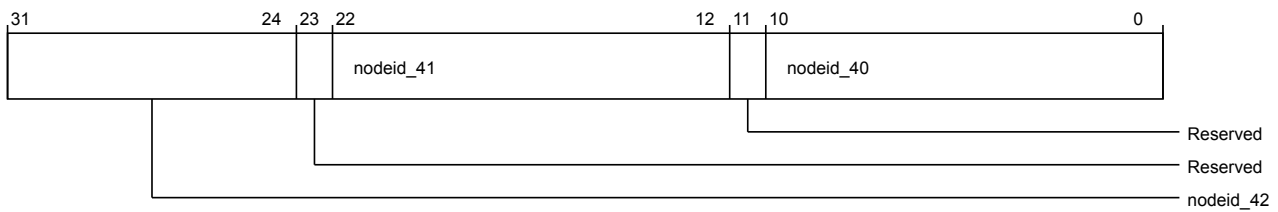


Figure 4-981 `por_rnsam_sys_cache_grp_hn_nodeid_reg10` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg10` lower register bit assignments.

Table 4-998 `por_rnsam_sys_cache_grp_hn_nodeid_reg10` (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_42	Hashed target node ID 42	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_41	Hashed target node ID 41	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_40	Hashed target node ID 40	RW	11'b000000000000

`sys_cache_grp_hn_nodeid_reg11`

Configures hashed node IDs for system cache groups. Controls target HN node IDs 44 to 47.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF70

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

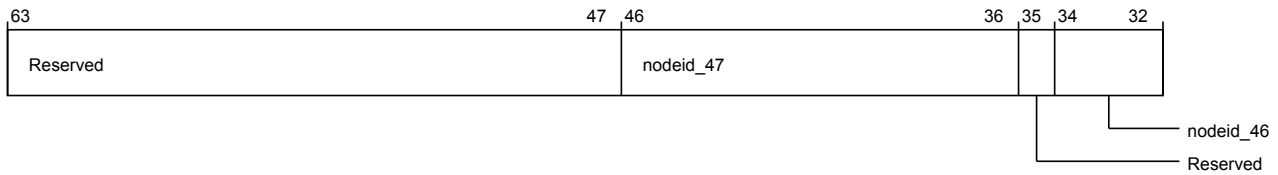


Figure 4-982 `por_rnsam_sys_cache_grp_hn_nodeid_reg11` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg11` higher register bit assignments.

Table 4-999 `por_rnsam_sys_cache_grp_hn_nodeid_reg11` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_47	Hashed target node ID 47	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_46	Hashed target node ID 46	RW	11'b000000000000

The following image shows the lower register bit assignments.

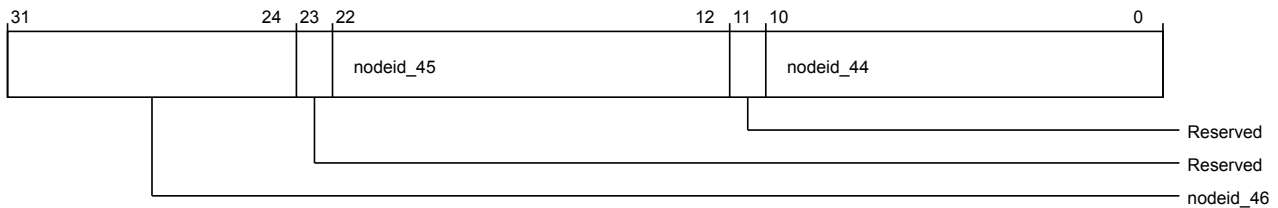


Figure 4-983 `por_rnsam_sys_cache_grp_hn_nodeid_reg11` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg11` lower register bit assignments.

Table 4-1000 `por_rnsam_sys_cache_grp_hn_nodeid_reg11` (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_46	Hashed target node ID 46	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_45	Hashed target node ID 45	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_44	Hashed target node ID 44	RW	11'b000000000000

`sys_cache_grp_hn_nodeid_reg12`

Configures hashed node IDs for system cache groups. Controls target HN node IDs 48 to 51.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF78
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

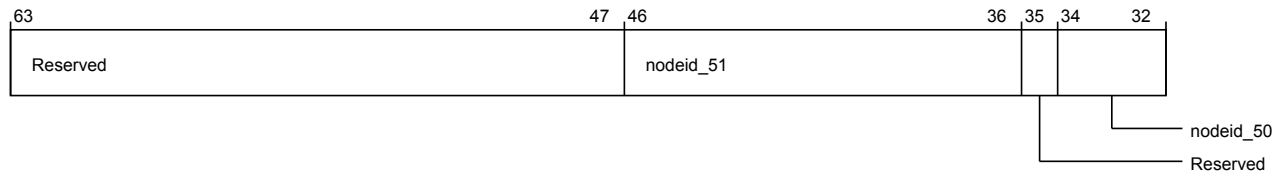


Figure 4-984 por_rnsam_sys_cache_grp_hn_nodeid_reg12 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg12 higher register bit assignments.

Table 4-1001 por_rnsam_sys_cache_grp_hn_nodeid_reg12 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_51	Hashed target node ID 51	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_50	Hashed target node ID 50	RW	11'b000000000000

The following image shows the lower register bit assignments.

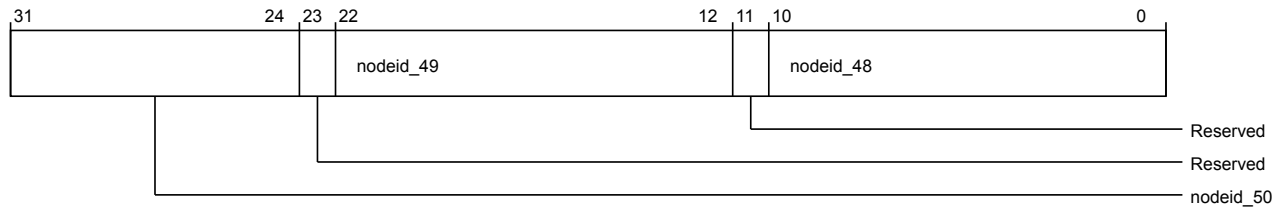


Figure 4-985 por_rnsam_sys_cache_grp_hn_nodeid_reg12 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg12 lower register bit assignments.

Table 4-1002 `por_rnsam_sys_cache_grp_hn_nodeid_reg12` (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_50	Hashed target node ID 50	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_49	Hashed target node ID 49	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_48	Hashed target node ID 48	RW	11'b000000000000

sys_cache_grp_hn_nodeid_reg13

Configures hashed node IDs for system cache groups. Controls target HN node IDs 52 to 55.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

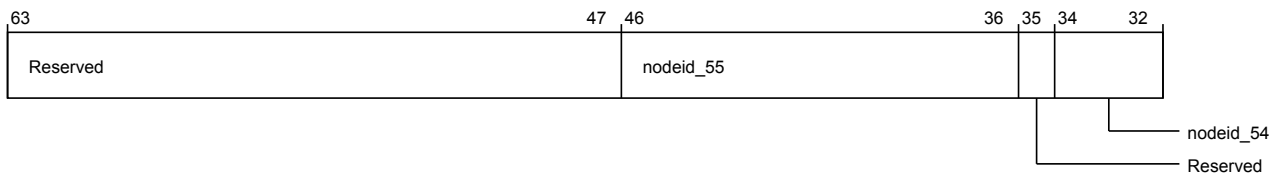


Figure 4-986 `por_rnsam_sys_cache_grp_hn_nodeid_reg13` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg13` higher register bit assignments.

Table 4-1003 `por_rnsam_sys_cache_grp_hn_nodeid_reg13` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_55	Hashed target node ID 55	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_54	Hashed target node ID 54	RW	11'b000000000000

The following image shows the lower register bit assignments.

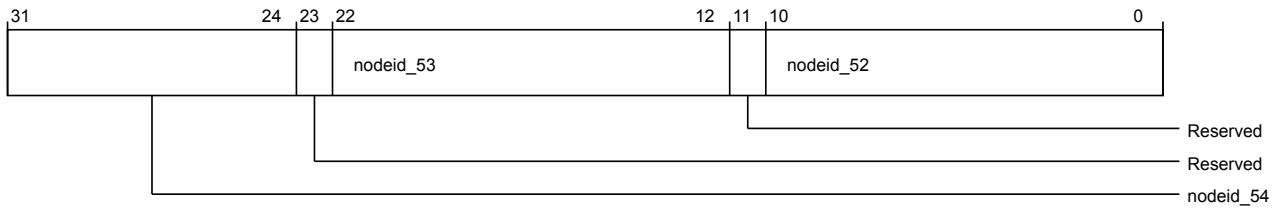


Figure 4-987 por_rnsam_sys_cache_grp_hn_nodeid_reg13 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg13 lower register bit assignments.

Table 4-1004 por_rnsam_sys_cache_grp_hn_nodeid_reg13 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_54	Hashed target node ID 54	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_53	Hashed target node ID 53	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_52	Hashed target node ID 52	RW	11'b000000000000

sys_cache_grp_hn_nodeid_reg14

Configures hashed node IDs for system cache groups. Controls target HN node IDs 56 to 59.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF88
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

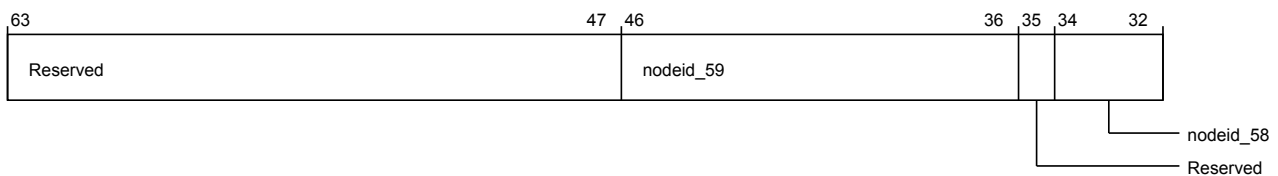


Figure 4-988 por_rnsam_sys_cache_grp_hn_nodeid_reg14 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg14 higher register bit assignments.

Table 4-1005 por_rnsam_sys_cache_grp_hn_nodeid_reg14 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_59	Hashed target node ID 59	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_58	Hashed target node ID 58	RW	11'b000000000000

The following image shows the lower register bit assignments.

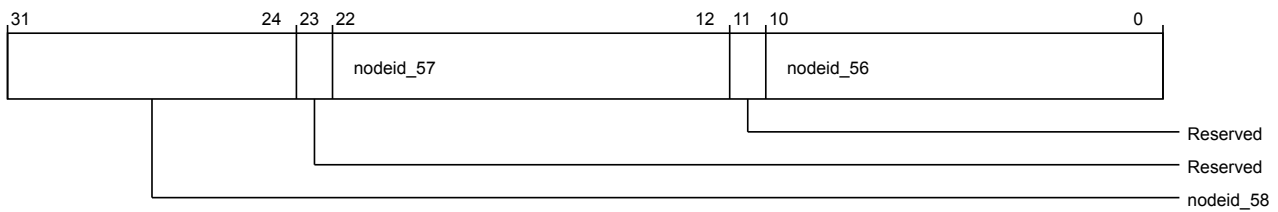


Figure 4-989 por_rnsam_sys_cache_grp_hn_nodeid_reg14 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg14 lower register bit assignments.

Table 4-1006 por_rnsam_sys_cache_grp_hn_nodeid_reg14 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_58	Hashed target node ID 58	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_57	Hashed target node ID 57	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_56	Hashed target node ID 56	RW	11'b000000000000

sys_cache_grp_hn_nodeid_reg15

Configures hashed node IDs for system cache groups. Controls target HN node IDs 60 to 63.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF90

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

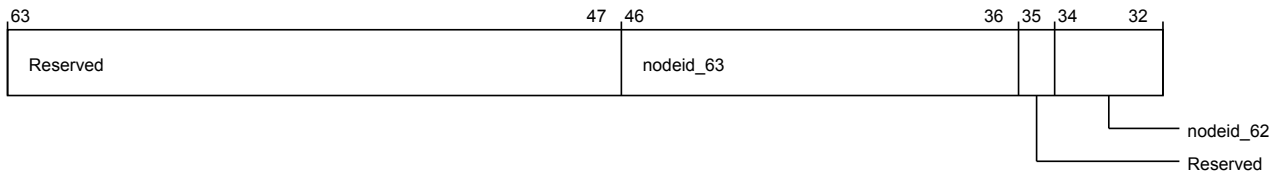


Figure 4-990 `por_rnsam_sys_cache_grp_hn_nodeid_reg15` (high)

The following table shows the `sys_cache_grp_hn_nodeid_reg15` higher register bit assignments.

Table 4-1007 `por_rnsam_sys_cache_grp_hn_nodeid_reg15` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_63	Hashed target node ID 63	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_62	Hashed target node ID 62	RW	11'b000000000000

The following image shows the lower register bit assignments.

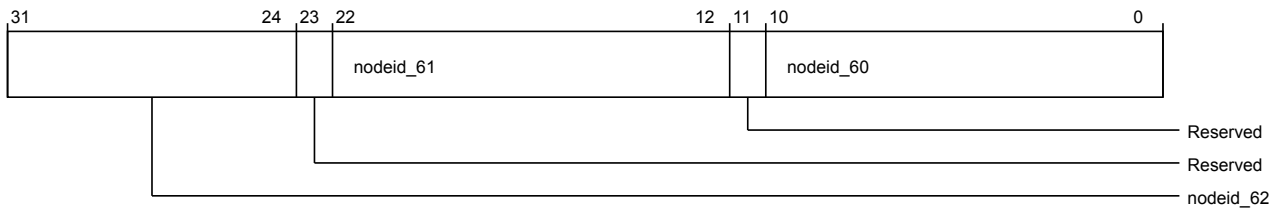


Figure 4-991 `por_rnsam_sys_cache_grp_hn_nodeid_reg15` (low)

The following table shows the `sys_cache_grp_hn_nodeid_reg15` lower register bit assignments.

Table 4-1008 `por_rnsam_sys_cache_grp_hn_nodeid_reg15` (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_62	Hashed target node ID 62	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_61	Hashed target node ID 61	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_60	Hashed target node ID 60	RW	11'b000000000000

`sys_cache_grp_sn_nodeid_reg8`

Configures hashed node IDs for system cache groups. Controls target SN node IDs 32 to 35.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1008
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

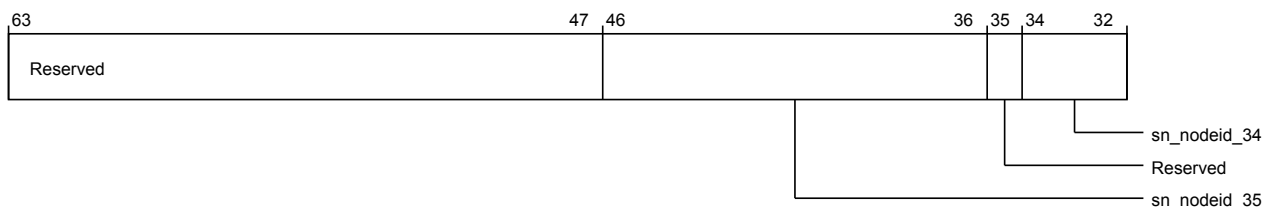


Figure 4-992 por_rnsam_sys_cache_grp_sn_nodeid_reg8 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg8 higher register bit assignments.

Table 4-1009 por_rnsam_sys_cache_grp_sn_nodeid_reg8 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_35	Hashed target SN node ID 35	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_34	Hashed target SN node ID 34	RW	11'b000000000000

The following image shows the lower register bit assignments.

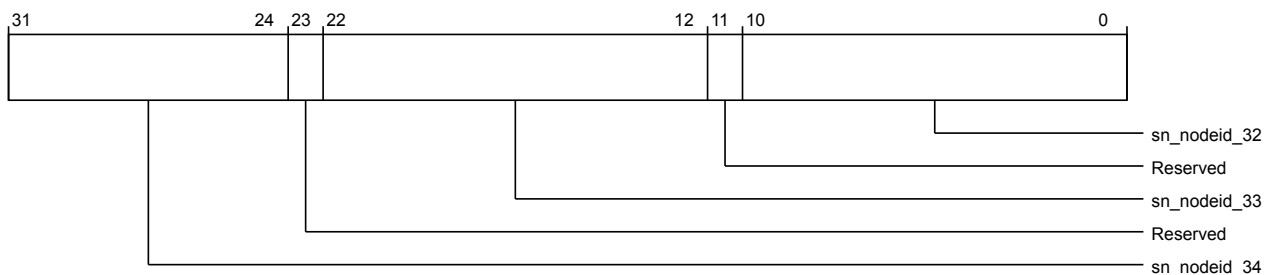


Figure 4-993 por_rnsam_sys_cache_grp_sn_nodeid_reg8 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg8 lower register bit assignments.

Table 4-1010 por_rnsam_sys_cache_grp_sn_nodeid_reg8 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_34	Hashed target SN node ID 34	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_33	Hashed target SN node ID 33	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_32	Hashed target SN node ID 32	RW	11'b000000000000

sys_cache_grp_sn_nodeid_reg9

Configures hashed node IDs for system cache groups. Controls target SN node IDs 36 to 39.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1010

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

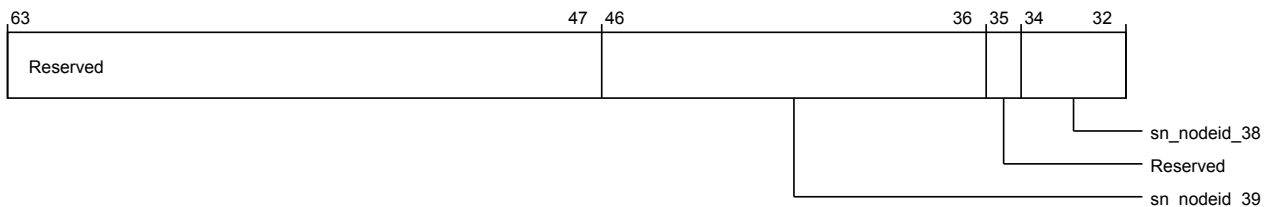


Figure 4-994 por_rnsam_sys_cache_grp_sn_nodeid_reg9 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg9 higher register bit assignments.

Table 4-1011 por_rnsam_sys_cache_grp_sn_nodeid_reg9 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_39	Hashed target SN node ID 39	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_38	Hashed target SN node ID 38	RW	11'b000000000000

The following image shows the lower register bit assignments.

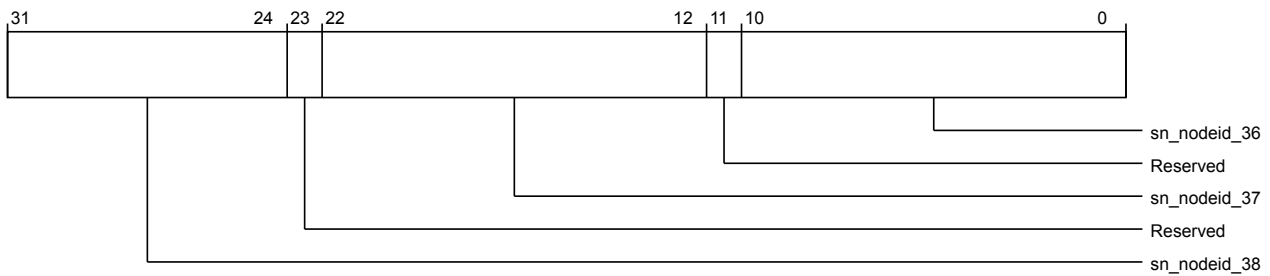


Figure 4-995 por_rnsam_sys_cache_grp_sn_nodeid_reg9 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg9 lower register bit assignments.

Table 4-1012 por_rnsam_sys_cache_grp_sn_nodeid_reg9 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_38	Hashed target SN node ID 38	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_37	Hashed target SN node ID 37	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_36	Hashed target SN node ID 36	RW	11'b000000000000

sys_cache_grp_sn_nodeid_reg10

Configures hashed node IDs for system cache groups. Controls target SN node IDs 40 to 43.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1018
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

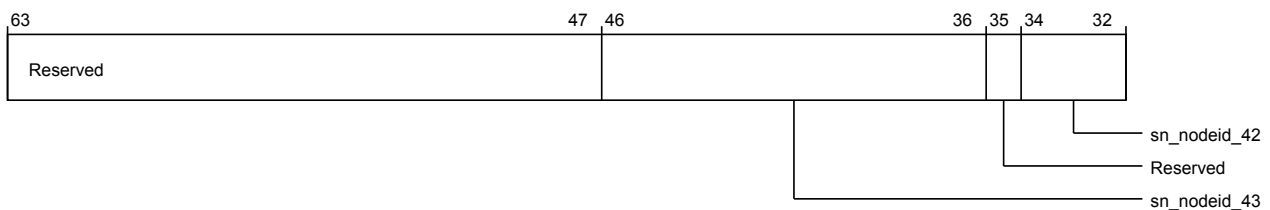


Figure 4-996 por_rnsam_sys_cache_grp_sn_nodeid_reg10 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg10 higher register bit assignments.

Table 4-1013 por_rnsam_sys_cache_grp_sn_nodeid_reg10 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_43	Hashed target SN node ID 43	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_42	Hashed target SN node ID 42	RW	11'b000000000000

The following image shows the lower register bit assignments.

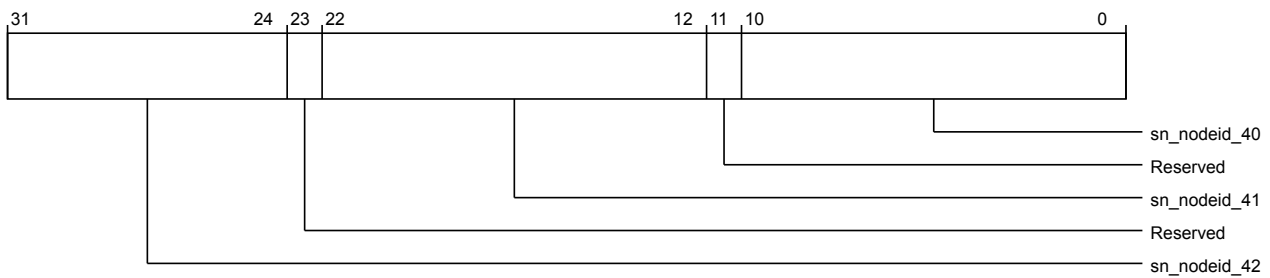


Figure 4-997 por_rnsam_sys_cache_grp_sn_nodeid_reg10 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg10 lower register bit assignments.

Table 4-1014 por_rnsam_sys_cache_grp_sn_nodeid_reg10 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_42	Hashed target SN node ID 42	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_41	Hashed target SN node ID 41	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_40	Hashed target SN node ID 40	RW	11'b000000000000

sys_cache_grp_sn_nodeid_reg11

Configures hashed node IDs for system cache groups. Controls target SN node IDs 44 to 47.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1020

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

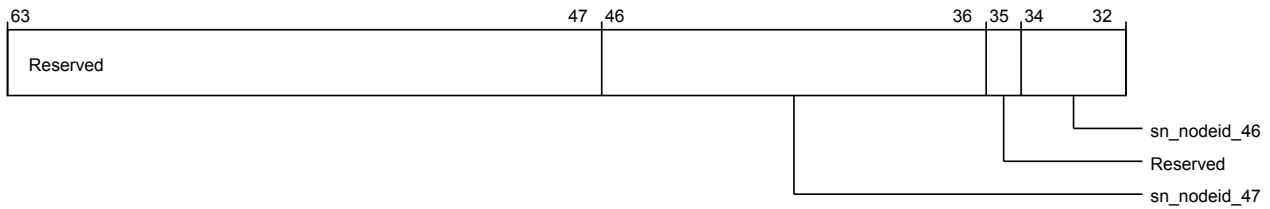


Figure 4-998 por_rnsam_sys_cache_grp_sn_nodeid_reg11 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg11 higher register bit assignments.

Table 4-1015 por_rnsam_sys_cache_grp_sn_nodeid_reg11 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_47	Hashed target SN node ID 47	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_46	Hashed target SN node ID 46	RW	11'b000000000000

The following image shows the lower register bit assignments.

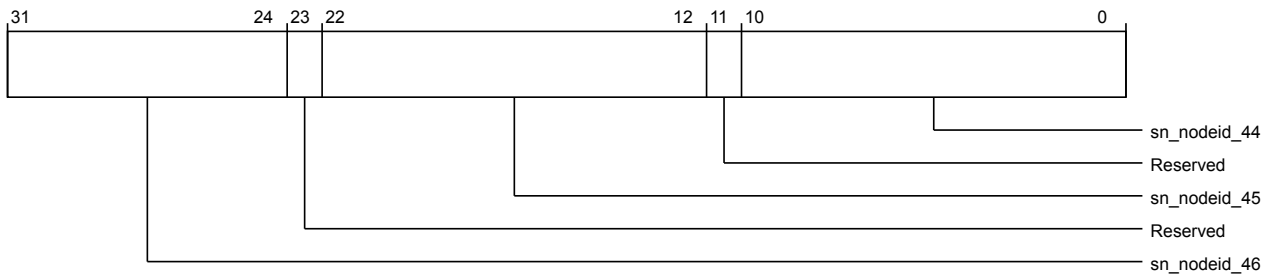


Figure 4-999 por_rnsam_sys_cache_grp_sn_nodeid_reg11 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg11 lower register bit assignments.

Table 4-1016 por_rnsam_sys_cache_grp_sn_nodeid_reg11 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_46	Hashed target SN node ID 46	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_45	Hashed target SN node ID 45	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_44	Hashed target SN node ID 44	RW	11'b000000000000

sys_cache_grp_sn_nodeid_reg12

Configures hashed node IDs for system cache groups. Controls target SN node IDs 48 to 51.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1028
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

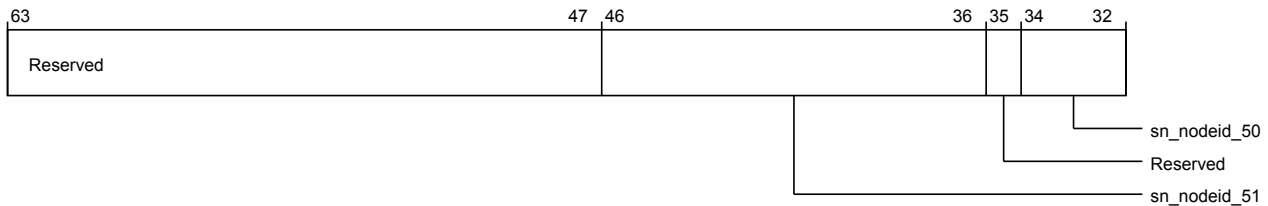


Figure 4-1000 por_rnsam_sys_cache_grp_sn_nodeid_reg12 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg12 higher register bit assignments.

Table 4-1017 por_rnsam_sys_cache_grp_sn_nodeid_reg12 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_51	Hashed target SN node ID 51	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_50	Hashed target SN node ID 50	RW	11'b000000000000

The following image shows the lower register bit assignments.

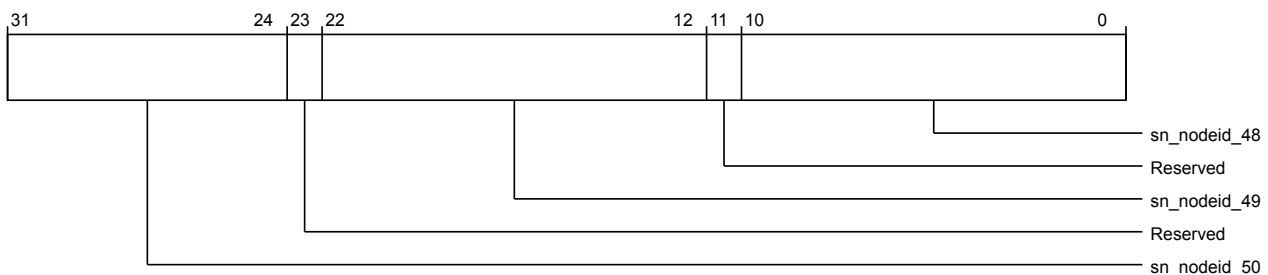


Figure 4-1001 por_rnsam_sys_cache_grp_sn_nodeid_reg12 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg12 lower register bit assignments.

Table 4-1018 `por_rnsam_sys_cache_grp_sn_nodeid_reg12` (low)

Bits	Field name	Description	Type	Reset
31:24	<code>sn_nodeid_50</code>	Hashed target SN node ID 50	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	<code>sn_nodeid_49</code>	Hashed target SN node ID 49	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	<code>sn_nodeid_48</code>	Hashed target SN node ID 48	RW	11'b000000000000

`sys_cache_grp_sn_nodeid_reg13`

Configures hashed node IDs for system cache groups. Controls target SN node IDs 52 to 55.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1030

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

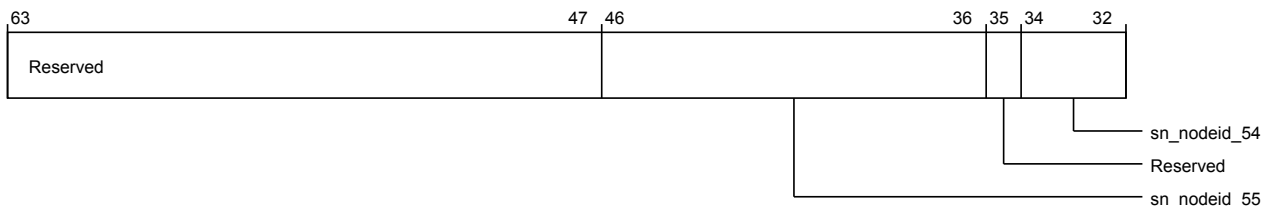


Figure 4-1002 `por_rnsam_sys_cache_grp_sn_nodeid_reg13` (high)

The following table shows the `sys_cache_grp_sn_nodeid_reg13` higher register bit assignments.

Table 4-1019 `por_rnsam_sys_cache_grp_sn_nodeid_reg13` (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	<code>sn_nodeid_55</code>	Hashed target SN node ID 55	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	<code>sn_nodeid_54</code>	Hashed target SN node ID 54	RW	11'b000000000000

The following image shows the lower register bit assignments.

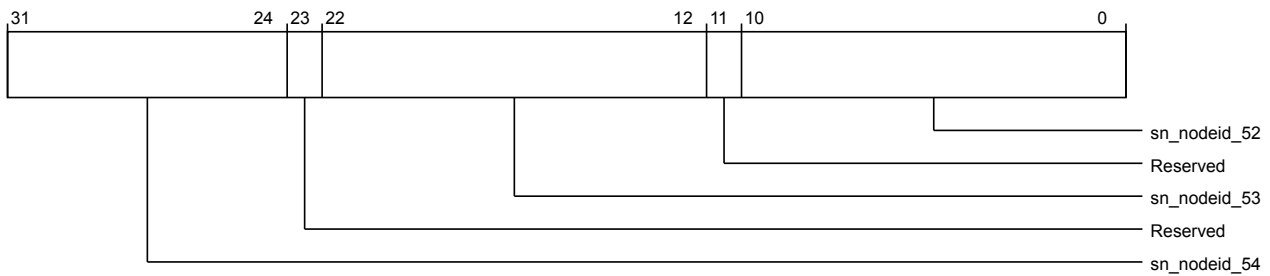


Figure 4-1003 por_rnsam_sys_cache_grp_sn_nodeid_reg13 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg13 lower register bit assignments.

Table 4-1020 por_rnsam_sys_cache_grp_sn_nodeid_reg13 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_54	Hashed target SN node ID 54	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_53	Hashed target SN node ID 53	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_52	Hashed target SN node ID 52	RW	11'b000000000000

sys_cache_grp_sn_nodeid_reg14

Configures hashed node IDs for system cache groups. Controls target SN node IDs 56 to 59.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1038

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

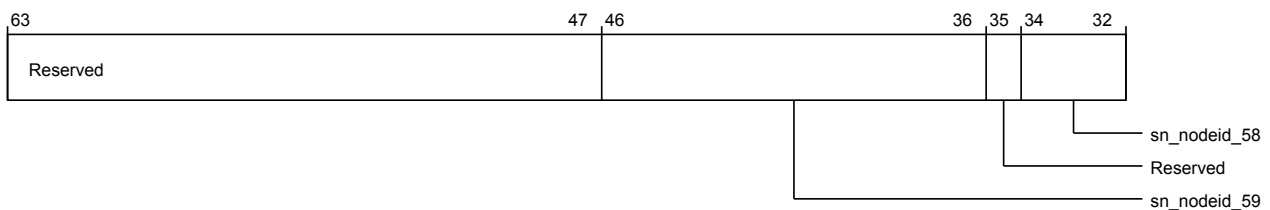


Figure 4-1004 por_rnsam_sys_cache_grp_sn_nodeid_reg14 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg14 higher register bit assignments.

Table 4-1021 por_rnsam_sys_cache_grp_sn_nodeid_reg14 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_59	Hashed target SN node ID 59	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_58	Hashed target SN node ID 58	RW	11'b000000000000

The following image shows the lower register bit assignments.

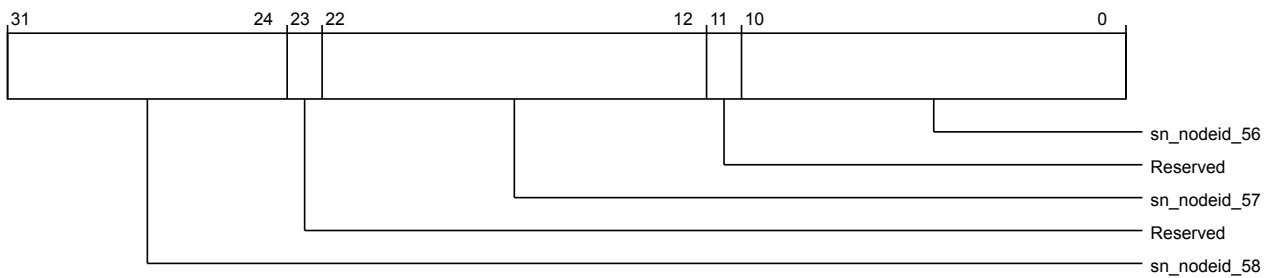


Figure 4-1005 por_rnsam_sys_cache_grp_sn_nodeid_reg14 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg14 lower register bit assignments.

Table 4-1022 por_rnsam_sys_cache_grp_sn_nodeid_reg14 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_58	Hashed target SN node ID 58	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_57	Hashed target SN node ID 57	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_56	Hashed target SN node ID 56	RW	11'b000000000000

sys_cache_grp_sn_nodeid_reg15

Configures hashed node IDs for system cache groups. Controls target SN node IDs 60 to 63.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1040

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

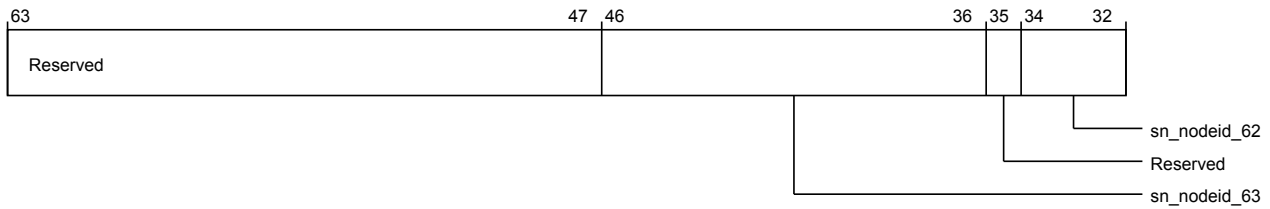


Figure 4-1006 por_rnsam_sys_cache_grp_sn_nodeid_reg15 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg15 higher register bit assignments.

Table 4-1023 por_rnsam_sys_cache_grp_sn_nodeid_reg15 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_63	Hashed target SN node ID 63	RW	11'b000000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_62	Hashed target SN node ID 62	RW	11'b000000000000

The following image shows the lower register bit assignments.

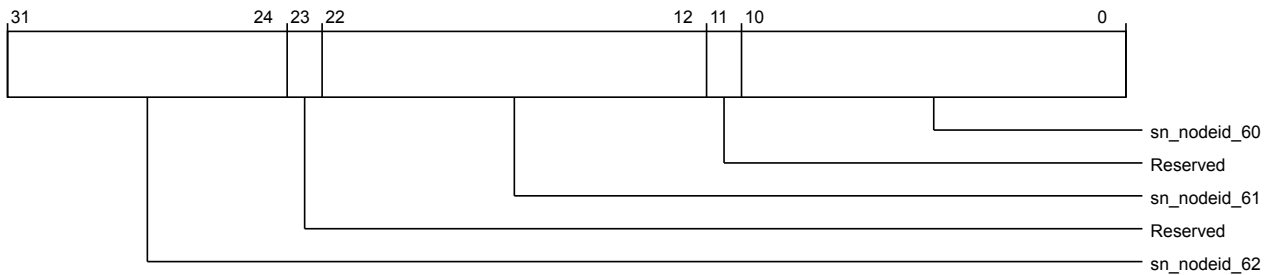


Figure 4-1007 por_rnsam_sys_cache_grp_sn_nodeid_reg15 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg15 lower register bit assignments.

Table 4-1024 por_rnsam_sys_cache_grp_sn_nodeid_reg15 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_62	Hashed target SN node ID 62	RW	11'b000000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_61	Hashed target SN node ID 61	RW	11'b000000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_60	Hashed target SN node ID 60	RW	11'b000000000000

4.3.10 SBSX register descriptions

This section lists the SBSX registers.

por_sbsx_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

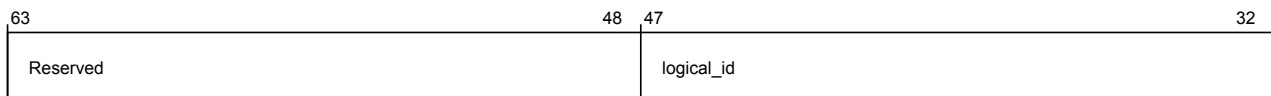


Figure 4-1008 por_sbsx_por_sbsx_node_info (high)

The following table shows the por_sbsx_node_info higher register bit assignments.

Table 4-1025 por_sbsx_por_sbsx_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

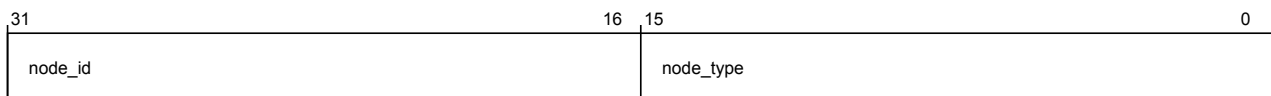


Figure 4-1009 por_sbsx_por_sbsx_node_info (low)

The following table shows the por_sbsx_node_info lower register bit assignments.

Table 4-1026 por_sbsx_por_sbsx_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0007

por_sbsx_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-1010 por_sbsx_por_sbsx_child_info (high)

The following table shows the por_sbsx_child_info higher register bit assignments.

Table 4-1027 por_sbsx_por_sbsx_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

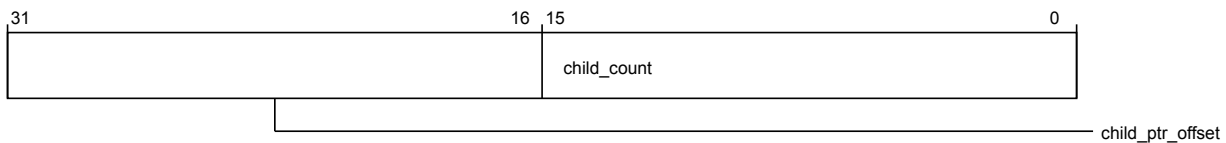


Figure 4-1011 por_sbsx_por_sbsx_child_info (low)

The following table shows the por_sbsx_child_info lower register bit assignments.

Table 4-1028 por_sbsx_por_sbsx_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_sbsx_unit_info

Provides component identification information for SBSX.

Its characteristics are:

Type	RO
Register width (Bits)	64

Address offset 14'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-1012 por_sbsx_por_sbsx_unit_info (high)

The following table shows the por_sbsx_unit_info higher register bit assignments.

Table 4-1029 por_sbsx_por_sbsx_unit_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

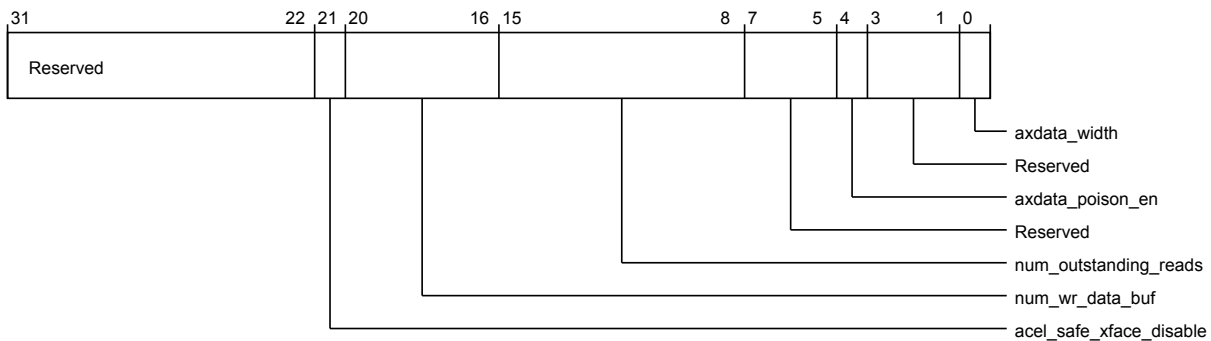


Figure 4-1013 por_sbsx_por_sbsx_unit_info (low)

The following table shows the por_sbsx_unit_info lower register bit assignments.

Table 4-1030 por_sbsx_por_sbsx_unit_info (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21	ace1_safe_xface_disable	ACE-Lite/AXI4 safe interface disable	RO	Configuration dependent
20:16	num_wr_data_buf	Number of write data buffers in SBSX	RO	Configuration dependent
15:8	num_outstanding_reads	Maximum number of outstanding AXI read requests from SBSX	RO	Configuration dependent
7:5	Reserved	Reserved	RO	-

Table 4-1030 por_sbsx_por_sbsx_unit_info (low) (continued)

Bits	Field name	Description	Type	Reset
4	axdata_poison_en	Data poison support on ACE-Lite/AXI4 interface 1'b0: Not supported 1'b1: Supported	RO	Configuration dependent
3:1	Reserved	Reserved	RO	-
0	axdata_width	Data width on ACE-Lite/AXI4 interface 1'b0: 128 bits 1'b1: 256 bits	RO	Configuration dependent

por_sbsx_aux_ctl

Functions as the auxiliary control register for the SBSX bridge.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

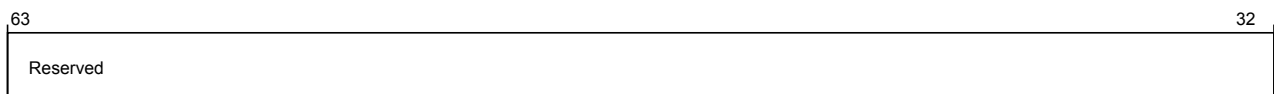


Figure 4-1014 por_sbsx_por_sbsx_aux_ctl (high)

The following table shows the por_sbsx_aux_ctl higher register bit assignments.

Table 4-1031 por_sbsx_por_sbsx_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

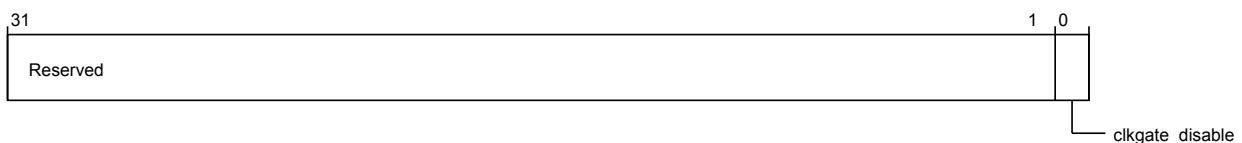


Figure 4-1015 por_sbsx_por_sbsx_aux_ctl (low)

The following table shows the por_sbsx_aux_ctl lower register bit assignments.

Table 4-1032 por_sbsx_por_sbsx_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	clkgate_disable	Disables internal clock gating in SBSX bridge	RW	1'b0

por_sbsx_errfr

Functions as the error feature register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3000

Register reset 64'b0000010100001

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

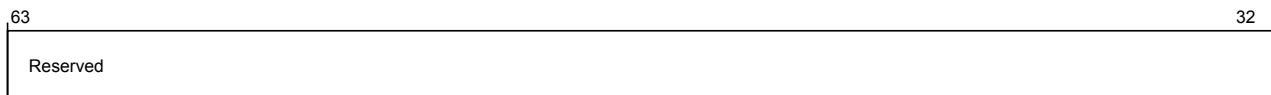


Figure 4-1016 por_sbsx_por_sbsx_errfr (high)

The following table shows the por_sbsx_errfr higher register bit assignments.

Table 4-1033 por_sbsx_por_sbsx_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

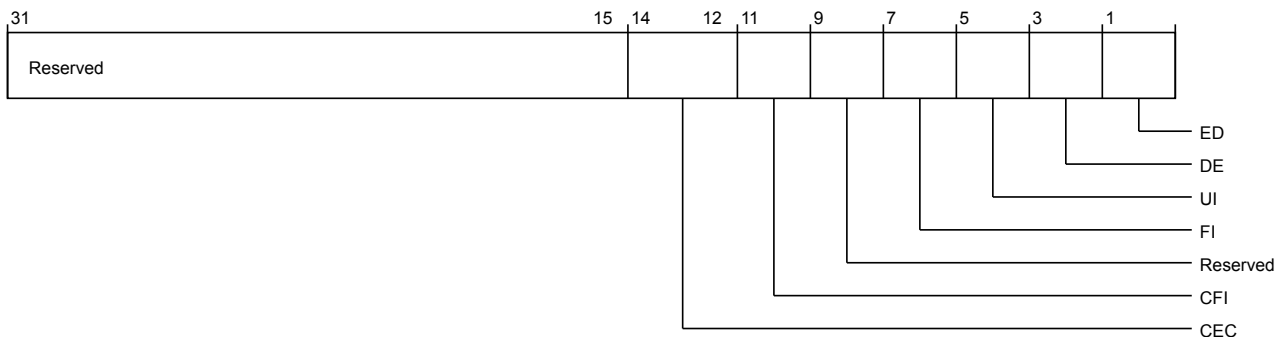


Figure 4-1017 por_sbsx_por_sbsx_errfr (low)

The following table shows the por_sbsx_errfr lower register bit assignments.

Table 4-1034 por_sbsx_por_sbsx_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b00
1:0	ED	Error detection	RO	2'b01

por_sbsx_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3008
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

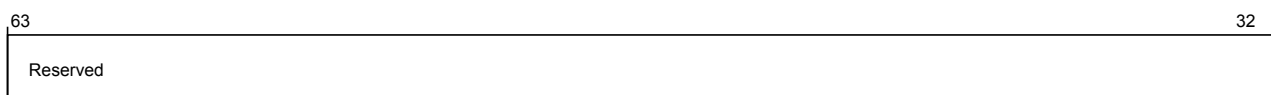


Figure 4-1018 por_sbsx_por_sbsx_errctlr (high)

The following table shows the por_sbsx_errctlr higher register bit assignments.

Table 4-1035 por_sbsx_por_sbsx_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

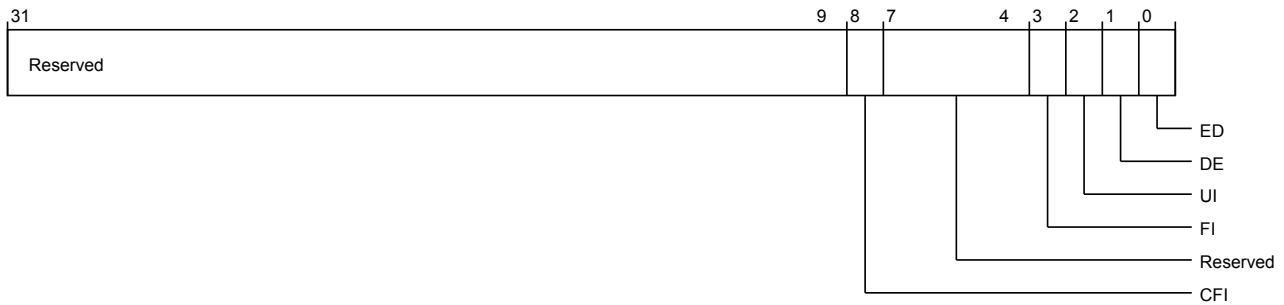


Figure 4-1019 `por_sbsx_errctlr` (low)

The following table shows the `por_sbsx_errctlr` lower register bit assignments.

Table 4-1036 `por_sbsx_errctlr` (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in <code>por_sbsx_errfr.CFI</code>	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in <code>por_sbsx_errfr.FI</code>	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in <code>por_sbsx_errfr.UI</code>	RW	1'b0
1	DE	Enables error deferment as specified in <code>por_sbsx_errfr.DE</code>	RW	1'b0
0	ED	Enables error detection as specified in <code>por_sbsx_errfr.ED</code>	RW	1'b0

`por_sbsx_errstatus`

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3010
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

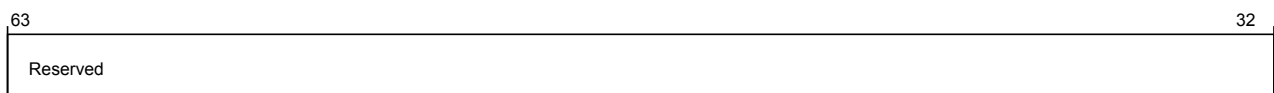


Figure 4-1020 `por_sbsx_errstatus` (high)

The following table shows the `por_sbsx_errstatus` higher register bit assignments.

Table 4-1037 por_sbsx_por_sbsx_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

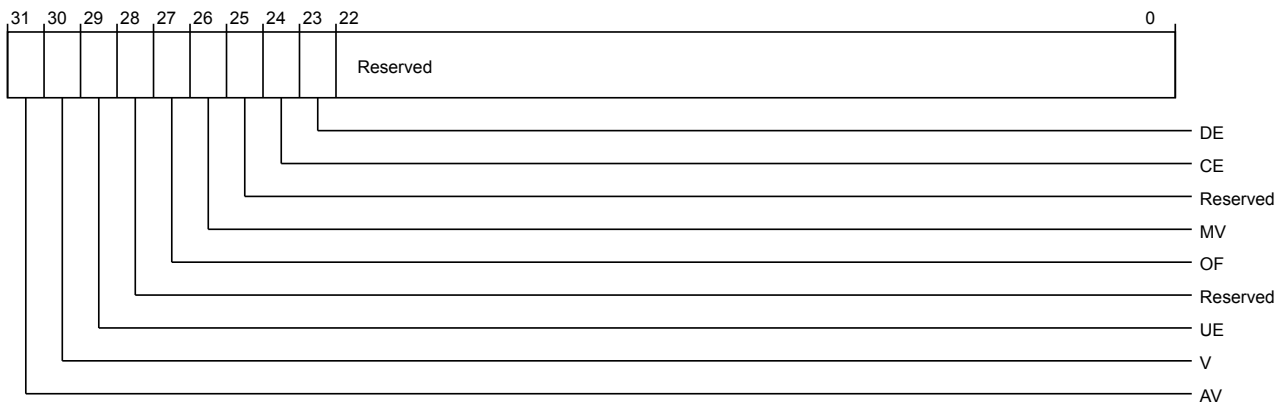


Figure 4-1021 por_sbsx_por_sbsx_errstatus (low)

The following table shows the `por_sbsx_errstatus` lower register bit assignments.

Table 4-1038 por_sbsx_por_sbsx_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; <code>por_sbsx_erraddr</code> contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0

Table 4-1038 `por_sbsx_por_sbsx_errstatus` (low) (continued)

Bits	Field name	Description	Type	Reset
26	MV	<p><code>por_sbsx_errmisc</code> valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear</p> <p>1'b1: Miscellaneous registers are valid</p> <p>1'b0: Miscellaneous registers are not valid</p>	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	<p>Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear</p> <p>1'b1: At least one transient corrected error recorded</p> <p>1'b0: No corrected errors recorded</p>	W1C	1'b0
23	DE	<p>Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear</p> <p>1'b1: At least one error is not corrected and is deferred</p> <p>1'b0: No errors deferred</p>	W1C	1'b0
22:0	Reserved	Reserved	RO	-

`por_sbsx_erraddr`

Contains the error record address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3018

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

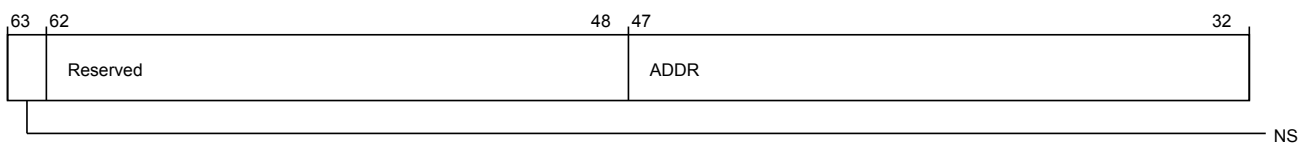


Figure 4-1022 `por_sbsx_por_sbsx_erraddr` (high)

The following table shows the `por_sbsx_erraddr` higher register bit assignments.

Table 4-1039 por_sbsx_por_sbsx_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_sbsx_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

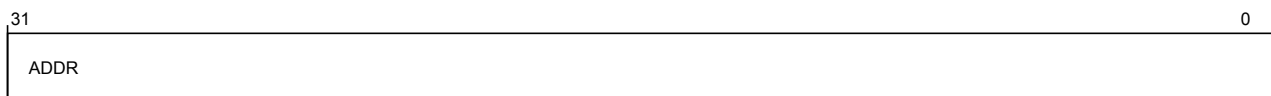


Figure 4-1023 por_sbsx_por_sbsx_erraddr (low)

The following table shows the por_sbsx_erraddr lower register bit assignments.

Table 4-1040 por_sbsx_por_sbsx_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_sbsx_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3020

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

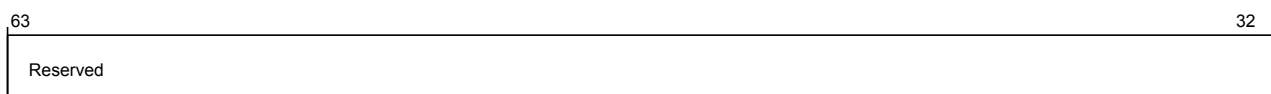


Figure 4-1024 por_sbsx_por_sbsx_errmisc (high)

The following table shows the por_sbsx_errmisc higher register bit assignments.

Table 4-1041 por_sbsx_por_sbsx_errmisc (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

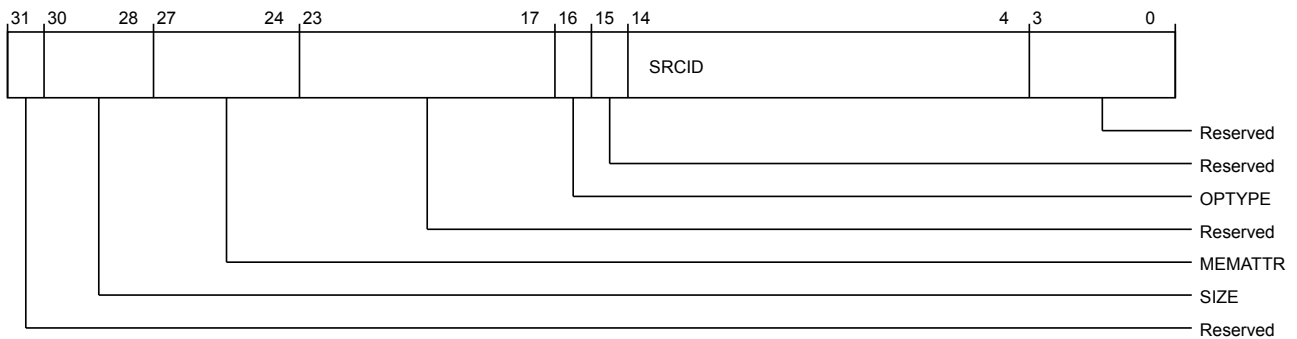


Figure 4-1025 por_sbsx_por_sbsx_errmisc (low)

The following table shows the por_sbsx_errmisc lower register bit assignments.

Table 4-1042 por_sbsx_por_sbsx_errmisc (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23:17	Reserved	Reserved	RO	-
16	OPTYPE	Error opcode type 1'b1: WR_NO_SNP_PTL (partial) 1'b0: WR_NO_SNP_FULL	RW	1'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	Reserved	Reserved	RO	-

por_sbsx_errfr_NS

Functions as the non-secure error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3100
Register reset	64'b00000010100001

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-1026 por_sbsx_por_sbsx_errfr_ns (high)

The following table shows the por_sbsx_errfr_NS higher register bit assignments.

Table 4-1043 por_sbsx_por_sbsx_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

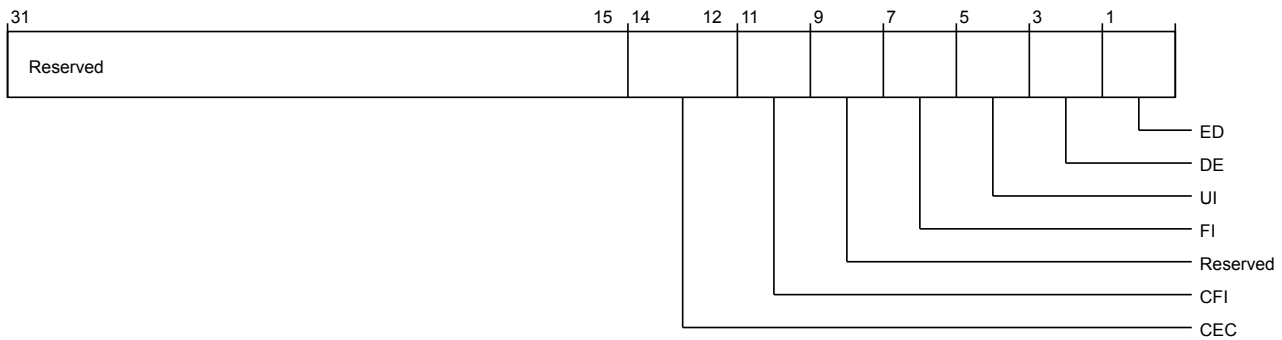


Figure 4-1027 por_sbsx_por_sbsx_errfr_ns (low)

The following table shows the por_sbsx_errfr_NS lower register bit assignments.

Table 4-1044 por_sbsx_por_sbsx_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10

Table 4-1044 `por_sbsx_por_sbsx_errfr_ns` (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	DE	Deferred errors	RO	2'b00
1:0	ED	Error detection	RO	2'b01

`por_sbsx_errctlr_NS`

Functions as the non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3108
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-1028 `por_sbsx_por_sbsx_errctlr_ns` (high)

The following table shows the `por_sbsx_errctlr_NS` higher register bit assignments.

Table 4-1045 `por_sbsx_por_sbsx_errctlr_ns` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

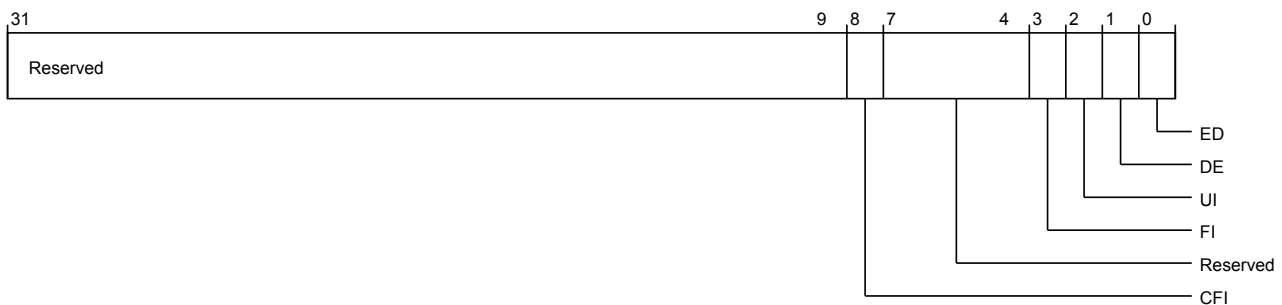


Figure 4-1029 `por_sbsx_por_sbsx_errctlr_ns` (low)

The following table shows the `por_sbsx_errctlr_NS` lower register bit assignments.

Table 4-1046 `por_sbsx_por_sbsx_errctlr_ns` (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in <code>por_sbsx_errfr_NS.CFI</code>	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in <code>por_sbsx_errfr_NS.FI</code>	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in <code>por_sbsx_errfr_NS.UI</code>	RW	1'b0
1	DE	Enables error deferment as specified in <code>por_sbsx_errfr_NS.DE</code>	RW	1'b0
0	ED	Enables error detection as specified in <code>por_sbsx_errfr_NS.ED</code>	RW	1'b0

`por_sbsx_errstatus_NS`

Functions as the non-secure error status register.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 14'h3110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

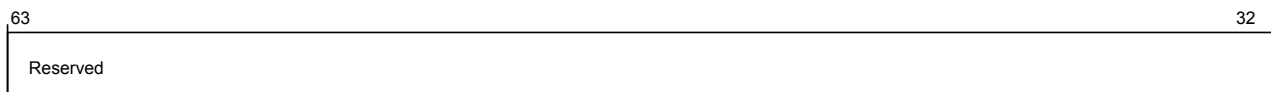


Figure 4-1030 `por_sbsx_por_sbsx_errstatus_ns` (high)

The following table shows the `por_sbsx_errstatus_NS` higher register bit assignments.

Table 4-1047 `por_sbsx_por_sbsx_errstatus_ns` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

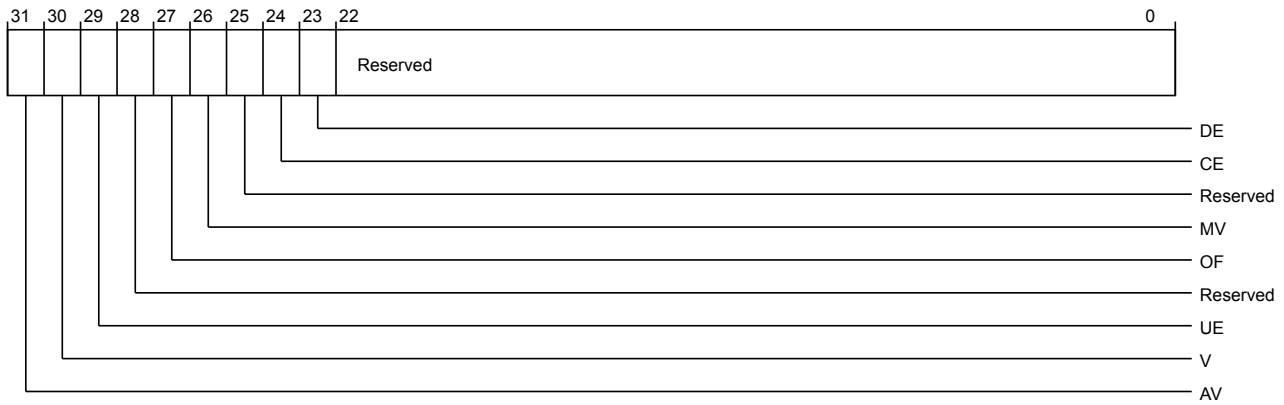


Figure 4-1031 `por_sbsx_por_sbsx_errstatus_ns` (low)

The following table shows the `por_sbsx_errstatus_NS` lower register bit assignments.

Table 4-1048 `por_sbsx_por_sbsx_errstatus_ns` (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; <code>por_sbsx_erraddr_NS</code> contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	<code>por_sbsx_errmisc_NS</code> valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 4-1048 `por_sbsx_por_sbsx_errstatus_ns` (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

`por_sbsx_erraddr_NS`

Contains the non-secure error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

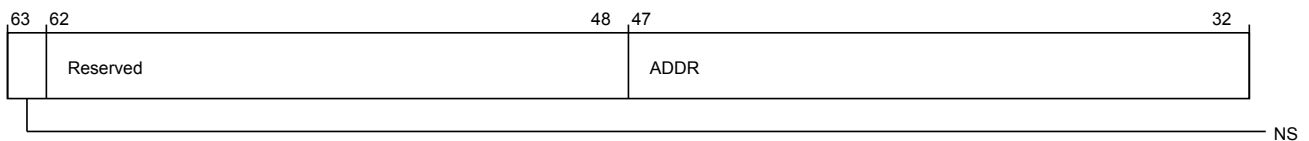


Figure 4-1032 `por_sbsx_por_sbsx_erraddr_ns` (high)

The following table shows the `por_sbsx_erraddr_NS` higher register bit assignments.

Table 4-1049 `por_sbsx_por_sbsx_erraddr_ns` (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: <code>por_sbsx_erraddr_NS.NS</code> is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

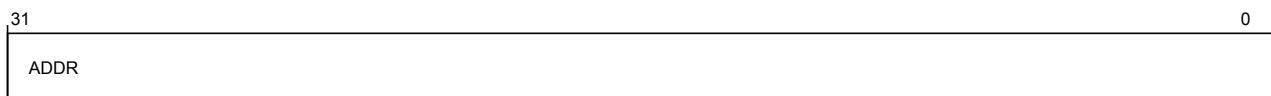


Figure 4-1033 `por_sbsx_por_sbsx_erraddr_ns` (low)

The following table shows the `por_sbsx_erraddr_NS` lower register bit assignments.

Table 4-1050 `por_sbsx_por_sbsx_erraddr_ns` (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

`por_sbsx_errmisc_NS`

Functions as the non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3120
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

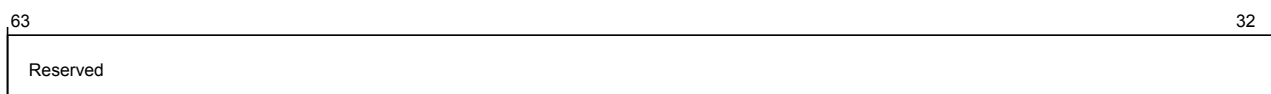


Figure 4-1034 `por_sbsx_por_sbsx_errmisc_ns` (high)

The following table shows the `por_sbsx_errmisc_NS` higher register bit assignments.

Table 4-1051 `por_sbsx_por_sbsx_errmisc_ns` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

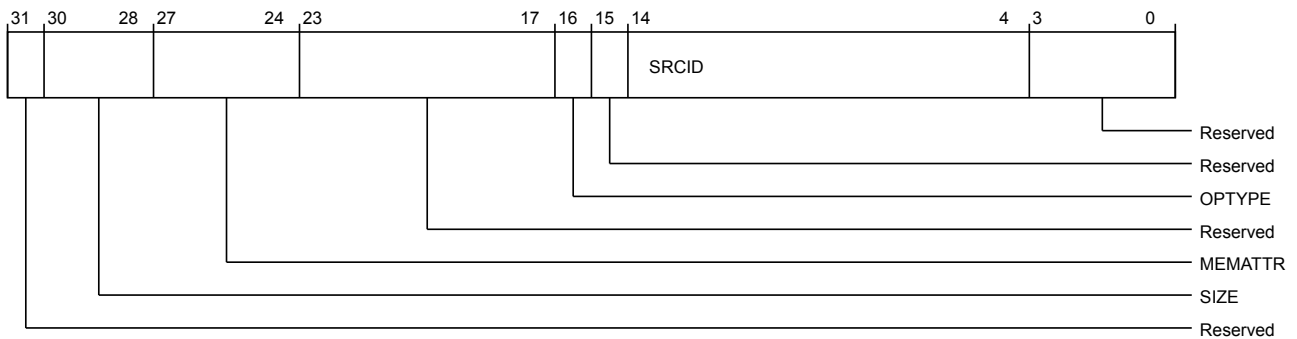


Figure 4-1035 `por_sbsx_por_sbsx_errmisc_ns` (low)

The following table shows the `por_sbsx_errmisc_NS` lower register bit assignments.

Table 4-1052 `por_sbsx_por_sbsx_errmisc_ns` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23:17	Reserved	Reserved	RO	-
16	OPTYPE	Error opcode type 1'b1: WR_NO_SNP_PTL (partial) 1'b0: WR_NO_SNP_FULL	RW	1'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	Reserved	Reserved	RO	-

`por_sbsx_pmu_event_sel`

Specifies the PMU event to be counted.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2000
Register reset	64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-1036 por_sbsx_por_sbsx_pmu_event_sel (high)

The following table shows the por_sbsx_pmu_event_sel higher register bit assignments.

Table 4-1053 por_sbsx_por_sbsx_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

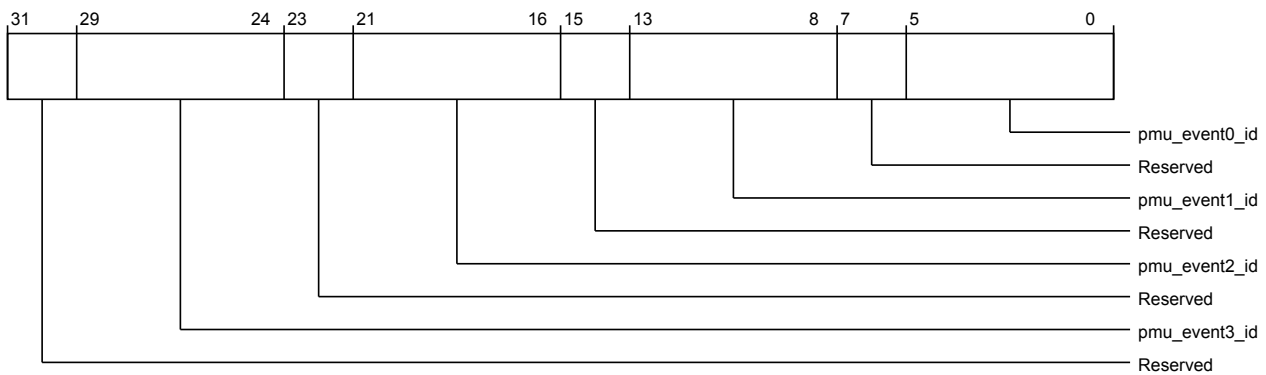


Figure 4-1037 por_sbsx_por_sbsx_pmu_event_sel (low)

The following table shows the por_sbsx_pmu_event_sel lower register bit assignments.

Table 4-1054 por_sbsx_por_sbsx_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	SBSX PMU Event 3 select; see pmu_event0_id for encodings	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	SBSX PMU Event 2 select; see pmu_event0_id for encodings	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	SBSX PMU Event 1 select; see pmu_event0_id for encodings	RW	6'b0

Table 4-1054 `por_sbsx_por_sbsx_pmu_event_sel` (low) (continued)

Bits	Field name	Description	Type	Reset
7:6	Reserved	Reserved	RO	-
5:0	<code>pmu_event0_id</code>	<p>SBSX PMU Event 0 select</p> <p>6'h00: No event</p> <p>6'h01: Read request</p> <p>6'h02: Write request</p> <p>6'h03: CMO request</p> <p>6'h04: RETRYACK TXRSP flit sent</p> <p>6'h05: TXDAT flit seen</p> <p>6'h06: TXRSP flit seen</p> <p>6'h11: Read request tracker occupancy count overflow</p> <p>6'h12: Write request tracker occupancy count overflow</p> <p>6'h13: CMO request tracker occupancy count overflow</p> <p>6'h14: WDB occupancy count overflow</p> <p>6'h15: Read AXI pending tracker occupancy count overflow</p> <p>6'h16: CMO AXI pending tracker occupancy count overflow</p> <p>6'h21: ARVALID set without ARREADY</p> <p>6'h22: AWVALID set without AWREADY</p> <p>6'h23: WVALID set without WREADY</p> <p>6'h24: TXDAT stall (TXDAT valid but no link credit available)</p> <p>6'h25: TXRSP stall (TXRSP valid but no link credit available)</p> <p>NOTE: All other encodings are reserved.</p>	RW	6'b0

4.3.11 CXHA configuration registers

This section lists the CXHA configuration registers.

por_cxg_ha_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

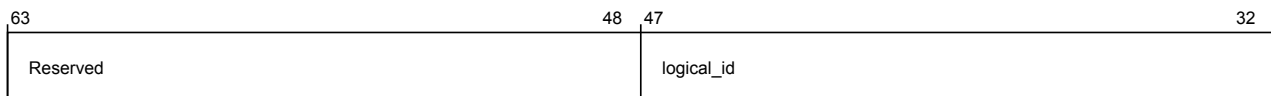


Figure 4-1038 por_cxg_ha_node_info (high)

The following table shows the por_cxg_ha_node_info higher register bit assignments.

Table 4-1055 por_cxg_ha_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

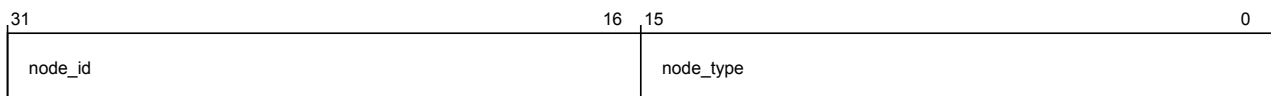


Figure 4-1039 por_cxg_ha_node_info (low)

The following table shows the por_cxg_ha_node_info lower register bit assignments.

Table 4-1056 por_cxg_ha_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0101

por_cxg_ha_id

Contains the CCIX-assigned HAID.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

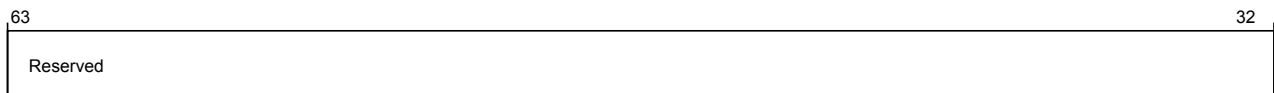


Figure 4-1040 por_cxg_ha_id (high)

The following table shows the por_cxg_ha_id higher register bit assignments.

Table 4-1057 por_cxg_ha_id (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

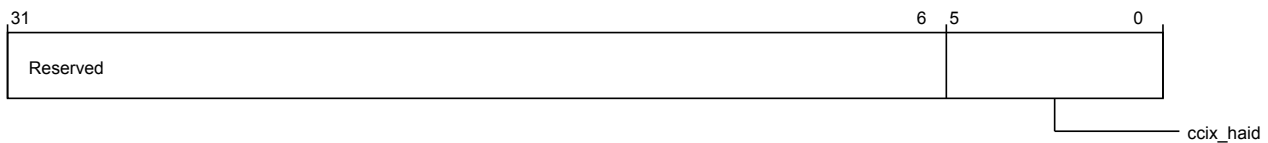


Figure 4-1041 por_cxg_ha_id (low)

The following table shows the por_cxg_ha_id lower register bit assignments.

Table 4-1058 por_cxg_ha_id (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5:0	ccix_haid	CCIX HAID	RW	6'h0

por_cxg_ha_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64

Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-1042 `por_cxg_ha_por_cxg_ha_child_info` (high)

The following table shows the `por_cxg_ha_child_info` higher register bit assignments.

Table 4-1059 `por_cxg_ha_por_cxg_ha_child_info` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

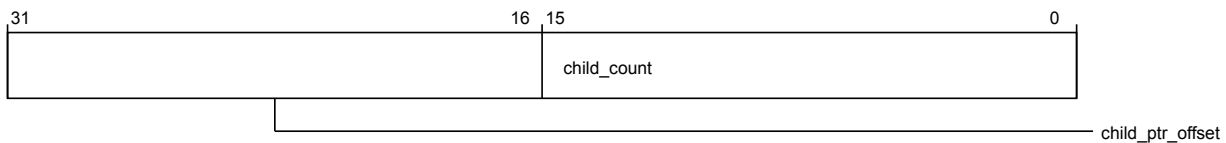


Figure 4-1043 `por_cxg_ha_por_cxg_ha_child_info` (low)

The following table shows the `por_cxg_ha_child_info` lower register bit assignments.

Table 4-1060 `por_cxg_ha_por_cxg_ha_child_info` (low)

Bits	Field name	Description	Type	Reset
31:16	<code>child_ptr_offset</code>	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	<code>child_count</code>	Number of child nodes; used in discovery process	RO	16'h0

`por_cxg_ha_aux_ctl`

Functions as the auxiliary control register for CXHA.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hA08
Register reset 64'b001000
Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

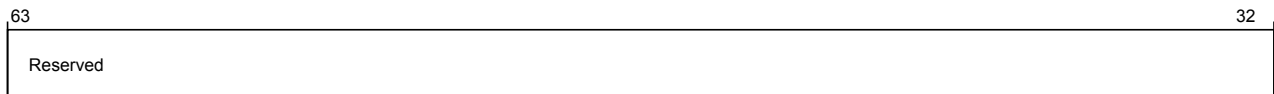


Figure 4-1044 por_cxg_ha_por_cxg_ha_aux_ctl (high)

The following table shows the por_cxg_ha_aux_ctl higher register bit assignments.

Table 4-1061 por_cxg_ha_por_cxg_ha_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

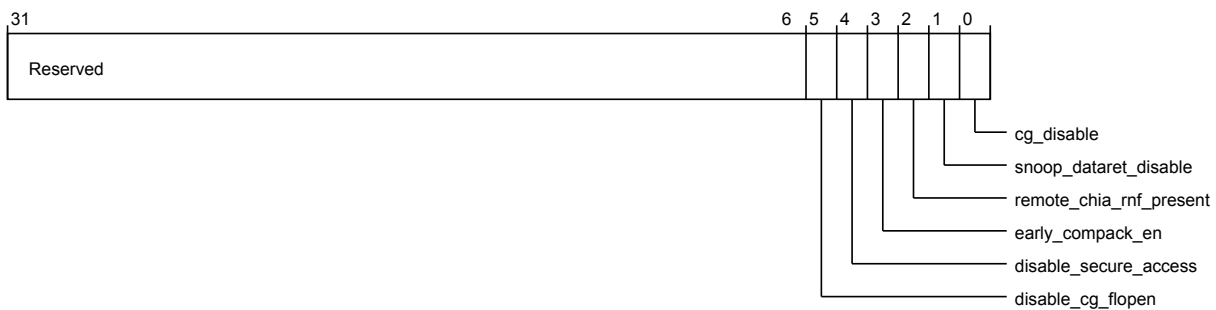


Figure 4-1045 por_cxg_ha_por_cxg_ha_aux_ctl (low)

The following table shows the por_cxg_ha_aux_ctl lower register bit assignments.

Table 4-1062 por_cxg_ha_por_cxg_ha_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5	disable_cg_flopen	Disables enhanced flop enable control for dynamic power savings	RW	1'b0
4	disable_secure_access	Converts all accesses to non-secure	RW	1'b0
3	early_compack_en	Early CompAck enable; enables sending early CompAck on CCIX for requests that require CompAck	RW	1'b1
2	remote_chia_rnf_present	Indicates existence of CHIA RN-F in system; HA uses this indication to send SnpToS or SnpToSC 1'b0: HA converts SnpShared, SnpClean, and SnpNotSharedDirty to SnpToSC 1'b1: HA converts SnpShared, SnpClean, and SnpNotSharedDirty to SnpToS	RW	1'b0
1	snoop_dataret_disable	Disables setting data return for CCIX snoop requests for all CHI snoop opcodes	RW	1'b0
0	cg_disable	Disables clock gating when set	RW	1'b0

por_cxg_ha_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h980
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

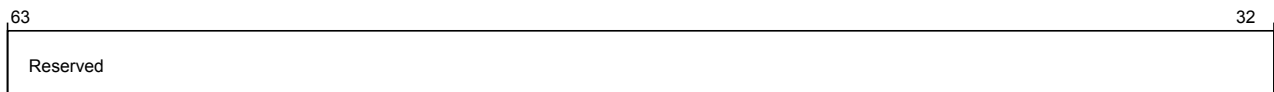


Figure 4-1046 por_cxg_ha_secure_register_groups_override (high)

The following table shows the por_cxg_ha_secure_register_groups_override higher register bit assignments.

Table 4-1063 por_cxg_ha_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

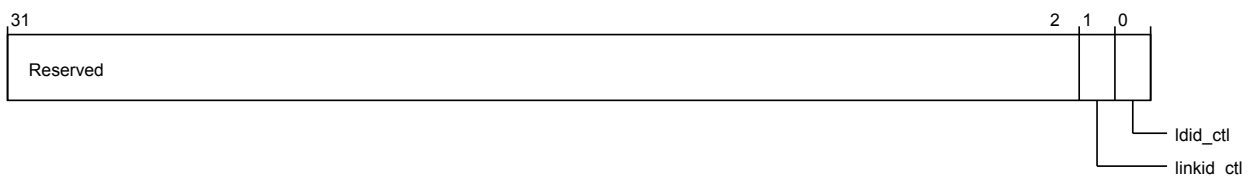


Figure 4-1047 por_cxg_ha_secure_register_groups_override (low)

The following table shows the por_cxg_ha_secure_register_groups_override lower register bit assignments.

Table 4-1064 por_cxg_ha_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	linkid_ctl	Allows non-secure access to secure HA Link ID registers	RW	1'b0
0	ldid_ctl	Allows non-secure access to secure HA LDID registers	RW	1'b0

por_cxg_ha_unit_info

Provides component identification information for CXHA.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h900
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

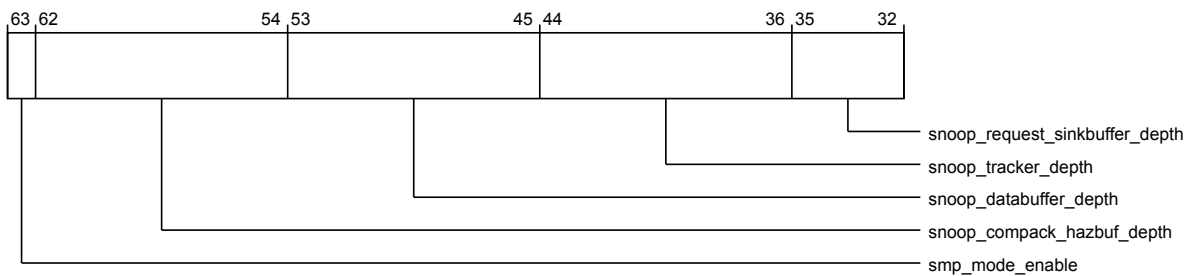


Figure 4-1048 por_cxg_ha_por_cxg_ha_unit_info (high)

The following table shows the por_cxg_ha_unit_info higher register bit assignments.

Table 4-1065 por_cxg_ha_por_cxg_ha_unit_info (high)

Bits	Field name	Description	Type	Reset
63	smp_mode_enable	SMP Mode Enable	RO	Configuration dependent
62:54	snoop_compack_hazbuf_depth	Depth of CompAck snoop hazard buffer	RO	Configuration dependent
53:45	snoop_databuffer_depth	Depth of snoop data buffer	RO	Configuration dependent
44:36	snoop_tracker_depth	Depth of snoop tracker; number of outstanding SNP requests on CCIX	RO	Configuration dependent
35:32	snoop_request_sinkbuffer_depth	Depth of snoop request sink buffer; number of CHI SNP requests that can be sunk by CXHA	RO	Configuration dependent

The following image shows the lower register bit assignments.

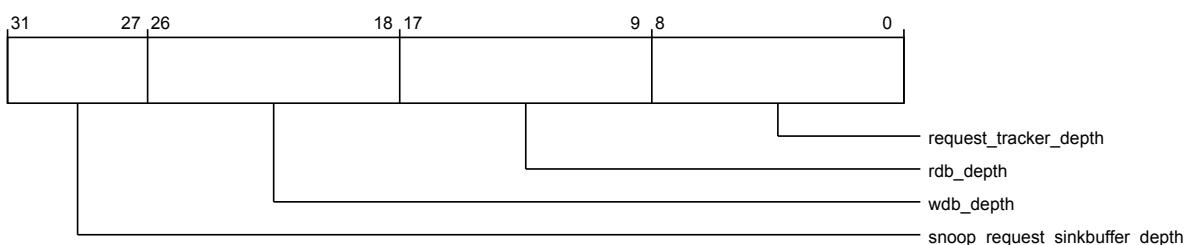


Figure 4-1049 por_cxg_ha_por_cxg_ha_unit_info (low)

The following table shows the por_cxg_ha_unit_info lower register bit assignments.

Table 4-1066 por_cxg_ha_por_cxg_ha_unit_info (low)

Bits	Field name	Description	Type	Reset
31:27	snoop_request_sinkbuffer_depth	Depth of snoop request sink buffer; number of CHI SNP requests that can be sunk by CXHA	RO	Configuration dependent
26:18	wdb_depth	Depth of write data buffer	RO	Configuration dependent
17:9	rdb_depth	Depth of read data buffer	RO	Configuration dependent
8:0	request_tracker_depth	Depth of request tracker	RO	Configuration dependent

por_cxg_ha_rnf_raid_to_ldid_reg0

Specifies the mapping of RAID to RN-F LDID for RAIDs 0 to 7.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

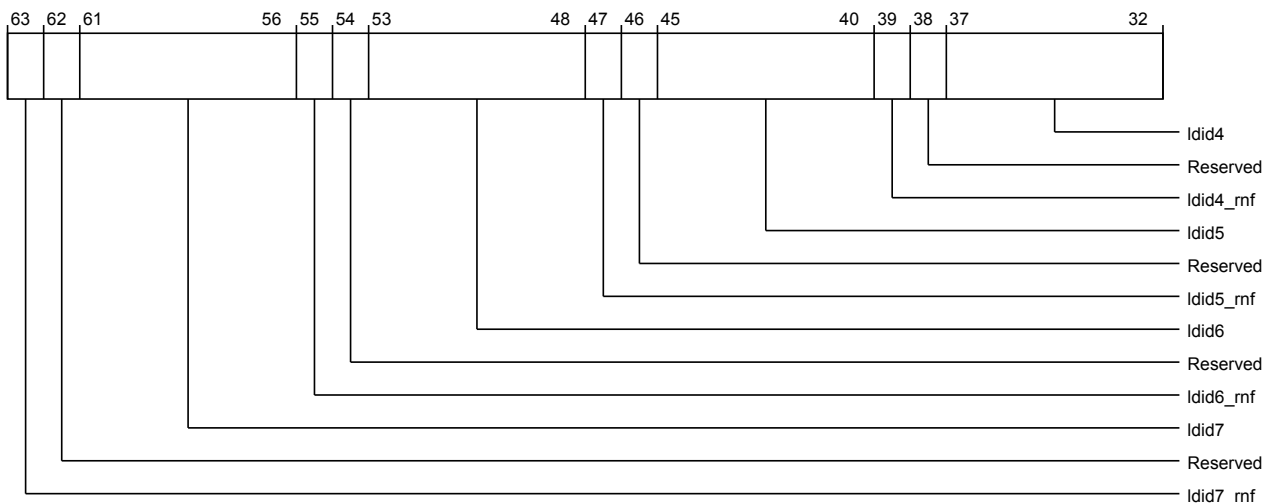


Figure 4-1050 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg0 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg0 higher register bit assignments.

Table 4-1067 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg0 (high)

Bits	Field name	Description	Type	Reset
63	ldid7_rnf	Specifies if RAID 7 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-

Table 4-1067 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg0` (high) (continued)

Bits	Field name	Description	Type	Reset
61:56	<code>ldid7</code>	Specifies the LDID for RAID 7	RW	6'h0
55	<code>ldid6_rnf</code>	Specifies if RAID 6 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	<code>ldid6</code>	Specifies the LDID for RAID 6	RW	6'h0
47	<code>ldid5_rnf</code>	Specifies if RAID 5 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	<code>ldid5</code>	Specifies the LDID for RAID 5	RW	6'h0
39	<code>ldid4_rnf</code>	Specifies if RAID 4 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	<code>ldid4</code>	Specifies the LDID for RAID 4	RW	6'h0

The following image shows the lower register bit assignments.

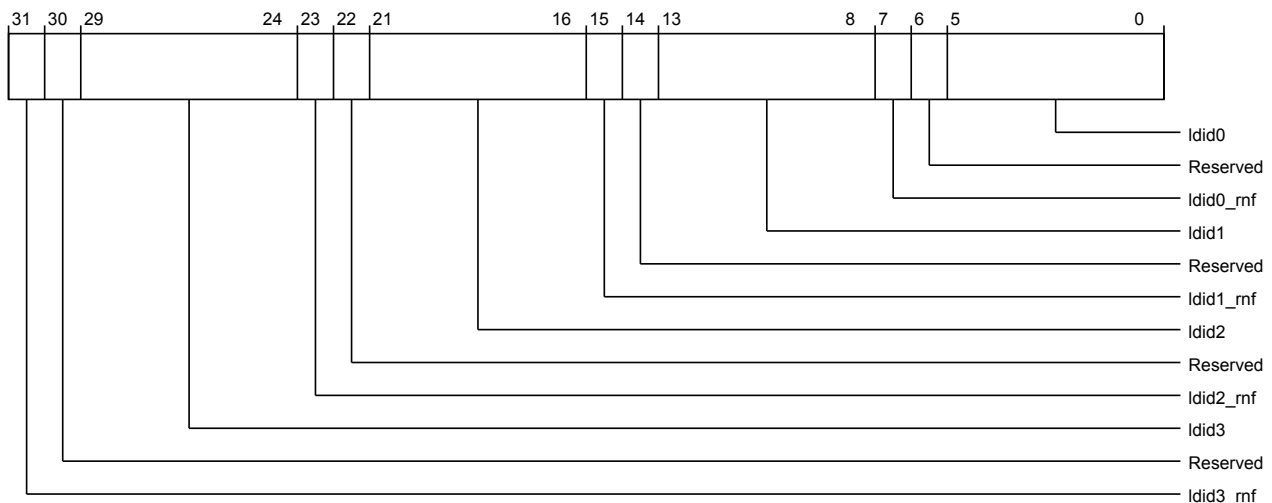


Figure 4-1051 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg0` (low)

The following table shows the `por_cxg_ha_rnf_raid_to_ldid_reg0` lower register bit assignments.

Table 4-1068 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg0` (low)

Bits	Field name	Description	Type	Reset
31	<code>ldid3_rnf</code>	Specifies if RAID 3 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	<code>ldid3</code>	Specifies the LDID for RAID 3	RW	6'h0
23	<code>ldid2_rnf</code>	Specifies if RAID 2 is RN-F	RW	1'b0

Table 4-1068 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg0` (low) (continued)

Bits	Field name	Description	Type	Reset
22	Reserved	Reserved	RO	-
21:16	<code>ldid2</code>	Specifies the LDID for RAID 2	RW	6'h0
15	<code>ldid1_rnf</code>	Specifies if RAID 1 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	<code>ldid1</code>	Specifies the LDID for RAID 1	RW	6'h0
7	<code>ldid0_rnf</code>	Specifies if RAID 0 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	<code>ldid0</code>	Specifies the LDID for RAID 0	RW	6'h0

`por_cxg_ha_rnf_raid_to_ldid_reg1`

Specifies the mapping of RAID to RN-F LDID for RAIDs 8 to 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC08
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ha_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

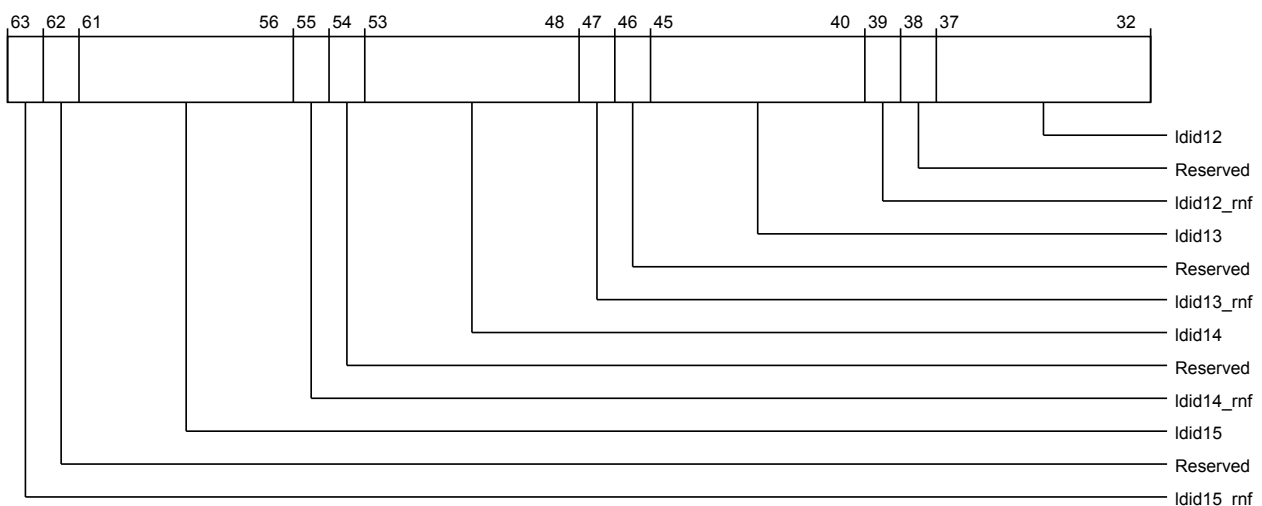


Figure 4-1052 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg1` (high)

The following table shows the `por_cxg_ha_rnf_raid_to_ldid_reg1` higher register bit assignments.

Table 4-1069 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg1 (high)

Bits	Field name	Description	Type	Reset
63	ldid15_rnf	Specifies if RAID 15 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid15	Specifies the LDID for RAID 15	RW	6'h0
55	ldid14_rnf	Specifies if RAID 14 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid14	Specifies the LDID for RAID 14	RW	6'h0
47	ldid13_rnf	Specifies if RAID 13 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid13	Specifies the LDID for RAID 13	RW	6'h0
39	ldid12_rnf	Specifies if RAID 12 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid12	Specifies the LDID for RAID 12	RW	6'h0

The following image shows the lower register bit assignments.

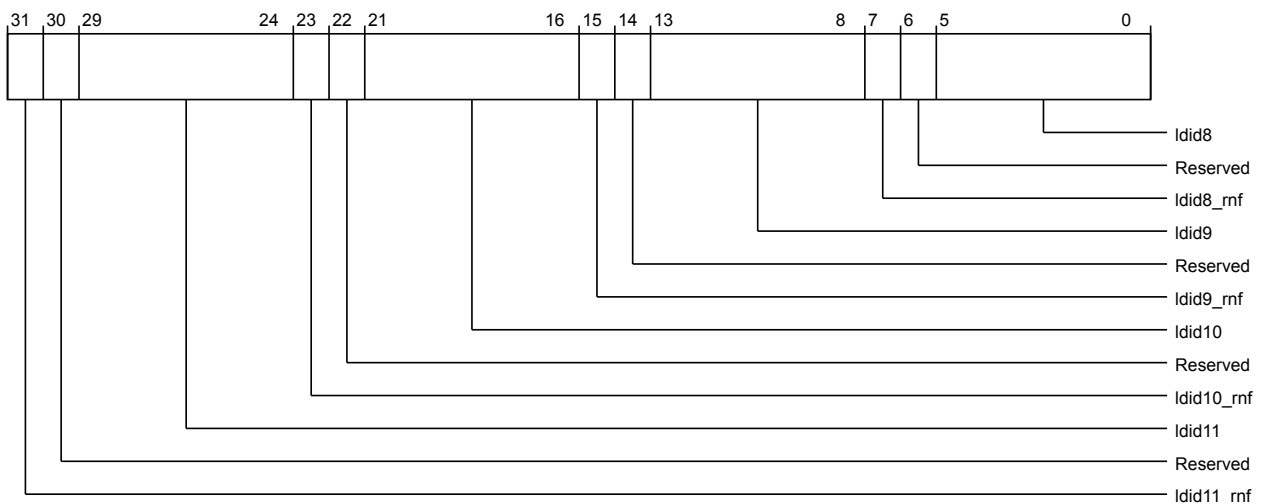


Figure 4-1053 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg1 (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg1 lower register bit assignments.

Table 4-1070 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg1 (low)

Bits	Field name	Description	Type	Reset
31	ldid11_rnf	Specifies if RAID 11 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-

Table 4-1070 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg1` (low) (continued)

Bits	Field name	Description	Type	Reset
29:24	<code>ldid11</code>	Specifies the LDID for RAID 11	RW	6'h0
23	<code>ldid10_rnf</code>	Specifies if RAID 10 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	<code>ldid10</code>	Specifies the LDID for RAID 10	RW	6'h0
15	<code>ldid9_rnf</code>	Specifies if RAID 9 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	<code>ldid9</code>	Specifies the LDID for RAID 9	RW	6'h0
7	<code>ldid8_rnf</code>	Specifies if RAID 8 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	<code>ldid8</code>	Specifies the LDID for RAID 8	RW	6'h0

`por_cxg_ha_rnf_raid_to_ldid_reg2`

Specifies the mapping of RAID to RN-F LDID for RAIDs 16 to 23.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC10
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ha_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

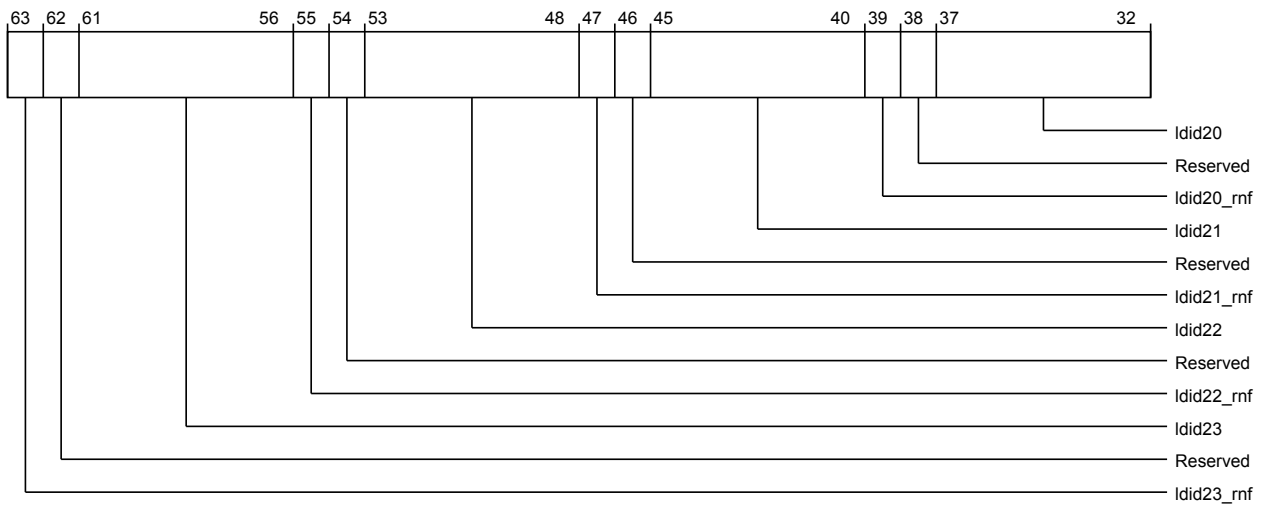


Figure 4-1054 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg2 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg2 higher register bit assignments.

Table 4-1071 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg2 (high)

Bits	Field name	Description	Type	Reset
63	ldid23_rnf	Specifies if RAID 23 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid23	Specifies the LDID for RAID 23	RW	6'h0
55	ldid22_rnf	Specifies if RAID 22 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid22	Specifies the LDID for RAID 22	RW	6'h0
47	ldid21_rnf	Specifies if RAID 21 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid21	Specifies the LDID for RAID 21	RW	6'h0
39	ldid20_rnf	Specifies if RAID 20 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid20	Specifies the LDID for RAID 20	RW	6'h0

The following image shows the lower register bit assignments.

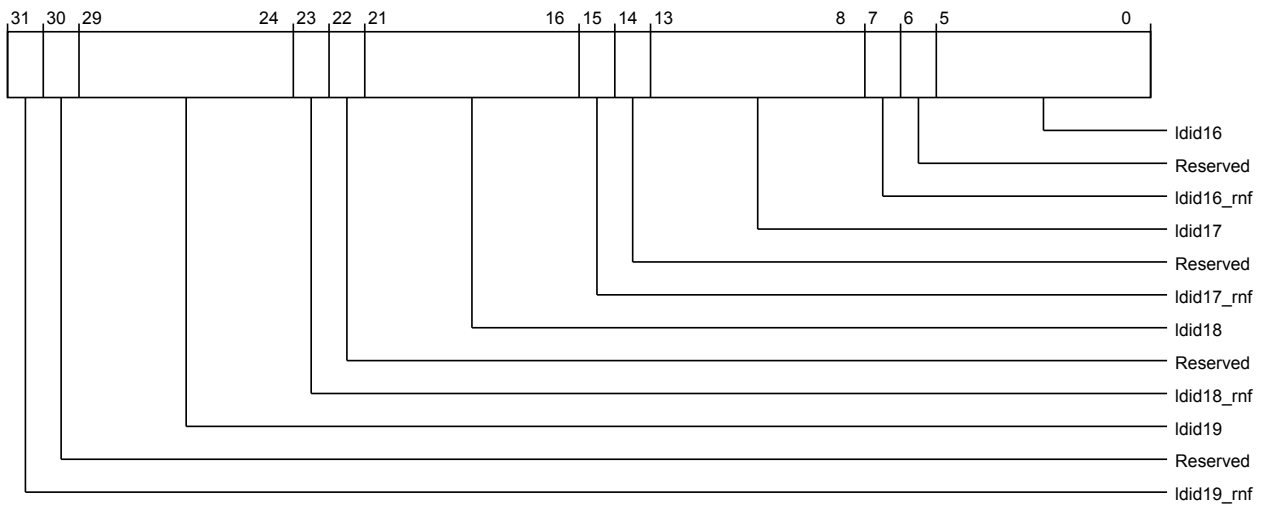


Figure 4-1055 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg2` (low)

The following table shows the `por_cxg_ha_rnf_raid_to_ldid_reg2` lower register bit assignments.

Table 4-1072 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg2` (low)

Bits	Field name	Description	Type	Reset
31	ldid19_rnf	Specifies if RAID 19 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid19	Specifies the LDID for RAID 19	RW	6'h0
23	ldid18_rnf	Specifies if RAID 18 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid18	Specifies the LDID for RAID 18	RW	6'h0
15	ldid17_rnf	Specifies if RAID 17 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid17	Specifies the LDID for RAID 17	RW	6'h0
7	ldid16_rnf	Specifies if RAID 16 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid16	Specifies the LDID for RAID 16	RW	6'h0

`por_cxg_ha_rnf_raid_to_ldid_reg3`

Specifies the mapping of RAID to RN-F LDID for RAIDs 24 to 31.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC18

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

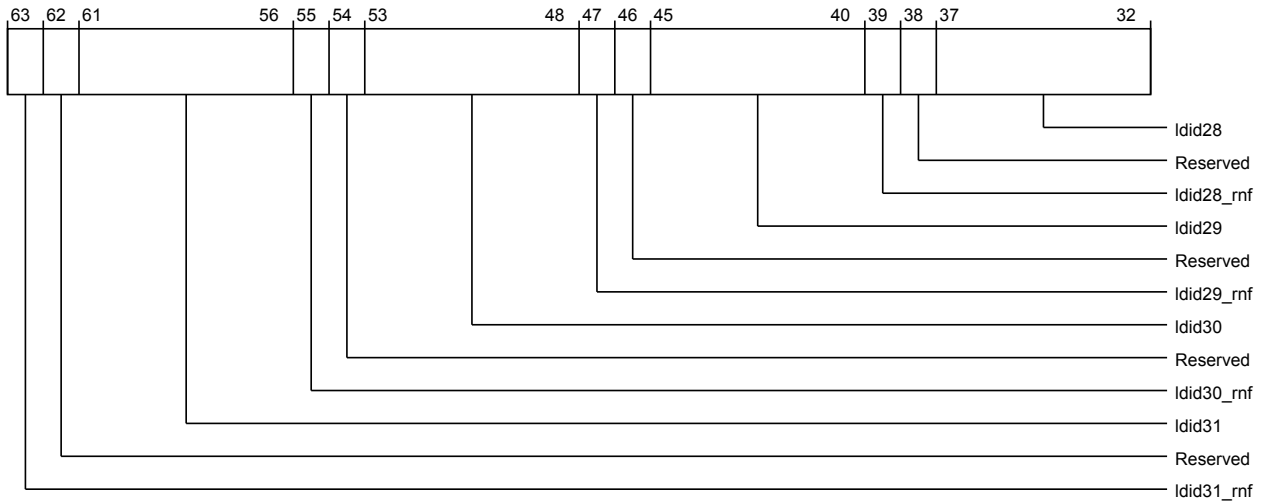


Figure 4-1056 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg3 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg3 higher register bit assignments.

Table 4-1073 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg3 (high)

Bits	Field name	Description	Type	Reset
63	ldid31_rnf	Specifies if RAID 31 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid31	Specifies the LDID for RAID 31	RW	6'h0
55	ldid30_rnf	Specifies if RAID 30 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid30	Specifies the LDID for RAID 30	RW	6'h0
47	ldid29_rnf	Specifies if RAID 29 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid29	Specifies the LDID for RAID 29	RW	6'h0
39	ldid28_rnf	Specifies if RAID 28 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid28	Specifies the LDID for RAID 28	RW	6'h0

The following image shows the lower register bit assignments.

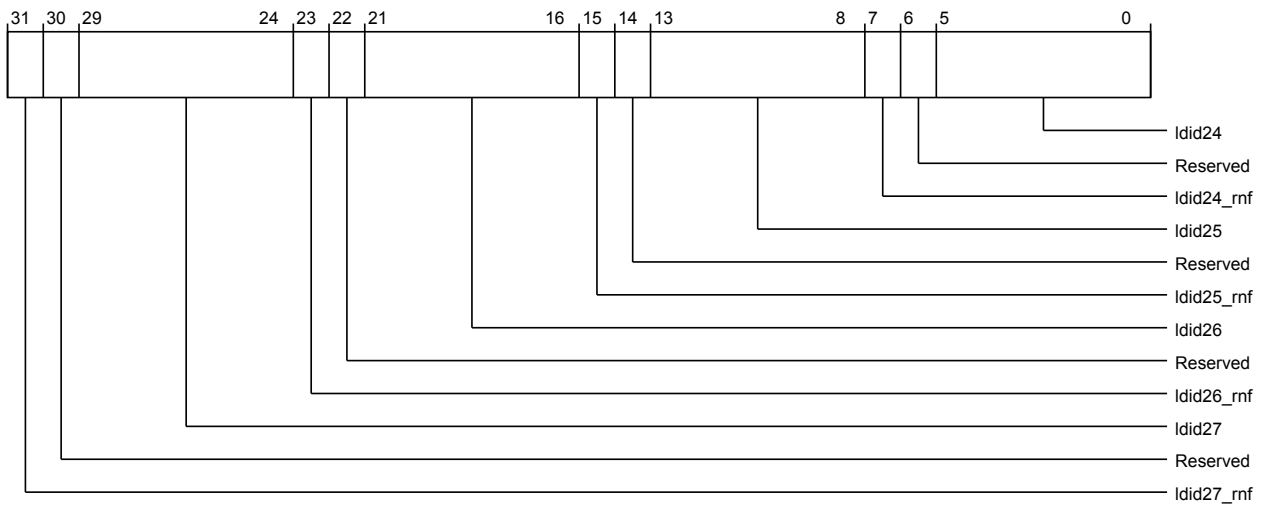


Figure 4-1057 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg3` (low)

The following table shows the `por_cxg_ha_rnf_raid_to_ldid_reg3` lower register bit assignments.

Table 4-1074 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg3` (low)

Bits	Field name	Description	Type	Reset
31	ldid27_rnf	Specifies if RAID 27 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid27	Specifies the LDID for RAID 27	RW	6'h0
23	ldid26_rnf	Specifies if RAID 26 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid26	Specifies the LDID for RAID 26	RW	6'h0
15	ldid25_rnf	Specifies if RAID 25 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid25	Specifies the LDID for RAID 25	RW	6'h0
7	ldid24_rnf	Specifies if RAID 24 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid24	Specifies the LDID for RAID 24	RW	6'h0

`por_cxg_ha_rnf_raid_to_ldid_reg4`

Specifies the mapping of RAID to RN-F LDID for RAIDs 32 to 39.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC20

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

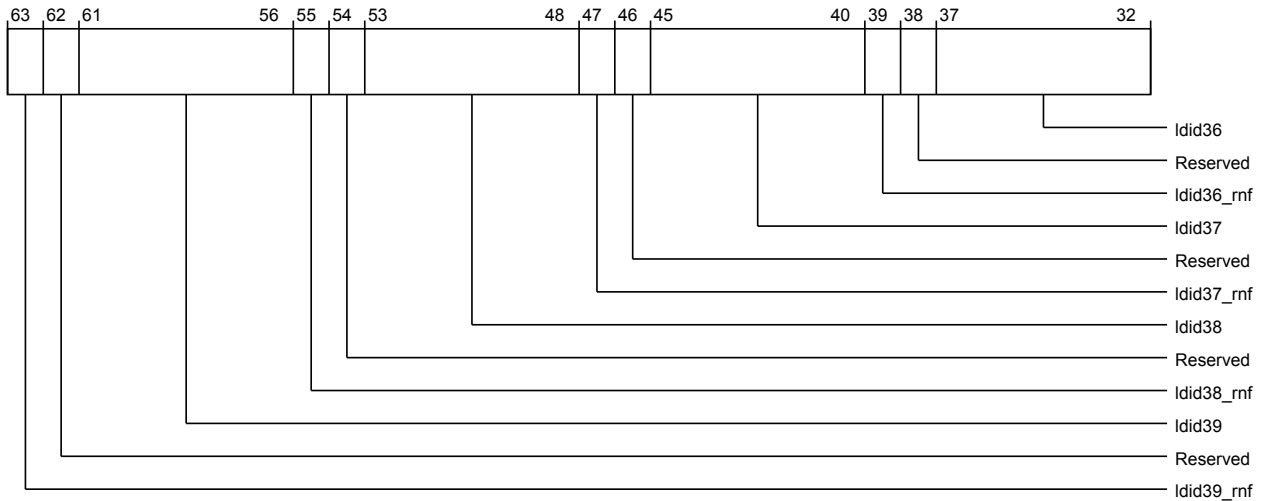


Figure 4-1058 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg4 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg4 higher register bit assignments.

Table 4-1075 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg4 (high)

Bits	Field name	Description	Type	Reset
63	ldid39_rnf	Specifies if RAID 39 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid39	Specifies the LDID for RAID 39	RW	6'h0
55	ldid38_rnf	Specifies if RAID 38 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid38	Specifies the LDID for RAID 38	RW	6'h0
47	ldid37_rnf	Specifies if RAID 37 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid37	Specifies the LDID for RAID 37	RW	6'h0
39	ldid36_rnf	Specifies if RAID 36 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid36	Specifies the LDID for RAID 36	RW	6'h0

The following image shows the lower register bit assignments.

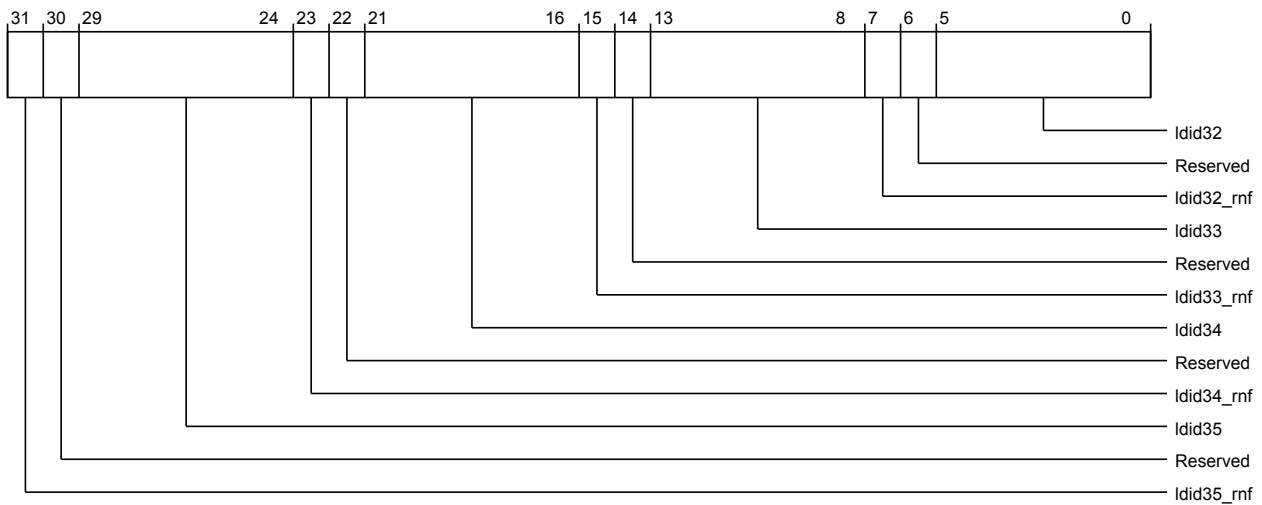


Figure 4-1059 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg4 (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg4 lower register bit assignments.

Table 4-1076 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg4 (low)

Bits	Field name	Description	Type	Reset
31	ldid35_rnf	Specifies if RAID 35 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid35	Specifies the LDID for RAID 35	RW	6'h0
23	ldid34_rnf	Specifies if RAID 34 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid34	Specifies the LDID for RAID 34	RW	6'h0
15	ldid33_rnf	Specifies if RAID 33 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid33	Specifies the LDID for RAID 33	RW	6'h0
7	ldid32_rnf	Specifies if RAID 32 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid32	Specifies the LDID for RAID 32	RW	6'h0

por_cxg_ha_rnf_raid_to_ldid_reg5

Specifies the mapping of RAID to RN-F LDID for RAIDs 40 to 47.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC28

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

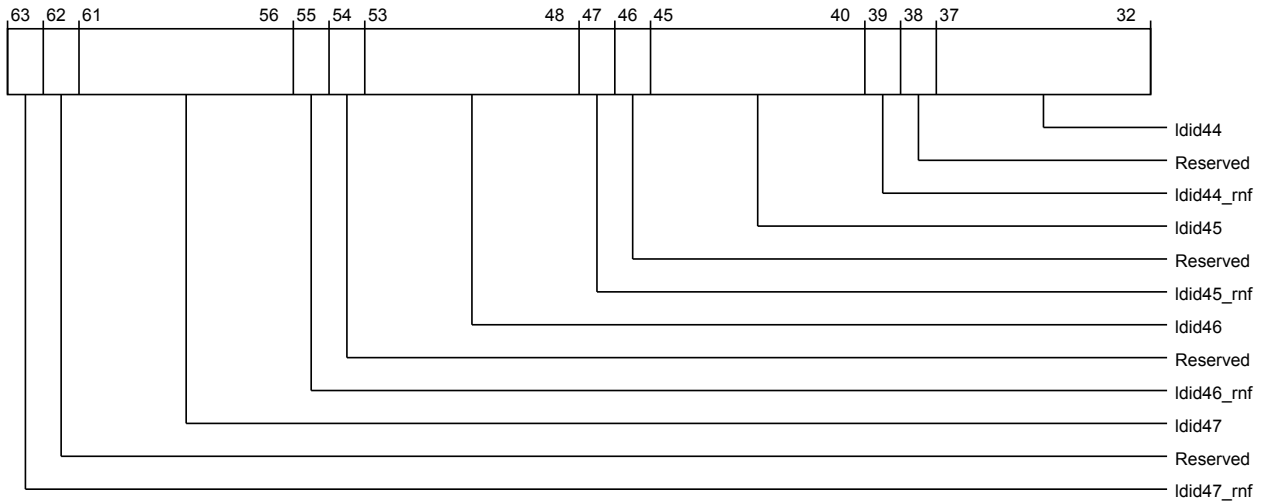


Figure 4-1060 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg5 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg5 higher register bit assignments.

Table 4-1077 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg5 (high)

Bits	Field name	Description	Type	Reset
63	ldid47_rnf	Specifies if RAID 47 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid47	Specifies the LDID for RAID 47	RW	6'h0
55	ldid46_rnf	Specifies if RAID 46 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid46	Specifies the LDID for RAID 46	RW	6'h0
47	ldid45_rnf	Specifies if RAID 45 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid45	Specifies the LDID for RAID 45	RW	6'h0
39	ldid44_rnf	Specifies if RAID 44 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid44	Specifies the LDID for RAID 44	RW	6'h0

The following image shows the lower register bit assignments.

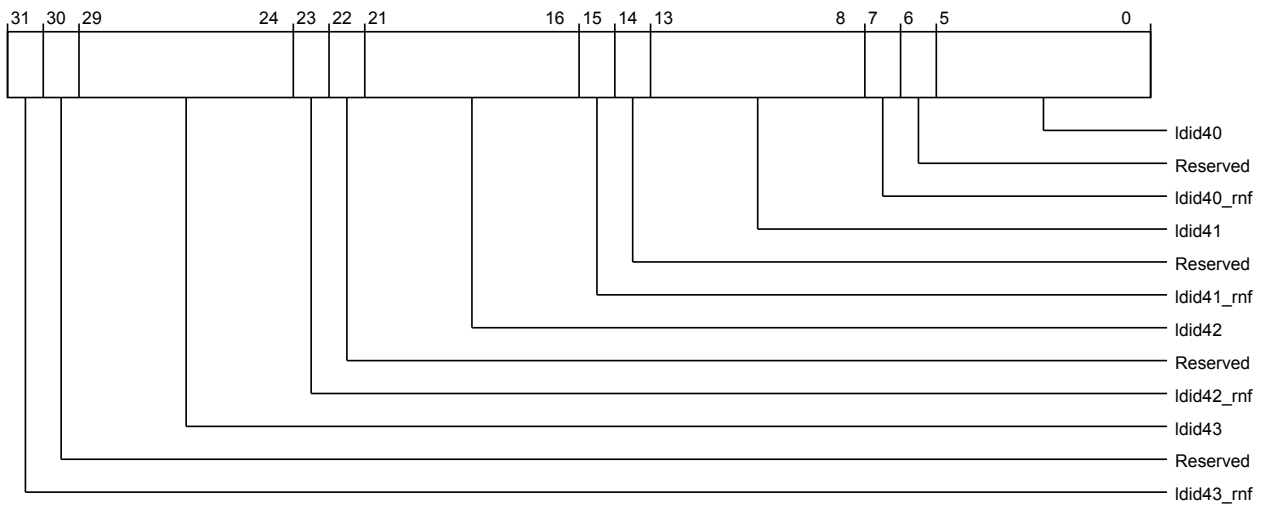


Figure 4-1061 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg5` (low)

The following table shows the `por_cxg_ha_rnf_raid_to_ldid_reg5` lower register bit assignments.

Table 4-1078 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg5` (low)

Bits	Field name	Description	Type	Reset
31	ldid43_rnf	Specifies if RAID 43 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid43	Specifies the LDID for RAID 43	RW	6'h0
23	ldid42_rnf	Specifies if RAID 42 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid42	Specifies the LDID for RAID 42	RW	6'h0
15	ldid41_rnf	Specifies if RAID 41 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid41	Specifies the LDID for RAID 41	RW	6'h0
7	ldid40_rnf	Specifies if RAID 40 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid40	Specifies the LDID for RAID 40	RW	6'h0

`por_cxg_ha_rnf_raid_to_ldid_reg6`

Specifies the mapping of RAID to RN-F LDID for RAIDs 48 to 55.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC30

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

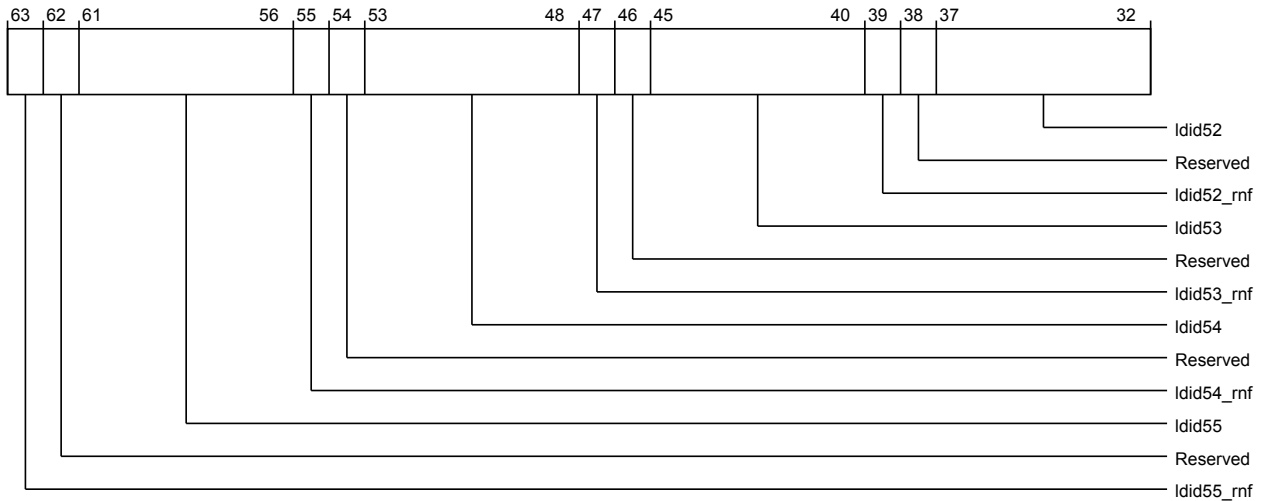


Figure 4-1062 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg6 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg6 higher register bit assignments.

Table 4-1079 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg6 (high)

Bits	Field name	Description	Type	Reset
63	ldid55_rnf	Specifies if RAID 55 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid55	Specifies the LDID for RAID 55	RW	6'h0
55	ldid54_rnf	Specifies if RAID 54 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid54	Specifies the LDID for RAID 54	RW	6'h0
47	ldid53_rnf	Specifies if RAID 53 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid53	Specifies the LDID for RAID 53	RW	6'h0
39	ldid52_rnf	Specifies if RAID 52 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid52	Specifies the LDID for RAID 52	RW	6'h0

The following image shows the lower register bit assignments.

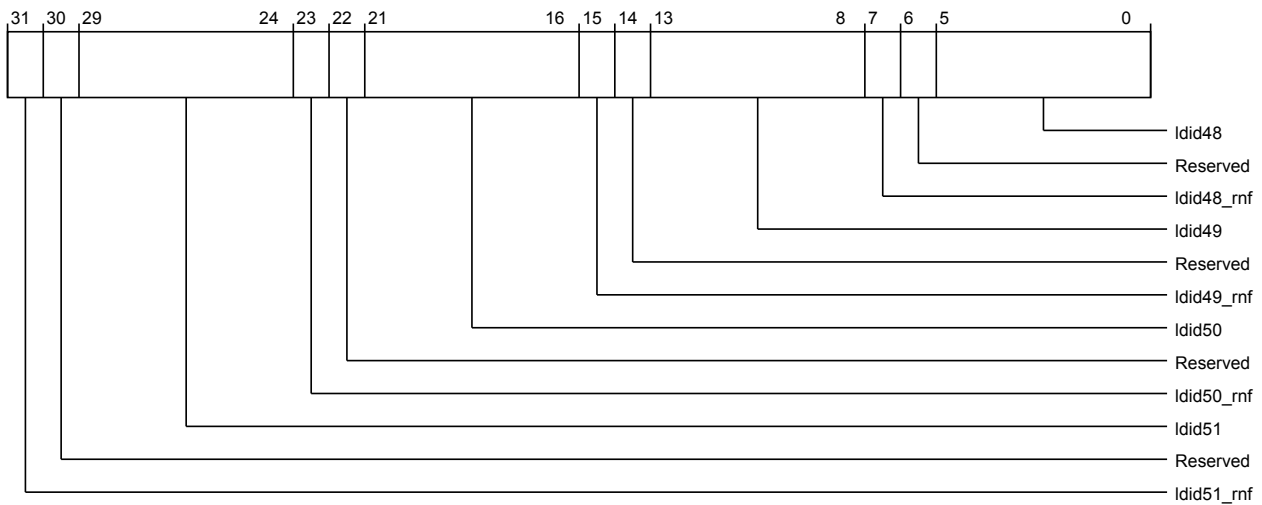


Figure 4-1063 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg6` (low)

The following table shows the `por_cxg_ha_rnf_raid_to_ldid_reg6` lower register bit assignments.

Table 4-1080 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg6` (low)

Bits	Field name	Description	Type	Reset
31	ldid51_rnf	Specifies if RAID 51 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid51	Specifies the LDID for RAID 51	RW	6'h0
23	ldid50_rnf	Specifies if RAID 50 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid50	Specifies the LDID for RAID 50	RW	6'h0
15	ldid49_rnf	Specifies if RAID 49 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid49	Specifies the LDID for RAID 49	RW	6'h0
7	ldid48_rnf	Specifies if RAID 48 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid48	Specifies the LDID for RAID 48	RW	6'h0

`por_cxg_ha_rnf_raid_to_ldid_reg7`

Specifies the mapping of RAID to RN-F LDID for RAIDs 56 to 63.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

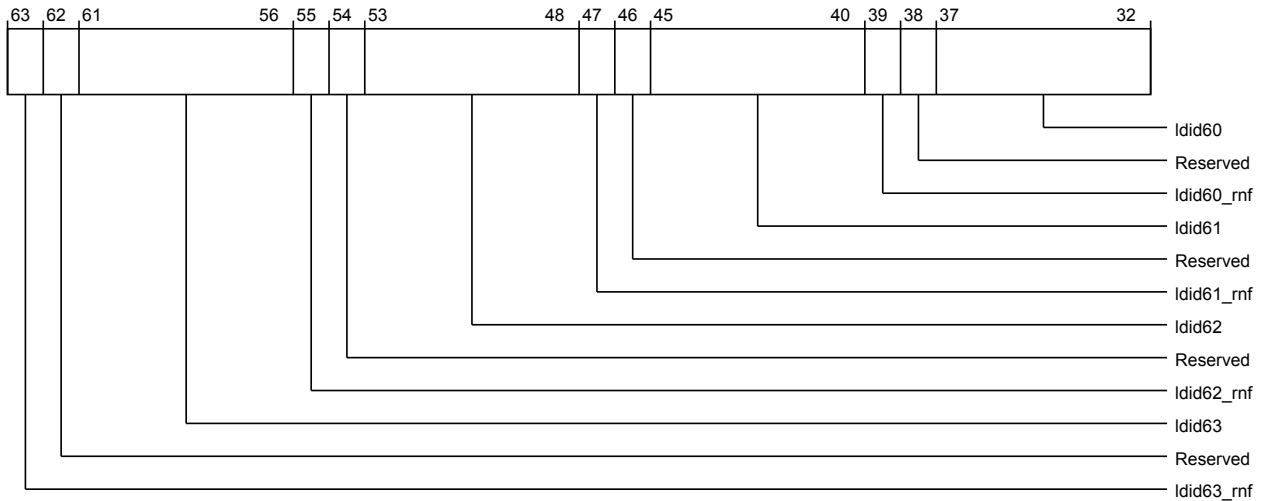


Figure 4-1064 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg7 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg7 higher register bit assignments.

Table 4-1081 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg7 (high)

Bits	Field name	Description	Type	Reset
63	ldid63_rnf	Specifies if RAID 63 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid63	Specifies the LDID for RAID 63	RW	6'h0
55	ldid62_rnf	Specifies if RAID 62 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid62	Specifies the LDID for RAID 62	RW	6'h0
47	ldid61_rnf	Specifies if RAID 61 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid61	Specifies the LDID for RAID 61	RW	6'h0
39	ldid60_rnf	Specifies if RAID 60 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid60	Specifies the LDID for RAID 60	RW	6'h0

The following image shows the lower register bit assignments.

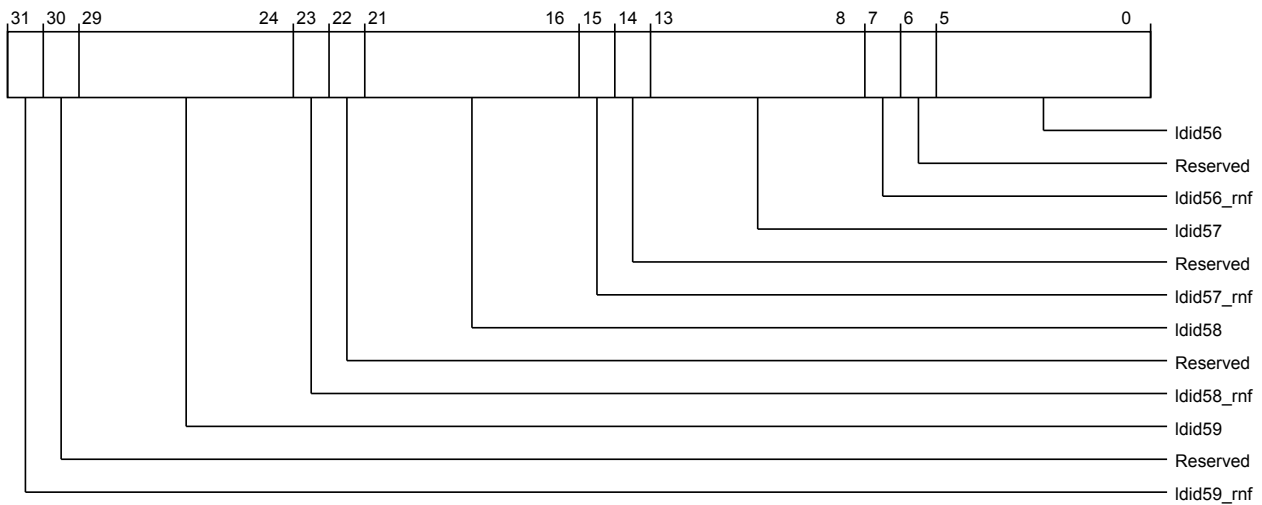


Figure 4-1065 `por_cxg_ha_por_cxg_ha_rnf RAID to LDID reg7 (low)`

The following table shows the `por_cxg_ha_rnf RAID to LDID reg7` lower register bit assignments.

Table 4-1082 `por_cxg_ha_por_cxg_ha_rnf RAID to LDID reg7 (low)`

Bits	Field name	Description	Type	Reset
31	<code>ldid59_rnf</code>	Specifies if RAID 59 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	<code>ldid59</code>	Specifies the LDID for RAID 59	RW	6'h0
23	<code>ldid58_rnf</code>	Specifies if RAID 58 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	<code>ldid58</code>	Specifies the LDID for RAID 58	RW	6'h0
15	<code>ldid57_rnf</code>	Specifies if RAID 57 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	<code>ldid57</code>	Specifies the LDID for RAID 57	RW	6'h0
7	<code>ldid56_rnf</code>	Specifies if RAID 56 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	<code>ldid56</code>	Specifies the LDID for RAID 56	RW	6'h0

`por_cxg_ha_agentid_to_linkid_reg0`

Specifies the mapping of Agent ID to Link ID for Agent IDs 0 to 7.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC40

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

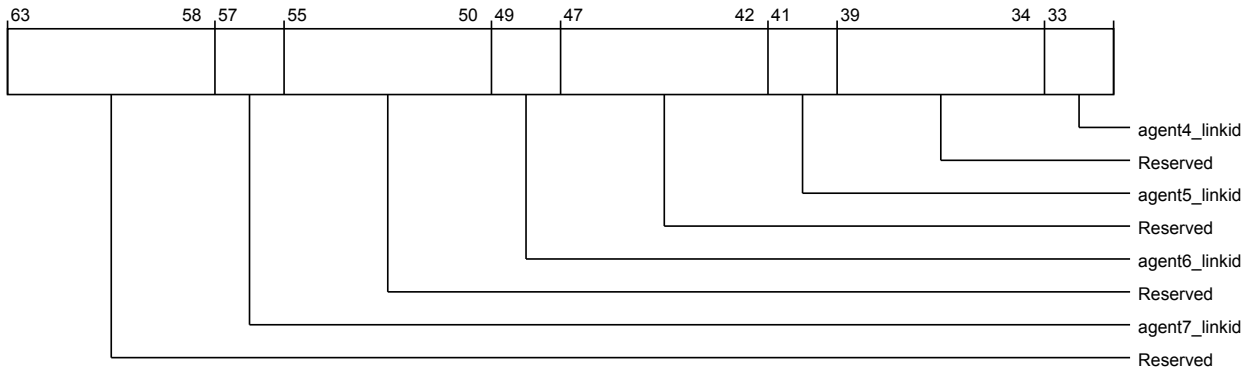


Figure 4-1066 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg0 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg0 higher register bit assignments.

Table 4-1083 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent7_linkid	Specifies Link ID 7	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent6_linkid	Specifies Link ID 6	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent5_linkid	Specifies Link ID 5	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent4_linkid	Specifies Link ID 4	RW	2'h0

The following image shows the lower register bit assignments.

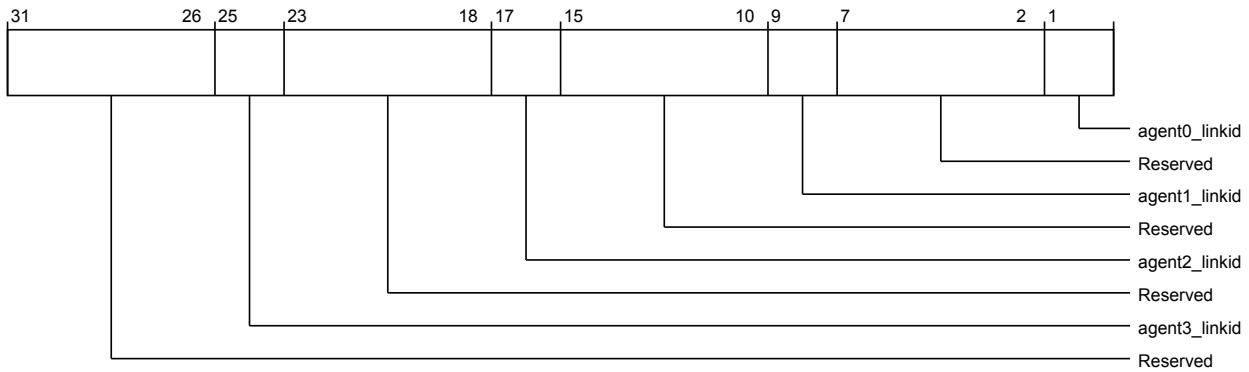


Figure 4-1067 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg0 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg0 lower register bit assignments.

Table 4-1084 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent3_linkid	Specifies Link ID 3	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent2_linkid	Specifies Link ID 2	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent1_linkid	Specifies Link ID 1	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent0_linkid	Specifies Link ID 0	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg1

Specifies the mapping of Agent ID to Link ID for Agent IDs 8 to 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC48
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

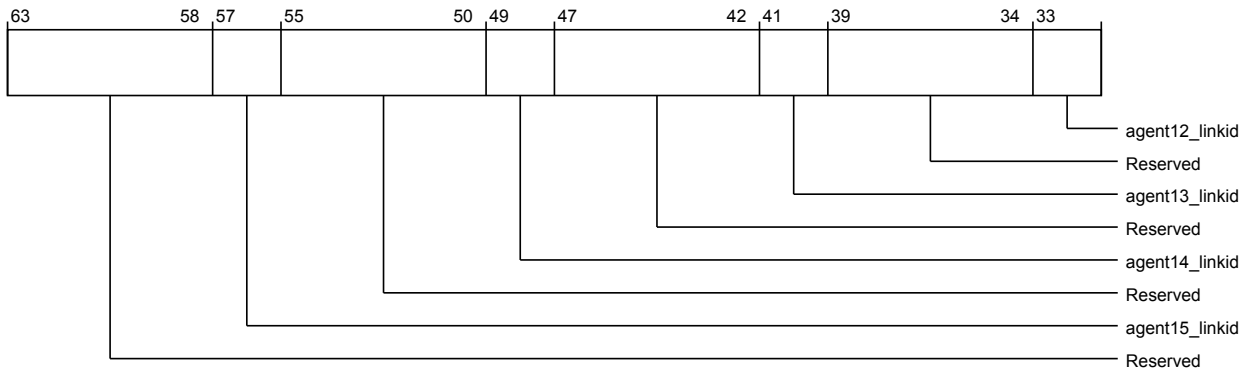


Figure 4-1068 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg1` (high)

The following table shows the `por_cxg_ha_agentid_to_linkid_reg1` higher register bit assignments.

Table 4-1085 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg1` (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent15_linkid	Specifies Link ID 15	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent14_linkid	Specifies Link ID 14	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent13_linkid	Specifies Link ID 13	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent12_linkid	Specifies Link ID 12	RW	2'h0

The following image shows the lower register bit assignments.

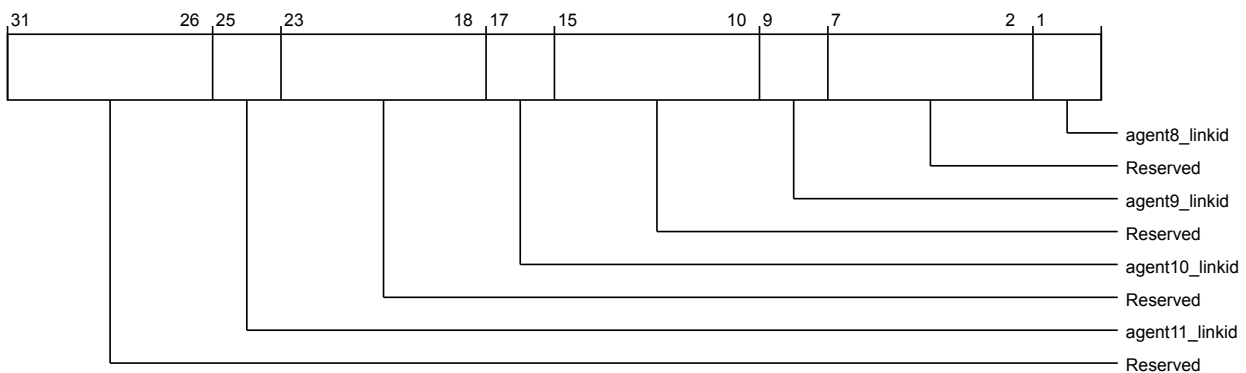


Figure 4-1069 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg1` (low)

The following table shows the `por_cxg_ha_agentid_to_linkid_reg1` lower register bit assignments.

Table 4-1086 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg1` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent11_linkid	Specifies Link ID 11	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent10_linkid	Specifies Link ID 10	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent9_linkid	Specifies Link ID 9	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent8_linkid	Specifies Link ID 8	RW	2'h0

`por_cxg_ha_agentid_to_linkid_reg2`

Specifies the mapping of Agent ID to Link ID for Agent IDs 16 to 23.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC50
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ha_secure_register_groups_override.linkid_ctl</code>

The following image shows the higher register bit assignments.

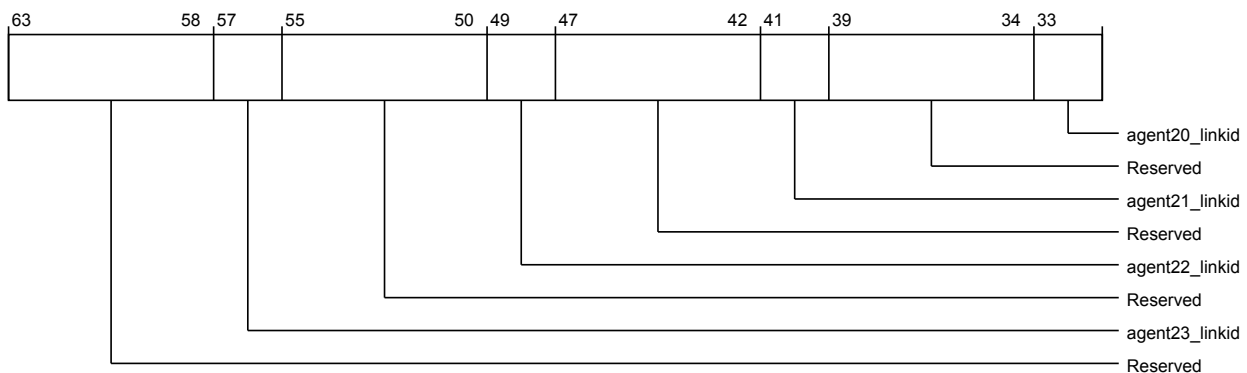


Figure 4-1070 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg2` (high)

The following table shows the `por_cxg_ha_agentid_to_linkid_reg2` higher register bit assignments.

Table 4-1087 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg2` (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent23_linkid	Specifies Link ID 23	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent22_linkid	Specifies Link ID 22	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent21_linkid	Specifies Link ID 21	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent20_linkid	Specifies Link ID 20	RW	2'h0

The following image shows the lower register bit assignments.

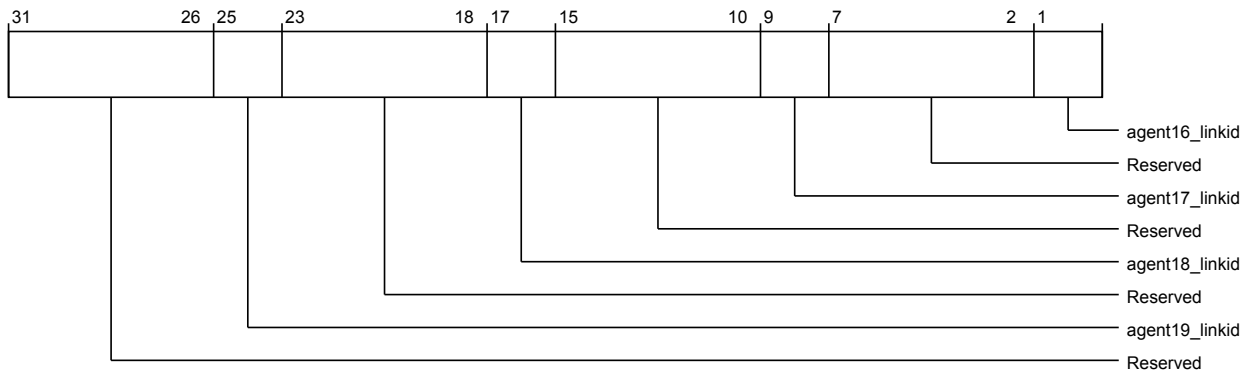


Figure 4-1071 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg2` (low)

The following table shows the `por_cxg_ha_agentid_to_linkid_reg2` lower register bit assignments.

Table 4-1088 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg2` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent19_linkid	Specifies Link ID 19	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent18_linkid	Specifies Link ID 18	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent17_linkid	Specifies Link ID 17	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent16_linkid	Specifies Link ID 16	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg3

Specifies the mapping of Agent ID to Link ID for Agent IDs 24 to 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC58
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

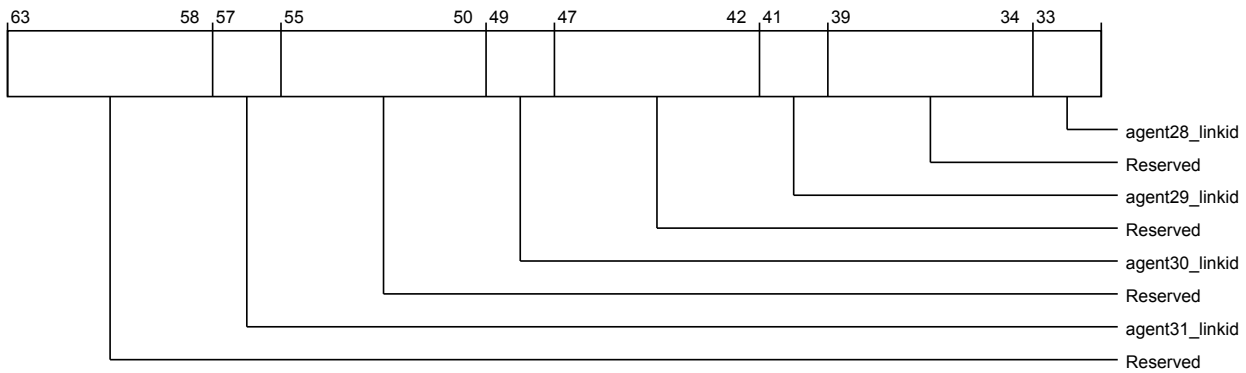


Figure 4-1072 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg3 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg3 higher register bit assignments.

Table 4-1089 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent31_linkid	Specifies Link ID 31	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent30_linkid	Specifies Link ID 30	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent29_linkid	Specifies Link ID 29	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent28_linkid	Specifies Link ID 28	RW	2'h0

The following image shows the lower register bit assignments.

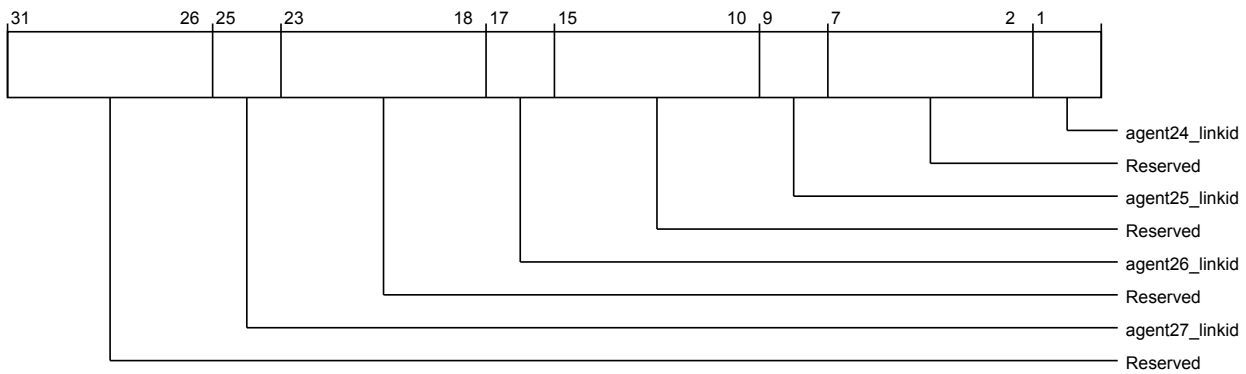


Figure 4-1073 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg3 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg3 lower register bit assignments.

Table 4-1090 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent27_linkid	Specifies Link ID 27	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent26_linkid	Specifies Link ID 26	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent25_linkid	Specifies Link ID 25	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent24_linkid	Specifies Link ID 24	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg4

Specifies the mapping of Agent ID to Link ID for Agent IDs 32 to 39.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC60
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

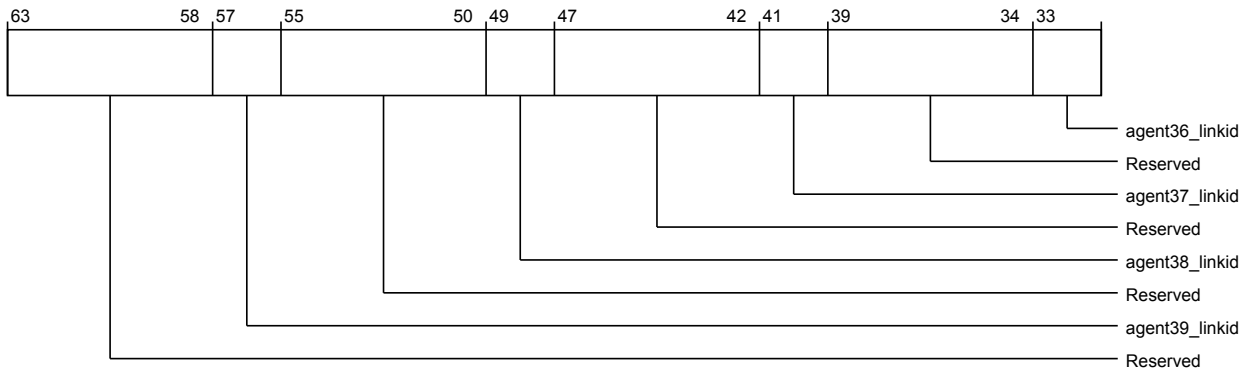


Figure 4-1074 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg4 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg4 higher register bit assignments.

Table 4-1091 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent39_linkid	Specifies Link ID 39	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent38_linkid	Specifies Link ID 38	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent37_linkid	Specifies Link ID 37	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent36_linkid	Specifies Link ID 36	RW	2'h0

The following image shows the lower register bit assignments.

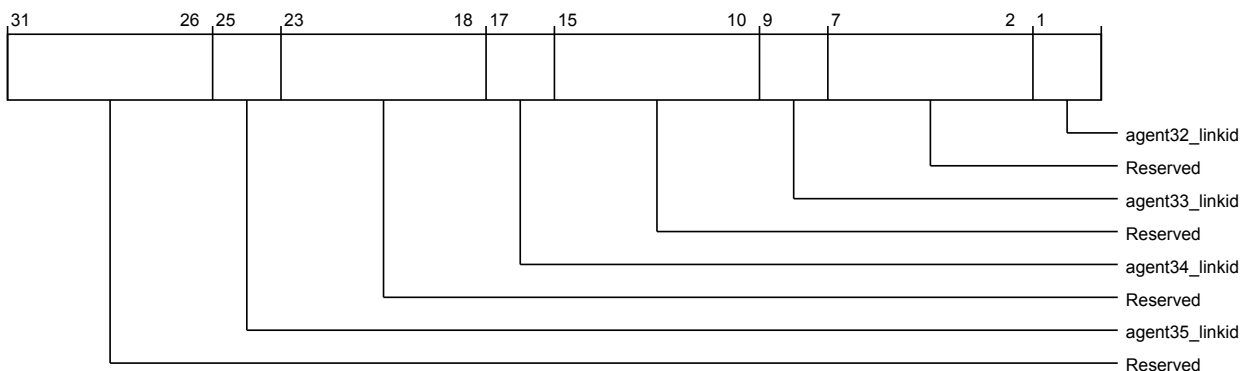


Figure 4-1075 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg4 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg4 lower register bit assignments.

Table 4-1092 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg4` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent35_linkid	Specifies Link ID 35	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent34_linkid	Specifies Link ID 34	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent33_linkid	Specifies Link ID 33	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent32_linkid	Specifies Link ID 32	RW	2'h0

`por_cxg_ha_agentid_to_linkid_reg5`

Specifies the mapping of Agent ID to Link ID for Agent IDs 40 to 47.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC68
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ha_secure_register_groups_override.linkid_ctl</code>

The following image shows the higher register bit assignments.

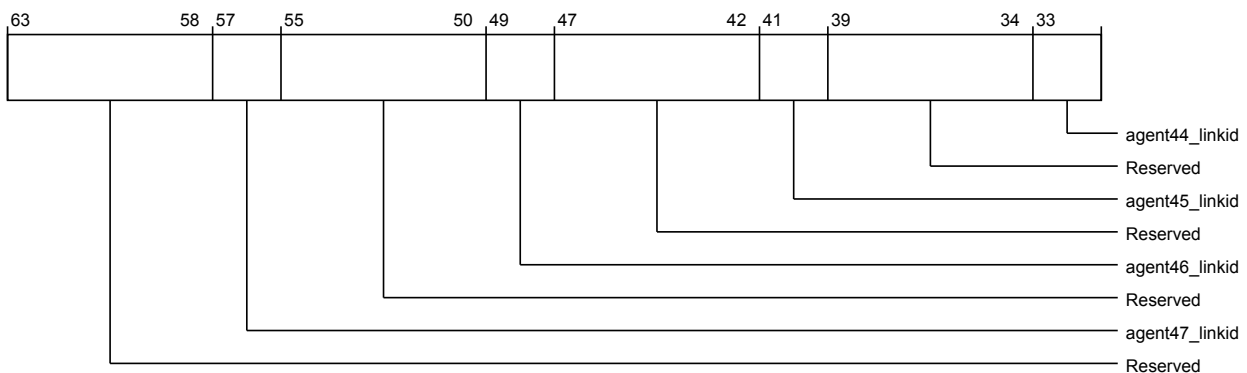


Figure 4-1076 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg5` (high)

The following table shows the `por_cxg_ha_agentid_to_linkid_reg5` higher register bit assignments.

Table 4-1093 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg5` (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent47_linkid	Specifies Link ID 47	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent46_linkid	Specifies Link ID 46	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent45_linkid	Specifies Link ID 45	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent44_linkid	Specifies Link ID 44	RW	2'h0

The following image shows the lower register bit assignments.

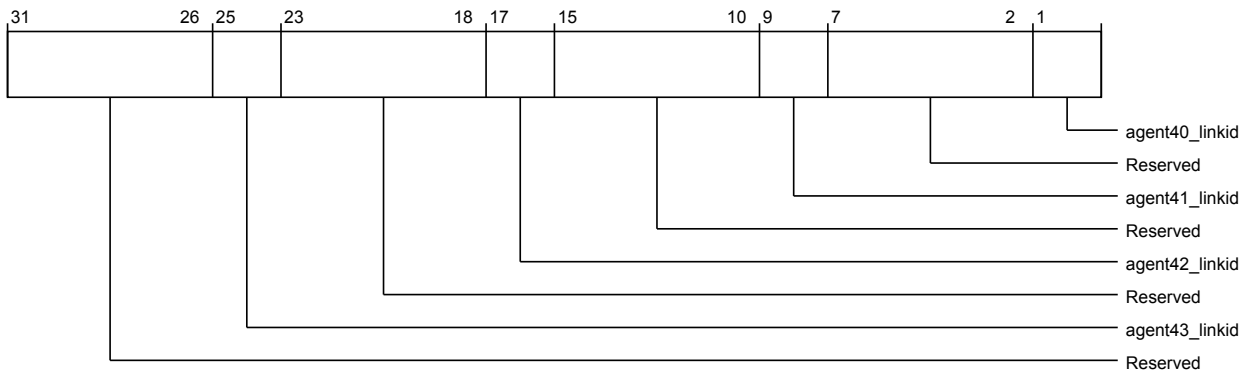


Figure 4-1077 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg5` (low)

The following table shows the `por_cxg_ha_agentid_to_linkid_reg5` lower register bit assignments.

Table 4-1094 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg5` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent43_linkid	Specifies Link ID 43	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent42_linkid	Specifies Link ID 42	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent41_linkid	Specifies Link ID 41	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent40_linkid	Specifies Link ID 40	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg6

Specifies the mapping of Agent ID to Link ID for Agent IDs 48 to 55.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC70
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

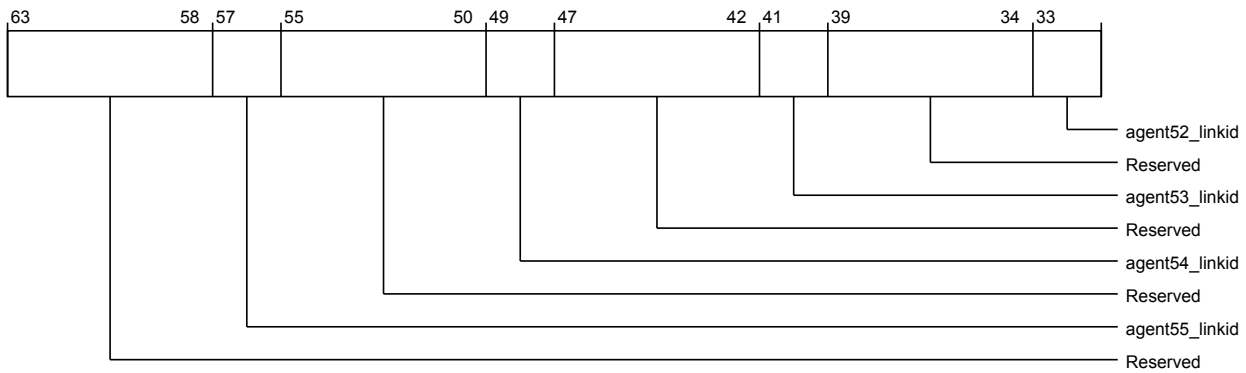


Figure 4-1078 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg6 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg6 higher register bit assignments.

Table 4-1095 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent55_linkid	Specifies Link ID 55	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent54_linkid	Specifies Link ID 54	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent53_linkid	Specifies Link ID 53	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent52_linkid	Specifies Link ID 52	RW	2'h0

The following image shows the lower register bit assignments.

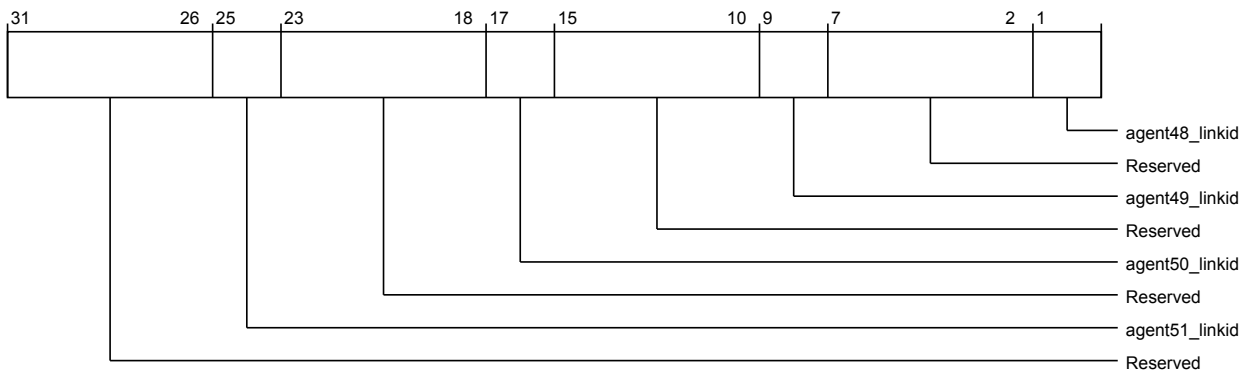


Figure 4-1079 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg6 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg6 lower register bit assignments.

Table 4-1096 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg6 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent51_linkid	Specifies Link ID 51	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent50_linkid	Specifies Link ID 50	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent49_linkid	Specifies Link ID 49	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent48_linkid	Specifies Link ID 48	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg7

Specifies the mapping of Agent ID to Link ID for Agent IDs 56 to 63.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC78
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

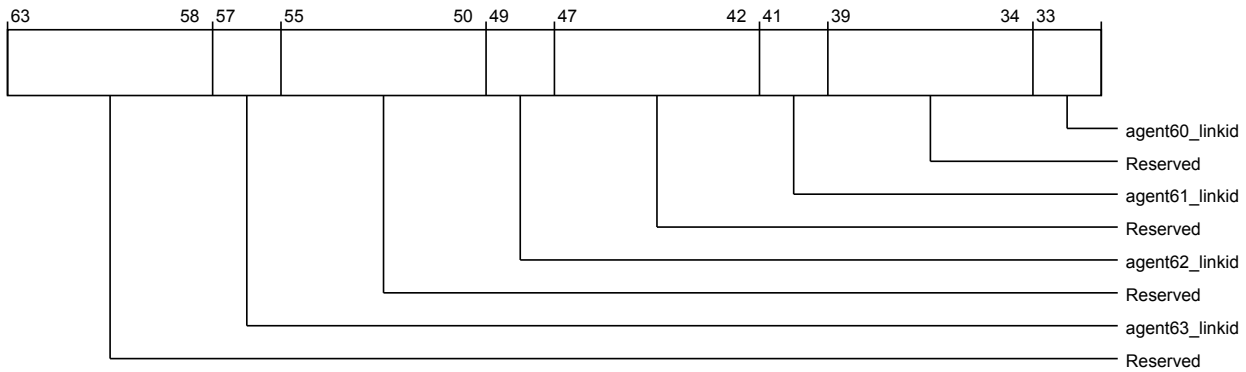


Figure 4-1080 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg7` (high)

The following table shows the `por_cxg_ha_agentid_to_linkid_reg7` higher register bit assignments.

Table 4-1097 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg7` (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent63_linkid	Specifies Link ID 63	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent62_linkid	Specifies Link ID 62	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent61_linkid	Specifies Link ID 61	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent60_linkid	Specifies Link ID 60	RW	2'h0

The following image shows the lower register bit assignments.

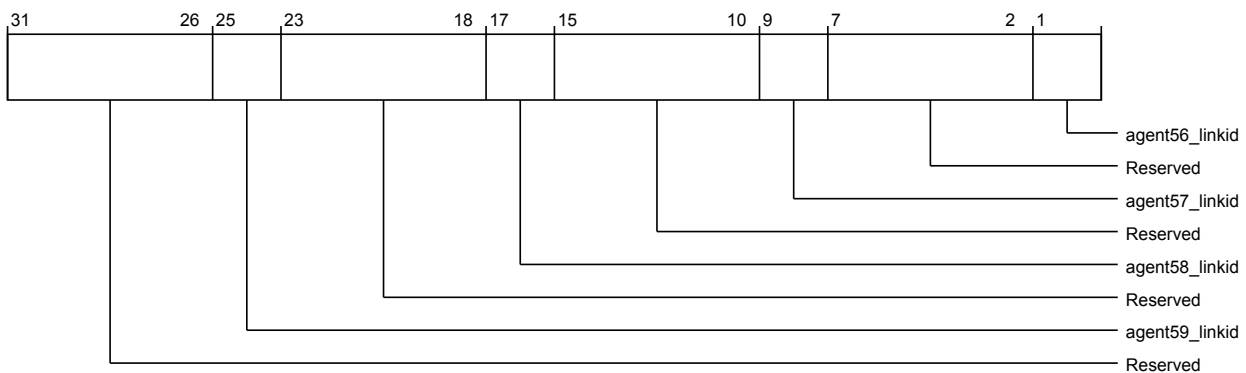


Figure 4-1081 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg7` (low)

The following table shows the `por_cxg_ha_agentid_to_linkid_reg7` lower register bit assignments.

Table 4-1098 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg7` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent59_linkid	Specifies Link ID 59	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent58_linkid	Specifies Link ID 58	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent57_linkid	Specifies Link ID 57	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent56_linkid	Specifies Link ID 56	RW	2'h0

`por_cxg_ha_agentid_to_linkid_val`

Specifies which Agent ID to Link ID mappings are valid.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ha_secure_register_groups_override.linkid_ctl</code>

The following image shows the higher register bit assignments.

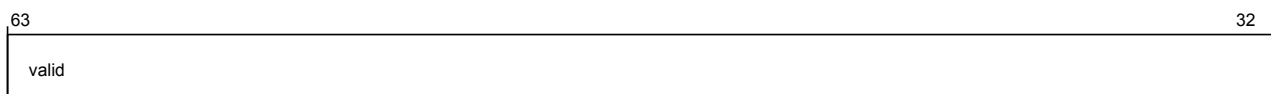


Figure 4-1082 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_val` (high)

The following table shows the `por_cxg_ha_agentid_to_linkid_val` higher register bit assignments.

Table 4-1099 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_val` (high)

Bits	Field name	Description	Type	Reset
63:32	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

The following image shows the lower register bit assignments.

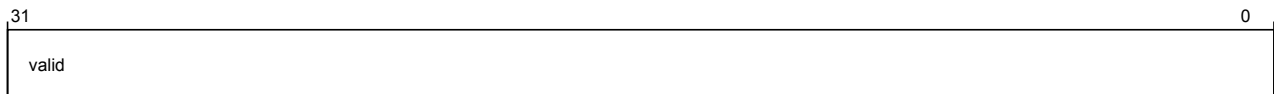


Figure 4-1083 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_val` (low)

The following table shows the `por_cxg_ha_agentid_to_linkid_val` lower register bit assignments.

Table 4-1100 `por_cxg_ha_por_cxg_ha_agentid_to_linkid_val` (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

`por_cxg_ha_rnf_raid_to_ldid_val`

Specifies which RAID to RN-F LDID mappings are valid.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD08
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ha_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

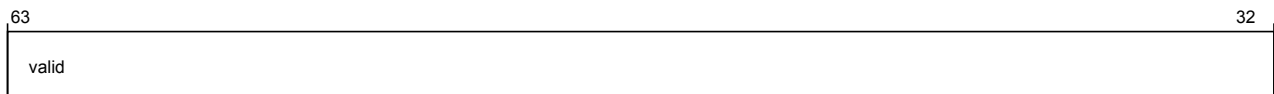


Figure 4-1084 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_val` (high)

The following table shows the `por_cxg_ha_rnf_raid_to_ldid_val` higher register bit assignments.

Table 4-1101 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_val` (high)

Bits	Field name	Description	Type	Reset
63:32	valid	Specifies whether the LDID is valid; bit number corresponds to logical RN-F LDID number (from 0 to 63)	RW	63'h0

The following image shows the lower register bit assignments.

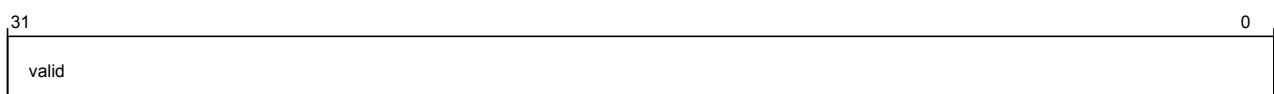


Figure 4-1085 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_val` (low)

The following table shows the `por_cxg_ha_rnf_raid_to_ldid_val` lower register bit assignments.

Table 4-1102 `por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_val` (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the LDID is valid; bit number corresponds to logical RN-F LDID number (from 0 to 63)	RW	63'h0

`por_cxg_ha_pmu_event_sel`

Specifies the PMU event to be counted.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2000
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

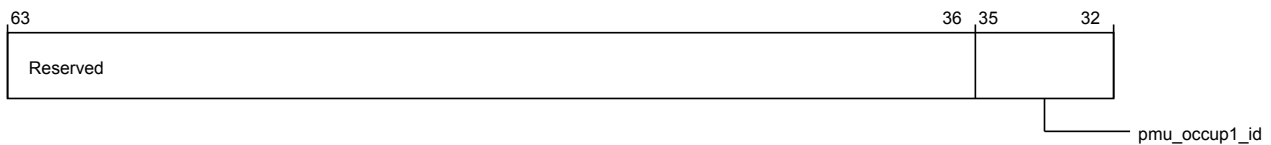


Figure 4-1086 `por_cxg_ha_por_cxg_ha_pmu_event_sel` (high)

The following table shows the `por_cxg_ha_pmu_event_sel` higher register bit assignments.

Table 4-1103 `por_cxg_ha_por_cxg_ha_pmu_event_sel` (high)

Bits	Field name	Description	Type	Reset
63:36	Reserved	Reserved	RO	-
35:32	pmu_occup1_id	CXHA PMU occupancy event selector ID	RW	4'b0

The following image shows the lower register bit assignments.

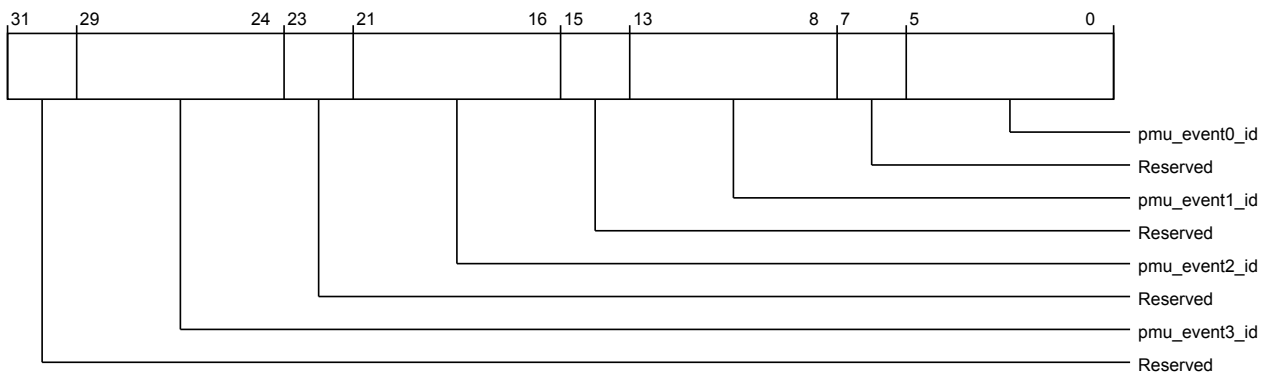


Figure 4-1087 `por_cxg_ha_por_cxg_ha_pmu_event_sel` (low)

The following table shows the `por_cxg_ha_pmu_event_sel` lower register bit assignments.

Table 4-1104 `por_cxg_ha_pmu_event_sel` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>pmu_event3_id</code>	CXHA PMU Event 3 ID; see <code>pmu_event0_id</code> for encodings	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	<code>pmu_event2_id</code>	CXHA PMU Event 2 ID; see <code>pmu_event0_id</code> for encodings	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	<code>pmu_event1_id</code>	CXHA PMU Event 1 ID; see <code>pmu_event0_id</code> for encodings	RW	6'b0
7:6	Reserved	Reserved	RO	-
5:0	<code>pmu_event0_id</code>	CXHA PMU Event 0 ID 6'b000000: CXHA_PMU_EVENT_NULL 6'b100001: CXHA_PMU_EVENT_RDDATBYP 6'b100010: CXHA_PMU_EVENT_CHIRSP_UP_STALL 6'b100011: CXHA_PMU_EVENT_CHIDAT_UP_STALL 6'b100100: CXHA_PMU_EVENT_SNPPCRD_LNK0_STALL 6'b100101: CXHA_PMU_EVENT_SNPPCRD_LNK1_STALL 6'b100110: CXHA_PMU_EVENT_SNPPCRD_LNK2_STALL 6'b100111: CXHA_PMU_EVENT_REQTRK_OCC 6'b101000: CXHA_PMU_EVENT_RDB_OCC 6'b101001: CXHA_PMU_EVENT_RDBBYP_OCC 6'b101010: CXHA_PMU_EVENT_WDB_OCC 6'b101011: CXHA_PMU_EVENT_SNPTRK_OCC 6'b101100: CXHA_PMU_EVENT_SDB_OCC 6'b101101: CXHA_PMU_EVENT_SNPHAZ_OCC	RW	6'b0

`por_cxg_ha_cxprtcl_link0_ctl`

Functions as the CXHA CCIX Protocol Link 0 control register. Works with `por_cxg_ha_cxprtcl_link0_status`.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1000
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

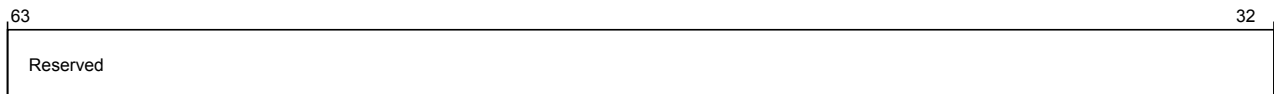


Figure 4-1088 por_cxg_ha_por_cxg_ha_cxprtcl_link0_ctl (high)

The following table shows the por_cxg_ha_cxprtcl_link0_ctl higher register bit assignments.

Table 4-1105 por_cxg_ha_por_cxg_ha_cxprtcl_link0_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

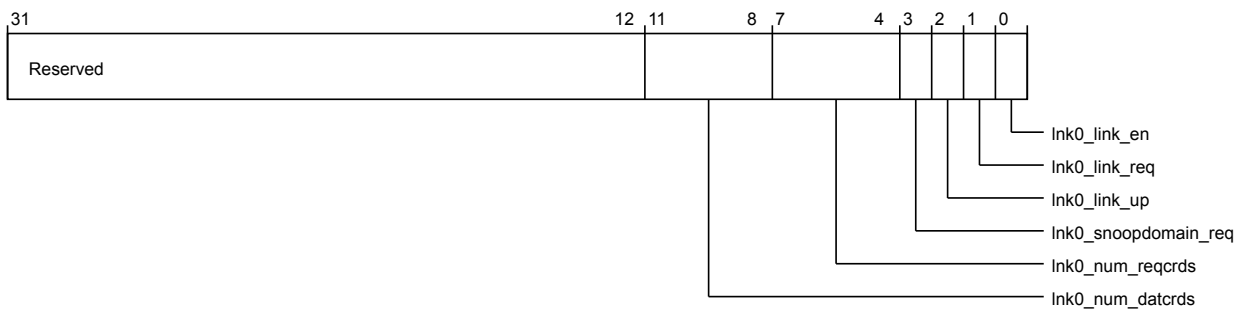


Figure 4-1089 por_cxg_ha_por_cxg_ha_cxprtcl_link0_ctl (low)

The following table shows the por_cxg_ha_cxprtcl_link0_ctl lower register bit assignments.

Table 4-1106 por_cxg_ha_por_cxg_ha_cxprtcl_link0_ctl (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	Ink0_num_datcrds	Controls the number of CCIX data credits assigned to Link 0 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0

Table 4-1106 por_cxg_ha_por_cxg_ha_cxprtcl_link0_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
7:4	lnk0_num_reqcrds	Controls the number of CCIX request credits assigned to Link 0 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	lnk0_snoopdomain_req	Controls Snoop domain enable (SYSCOREQ) for CCIX Link 0	RW	1'b0
2	lnk0_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0: Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1: Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
1	lnk0_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state. 1'b1: Link Up request	RW	1'b0
0	lnk0_link_en	Enables CCIX Link 0 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

por_cxg_ha_cxprtcl_link0_status

Functions as the CXHA CCIX Protocol Link 0 status register. Works with por_cxg_ha_cxprtcl_link0_ctl.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h1008
Register reset	64'b010
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

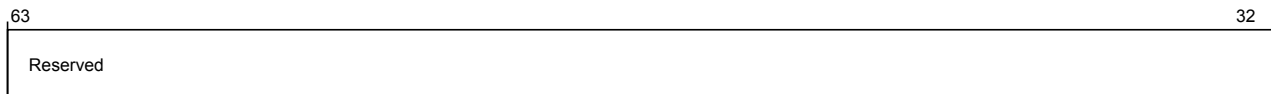


Figure 4-1090 por_cxg_ha_por_cxg_ha_cxprtcl_link0_status (high)

The following table shows the por_cxg_ha_cxprtcl_link0_status higher register bit assignments.

Table 4-1107 por_cxg_ha_por_cxg_ha_cxprtcl_link0_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

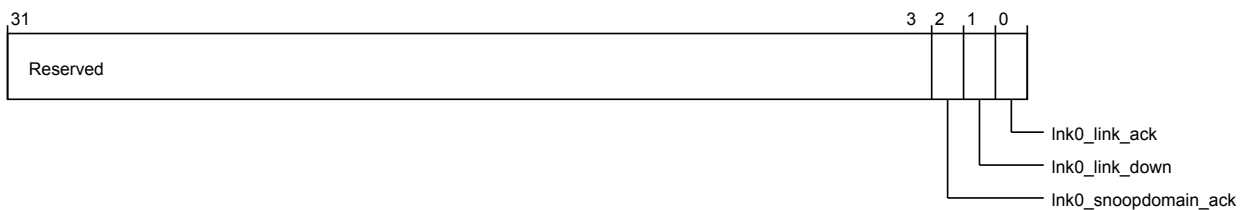


Figure 4-1091 por_cxg_ha_por_cxg_ha_cxprtcl_link0_status (low)

The following table shows the por_cxg_ha_cxprtcl_link0_status lower register bit assignments.

Table 4-1108 por_cxg_ha_por_cxg_ha_cxprtcl_link0_status (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	lnk0_snoopdomain_ack	Provides Snoop domain status (SYSCOACK) for CCIX Link 0	RO	1'b0
1	lnk0_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk0_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

por_cxg_ha_cxprtcl_link1_ctl

Functions as the CXHA CCIX Protocol Link 1 control register. Works with por_cxg_ha_cxprtcl_link1_status.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1010
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

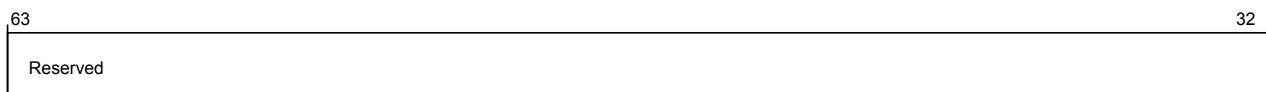


Figure 4-1092 por_cxg_ha_por_cxg_ha_cxprtcl_link1_ctl (high)

The following table shows the por_cxg_ha_cxprtcl_link1_ctl higher register bit assignments.

Table 4-1109 por_cxg_ha_por_cxg_ha_cxprtcl_link1_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

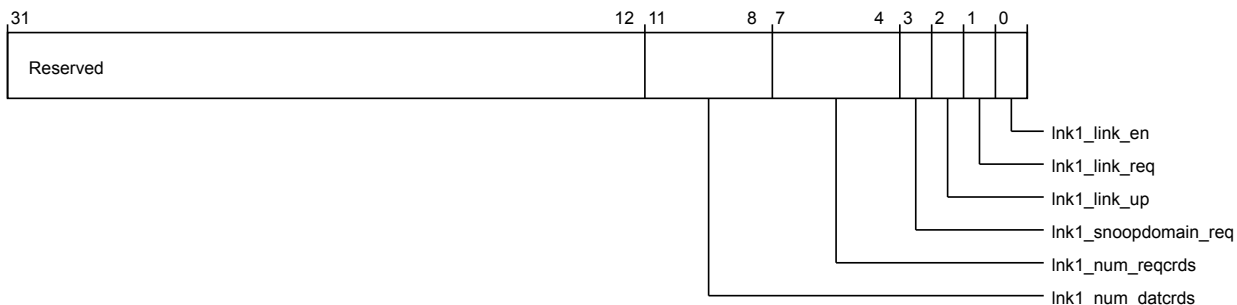


Figure 4-1093 por_cxg_ha_por_cxg_ha_cxprtcl_link1_ctl (low)

The following table shows the por_cxg_ha_cxprtcl_link1_ctl lower register bit assignments.

Table 4-1110 por_cxg_ha_por_cxg_ha_cxprtcl_link1_ctl (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	lnk1_num_daterds	Controls the number of CCIX data credits assigned to Link 1 4'h0: Total credits equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
7:4	lnk1_num_reqcrds	Controls the number of CCIX request credits assigned to Link 1 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	lnk1_snoopdomain_req	Controls Snoop domain enable (SYSCOREQ) for CCIX Link 1	RW	1'b0
2	lnk1_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0: Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1: Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
1	lnk1_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state. 1'b1: Link Up request	RW	1'b0
0	lnk1_link_en	Enables CCIX Link 1 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

por_cxg_ha_cxprtcl_link1_status

Functions as the CXHA CCIX Protocol Link 1 status register. Works with por_cxg_ha_cxprtcl_link1_ctl.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h1018
Register reset	64'b010
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

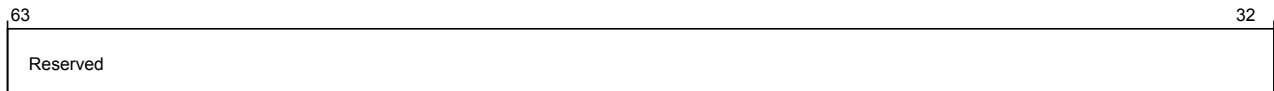


Figure 4-1094 por_cxg_ha_por_cxg_ha_cxprtcl_link1_status (high)

The following table shows the por_cxg_ha_cxprtcl_link1_status higher register bit assignments.

Table 4-1111 por_cxg_ha_por_cxg_ha_cxprtcl_link1_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

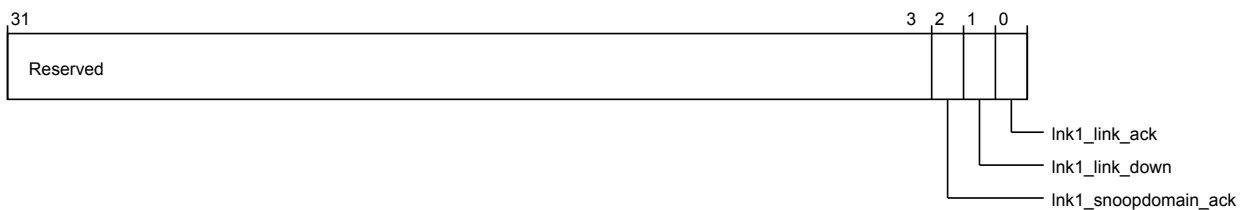


Figure 4-1095 por_cxg_ha_por_cxg_ha_cxprtcl_link1_status (low)

The following table shows the por_cxg_ha_cxprtcl_link1_status lower register bit assignments.

Table 4-1112 por_cxg_ha_por_cxg_ha_cxprtcl_link1_status (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	Ink1_snoopdomain_ack	Provides Snoop domain status (SYSCOACK) for CCIX Link 1	RO	1'b0

Table 4-1112 por_cxg_ha_por_cxg_ha_cxprtcl_link1_status (low) (continued)

Bits	Field name	Description	Type	Reset
1	lnk1_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk1_link_ack	Link Up/Down Acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

por_cxg_ha_cxprtcl_link2_ctl

Functions as the CXHA CCIX Protocol Link 2 control register. Works with por_cxg_ha_cxprtcl_link2_status.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1020
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

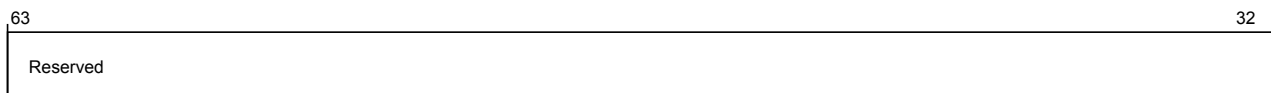


Figure 4-1096 por_cxg_ha_por_cxg_ha_cxprtcl_link2_ctl (high)

The following table shows the por_cxg_ha_cxprtcl_link2_ctl higher register bit assignments.

Table 4-1113 por_cxg_ha_por_cxg_ha_cxprtcl_link2_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

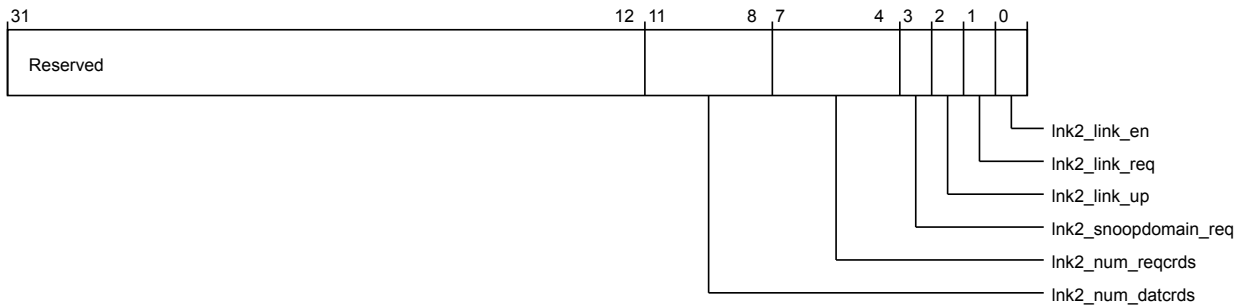


Figure 4-1097 por_cxg_ha_por_cxg_ha_cxprtcl_link2_ctl (low)

The following table shows the por_cxg_ha_cxprtcl_link2_ctl lower register bit assignments.

Table 4-1114 por_cxg_ha_por_cxg_ha_cxprtcl_link2_ctl (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	Ink2_num_datcrds	Controls the number of CCIX data credits assigned to Link 2 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
7:4	Ink2_num_reqcrds	Controls the number of CCIX request credits assigned to Link 2 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	Ink2_snoopdomain_req	Controls Snoop domain enable (SYSCOREQ) for CCIX Link 2	RW	1'b0
2	Ink2_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0: Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1: Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0

Table 4-1114 por_cxg_ha_por_cxg_ha_cxprtcl_link2_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
1	lnk2_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state. 1'b1: Link Up request	RW	1'b0
0	lnk2_link_en	Enables CCIX Link 2 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

por_cxg_ha_cxprtcl_link2_status

Functions as the CXHA CCIX Protocol Link 2 status register. Works with por_cxg_ha_cxprtcl_link2_ctl.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h1028
Register reset	64'b010
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1098 por_cxg_ha_por_cxg_ha_cxprtcl_link2_status (high)

The following table shows the por_cxg_ha_cxprtcl_link2_status higher register bit assignments.

Table 4-1115 por_cxg_ha_por_cxg_ha_cxprtcl_link2_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

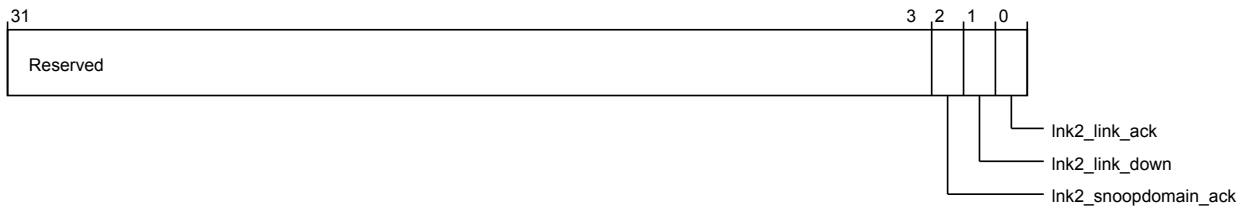


Figure 4-1099 por_cxg_ha_por_cxg_ha_cxprtcl_link2_status (low)

The following table shows the por_cxg_ha_cxprtcl_link2_status lower register bit assignments.

Table 4-1116 por_cxg_ha_por_cxg_ha_cxprtcl_link2_status (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	lnk2_snoopdomain_ack	Provides Snoop domain status (SYSCOACK) for CCIX Link 2	RO	1'b0
1	lnk2_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk2_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

por_cxg_ha_errfr

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3000
Register reset	64'b00000010100101
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

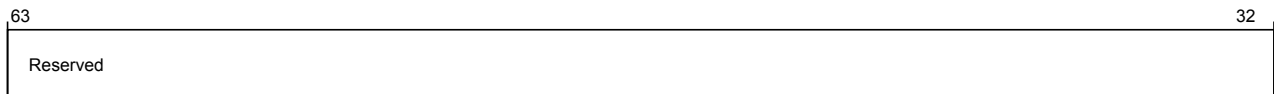


Figure 4-1100 `por_cxg_ha_por_cxg_ha_errfr` (high)

The following table shows the `por_cxg_ha_errfr` higher register bit assignments.

Table 4-1117 `por_cxg_ha_por_cxg_ha_errfr` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

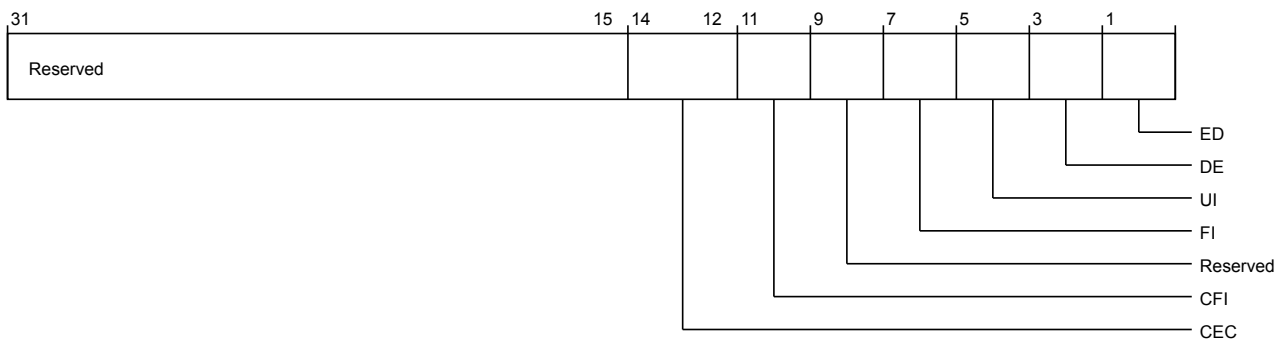


Figure 4-1101 `por_cxg_ha_por_cxg_ha_errfr` (low)

The following table shows the `por_cxg_ha_errfr` lower register bit assignments.

Table 4-1118 `por_cxg_ha_por_cxg_ha_errfr` (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in <code>por_cxg_ha_errmisc[39:32]</code> 3'b100: Implements 16-bit error counter in <code>por_cxg_ha_errmisc[47:32]</code>	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_cxg_ha_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3008
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

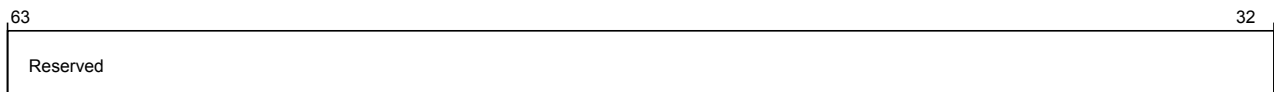


Figure 4-1102 por_cxg_ha_errctlr (high)

The following table shows the por_cxg_ha_errctlr higher register bit assignments.

Table 4-1119 por_cxg_ha_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

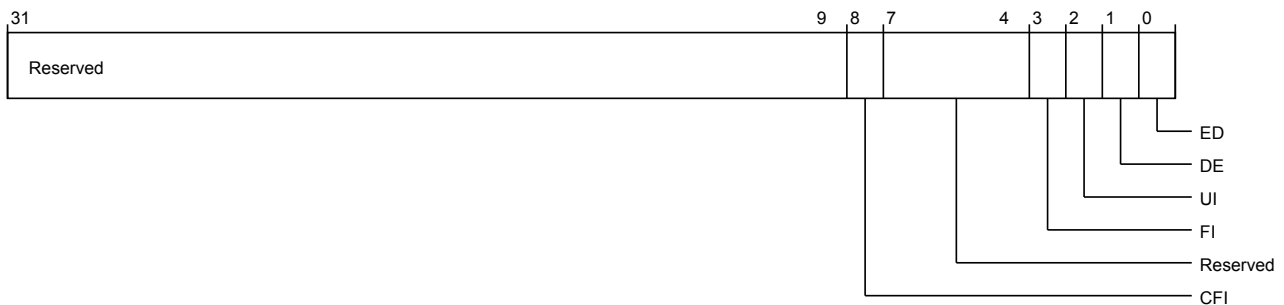


Figure 4-1103 por_cxg_ha_errctlr (low)

The following table shows the por_cxg_ha_errctlr lower register bit assignments.

Table 4-1120 por_cxg_ha_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_cxg_ha_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-

Table 4-1120 por_cxg_ha_por_cxg_ha_errctlr (low) (continued)

Bits	Field name	Description	Type	Reset
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_cxg_ha_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_cxg_ha_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_cxg_ha_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_cxg_ha_errfr.ED	RW	1'b0

por_cxg_ha_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 14'h3010
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

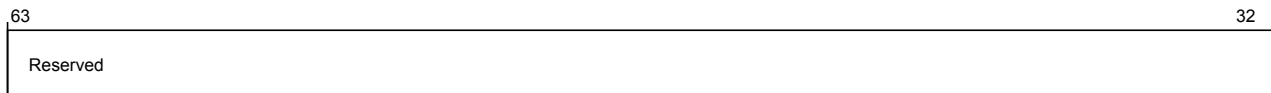


Figure 4-1104 por_cxg_ha_por_cxg_ha_errstatus (high)

The following table shows the por_cxg_ha_errstatus higher register bit assignments.

Table 4-1121 por_cxg_ha_por_cxg_ha_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

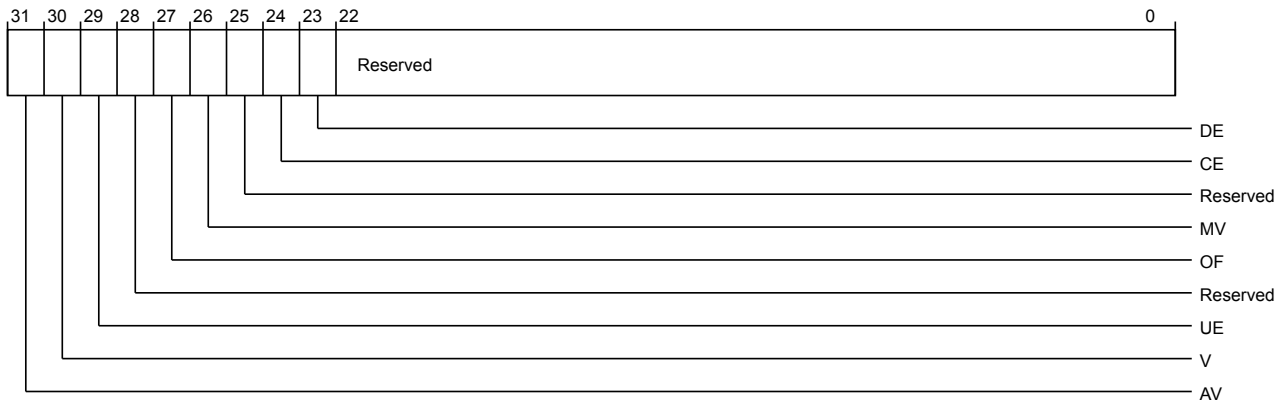


Figure 4-1105 `por_cxg_ha_errstatus` (low)

The following table shows the `por_cxg_ha_errstatus` lower register bit assignments.

Table 4-1122 `por_cxg_ha_errstatus` (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; <code>por_cxg_ha_erraddr</code> contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	<code>por_cxg_ha_errmisc</code> valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 4-1122 por_cxg_ha_por_cxg_ha_errstatus (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_cxg_ha_erraddr

Contains the error record address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3018

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

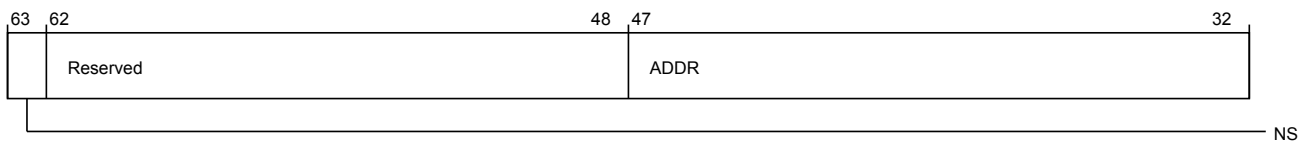


Figure 4-1106 por_cxg_ha_por_cxg_ha_erraddr (high)

The following table shows the `por_cxg_ha_erraddr` higher register bit assignments.

Table 4-1123 por_cxg_ha_por_cxg_ha_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_cxg_ha_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

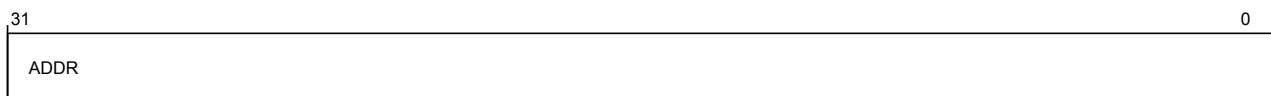


Figure 4-1107 por_cxg_ha_por_cxg_ha_erraddr (low)

The following table shows the por_cxg_ha_erraddr lower register bit assignments.

Table 4-1124 por_cxg_ha_por_cxg_ha_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_cxg_ha_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3020

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

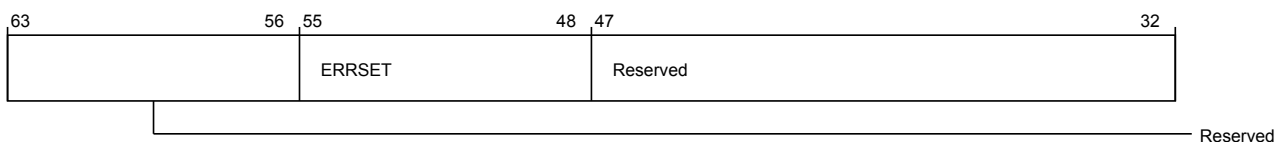


Figure 4-1108 por_cxg_ha_por_cxg_ha_errmisc (high)

The following table shows the por_cxg_ha_errmisc higher register bit assignments.

Table 4-1125 por_cxg_ha_por_cxg_ha_errmisc (high)

Bits	Field name	Description	Type	Reset
63:56	Reserved	Reserved	RO	-
55:48	ERRSET	RAM entry set address for parity error	RW	8'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

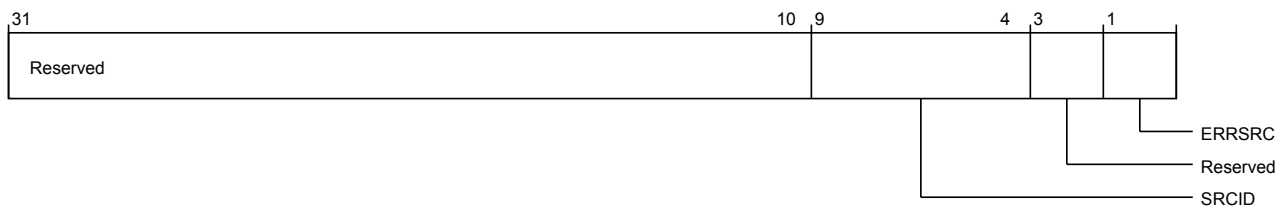


Figure 4-1109 por_cxg_ha_por_cxg_ha_errmisc (low)

The following table shows the por_cxg_ha_errmisc lower register bit assignments.

Table 4-1126 por_cxg_ha_por_cxg_ha_errmisc (low)

Bits	Field name	Description	Type	Reset
31:10	Reserved	Reserved	RO	-
9:4	SRCID	CCIX RAID of the requestor or the snoop target	RW	6'b0
3:2	Reserved	Reserved	RO	-
1:0	ERRSRC	Source of the parity error 2'b00: Read data buffer 0 2'b01: Read data buffer 1 2'b10: Write data buffer 0 2'b11: Write data buffer 1	RW	2'b00

por_cxg_ha_errfr_NS

Functions as the non-secure error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3100
Register reset	64'b00000010100101
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

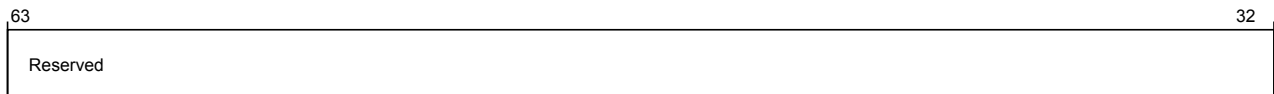


Figure 4-1110 por_cxg_ha_errfr_ns (high)

The following table shows the por_cxg_ha_errfr_NS higher register bit assignments.

Table 4-1127 por_cxg_ha_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

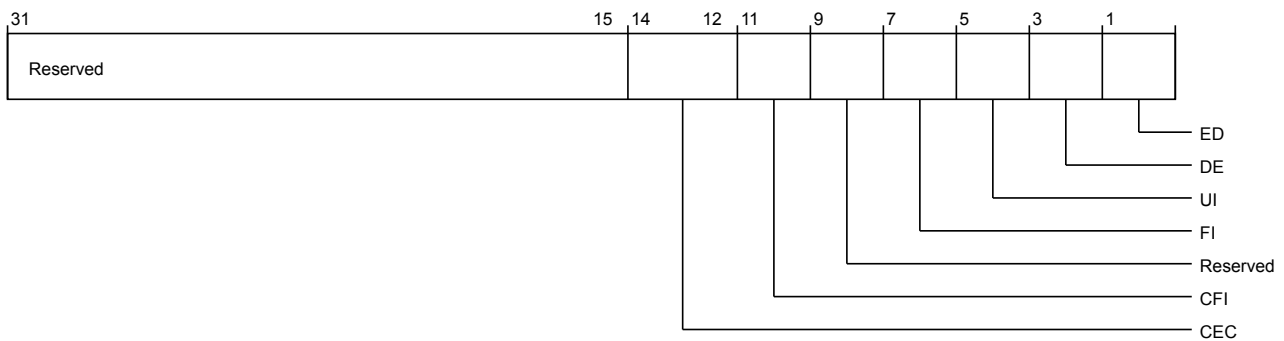


Figure 4-1111 por_cxg_ha_errfr_ns (low)

The following table shows the por_cxg_ha_errfr_NS lower register bit assignments.

Table 4-1128 por_cxg_ha_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in por_cxg_ha_errmisc[39:32] 3'b100: Implements 16-bit error counter in por_cxg_ha_errmisc[47:32]	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_cxg_ha_errctlr_NS

Functions as the non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3108
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

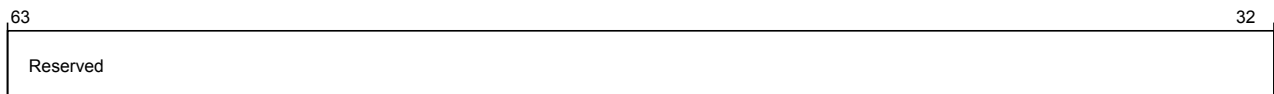


Figure 4-1112 por_cxg_ha_errctlr_ns (high)

The following table shows the por_cxg_ha_errctlr_NS higher register bit assignments.

Table 4-1129 por_cxg_ha_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

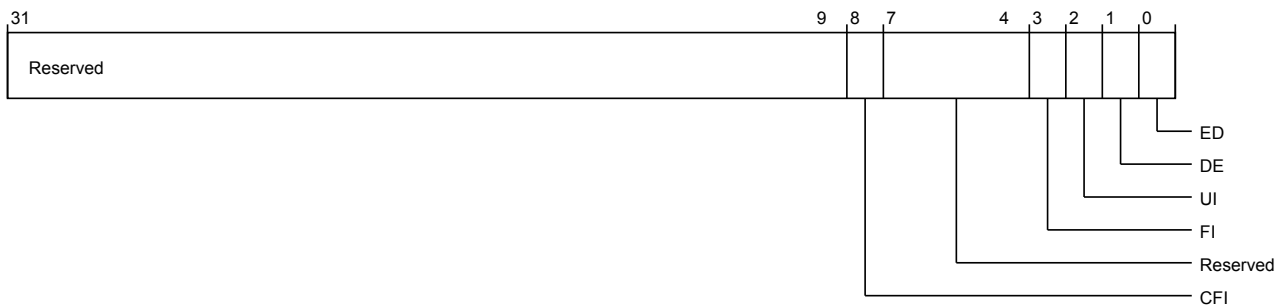


Figure 4-1113 por_cxg_ha_errctlr_ns (low)

The following table shows the por_cxg_ha_errctlr_NS lower register bit assignments.

Table 4-1130 por_cxg_ha_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_cxg_ha_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-

Table 4-1130 `por_cxg_ha_por_cxg_ha_errctlr_ns` (low) (continued)

Bits	Field name	Description	Type	Reset
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in <code>por_cxg_ha_errfr.FI</code>	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in <code>por_cxg_ha_errfr.UI</code>	RW	1'b0
1	DE	Enables error deferment as specified in <code>por_cxg_ha_errfr.DE</code>	RW	1'b0
0	ED	Enables error detection as specified in <code>por_cxg_ha_errfr.ED</code>	RW	1'b0

`por_cxg_ha_errstatus_NS`

Functions as the non-secure error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3110
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

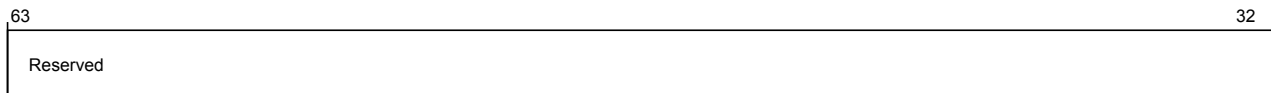


Figure 4-1114 `por_cxg_ha_por_cxg_ha_errstatus_ns` (high)

The following table shows the `por_cxg_ha_errstatus_NS` higher register bit assignments.

Table 4-1131 `por_cxg_ha_por_cxg_ha_errstatus_ns` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

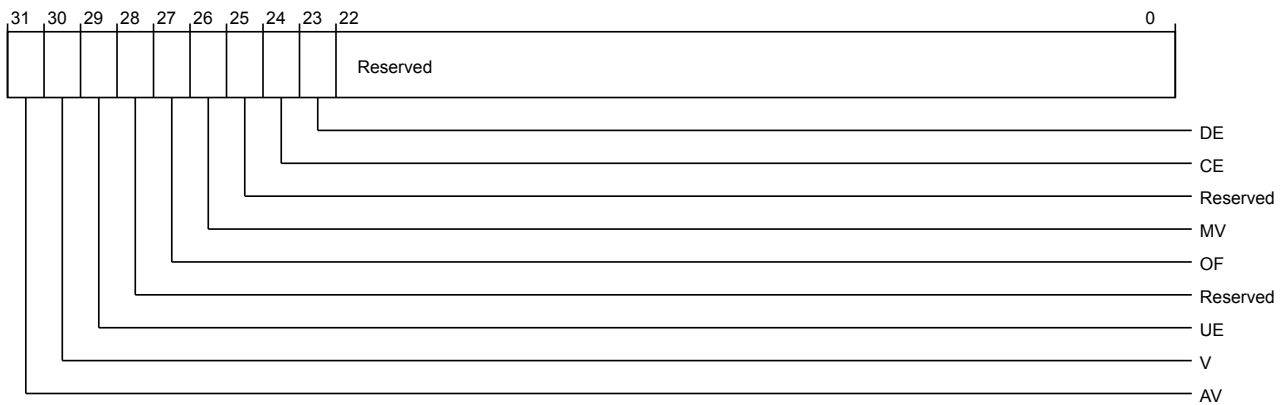


Figure 4-1115 `por_cxg_ha_por_cxg_ha_errstatus_ns` (low)

The following table shows the `por_cxg_ha_errstatus_NS` lower register bit assignments.

Table 4-1132 `por_cxg_ha_por_cxg_ha_errstatus_ns` (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; <code>por_cxg_ha_erraddr</code> contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	<code>por_cxg_ha_errmisc</code> valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 4-1132 por_cxg_ha_por_cxg_ha_errstatus_ns (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_cxg_ha_erraddr_NS

Contains the non-secure error record address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3118

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

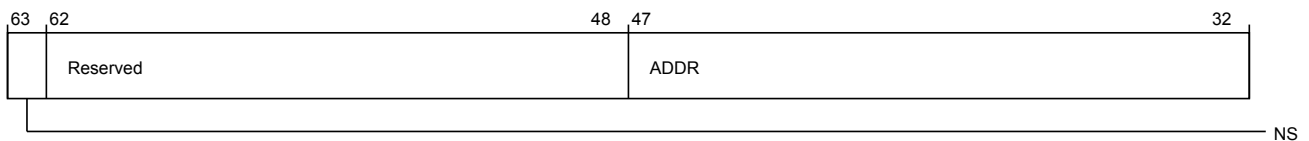


Figure 4-1116 por_cxg_ha_por_cxg_ha_erraddr_ns (high)

The following table shows the por_cxg_ha_erraddr_NS higher register bit assignments.

Table 4-1133 por_cxg_ha_por_cxg_ha_erraddr_ns (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_cxg_ha_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

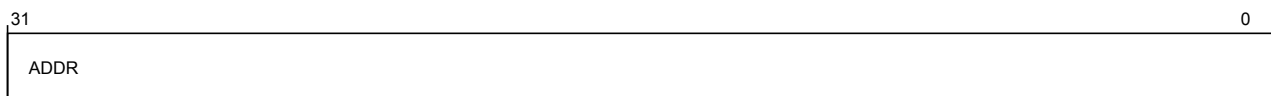


Figure 4-1117 por_cxg_ha_por_cxg_ha_erraddr_ns (low)

The following table shows the por_cxg_ha_erraddr_NS lower register bit assignments.

Table 4-1134 por_cxg_ha_por_cxg_ha_erraddr_ns (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_cxg_ha_errmisc_NS

Functions as the non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3120

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

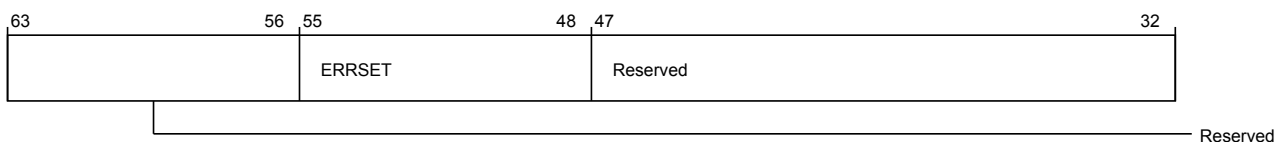


Figure 4-1118 por_cxg_ha_por_cxg_ha_errmisc_ns (high)

The following table shows the por_cxg_ha_errmisc_NS higher register bit assignments.

Table 4-1135 por_cxg_ha_por_cxg_ha_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63:56	Reserved	Reserved	RO	-
55:48	ERRSET	RAM entry set address for parity error	RW	8'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

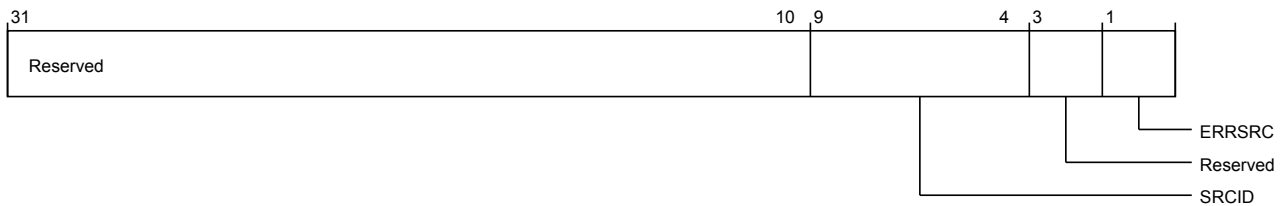


Figure 4-1119 por_cxg_ha_por_cxg_ha_errmisc_ns (low)

The following table shows the por_cxg_ha_errmisc_NS lower register bit assignments.

Table 4-1136 por_cxg_ha_por_cxg_ha_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31:10	Reserved	Reserved	RO	-
9:4	SRCID	CCIX RAID of the requestor or the snoop target	RW	6'b0
3:2	Reserved	Reserved	RO	-
1:0	ERRSRC	Source of the parity error 2'b00: Read data buffer 0 2'b01: Read data buffer 1 2'b10: Write data buffer 0 2'b11: Write data buffer 1	RW	2'b00

4.3.12 CXRA configuration registers

This section lists the CXRA configuration registers.

por_cxg_ra_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

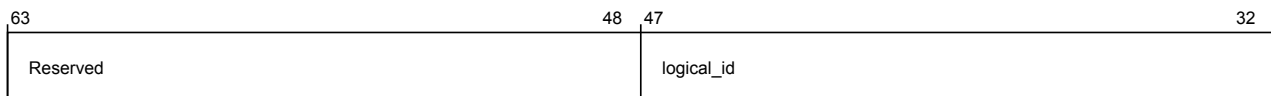


Figure 4-1120 por_cxg_ra_por_cxg_ra_node_info (high)

The following table shows the por_cxg_ra_node_info higher register bit assignments.

Table 4-1137 por_cxg_ra_por_cxg_ra_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

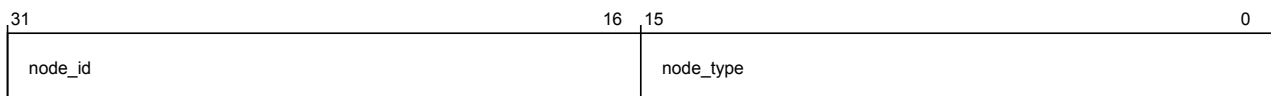


Figure 4-1121 por_cxg_ra_por_cxg_ra_node_info (low)

The following table shows the por_cxg_ra_node_info lower register bit assignments.

Table 4-1138 por_cxg_ra_por_cxg_ra_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0100

por_cxg_ra_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

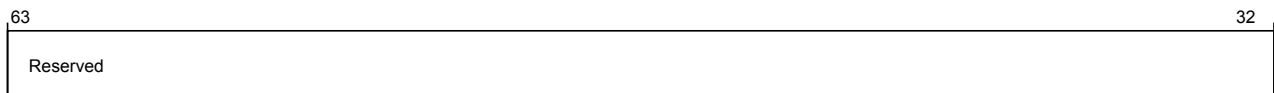


Figure 4-1122 por_cxg_ra_por_cxg_ra_child_info (high)

The following table shows the por_cxg_ra_child_info higher register bit assignments.

Table 4-1139 por_cxg_ra_por_cxg_ra_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

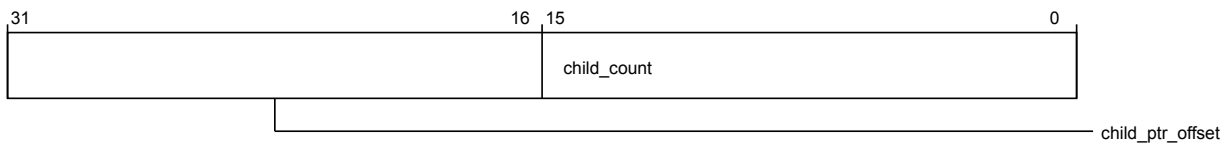


Figure 4-1123 por_cxg_ra_por_cxg_ra_child_info (low)

The following table shows the por_cxg_ra_child_info lower register bit assignments.

Table 4-1140 por_cxg_ra_por_cxg_ra_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

por_cxg_ra_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type	RW
Register width (Bits)	64

Address offset	14'h980
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

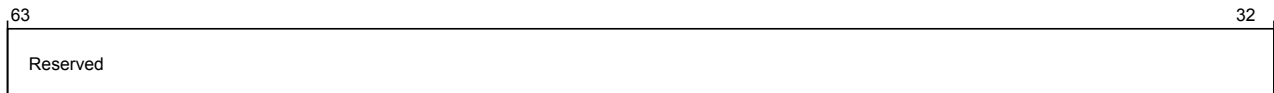


Figure 4-1124 por_cxg_ra_por_cxg_ra_secure_register_groups_override (high)

The following table shows the por_cxg_ra_secure_register_groups_override higher register bit assignments.

Table 4-1141 por_cxg_ra_por_cxg_ra_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

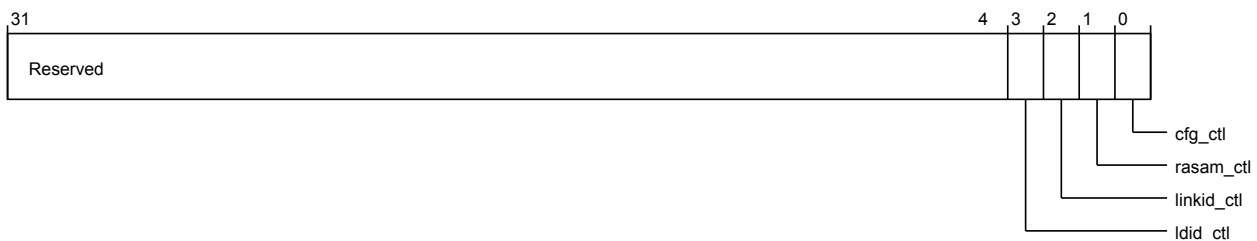


Figure 4-1125 por_cxg_ra_por_cxg_ra_secure_register_groups_override (low)

The following table shows the por_cxg_ra_secure_register_groups_override lower register bit assignments.

Table 4-1142 por_cxg_ra_por_cxg_ra_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	ldid_ctl	Allows non-secure access to secure RA LDID registers	RW	1'b0
2	linkid_ctl	Allows non-secure access to secure RA Link ID registers	RW	1'b0
1	rasam_ctl	Allows non-secure access to secure RA SAM control registers	RW	1'b0
0	cfg_ctl	Allows non-secure access to secure configuration control register	RW	1'b0

por_cxg_ra_unit_info

Provides component identification information for CXRA.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h900
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

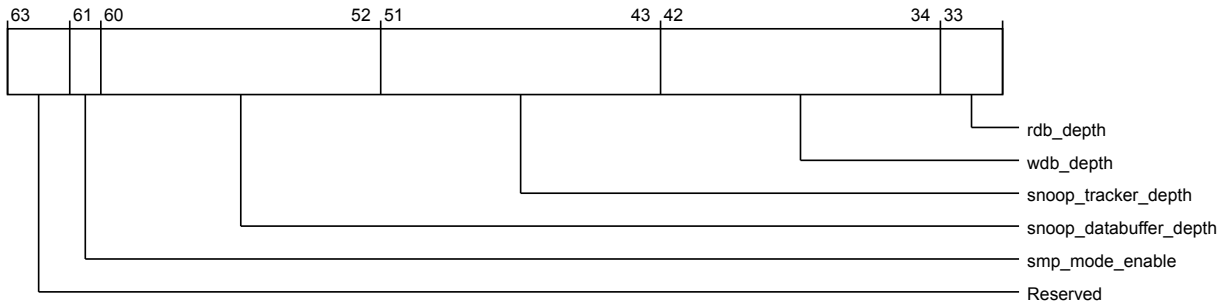


Figure 4-1126 por_cxg_ra_por_cxg_ra_unit_info (high)

The following table shows the por_cxg_ra_unit_info higher register bit assignments.

Table 4-1143 por_cxg_ra_por_cxg_ra_unit_info (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61	smp_mode_enable	SMP Mode Enable	RO	Configuration dependent
60:52	snoop_databuffer_depth	Depth of Snoop Data Buffer - number of outstanding SNP requests on CHI	RO	Configuration dependent
51:43	snoop_tracker_depth	Depth of Snoop Tracker - number of outstanding SNP requests on CCIX	RO	Configuration dependent
42:34	wdb_depth	Depth of Write Data Buffer	RO	Configuration dependent
33:32	rdb_depth	Depth of Read Data Buffer	RO	Configuration dependent

The following image shows the lower register bit assignments.

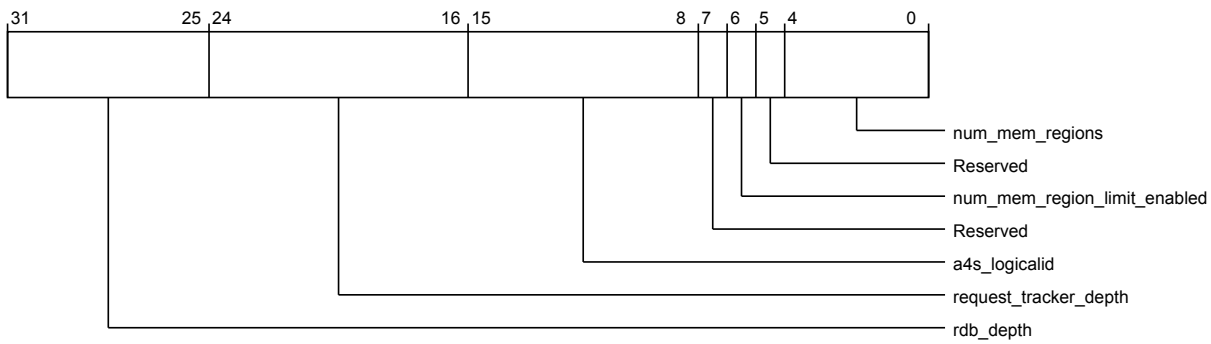


Figure 4-1127 por_cxg_ra_por_cxg_ra_unit_info (low)

The following table shows the por_cxg_ra_unit_info lower register bit assignments.

Table 4-1144 por_cxg_ra_por_cxg_ra_unit_info (low)

Bits	Field name	Description	Type	Reset
31:25	rdb_depth	Depth of Read Data Buffer	RO	Configuration dependent
24:16	request_tracker_depth	Depth of Request Tracker - number of outstanding Memory requests on CCIX	RO	Configuration dependent
15:8	a4s_logicalid	AXI4Stream interfaces logical ID	RO	Configuration dependent
7	Reserved	Reserved	RO	-
6	num_mem_region_limit_enabled	Memory region limiting enabled	RO	Configuration dependent
5	Reserved	Reserved	RO	-
4:0	num_mem_regions	Number of memory regions supported	RO	Configuration dependent

por_cxg_ra_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA00

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_cxg_ra_secure_register_groups_override.cfg_ctl

The following image shows the higher register bit assignments.

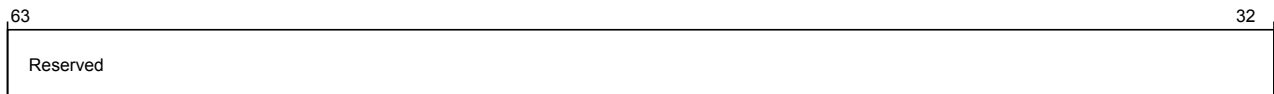


Figure 4-1128 por_cxg_ra_por_cxg_ra_cfg_ctl (high)

The following table shows the por_cxg_ra_cfg_ctl higher register bit assignments.

Table 4-1145 por_cxg_ra_por_cxg_ra_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

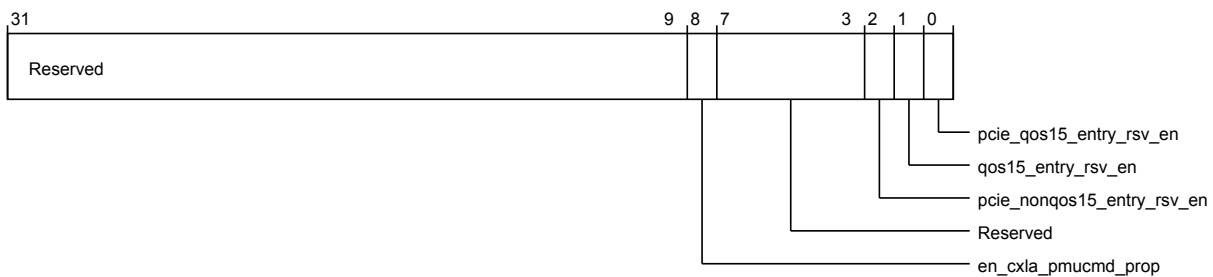


Figure 4-1129 por_cxg_ra_por_cxg_ra_cfg_ctl (low)

The following table shows the por_cxg_ra_cfg_ctl lower register bit assignments.

Table 4-1146 por_cxg_ra_por_cxg_ra_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	en_cxla_pmucmd_prop	When set, enables the propagation of PMU commands to CXLA NOTE: By default, CXLA PMU command propagation is disabled.	RW	1'b0
7:3	Reserved	Reserved	RO	-
2	pcie_nonqos15_entry_rsv_en	Enables entry reservation for non QoS15 traffic from PCIe RN-I/RN-D 1'b1: Reserves tracker entry for non QoS15 requests from PCIe RN-I/RN-D 1'b0: Does not reserve tracker entry for non QoS15 requests from PCIe RN-I/RN-D	RW	Configuration dependent

Table 4-1146 por_cxg_ra_por_cxg_ra_cfg_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
1	qos15_entry_rsv_en	Enables entry reservation for QoS15 traffic 1'b1: Reserves tracker entry for QoS15 requests 1'b0: Does not reserve tracker entry for QoS15 requests	RW	1'b1
0	pcie_qos15_entry_rsv_en	Enables entry reservation for QoS15 traffic from PCIe RN-I/RN-D 1'b1: Reserves tracker entry for QoS15 requests from PCIe RN-I/RN-D 1'b0: Does not reserve tracker entry for QoS15 requests from PCIe RN-I/RN-D	RW	Configuration dependent

por_cxg_ra_aux_ctl

Functions as the auxiliary control register for CXRA.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset 64'b0000000110

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

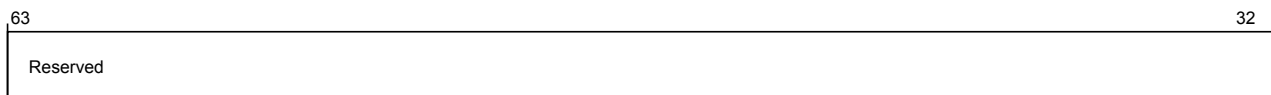


Figure 4-1130 por_cxg_ra_por_cxg_ra_aux_ctl (high)

The following table shows the por_cxg_ra_aux_ctl higher register bit assignments.

Table 4-1147 por_cxg_ra_por_cxg_ra_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

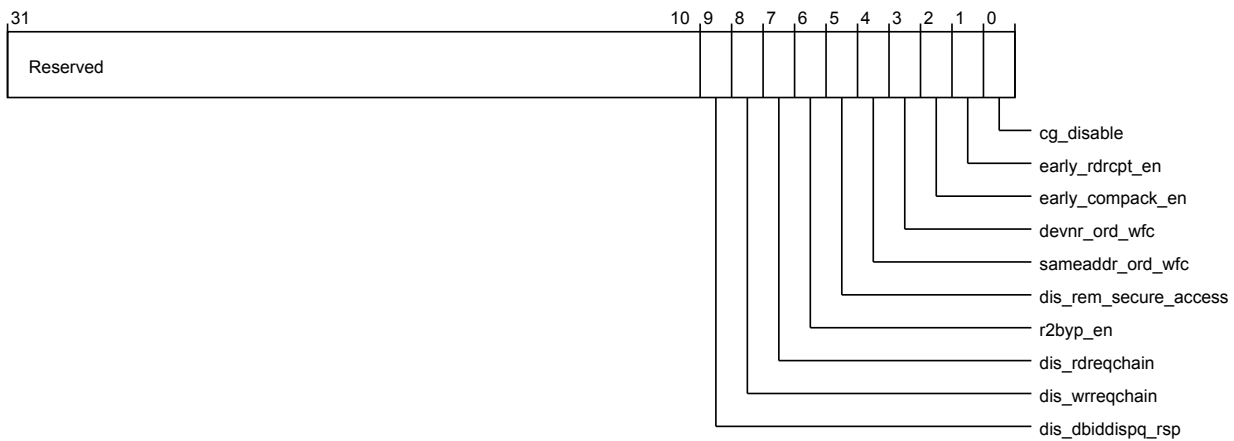


Figure 4-1131 `por_cxg_ra_por_cxg_ra_aux_ctl (low)`

The following table shows the `por_cxg_ra_aux_ctl` lower register bit assignments.

Table 4-1148 `por_cxg_ra_por_cxg_ra_aux_ctl (low)`

Bits	Field name	Description	Type	Reset
31:10	Reserved	Reserved	RO	-
9	<code>dis_dbiddispq_rsp</code>	When set, disables the dispatch of DBID responses from a separate DispatchQ.	RW	1'b0
8	<code>dis_wrreqchain</code>	When set, disables chaining of write requests.	RW	1'b0
7	<code>dis_rdreqchain</code>	When set, disables chaining of read and dataless requests.	RW	1'b0
6	<code>r2byp_en</code>	When set, enables request bypass. Applies to read and dataless requests only. Note: When set will affect the capability to chain a request on the TX side	RW	1'b0
5	<code>dis_rem_secure_access</code>	When set, treats all the incoming snoops as non-secure and forces the NS bit to 1	RW	1'b0
4	<code>sameaddr_ord_wfc</code>	When set, enables waiting for completion (COMP) before dispatching next same Addr dependent transaction (TXN)	RW	1'b0
3	<code>devnr_ord_wfc</code>	When set, enables waiting for completion (COMP) before dispatching next Device-nR dependent transaction (TXN)	RW	1'b0
2	<code>early_compack_en</code>	Early CompAck enable; enables sending early CompAck on CCIX for requests that require CompAck	RW	1'b1
1	<code>early_rdrpt_en</code>	Early ReadReceipt enable; enables sending early ReadReceipt for ordered read requests	RW	1'b1
0	<code>cg_disable</code>	Disables clock gating when set	RW	1'b0

`por_cxg_ra_sam_addr_region_reg0`

Configures Address Region 0 for RA SAM.

Its characteristics are:

Type RW

Register width (Bits) 64
Address offset 14'hDA8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

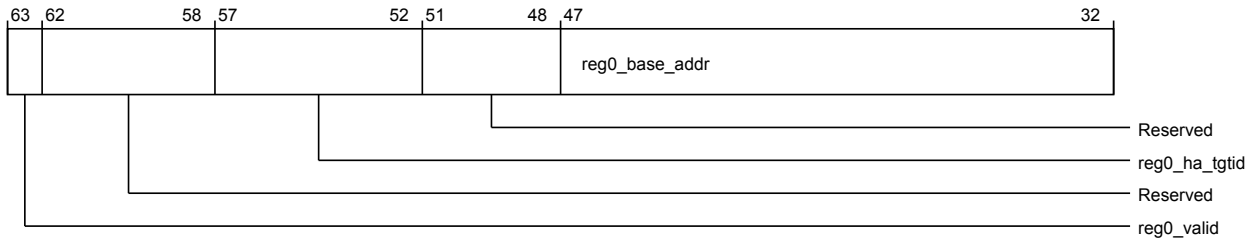


Figure 4-1132 por_cxg_ra_por_cxg_ra_sam_addr_region_reg0 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg0 higher register bit assignments.

Table 4-1149 por_cxg_ra_por_cxg_ra_sam_addr_region_reg0 (high)

Bits	Field name	Description	Type	Reset
63	reg0_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg0_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg0_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

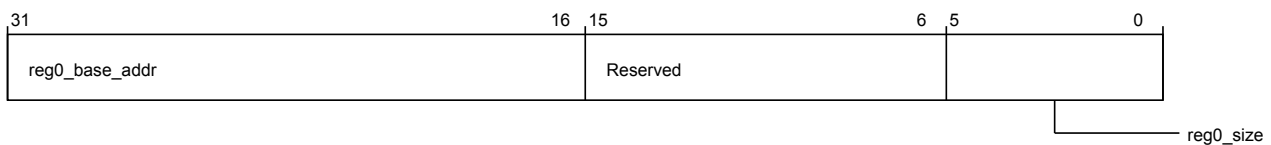


Figure 4-1133 por_cxg_ra_por_cxg_ra_sam_addr_region_reg0 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg0 lower register bit assignments.

Table 4-1150 `por_cxg_ra_por_cxg_ra_sam_addr_region_reg0` (low)

Bits	Field name	Description	Type	Reset
31:16	<code>reg0_base_addr</code>	Specifies the 2 ⁿ -aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	<code>reg0_size</code>	Specifies the size of the memory region	RW	1'b0

`por_cxg_ra_sam_addr_region_reg1`

Configures Address Region 1 for RA SAM.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDB0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.rasam_ctl</code>

The following image shows the higher register bit assignments.

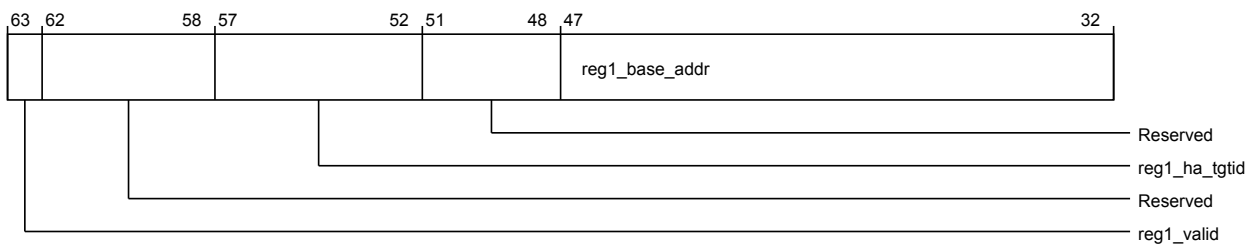


Figure 4-1134 `por_cxg_ra_por_cxg_ra_sam_addr_region_reg1` (high)

The following table shows the `por_cxg_ra_sam_addr_region_reg1` higher register bit assignments.

Table 4-1151 `por_cxg_ra_por_cxg_ra_sam_addr_region_reg1` (high)

Bits	Field name	Description	Type	Reset
63	<code>reg1_valid</code>	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	<code>reg1_ha_tgtid</code>	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	<code>reg1_base_addr</code>	Specifies the 2 ⁿ -aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

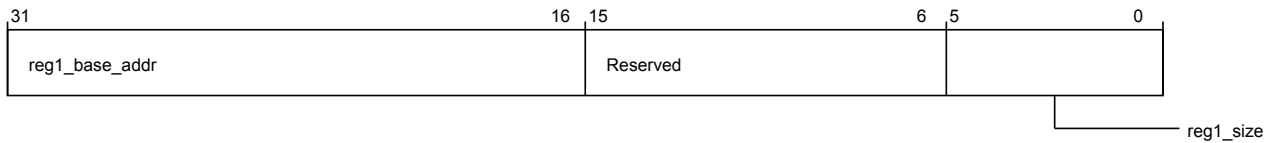


Figure 4-1135 `por_cxg_ra_por_cxg_ra_sam_addr_region_reg1` (low)

The following table shows the `por_cxg_ra_sam_addr_region_reg1` lower register bit assignments.

Table 4-1152 `por_cxg_ra_por_cxg_ra_sam_addr_region_reg1` (low)

Bits	Field name	Description	Type	Reset
31:16	reg1_base_addr	Specifies the 2 ⁿ -aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg1_size	Specifies the size of the memory region	RW	1'b0

`por_cxg_ra_sam_addr_region_reg2`

Configures Address Region 2 for RA SAM.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDB8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.rasam_ctl</code>

The following image shows the higher register bit assignments.

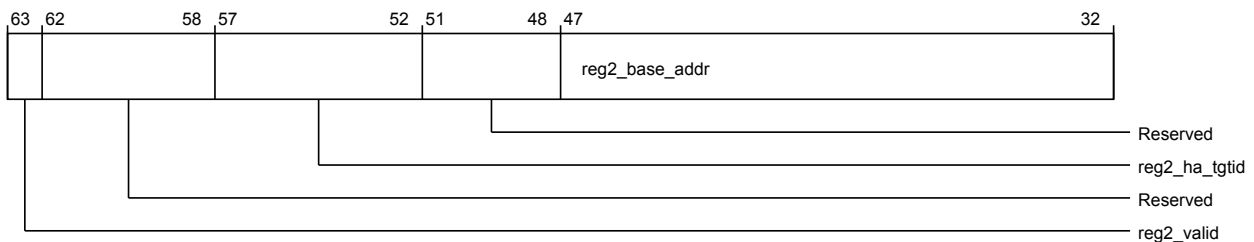


Figure 4-1136 `por_cxg_ra_por_cxg_ra_sam_addr_region_reg2` (high)

The following table shows the `por_cxg_ra_sam_addr_region_reg2` higher register bit assignments.

Table 4-1153 por_cxg_ra_por_cxg_ra_sam_addr_region_reg2 (high)

Bits	Field name	Description	Type	Reset
63	reg2_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg2_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg2_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

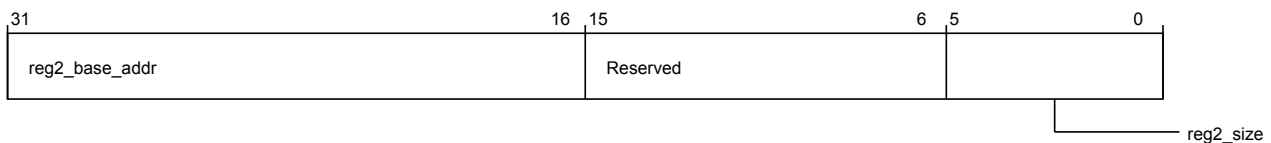


Figure 4-1137 por_cxg_ra_por_cxg_ra_sam_addr_region_reg2 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg2 lower register bit assignments.

Table 4-1154 por_cxg_ra_por_cxg_ra_sam_addr_region_reg2 (low)

Bits	Field name	Description	Type	Reset
31:16	reg2_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg2_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg3

Configures Address Region 3 for RA SAM.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDC0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

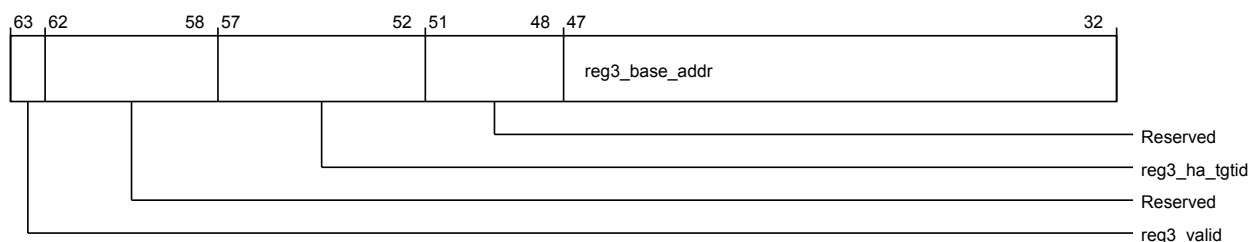


Figure 4-1138 por_cxg_ra_por_cxg_ra_sam_addr_region_reg3 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg3 higher register bit assignments.

Table 4-1155 por_cxg_ra_por_cxg_ra_sam_addr_region_reg3 (high)

Bits	Field name	Description	Type	Reset
63	reg3_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg3_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg3_base_addr	Specifies the 2 ⁿ -aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

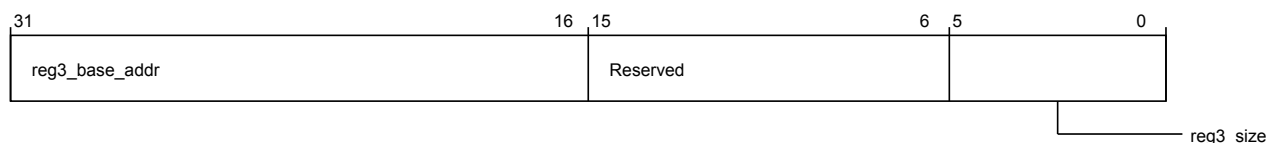


Figure 4-1139 por_cxg_ra_por_cxg_ra_sam_addr_region_reg3 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg3 lower register bit assignments.

Table 4-1156 por_cxg_ra_por_cxg_ra_sam_addr_region_reg3 (low)

Bits	Field name	Description	Type	Reset
31:16	reg3_base_addr	Specifies the 2 ⁿ -aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg3_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg4

Configures Address Region 4 for RA SAM.

Its characteristics are:

Type RW

Register width (Bits) 64
Address offset 14'hDC8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

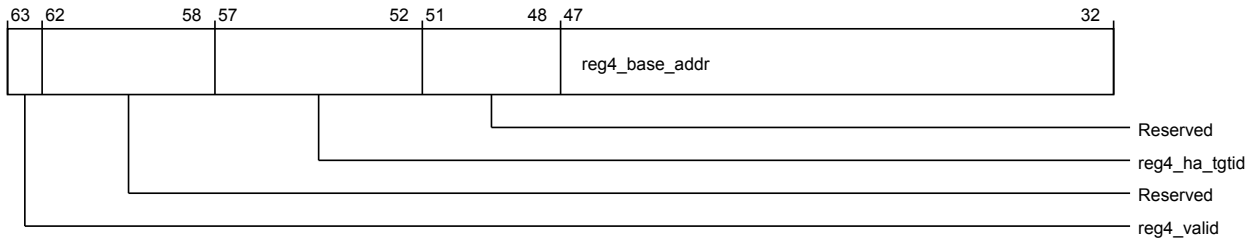


Figure 4-1140 por_cxg_ra_por_cxg_ra_sam_addr_region_reg4 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg4 higher register bit assignments.

Table 4-1157 por_cxg_ra_por_cxg_ra_sam_addr_region_reg4 (high)

Bits	Field name	Description	Type	Reset
63	reg4_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg4_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg4_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

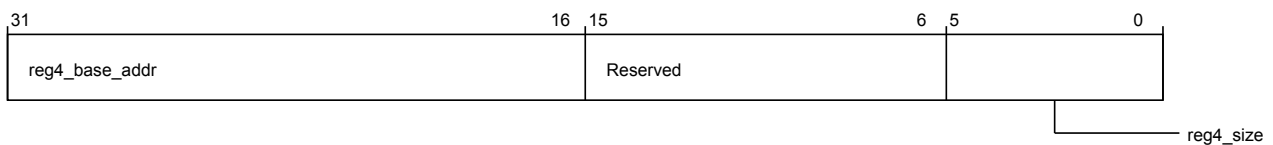


Figure 4-1141 por_cxg_ra_por_cxg_ra_sam_addr_region_reg4 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg4 lower register bit assignments.

Table 4-1158 `por_cxg_ra_por_cxg_ra_sam_addr_region_reg4` (low)

Bits	Field name	Description	Type	Reset
31:16	<code>reg4_base_addr</code>	Specifies the 2 ⁿ -aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	<code>reg4_size</code>	Specifies the size of the memory region	RW	1'b0

`por_cxg_ra_sam_addr_region_reg5`

Configures Address Region 5 for RA SAM.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDD0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.rasam_ctl</code>

The following image shows the higher register bit assignments.

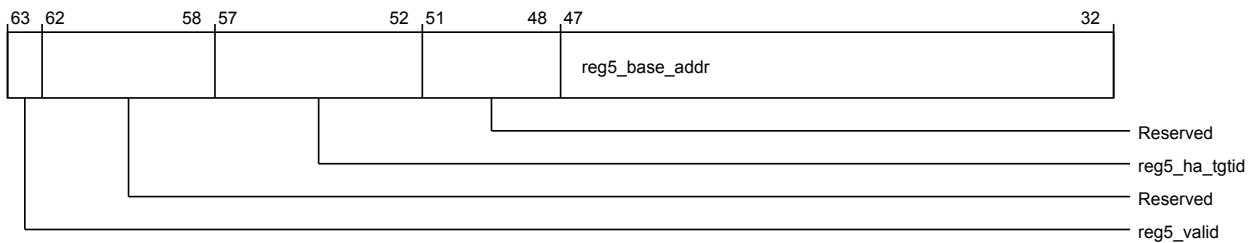


Figure 4-1142 `por_cxg_ra_por_cxg_ra_sam_addr_region_reg5` (high)

The following table shows the `por_cxg_ra_sam_addr_region_reg5` higher register bit assignments.

Table 4-1159 `por_cxg_ra_por_cxg_ra_sam_addr_region_reg5` (high)

Bits	Field name	Description	Type	Reset
63	<code>reg5_valid</code>	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	<code>reg5_ha_tgtid</code>	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	<code>reg5_base_addr</code>	Specifies the 2 ⁿ -aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

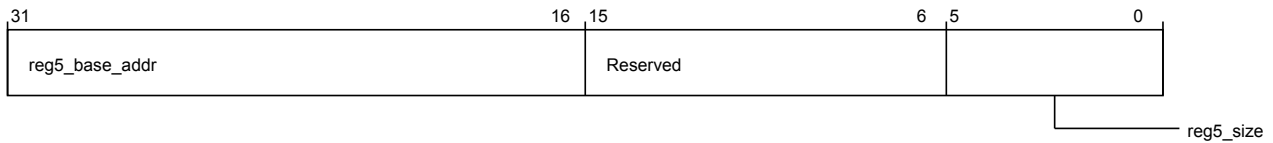


Figure 4-1143 por_cxg_ra_por_cxg_ra_sam_addr_region_reg5 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg5 lower register bit assignments.

Table 4-1160 por_cxg_ra_por_cxg_ra_sam_addr_region_reg5 (low)

Bits	Field name	Description	Type	Reset
31:16	reg5_base_addr	Specifies the 2 ⁿ -aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg5_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg6

Configures Address Region 6 for RA SAM.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDD8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

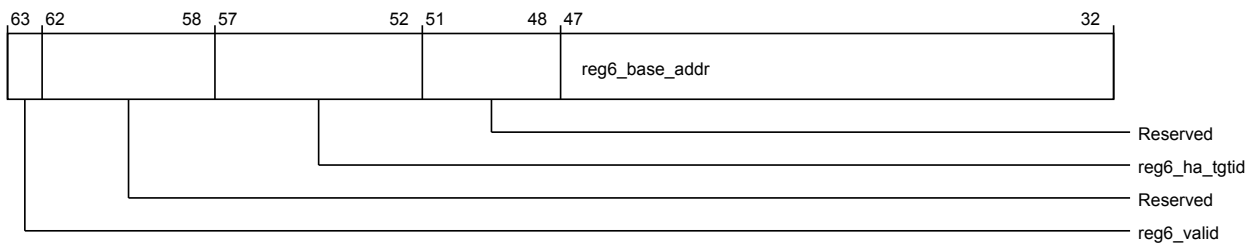


Figure 4-1144 por_cxg_ra_por_cxg_ra_sam_addr_region_reg6 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg6 higher register bit assignments.

Table 4-1161 por_cxg_ra_por_cxg_ra_sam_addr_region_reg6 (high)

Bits	Field name	Description	Type	Reset
63	reg6_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg6_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg6_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

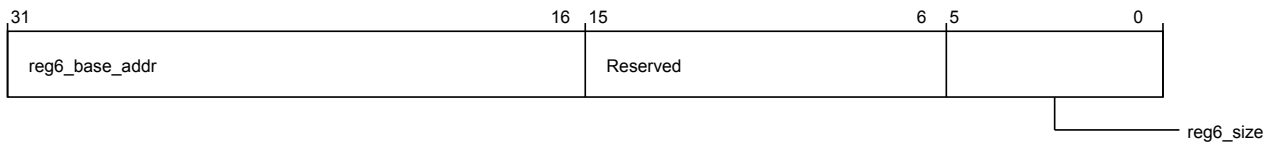


Figure 4-1145 por_cxg_ra_por_cxg_ra_sam_addr_region_reg6 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg6 lower register bit assignments.

Table 4-1162 por_cxg_ra_por_cxg_ra_sam_addr_region_reg6 (low)

Bits	Field name	Description	Type	Reset
31:16	reg6_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg6_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg7

Configures Address Region 7 for RA SAM.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hDE0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

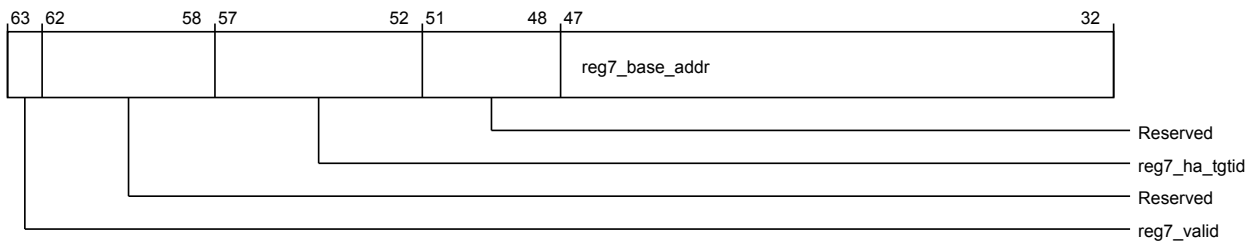


Figure 4-1146 por_cxg_ra_por_cxg_ra_sam_addr_region_reg7 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg7 higher register bit assignments.

Table 4-1163 por_cxg_ra_por_cxg_ra_sam_addr_region_reg7 (high)

Bits	Field name	Description	Type	Reset
63	reg7_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg7_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg7_base_addr	Specifies the 2 ⁿ -aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

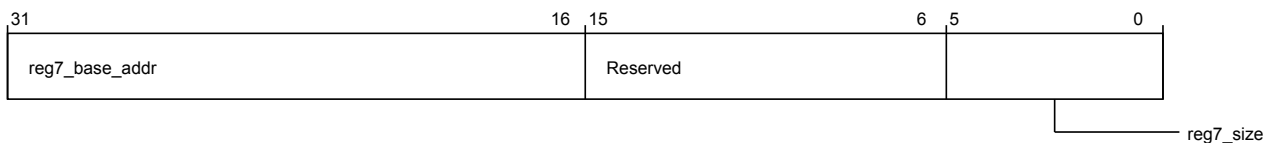


Figure 4-1147 por_cxg_ra_por_cxg_ra_sam_addr_region_reg7 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg7 lower register bit assignments.

Table 4-1164 por_cxg_ra_por_cxg_ra_sam_addr_region_reg7 (low)

Bits	Field name	Description	Type	Reset
31:16	reg7_base_addr	Specifies the 2 ⁿ -aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg7_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_mem_region0_limit_reg

Specifies the memory region 0 limit address.

Its characteristics are:

Type RW

Register width (Bits) 64
Address offset 14'hE00
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

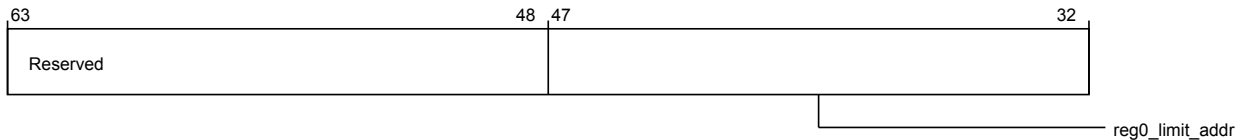


Figure 4-1148 por_cxg_ra_por_cxg_ra_sam_mem_region0_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region0_limit_reg higher register bit assignments.

Table 4-1165 por_cxg_ra_por_cxg_ra_sam_mem_region0_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg0_limit_addr	Memory region 0 limit address	RW	32'h0

The following image shows the lower register bit assignments.

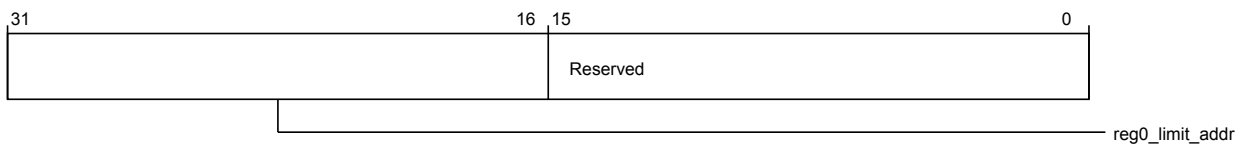


Figure 4-1149 por_cxg_ra_por_cxg_ra_sam_mem_region0_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region0_limit_reg lower register bit assignments.

Table 4-1166 por_cxg_ra_por_cxg_ra_sam_mem_region0_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg0_limit_addr	Memory region 0 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region1_limit_reg

Specifies the memory region 1 limit address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE08

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

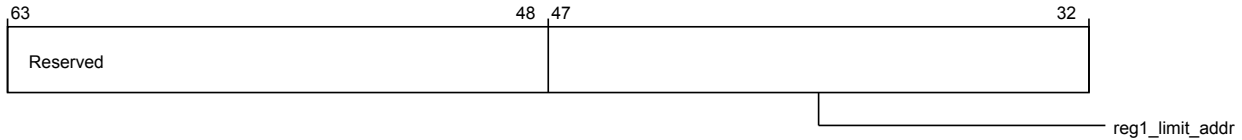


Figure 4-1150 por_cxg_ra_por_cxg_ra_sam_mem_region1_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region1_limit_reg higher register bit assignments.

Table 4-1167 por_cxg_ra_por_cxg_ra_sam_mem_region1_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg1_limit_addr	Memory region 1 limit address	RW	32'h0

The following image shows the lower register bit assignments.

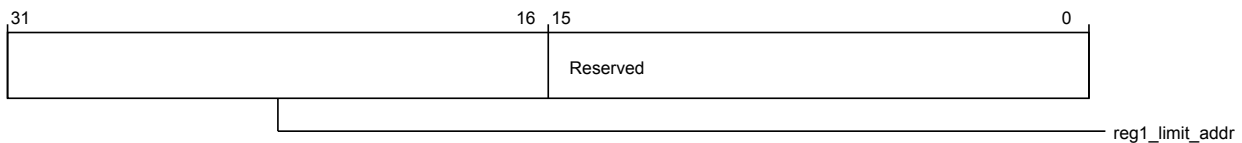


Figure 4-1151 por_cxg_ra_por_cxg_ra_sam_mem_region1_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region1_limit_reg lower register bit assignments.

Table 4-1168 por_cxg_ra_por_cxg_ra_sam_mem_region1_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg1_limit_addr	Memory region 1 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region2_limit_reg

Specifies the memory region 2 limit address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE10

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override `por_cxg_ra_secure_register_groups_override.rasam_ctl`

The following image shows the higher register bit assignments.

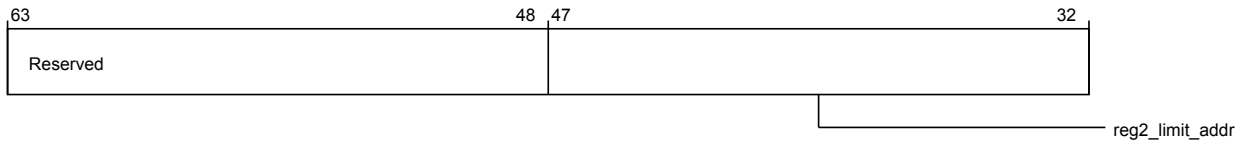


Figure 4-1152 `por_cxg_ra_por_cxg_ra_sam_mem_region2_limit_reg` (high)

The following table shows the `por_cxg_ra_sam_mem_region2_limit_reg` higher register bit assignments.

Table 4-1169 `por_cxg_ra_por_cxg_ra_sam_mem_region2_limit_reg` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg2_limit_addr	Memory region 2 limit address	RW	32'h0

The following image shows the lower register bit assignments.

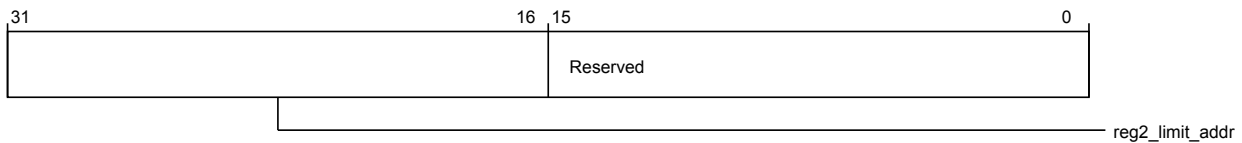


Figure 4-1153 `por_cxg_ra_por_cxg_ra_sam_mem_region2_limit_reg` (low)

The following table shows the `por_cxg_ra_sam_mem_region2_limit_reg` lower register bit assignments.

Table 4-1170 `por_cxg_ra_por_cxg_ra_sam_mem_region2_limit_reg` (low)

Bits	Field name	Description	Type	Reset
31:16	reg2_limit_addr	Memory region 2 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

`por_cxg_ra_sam_mem_region3_limit_reg`

Specifies the memory region 3 limit address.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE18
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.rasam_ctl</code>

The following image shows the higher register bit assignments.

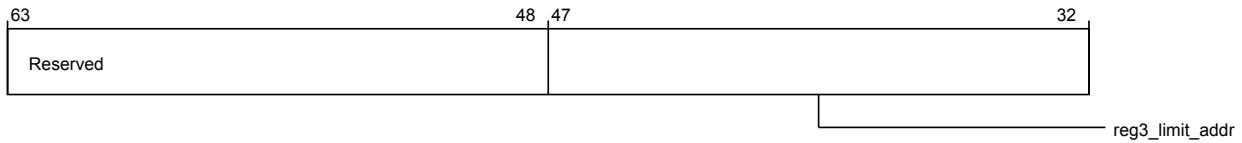


Figure 4-1154 `por_cxg_ra_por_cxg_ra_sam_mem_region3_limit_reg` (high)

The following table shows the `por_cxg_ra_sam_mem_region3_limit_reg` higher register bit assignments.

Table 4-1171 `por_cxg_ra_por_cxg_ra_sam_mem_region3_limit_reg` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>reg3_limit_addr</code>	Memory region 3 limit address	RW	32'h0

The following image shows the lower register bit assignments.

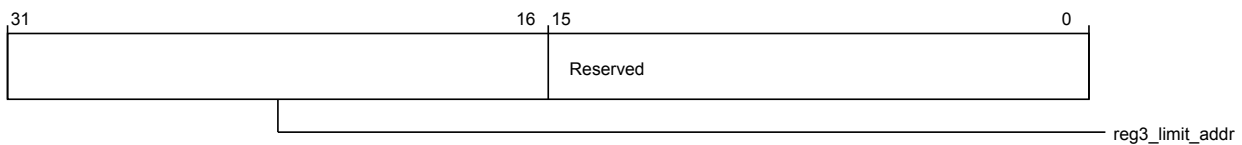


Figure 4-1155 `por_cxg_ra_por_cxg_ra_sam_mem_region3_limit_reg` (low)

The following table shows the `por_cxg_ra_sam_mem_region3_limit_reg` lower register bit assignments.

Table 4-1172 `por_cxg_ra_por_cxg_ra_sam_mem_region3_limit_reg` (low)

Bits	Field name	Description	Type	Reset
31:16	<code>reg3_limit_addr</code>	Memory region 3 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

`por_cxg_ra_sam_mem_region4_limit_reg`

Specifies the memory region 4 limit address.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE20
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.rasam_ctl</code>

The following image shows the higher register bit assignments.

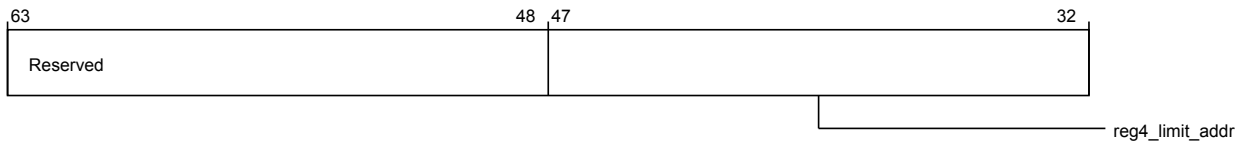


Figure 4-1156 por_cxg_ra_por_cxg_ra_sam_mem_region4_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region4_limit_reg higher register bit assignments.

Table 4-1173 por_cxg_ra_por_cxg_ra_sam_mem_region4_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg4_limit_addr	Memory region 4 limit address	RW	32'h0

The following image shows the lower register bit assignments.

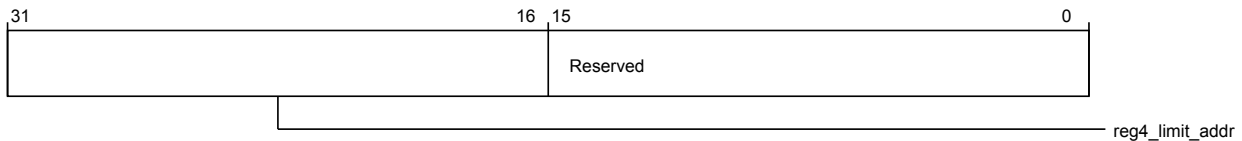


Figure 4-1157 por_cxg_ra_por_cxg_ra_sam_mem_region4_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region4_limit_reg lower register bit assignments.

Table 4-1174 por_cxg_ra_por_cxg_ra_sam_mem_region4_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg4_limit_addr	Memory region 4 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region5_limit_reg

Specifies the memory region 5 limit address.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE28
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

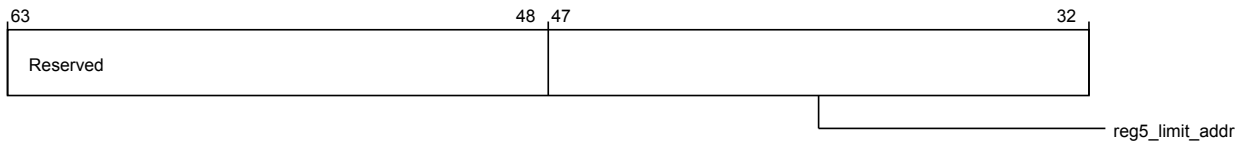


Figure 4-1158 por_cxg_ra_por_cxg_ra_sam_mem_region5_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region5_limit_reg higher register bit assignments.

Table 4-1175 por_cxg_ra_por_cxg_ra_sam_mem_region5_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg5_limit_addr	Memory region 5 limit address	RW	32'h0

The following image shows the lower register bit assignments.

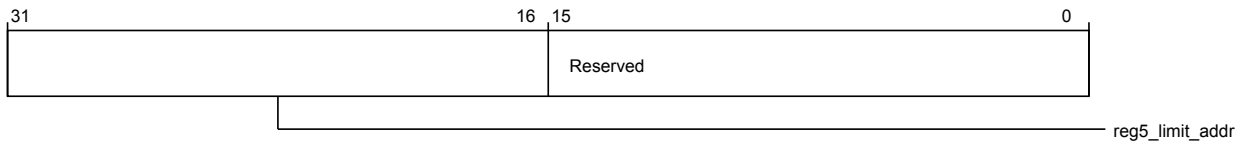


Figure 4-1159 por_cxg_ra_por_cxg_ra_sam_mem_region5_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region5_limit_reg lower register bit assignments.

Table 4-1176 por_cxg_ra_por_cxg_ra_sam_mem_region5_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg5_limit_addr	Memory region 5 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region6_limit_reg

Specifies the memory region 6 limit address.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE30
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

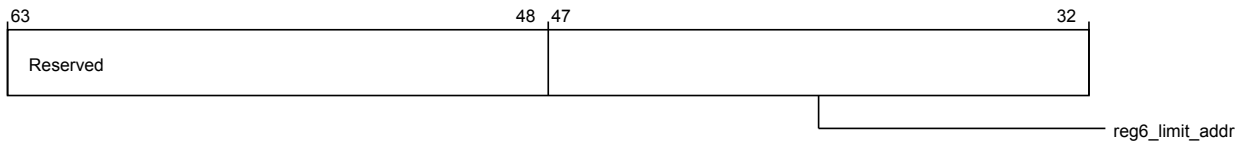


Figure 4-1160 por_cxg_ra_por_cxg_ra_sam_mem_region6_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region6_limit_reg higher register bit assignments.

Table 4-1177 por_cxg_ra_por_cxg_ra_sam_mem_region6_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg6_limit_addr	Memory region 6 limit address	RW	32'h0

The following image shows the lower register bit assignments.

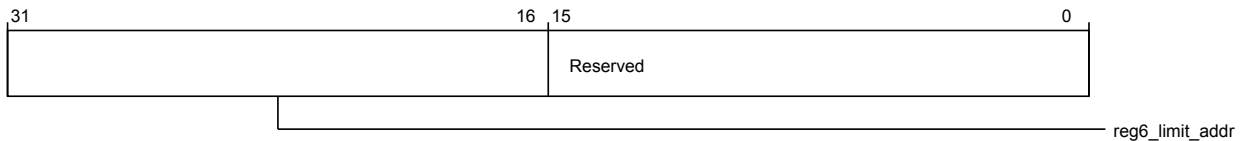


Figure 4-1161 por_cxg_ra_por_cxg_ra_sam_mem_region6_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region6_limit_reg lower register bit assignments.

Table 4-1178 por_cxg_ra_por_cxg_ra_sam_mem_region6_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg6_limit_addr	Memory region 6 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region7_limit_reg

Specifies the memory region 7 limit address.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE38
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

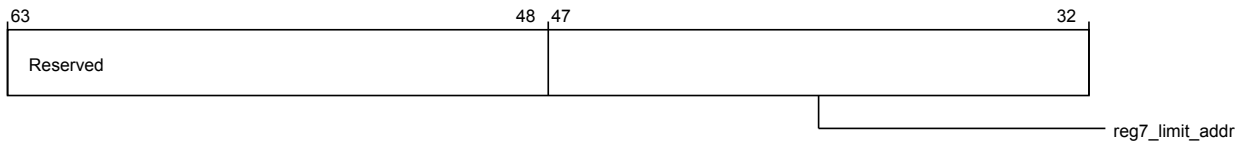


Figure 4-1162 por_cxg_ra_por_cxg_ra_sam_mem_region7_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region7_limit_reg higher register bit assignments.

Table 4-1179 por_cxg_ra_por_cxg_ra_sam_mem_region7_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg7_limit_addr	Memory region 7 limit address	RW	32'h0

The following image shows the lower register bit assignments.

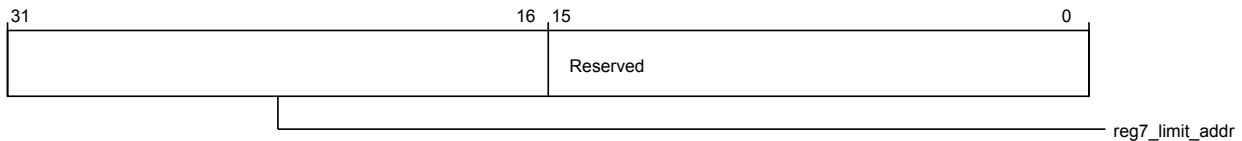


Figure 4-1163 por_cxg_ra_por_cxg_ra_sam_mem_region7_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region7_limit_reg lower register bit assignments.

Table 4-1180 por_cxg_ra_por_cxg_ra_sam_mem_region7_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg7_limit_addr	Memory region 7 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_agentid_to_linkid_reg0

Specifies the mapping of Agent ID to Link ID for Agent IDs 0 to 7.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE60
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

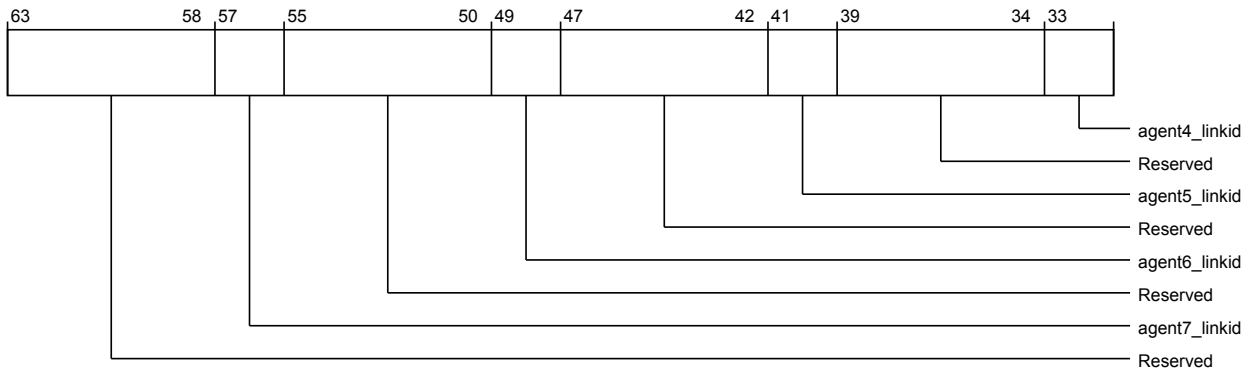


Figure 4-1164 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg0 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg0 higher register bit assignments.

Table 4-1181 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent7_linkid	Specifies the Link ID for Agent ID 7	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent6_linkid	Specifies the Link ID for Agent ID 6	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent5_linkid	Specifies the Link ID for Agent ID 5	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent4_linkid	Specifies the Link ID for Agent ID 4	RW	2'h0

The following image shows the lower register bit assignments.

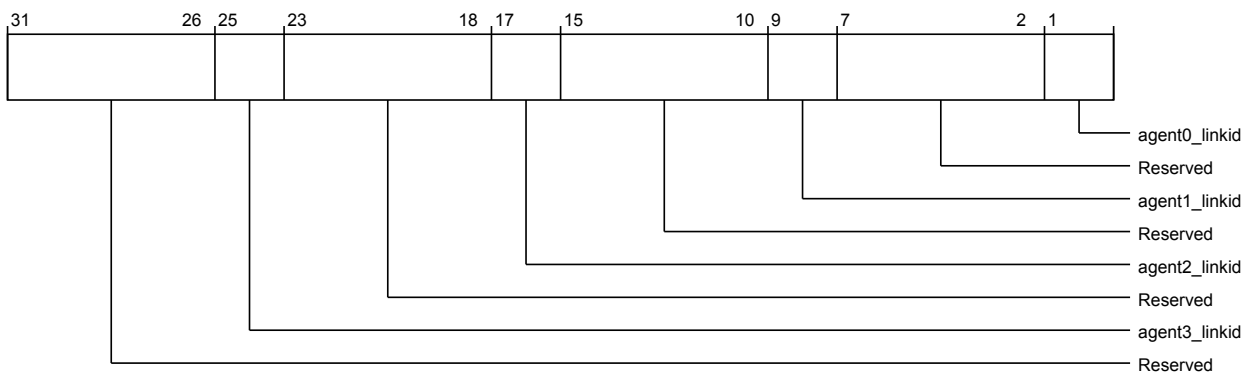


Figure 4-1165 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg0 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg0 lower register bit assignments.

Table 4-1182 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg0` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent3_linkid	Specifies the Link ID for Agent ID 3	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent2_linkid	Specifies the Link ID for Agent ID 2	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent1_linkid	Specifies the Link ID for Agent ID 1	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent0_linkid	Specifies the Link ID for Agent ID 0	RW	2'h0

`por_cxg_ra_agentid_to_linkid_reg1`

Specifies the mapping of Agent ID to Link ID for Agent IDs 8 to 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE68
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.linkid_ctl</code>

The following image shows the higher register bit assignments.

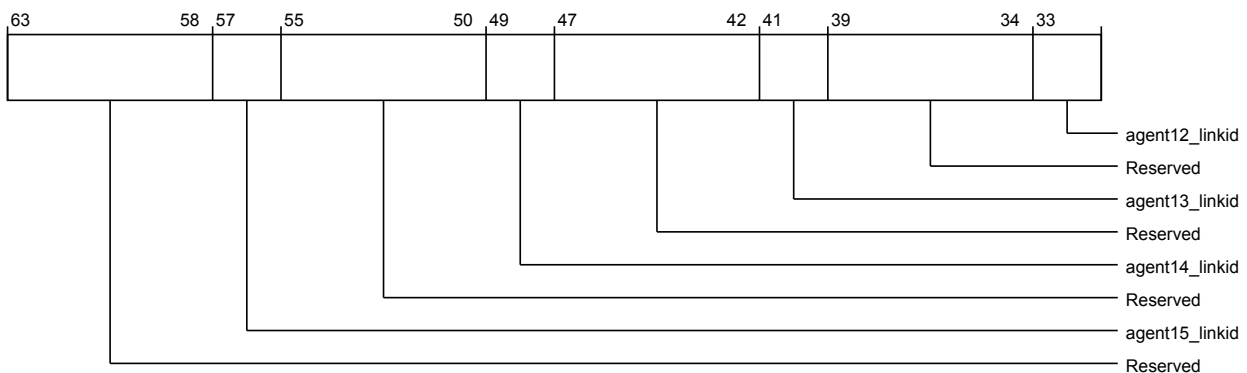


Figure 4-1166 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg1` (high)

The following table shows the `por_cxg_ra_agentid_to_linkid_reg1` higher register bit assignments.

Table 4-1183 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg1` (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent15_linkid	Specifies the Link ID for Agent ID 15	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent14_linkid	Specifies the Link ID for Agent ID 14	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent13_linkid	Specifies the Link ID for Agent ID 13	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent12_linkid	Specifies the Link ID for Agent ID 12	RW	2'h0

The following image shows the lower register bit assignments.

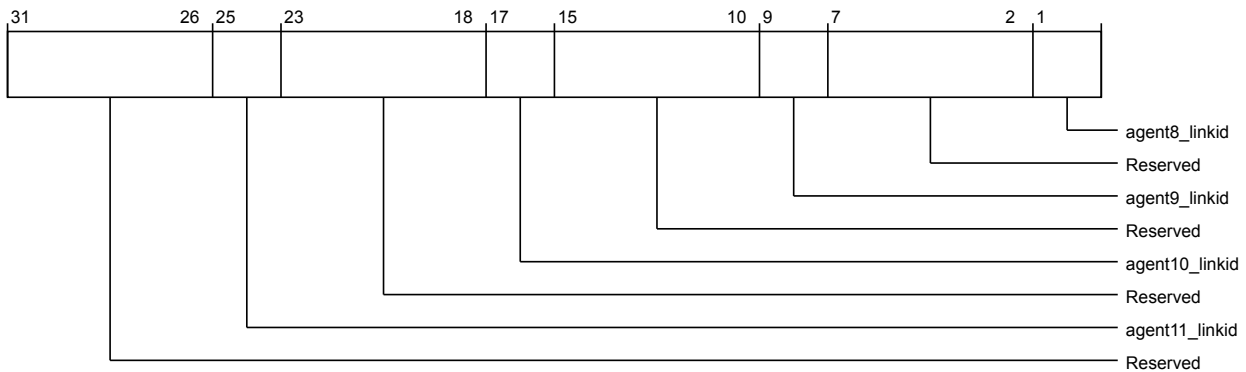


Figure 4-1167 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg1` (low)

The following table shows the `por_cxg_ra_agentid_to_linkid_reg1` lower register bit assignments.

Table 4-1184 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg1` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent11_linkid	Specifies the Link ID for Agent ID 11	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent10_linkid	Specifies the Link ID for Agent ID 10	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent9_linkid	Specifies the Link ID for Agent ID 9	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent8_linkid	Specifies the Link ID for Agent ID 8	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg2

Specifies the mapping of Agent ID to Link ID for Agent IDs 16 to 23.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE70
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

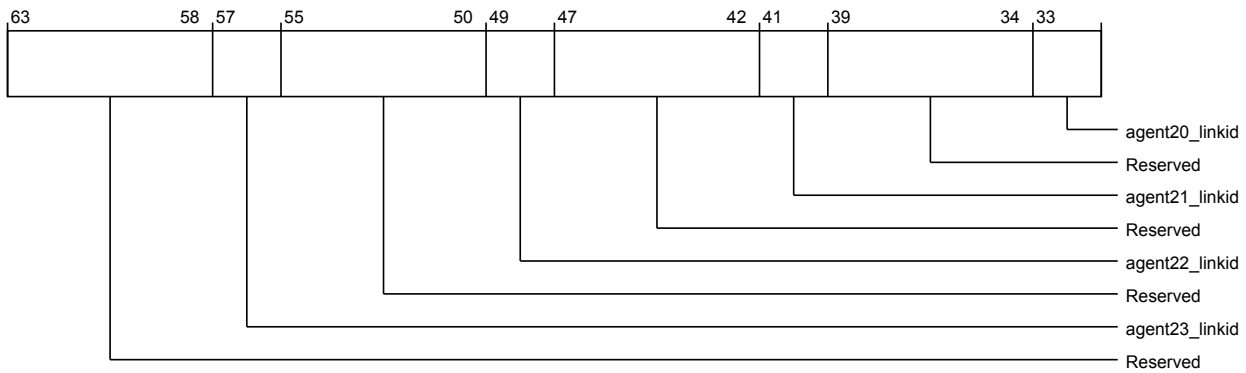


Figure 4-1168 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg2 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg2 higher register bit assignments.

Table 4-1185 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent23_linkid	Specifies the Link ID for Agent ID 23	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent22_linkid	Specifies the Link ID for Agent ID 22	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent21_linkid	Specifies the Link ID for Agent ID 21	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent20_linkid	Specifies the Link ID for Agent ID 20	RW	2'h0

The following image shows the lower register bit assignments.

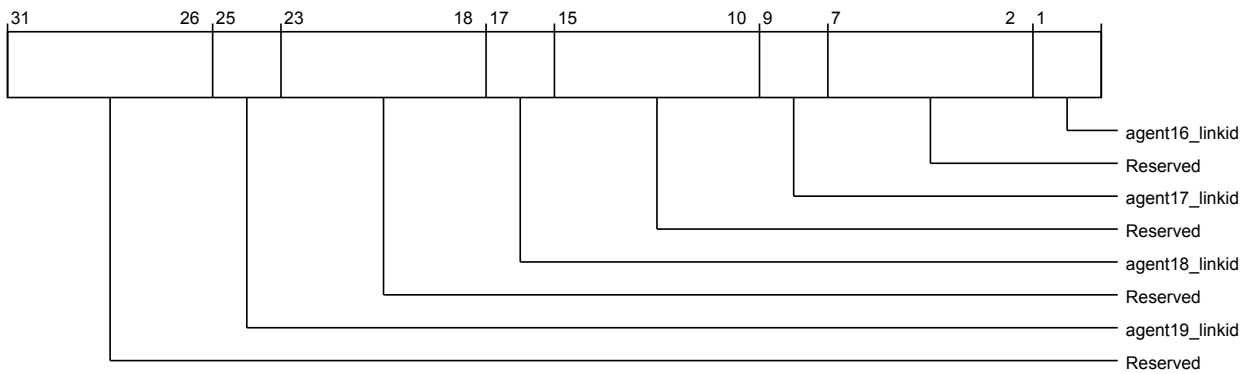


Figure 4-1169 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg2 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg2 lower register bit assignments.

Table 4-1186 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent19_linkid	Specifies the Link ID for Agent ID 19	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent18_linkid	Specifies the Link ID for Agent ID 18	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent17_linkid	Specifies the Link ID for Agent ID 17	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent16_linkid	Specifies the Link ID for Agent ID 16	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg3

Specifies the mapping of Agent ID to Link ID for Agent IDs 24 to 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE78
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

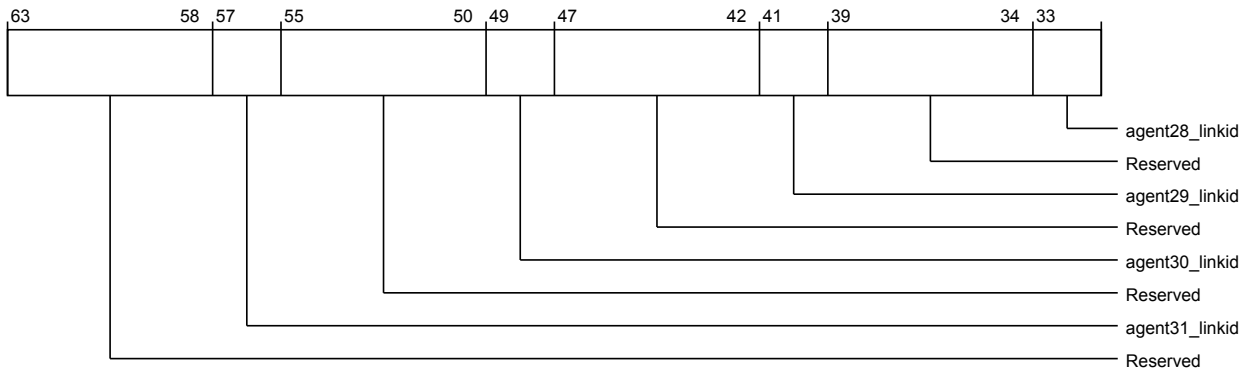


Figure 4-1170 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg3 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg3 higher register bit assignments.

Table 4-1187 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent31_linkid	Specifies the Link ID for Agent ID 31	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent30_linkid	Specifies the Link ID for Agent ID 30	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent29_linkid	Specifies the Link ID for Agent ID 29	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent28_linkid	Specifies the Link ID for Agent ID 28	RW	2'h0

The following image shows the lower register bit assignments.

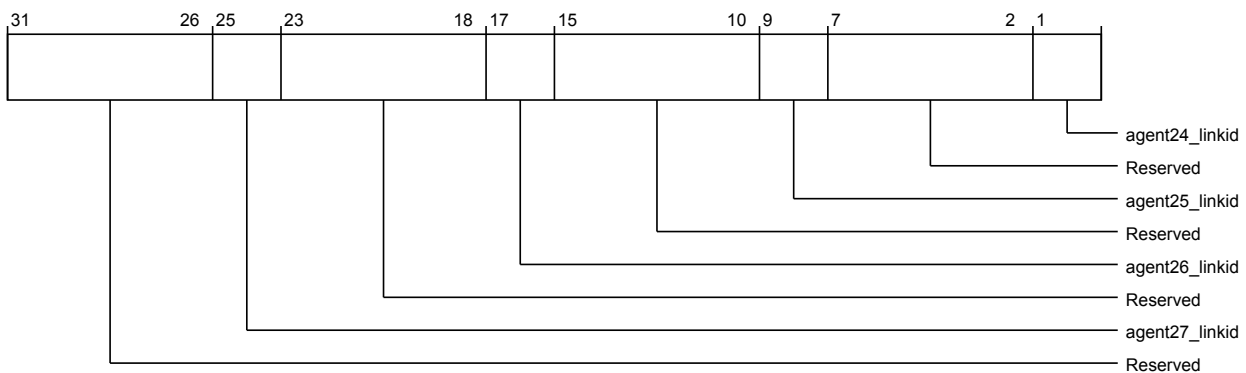


Figure 4-1171 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg3 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg3 lower register bit assignments.

Table 4-1188 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg3` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent27_linkid	Specifies the Link ID for Agent ID 27	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent26_linkid	Specifies the Link ID for Agent ID 26	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent25_linkid	Specifies the Link ID for Agent ID 25	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent24_linkid	Specifies the Link ID for Agent ID 24	RW	2'h0

`por_cxg_ra_agentid_to_linkid_reg4`

Specifies the mapping of Agent ID to Link ID for Agent IDs 32 to 39.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE80
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.linkid_ctl</code>

The following image shows the higher register bit assignments.

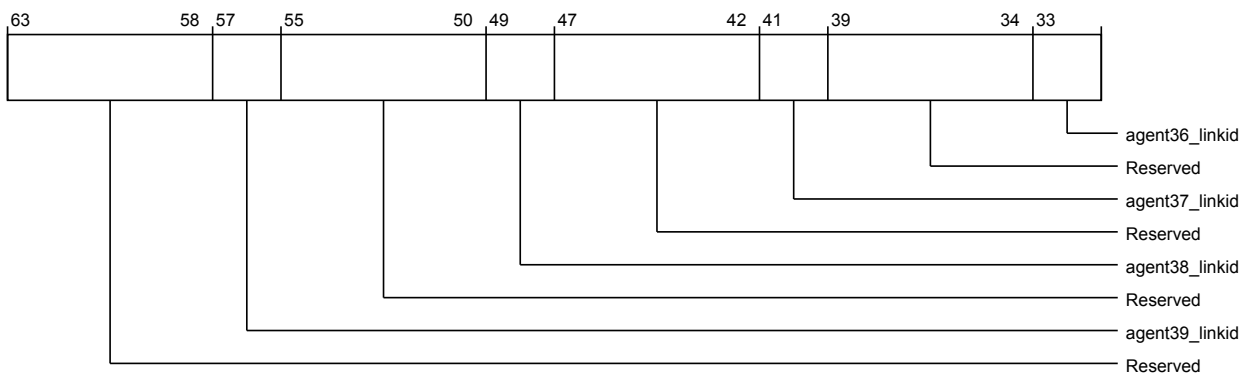


Figure 4-1172 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg4` (high)

The following table shows the `por_cxg_ra_agentid_to_linkid_reg4` higher register bit assignments.

Table 4-1189 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent39_linkid	Specifies the Link ID for Agent ID 39	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent38_linkid	Specifies the Link ID for Agent ID 38	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent37_linkid	Specifies the Link ID for Agent ID 37	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent36_linkid	Specifies the Link ID for Agent ID 36	RW	2'h0

The following image shows the lower register bit assignments.

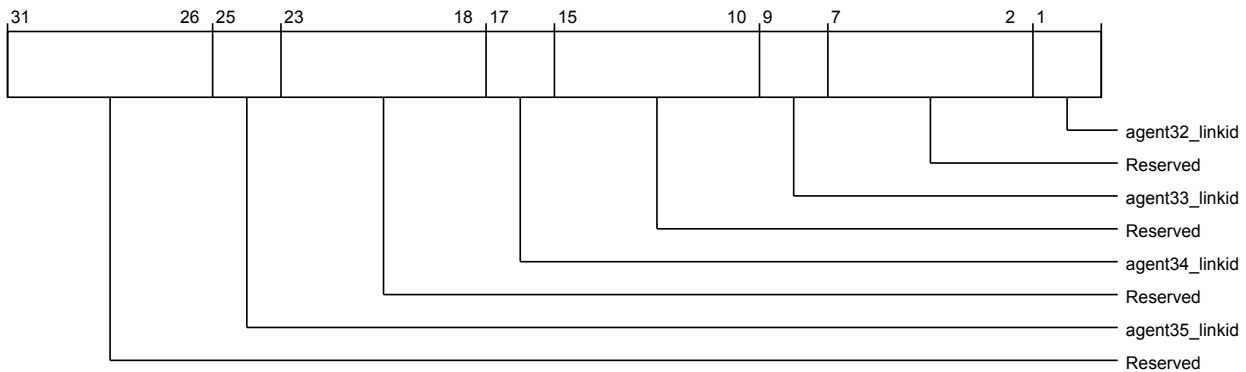


Figure 4-1173 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg4 (low)

The following table shows the `por_cxg_ra_agentid_to_linkid_reg4` lower register bit assignments.

Table 4-1190 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg4 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent35_linkid	Specifies the Link ID for Agent ID 35	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent34_linkid	Specifies the Link ID for Agent ID 34	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent33_linkid	Specifies the Link ID for Agent ID 33	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent32_linkid	Specifies the Link ID for Agent ID 32	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg5

Specifies the mapping of Agent ID to Link ID for Agent IDs 40 to 47.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE88
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

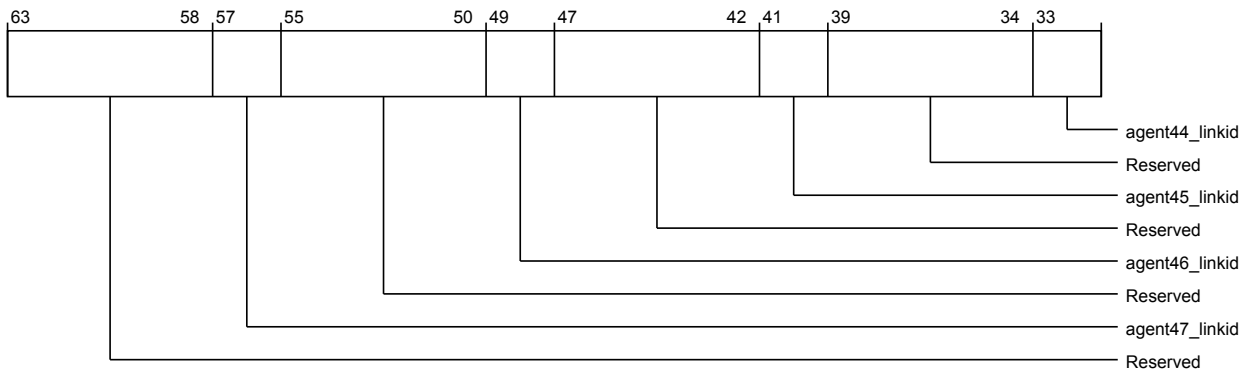


Figure 4-1174 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg5 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg5 higher register bit assignments.

Table 4-1191 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent47_linkid	Specifies the Link ID for Agent ID 47	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent46_linkid	Specifies the Link ID for Agent ID 46	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent45_linkid	Specifies the Link ID for Agent ID 45	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent44_linkid	Specifies the Link ID for Agent ID 44	RW	2'h0

The following image shows the lower register bit assignments.

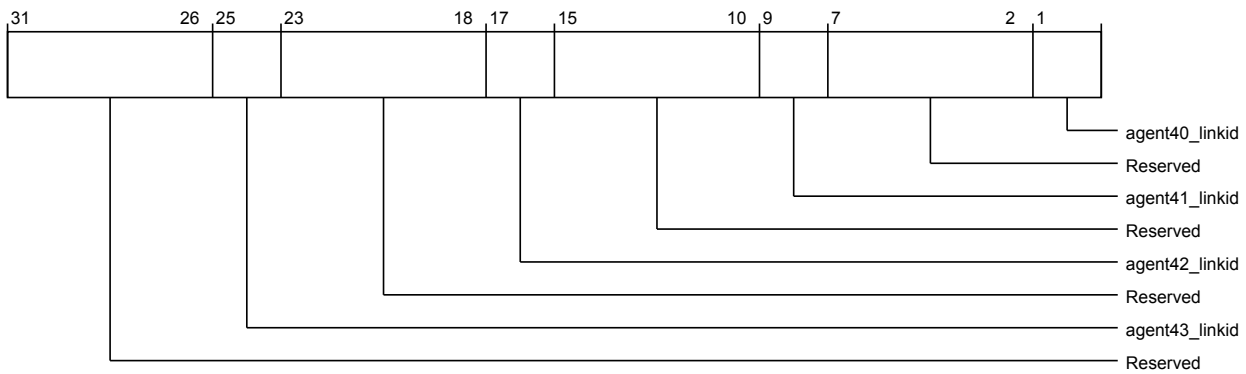


Figure 4-1175 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg5 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg5 lower register bit assignments.

Table 4-1192 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent43_linkid	Specifies the Link ID for Agent ID 43	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent42_linkid	Specifies the Link ID for Agent ID 42	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent41_linkid	Specifies the Link ID for Agent ID 41	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent40_linkid	Specifies the Link ID for Agent ID 40	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg6

Specifies the mapping of Agent ID to Link ID for Agent IDs 48 to 55.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE90
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

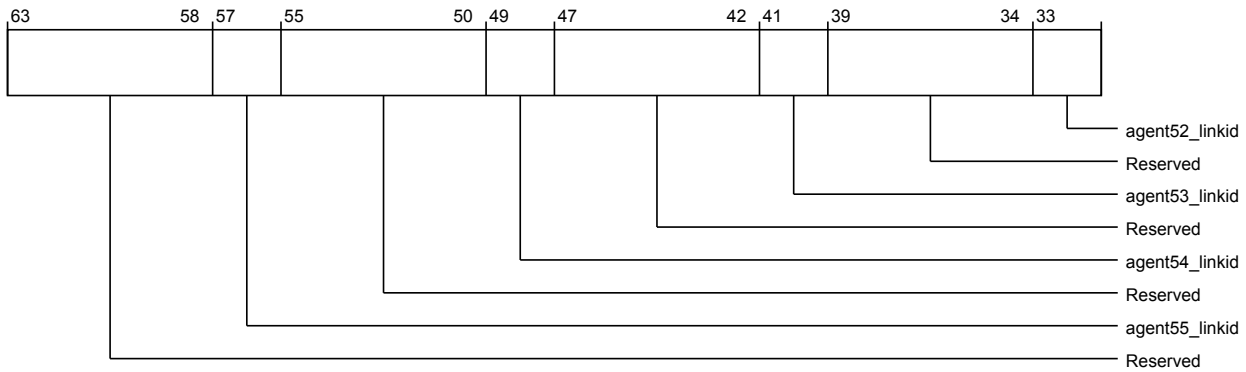


Figure 4-1176 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg6 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg6 higher register bit assignments.

Table 4-1193 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent55_linkid	Specifies the Link ID for Agent ID 55	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent54_linkid	Specifies the Link ID for Agent ID 54	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent53_linkid	Specifies the Link ID for Agent ID 53	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent52_linkid	Specifies the Link ID for Agent ID 52	RW	2'h0

The following image shows the lower register bit assignments.

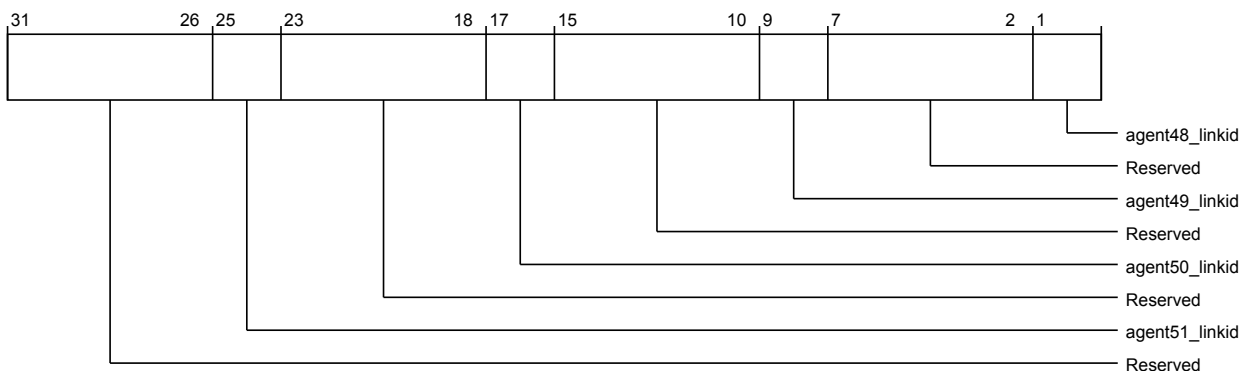


Figure 4-1177 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg6 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg6 lower register bit assignments.

Table 4-1194 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg6` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent51_linkid	Specifies the Link ID for Agent ID 51	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent50_linkid	Specifies the Link ID for Agent ID 50	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent49_linkid	Specifies the Link ID for Agent ID 49	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent48_linkid	Specifies the Link ID for Agent ID 48	RW	2'h0

`por_cxg_ra_agentid_to_linkid_reg7`

Specifies the mapping of Agent ID to Link ID for Agent IDs 56 to 63.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hE98
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.linkid_ctl</code>

The following image shows the higher register bit assignments.

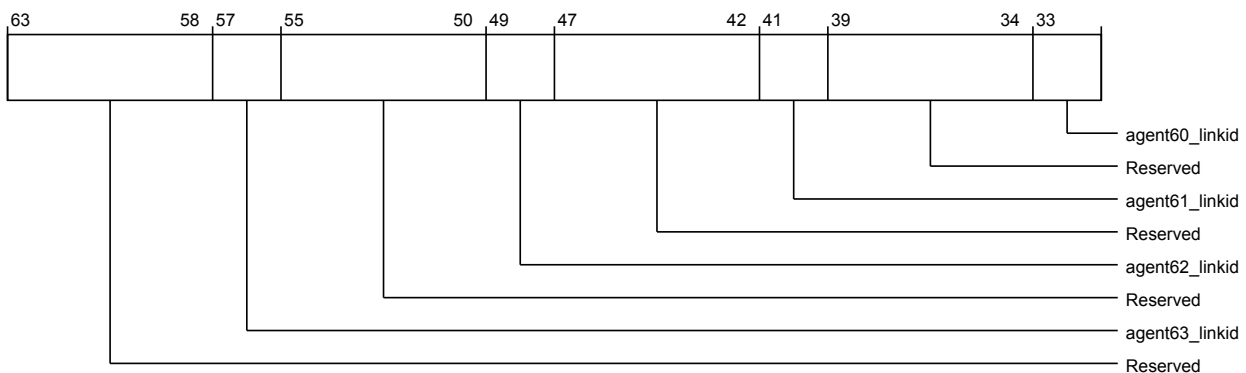


Figure 4-1178 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg7` (high)

The following table shows the `por_cxg_ra_agentid_to_linkid_reg7` higher register bit assignments.

Table 4-1195 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg7` (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent63_linkid	Specifies the Link ID for Agent ID 63	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent62_linkid	Specifies the Link ID for Agent ID 62	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent61_linkid	Specifies the Link ID for Agent ID 61	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent60_linkid	Specifies the Link ID for Agent ID 60	RW	2'h0

The following image shows the lower register bit assignments.

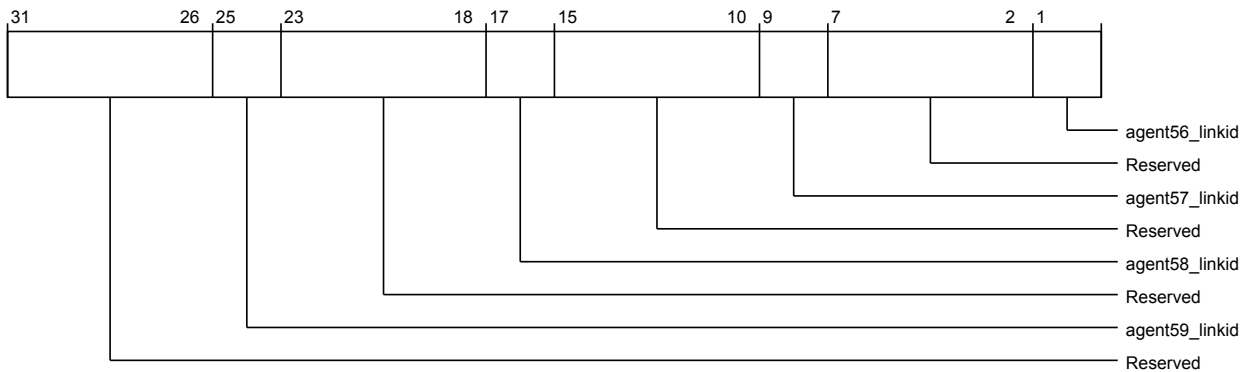


Figure 4-1179 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg7` (low)

The following table shows the `por_cxg_ra_agentid_to_linkid_reg7` lower register bit assignments.

Table 4-1196 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg7` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent59_linkid	Specifies the Link ID for Agent ID 59	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent58_linkid	Specifies the Link ID for Agent ID 58	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent57_linkid	Specifies the Link ID for Agent ID 57	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent56_linkid	Specifies the Link ID for Agent ID 56	RW	2'h0

por_cxg_ra_rnf_ldid_to_raid_reg0

Specifies the mapping of RN-F LDID to RAID for LDIDs 0 to 7.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hEA0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

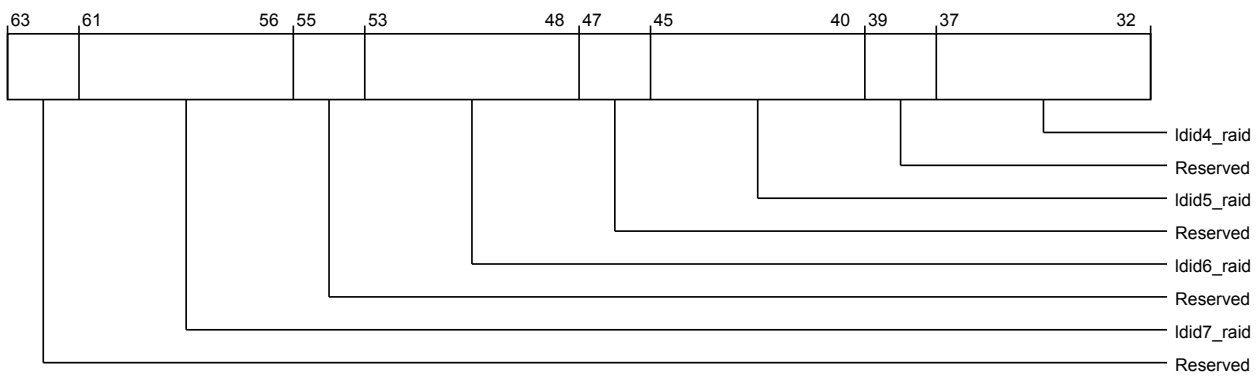


Figure 4-1180 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg0 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg0 higher register bit assignments.

Table 4-1197 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid7_raid	Specifies the RAID for LDID 7	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid6_raid	Specifies the RAID for LDID 6	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid5_raid	Specifies the RAID for LDID 5	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid4_raid	Specifies the RAID for LDID 4	RW	6'h0

The following image shows the lower register bit assignments.

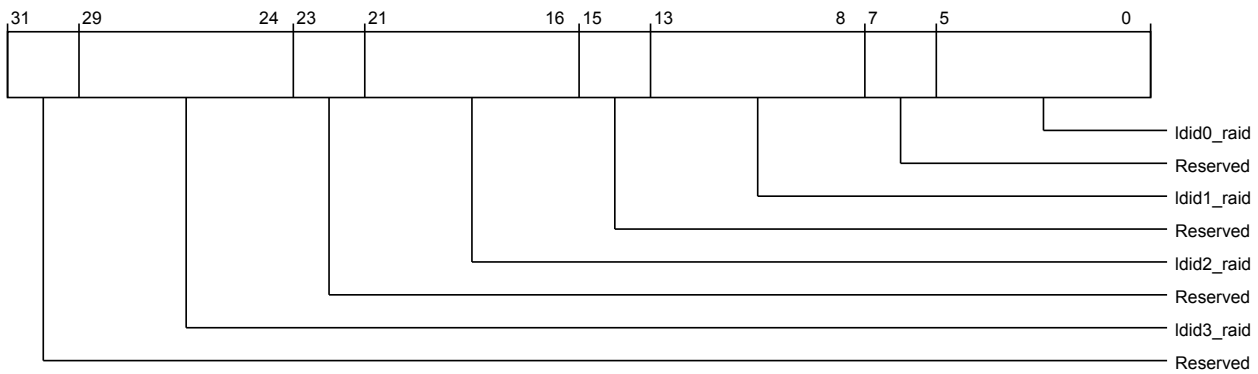


Figure 4-1181 por_cxg_ra_rnf_ldid_to_raid_reg0 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg0 lower register bit assignments.

Table 4-1198 por_cxg_ra_rnf_ldid_to_raid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid3_raid	Specifies the RAID for LDID 3	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid2_raid	Specifies the RAID for LDID 2	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid1_raid	Specifies the RAID for LDID 1	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid0_raid	Specifies the RAID for LDID 0	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg1

Specifies the mapping of RN-F LDID to RAID for LDIDs 8 to 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hEA8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

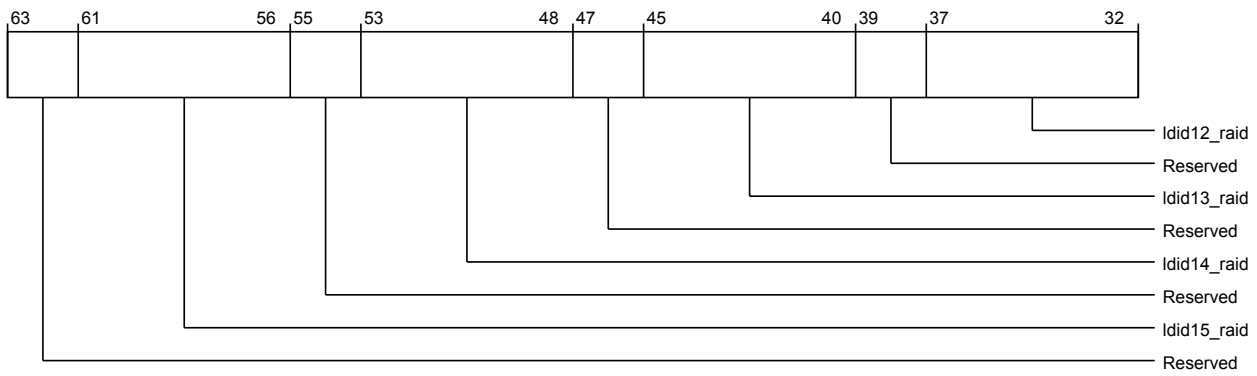


Figure 4-1182 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg1` (high)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_reg1` higher register bit assignments.

Table 4-1199 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg1` (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid15_raid	Specifies the RAID for LDID 15	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid14_raid	Specifies the RAID for LDID 14	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid13_raid	Specifies the RAID for LDID 13	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid12_raid	Specifies the RAID for LDID 12	RW	6'h0

The following image shows the lower register bit assignments.

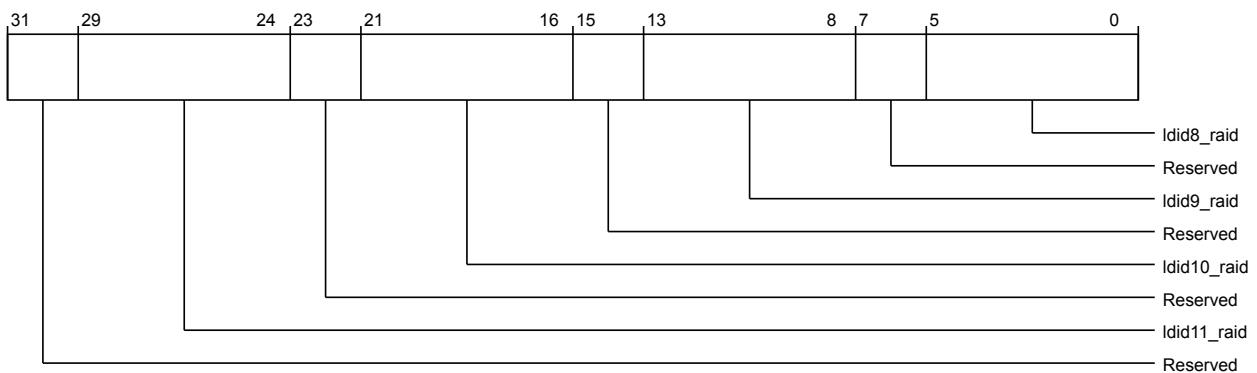


Figure 4-1183 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg1` (low)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_reg1` lower register bit assignments.

Table 4-1200 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg1` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>ldid11_raid</code>	Specifies the RAID for LDID 11	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	<code>ldid10_raid</code>	Specifies the RAID for LDID 10	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	<code>ldid9_raid</code>	Specifies the RAID for LDID 9	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	<code>ldid8_raid</code>	Specifies the RAID for LDID 8	RW	6'h0

`por_cxg_ra_rnf_ldid_to_raid_reg2`

Specifies the mapping of RN-F LDID to RAID for LDIDs 16 to 23.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hEB0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

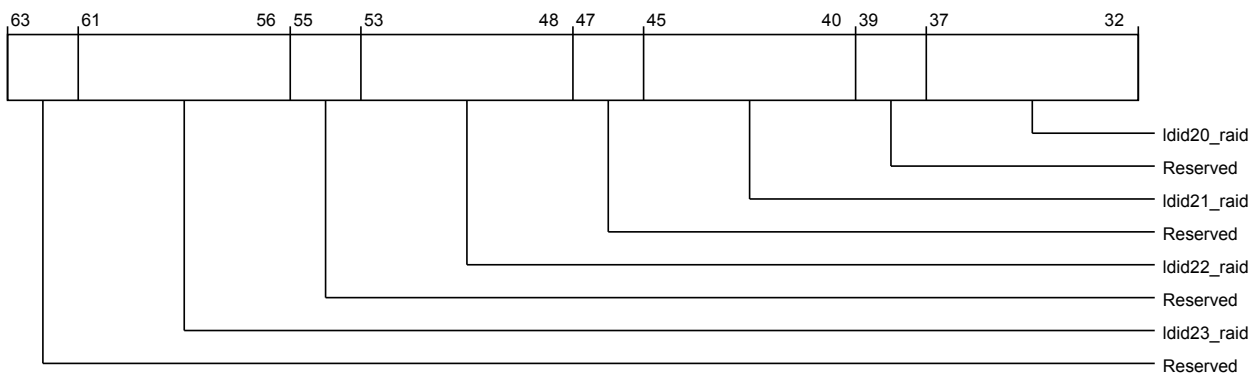


Figure 4-1184 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg2` (high)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_reg2` higher register bit assignments.

Table 4-1201 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid23_raid	Specifies the RAID for LDID 23	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid22_raid	Specifies the RAID for LDID 22	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid21_raid	Specifies the RAID for LDID 21	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid20_raid	Specifies the RAID for LDID 20	RW	6'h0

The following image shows the lower register bit assignments.

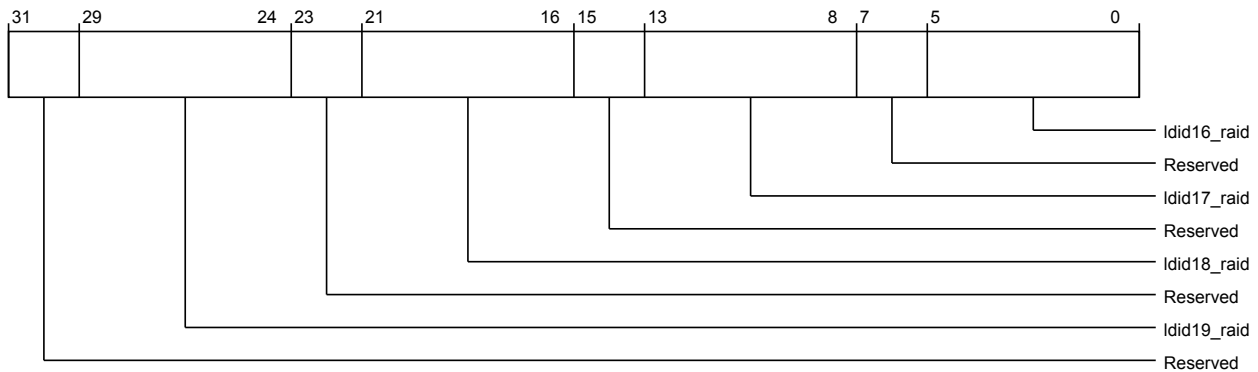


Figure 4-1185 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg2 (low)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_reg2` lower register bit assignments.

Table 4-1202 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid19_raid	Specifies the RAID for LDID 19	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid18_raid	Specifies the RAID for LDID 18	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid17_raid	Specifies the RAID for LDID 17	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid16_raid	Specifies the RAID for LDID 16	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg3

Specifies the mapping of RN-F LDID to RAID for LDIDs 24 to 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hEB8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

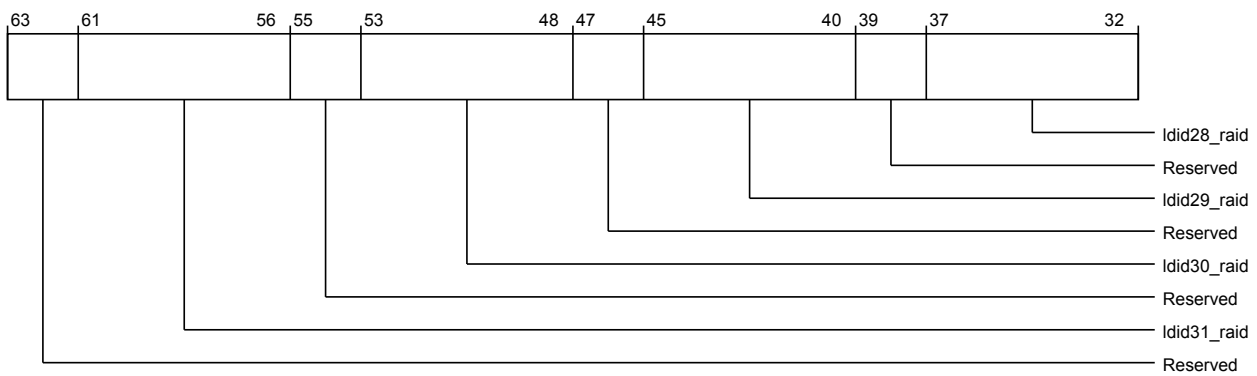


Figure 4-1186 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg3 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg3 higher register bit assignments.

Table 4-1203 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid31_raid	Specifies the RAID for LDID 31	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid30_raid	Specifies the RAID for LDID 30	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid29_raid	Specifies the RAID for LDID 29	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid28_raid	Specifies the RAID for LDID 28	RW	6'h0

The following image shows the lower register bit assignments.

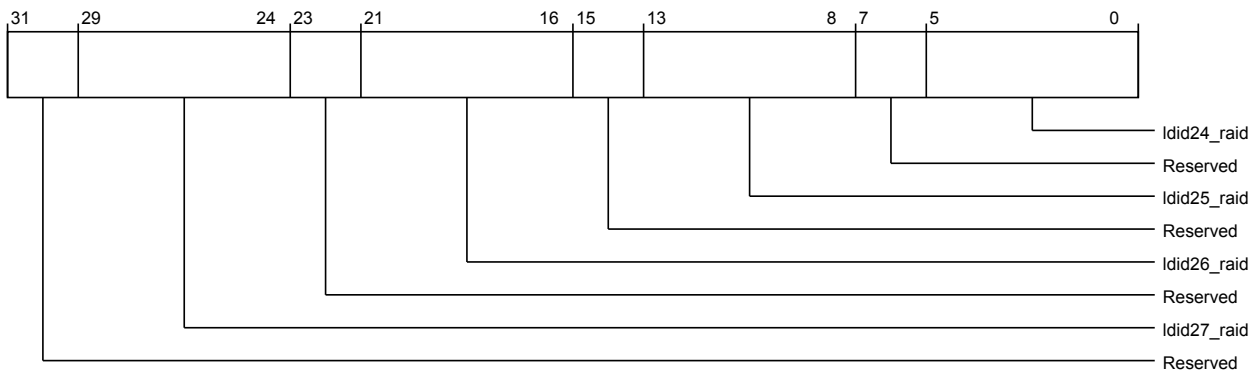


Figure 4-1187 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg3 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg3 lower register bit assignments.

Table 4-1204 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid27_raid	Specifies the RAID for LDID 27	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid26_raid	Specifies the RAID for LDID 26	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid25_raid	Specifies the RAID for LDID 25	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid24_raid	Specifies the RAID for LDID 24	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg4

Specifies the mapping of RN-F LDID to RAID for LDIDs 32 to 39.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hEC0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

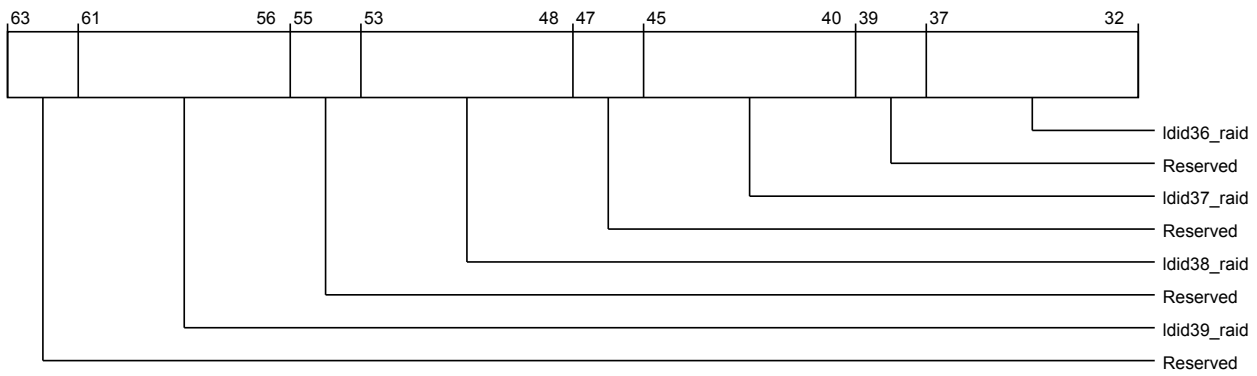


Figure 4-1188 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg4` (high)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_reg4` higher register bit assignments.

Table 4-1205 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg4` (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid39_raid	Specifies the RAID for LDID 39	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid38_raid	Specifies the RAID for LDID 38	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid37_raid	Specifies the RAID for LDID 37	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid36_raid	Specifies the RAID for LDID 36	RW	6'h0

The following image shows the lower register bit assignments.

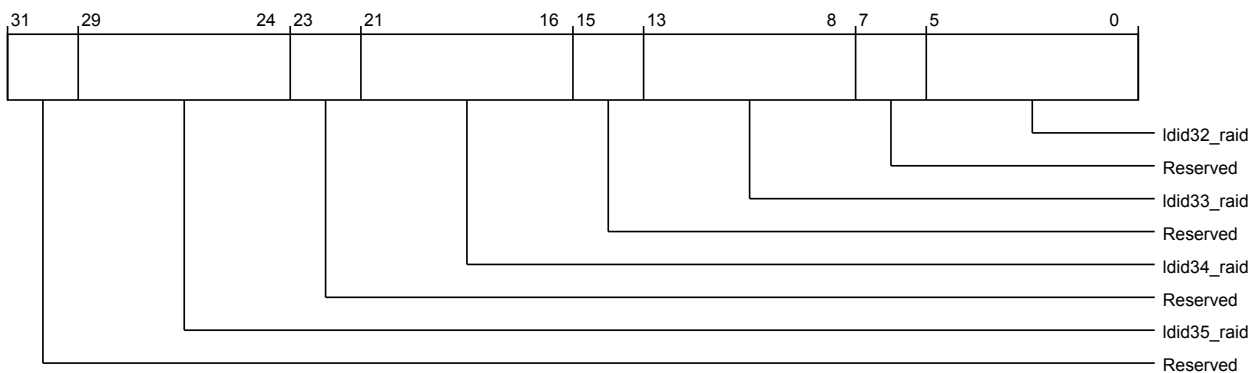


Figure 4-1189 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg4` (low)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_reg4` lower register bit assignments.

Table 4-1206 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg4` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>ldid35_raid</code>	Specifies the RAID for LDID 35	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	<code>ldid34_raid</code>	Specifies the RAID for LDID 34	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	<code>ldid33_raid</code>	Specifies the RAID for LDID 33	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	<code>ldid32_raid</code>	Specifies the RAID for LDID 32	RW	6'h0

`por_cxg_ra_rnf_ldid_to_raid_reg5`

Specifies the mapping of RN-F LDID to RAID for LDIDs 40 to 47.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hEC8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

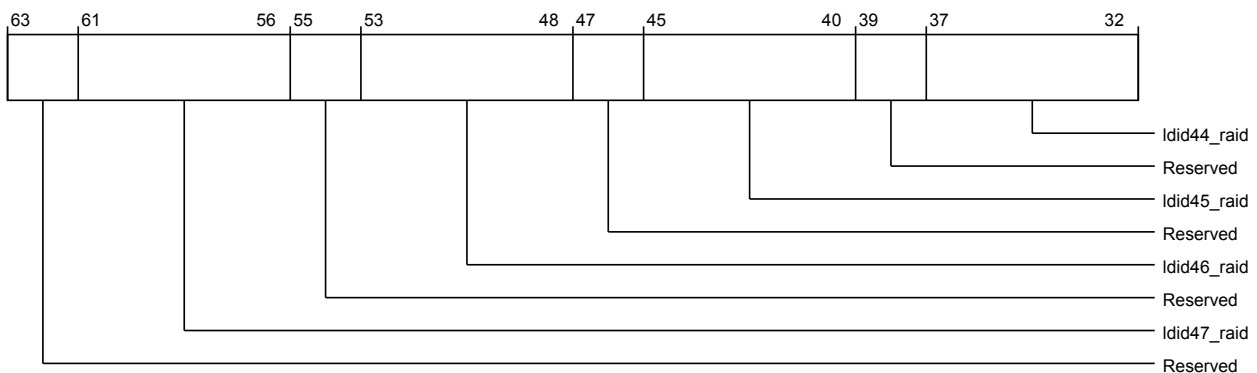


Figure 4-1190 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg5` (high)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_reg5` higher register bit assignments.

Table 4-1207 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid47_raid	Specifies the RAID for LDID 47	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid46_raid	Specifies the RAID for LDID 46	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid45_raid	Specifies the RAID for LDID 45	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid44_raid	Specifies the RAID for LDID 44	RW	6'h0

The following image shows the lower register bit assignments.

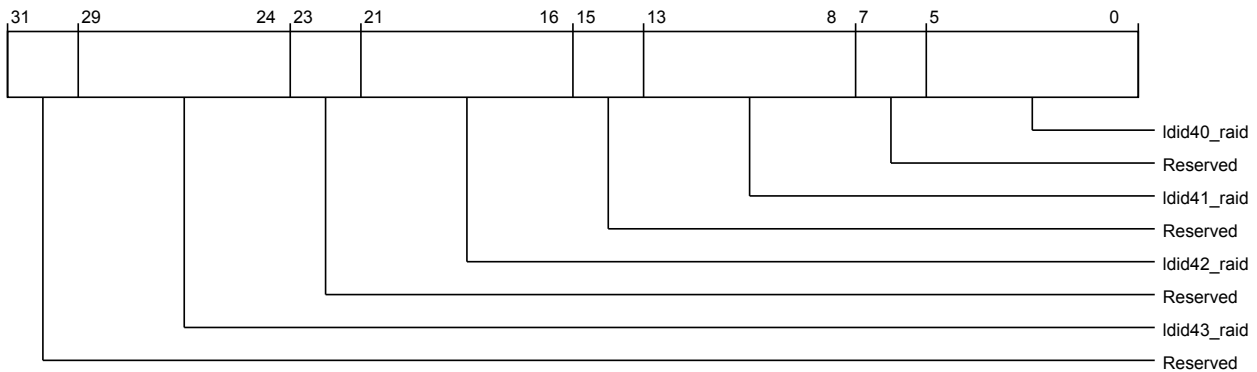


Figure 4-1191 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg5 (low)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_reg5` lower register bit assignments.

Table 4-1208 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid43_raid	Specifies the RAID for LDID 43	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid42_raid	Specifies the RAID for LDID 42	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid41_raid	Specifies the RAID for LDID 41	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid40_raid	Specifies the RAID for LDID 40	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg6

Specifies the mapping of RN-F LDID to RAID for LDIDs 48 to 55.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hED0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

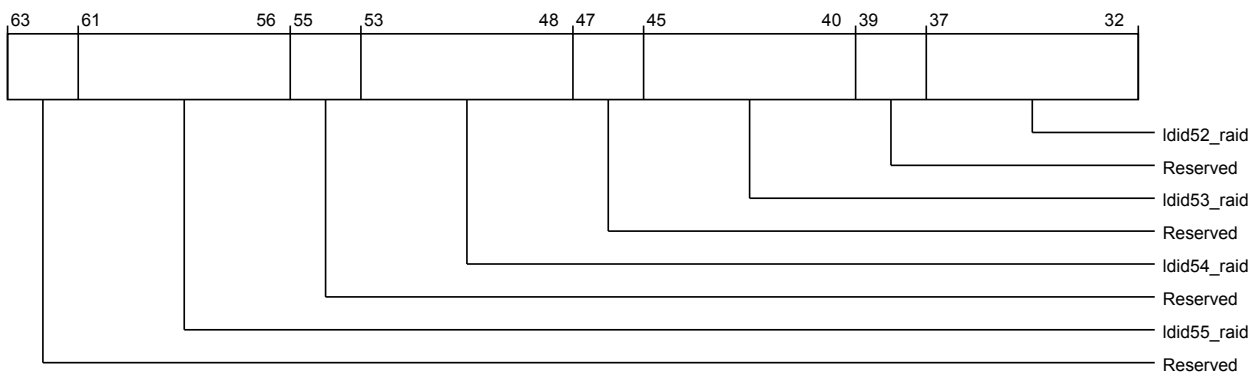


Figure 4-1192 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg6 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg6 higher register bit assignments.

Table 4-1209 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	Ldid55_raid	Specifies the RAID for LDID 55	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	Ldid54_raid	Specifies the RAID for LDID 54	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	Ldid53_raid	Specifies the RAID for LDID 53	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	Ldid52_raid	Specifies the RAID for LDID 52	RW	6'h0

The following image shows the lower register bit assignments.

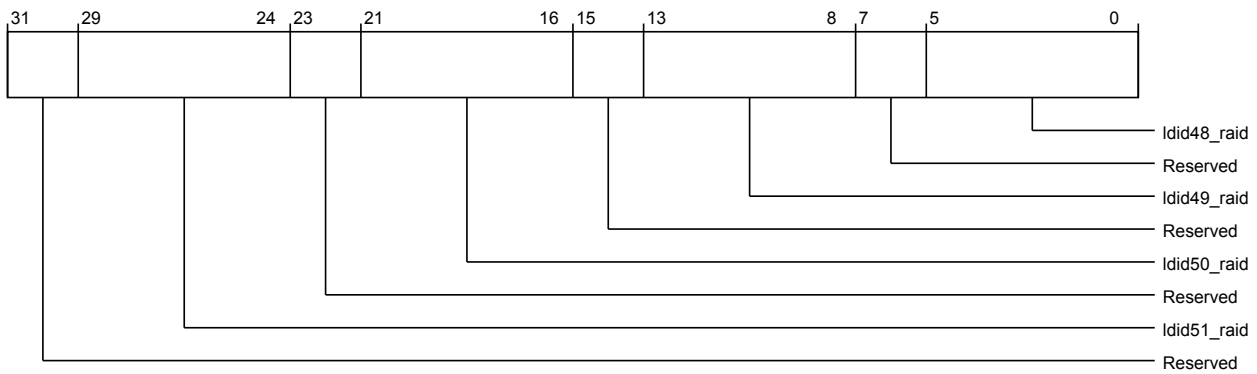


Figure 4-1193 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg6` (low)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_reg6` lower register bit assignments.

Table 4-1210 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg6` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid51_raid	Specifies the RAID for LDID 51	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid50_raid	Specifies the RAID for LDID 50	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid49_raid	Specifies the RAID for LDID 49	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid48_raid	Specifies the RAID for LDID 48	RW	6'h0

`por_cxg_ra_rnf_ldid_to_raid_reg7`

Specifies the mapping of RN-F LDID to RAID for LDIDs 56 to 63.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hED8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

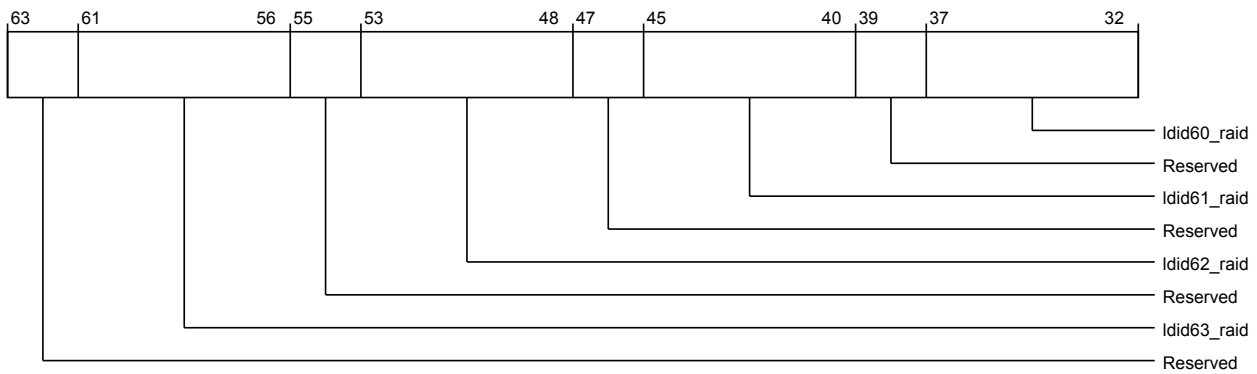


Figure 4-1194 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg7 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg7 higher register bit assignments.

Table 4-1211 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid63_raid	Specifies the RAID for LDID 63	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid62_raid	Specifies the RAID for LDID 62	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid61_raid	Specifies the RAID for LDID 61	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid60_raid	Specifies the RAID for LDID 60	RW	6'h0

The following image shows the lower register bit assignments.

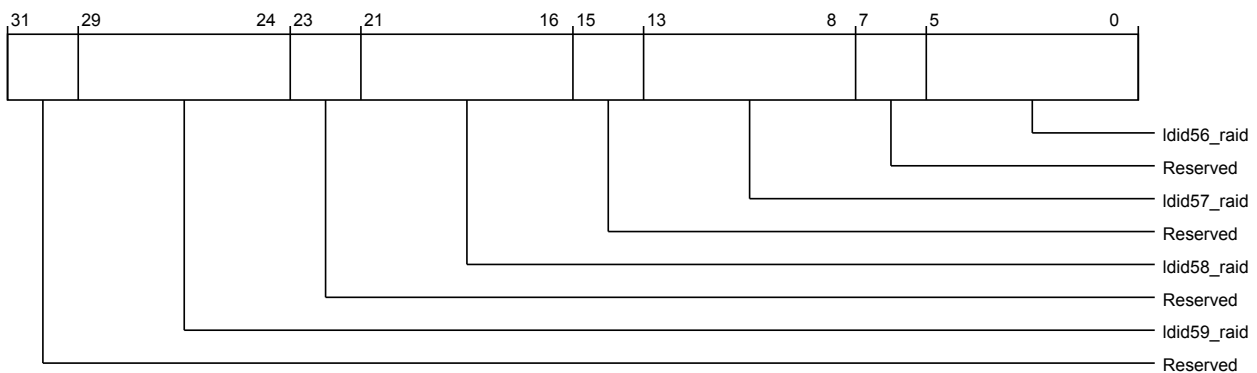


Figure 4-1195 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg7 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg7 lower register bit assignments.

Table 4-1212 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid59_raid	Specifies the RAID for LDID 59	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid58_raid	Specifies the RAID for LDID 58	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid57_raid	Specifies the RAID for LDID 57	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid56_raid	Specifies the RAID for LDID 56	RW	6'h0

por_cxg_ra_rni_ldid_to_raid_reg0

Specifies the mapping of RN-I LDID to RAID for LDIDs 0 to 7.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hEE0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

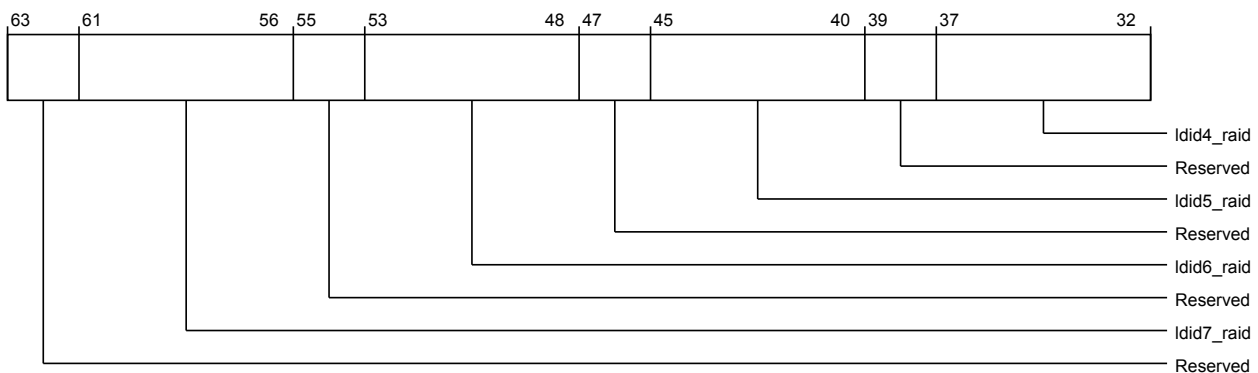


Figure 4-1196 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg0 (high)

The following table shows the `por_cxg_ra_rni_ldid_to_raid_reg0` higher register bit assignments.

Table 4-1213 `por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg0` (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	<code>ldid7_raid</code>	Specifies the RAID for LDID 7	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	<code>ldid6_raid</code>	Specifies the RAID for LDID 6	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	<code>ldid5_raid</code>	Specifies the RAID for LDID 5	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	<code>ldid4_raid</code>	Specifies the RAID for LDID 4	RW	6'h0

The following image shows the lower register bit assignments.

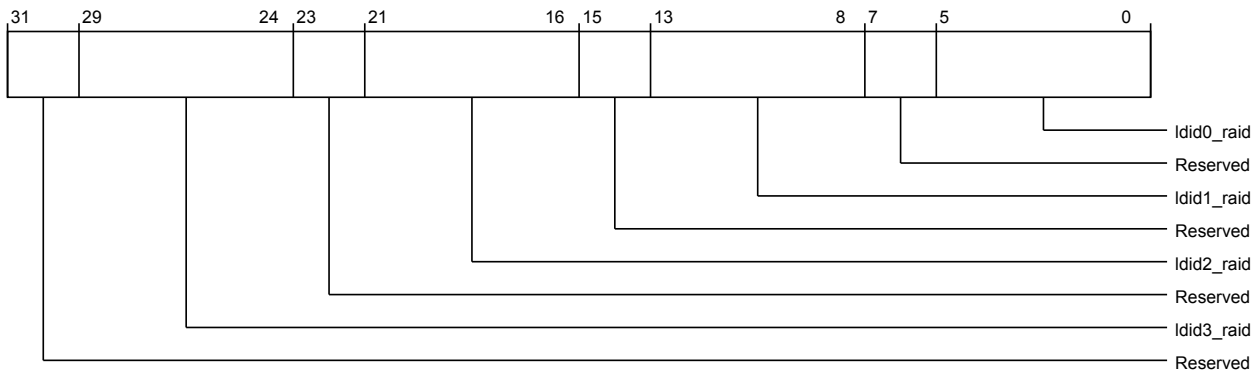


Figure 4-1197 `por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg0` (low)

The following table shows the `por_cxg_ra_rni_ldid_to_raid_reg0` lower register bit assignments.

Table 4-1214 `por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg0` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>ldid3_raid</code>	Specifies the RAID for LDID 3	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	<code>ldid2_raid</code>	Specifies the RAID for LDID 2	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	<code>ldid1_raid</code>	Specifies the RAID for LDID 1	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	<code>ldid0_raid</code>	Specifies the RAID for LDID 0	RW	6'h0

por_cxg_ra_rni_ldid_to_raid_reg1

Specifies the mapping of RN-I LDID to RAID for LDIDs 8 to 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hEE8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

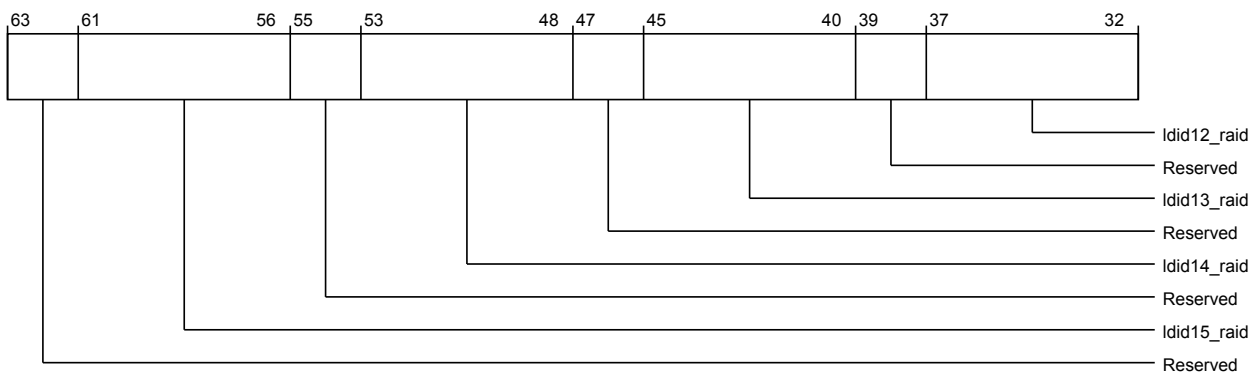


Figure 4-1198 `por_cxg_ra_rni_ldid_to_raid_reg1` (high)

The following table shows the `por_cxg_ra_rni_ldid_to_raid_reg1` higher register bit assignments.

Table 4-1215 `por_cxg_ra_rni_ldid_to_raid_reg1` (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid15_raid	Specifies the RAID for LDID 15	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid14_raid	Specifies the RAID for LDID 14	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid13_raid	Specifies the RAID for LDID 13	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid12_raid	Specifies the RAID for LDID 12	RW	6'h0

The following image shows the lower register bit assignments.

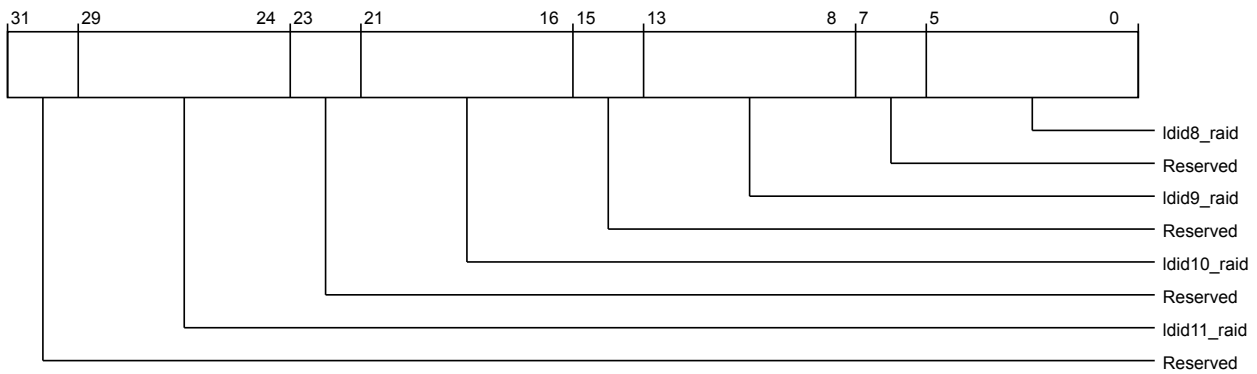


Figure 4-1199 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg1 (low)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg1 lower register bit assignments.

Table 4-1216 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid11_raid	Specifies the RAID for LDID 11	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid10_raid	Specifies the RAID for LDID 10	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid9_raid	Specifies the RAID for LDID 9	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid8_raid	Specifies the RAID for LDID 8	RW	6'h0

por_cxg_ra_rni_ldid_to_raid_reg2

Specifies the mapping of RN-I LDID to RAID for LDIDs 16 to 23.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hEF0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

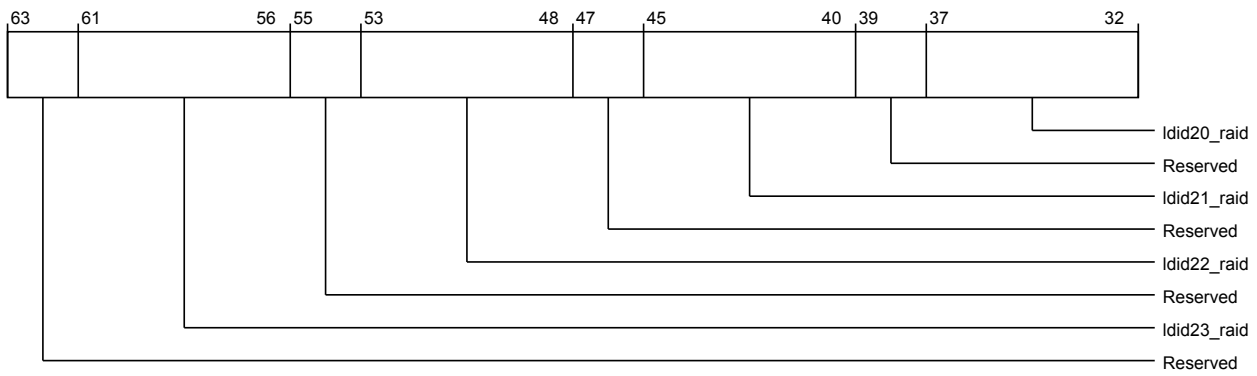


Figure 4-1200 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg2 (high)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg2 higher register bit assignments.

Table 4-1217 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	Ldid23_raid	Specifies the RAID for LDID 23	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	Ldid22_raid	Specifies the RAID for LDID 22	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	Ldid21_raid	Specifies the RAID for LDID 21	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	Ldid20_raid	Specifies the RAID for LDID 20	RW	6'h0

The following image shows the lower register bit assignments.

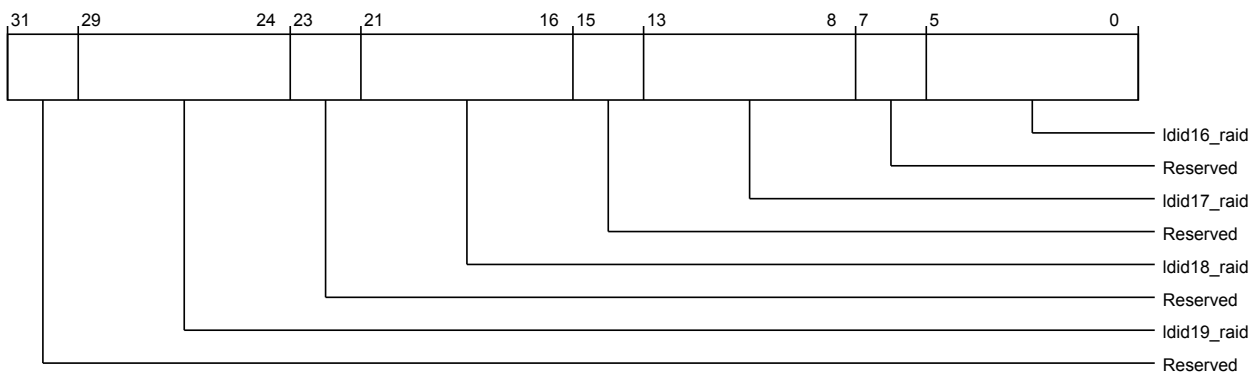


Figure 4-1201 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg2 (low)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg2 lower register bit assignments.

Table 4-1218 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid19_raid	Specifies the RAID for LDID 19	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid18_raid	Specifies the RAID for LDID 18	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid17_raid	Specifies the RAID for LDID 17	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid16_raid	Specifies the RAID for LDID 16	RW	6'h0

por_cxg_ra_rni_ldid_to_raid_reg3

Specifies the mapping of RN-I LDID to RAID for LDIDs 24 to 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hEF8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

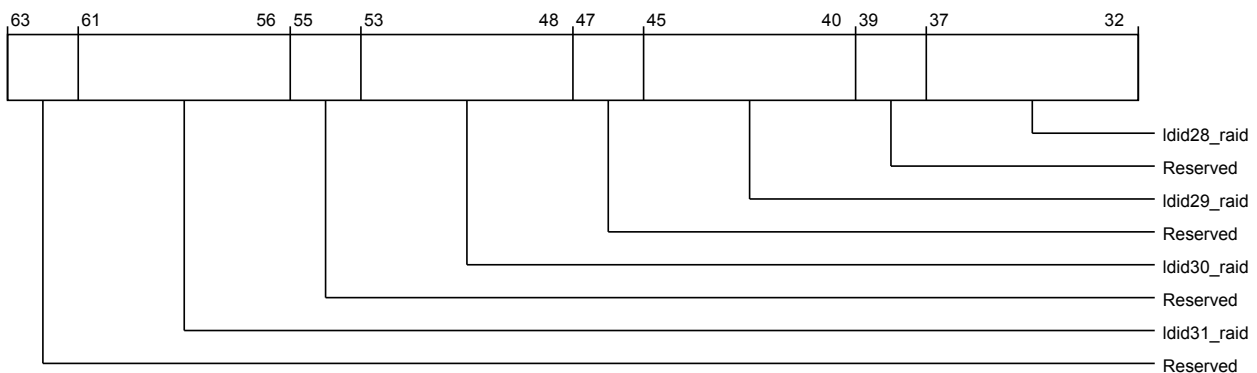


Figure 4-1202 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg3 (high)

The following table shows the `por_cxg_ra_rni_ldid_to_raid_reg3` higher register bit assignments.

Table 4-1219 `por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg3` (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	<code>ldid31_raid</code>	Specifies the RAID for LDID 31	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	<code>ldid30_raid</code>	Specifies the RAID for LDID 30	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	<code>ldid29_raid</code>	Specifies the RAID for LDID 29	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	<code>ldid28_raid</code>	Specifies the RAID for LDID 28	RW	6'h0

The following image shows the lower register bit assignments.

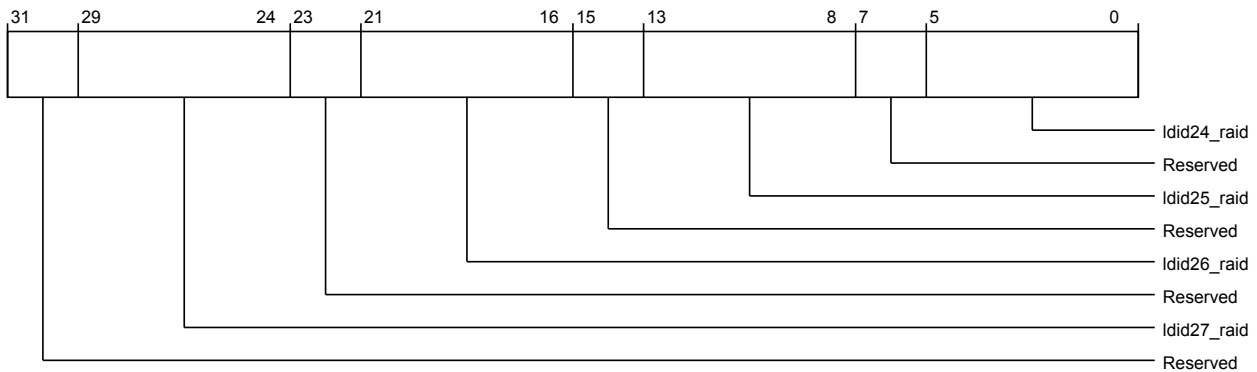


Figure 4-1203 `por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg3` (low)

The following table shows the `por_cxg_ra_rni_ldid_to_raid_reg3` lower register bit assignments.

Table 4-1220 `por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg3` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>ldid27_raid</code>	Specifies the RAID for LDID 27	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	<code>ldid26_raid</code>	Specifies the RAID for LDID 26	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	<code>ldid25_raid</code>	Specifies the RAID for LDID 25	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	<code>ldid24_raid</code>	Specifies the RAID for LDID 24	RW	6'h0

por_cxg_ra_rnd_ldid_to_raid_reg0

Specifies the mapping of RN-D LDID to RAID for LDIDs 0 to 7.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

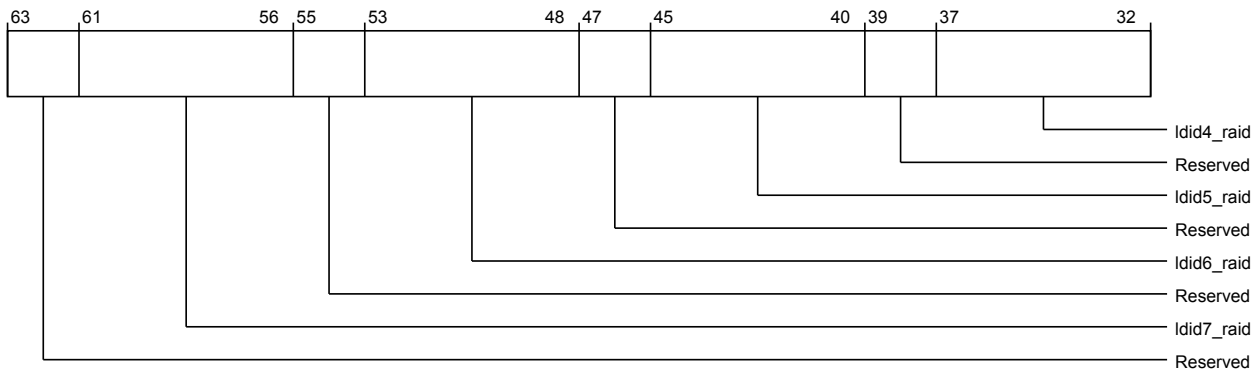


Figure 4-1204 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg0 (high)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_reg0 higher register bit assignments.

Table 4-1221 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid7_raid	Specifies the RAID for LDID 7	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid6_raid	Specifies the RAID for LDID 6	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid5_raid	Specifies the RAID for LDID 5	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid4_raid	Specifies the RAID for LDID 4	RW	6'h0

The following image shows the lower register bit assignments.

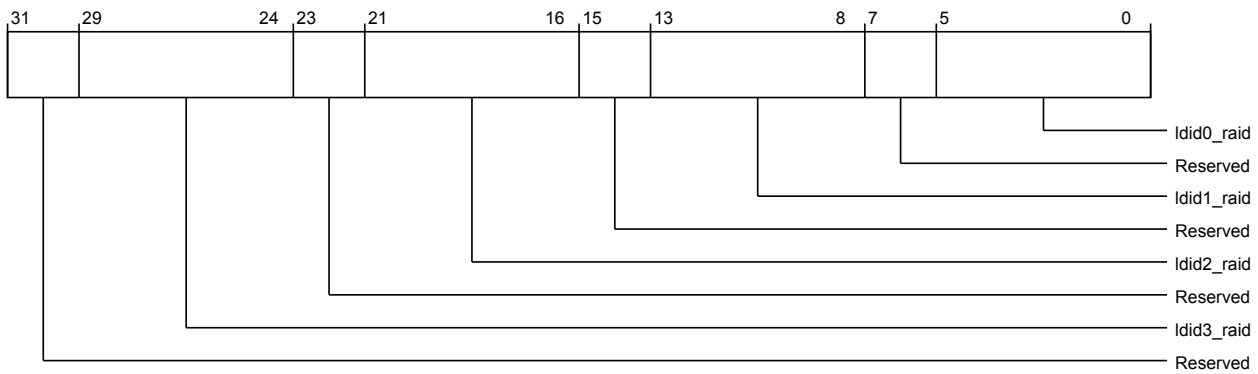


Figure 4-1205 `por_cxg_ra_rnd_ldid_to_raid_reg0` (low)

The following table shows the `por_cxg_ra_rnd_ldid_to_raid_reg0` lower register bit assignments.

Table 4-1222 `por_cxg_ra_rnd_ldid_to_raid_reg0` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid3_raid	Specifies the RAID for LDID 3	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid2_raid	Specifies the RAID for LDID 2	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid1_raid	Specifies the RAID for LDID 1	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid0_raid	Specifies the RAID for LDID 0	RW	6'h0

`por_cxg_ra_rnd_ldid_to_raid_reg1`

Specifies the mapping of RN-D LDID to RAID for LDIDs 8 to 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF08
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

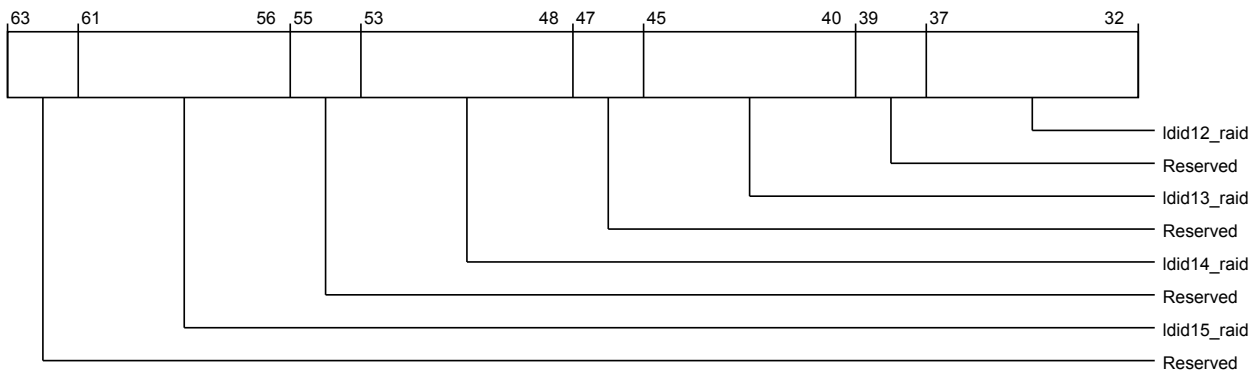


Figure 4-1206 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg1` (high)

The following table shows the `por_cxg_ra_rnd_ldid_to_raid_reg1` higher register bit assignments.

Table 4-1223 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg1` (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid15_raid	Specifies the RAID for LDID 15	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid14_raid	Specifies the RAID for LDID 14	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid13_raid	Specifies the RAID for LDID 13	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid12_raid	Specifies the RAID for LDID 12	RW	6'h0

The following image shows the lower register bit assignments.

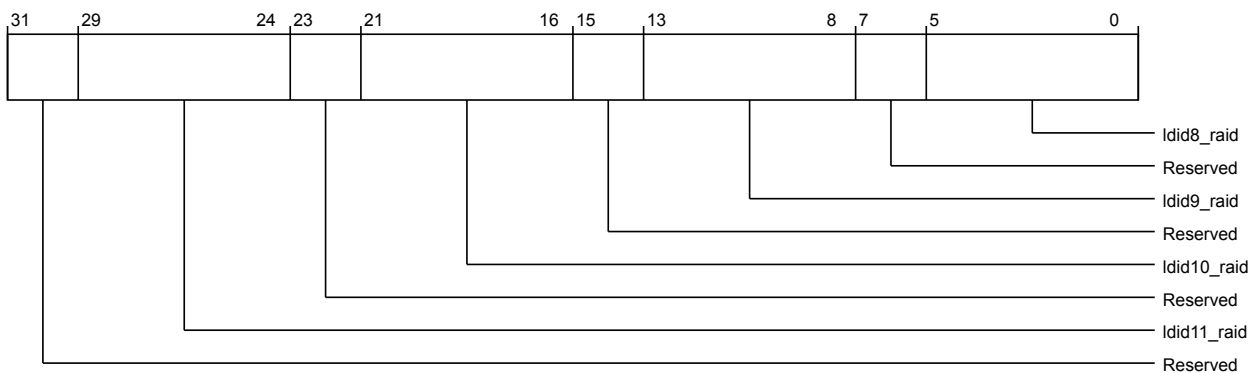


Figure 4-1207 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg1` (low)

The following table shows the `por_cxg_ra_rnd_ldid_to_raid_reg1` lower register bit assignments.

Table 4-1224 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg1` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>ldid11_raid</code>	Specifies the RAID for LDID 11	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	<code>ldid10_raid</code>	Specifies the RAID for LDID 10	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	<code>ldid9_raid</code>	Specifies the RAID for LDID 9	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	<code>ldid8_raid</code>	Specifies the RAID for LDID 8	RW	6'h0

`por_cxg_ra_rnd_ldid_to_raid_reg2`

Specifies the mapping of RN-D LDID to RAID for LDIDs 16 to 23.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF10
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

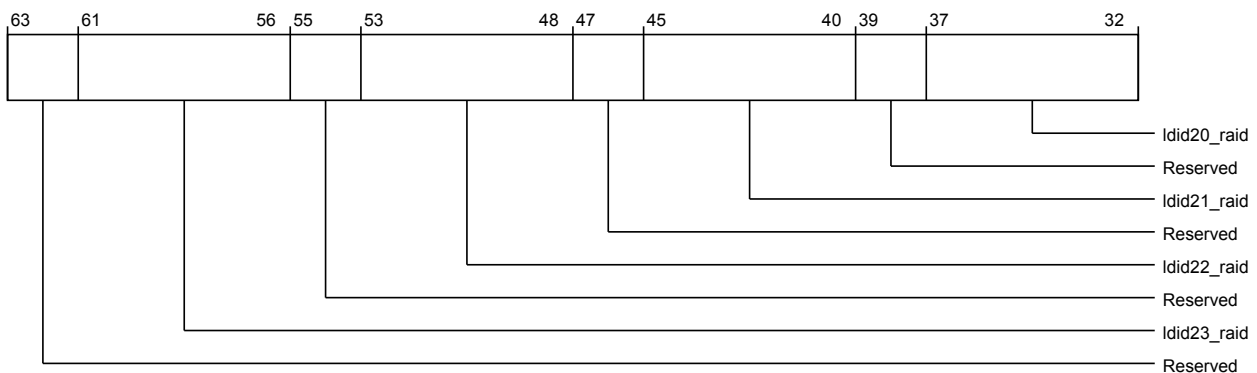


Figure 4-1208 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg2` (high)

The following table shows the `por_cxg_ra_rnd_ldid_to_raid_reg2` higher register bit assignments.

Table 4-1225 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg2` (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	<code>ldid23_raid</code>	Specifies the RAID for LDID 23	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	<code>ldid22_raid</code>	Specifies the RAID for LDID 22	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	<code>ldid21_raid</code>	Specifies the RAID for LDID 21	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	<code>ldid20_raid</code>	Specifies the RAID for LDID 20	RW	6'h0

The following image shows the lower register bit assignments.

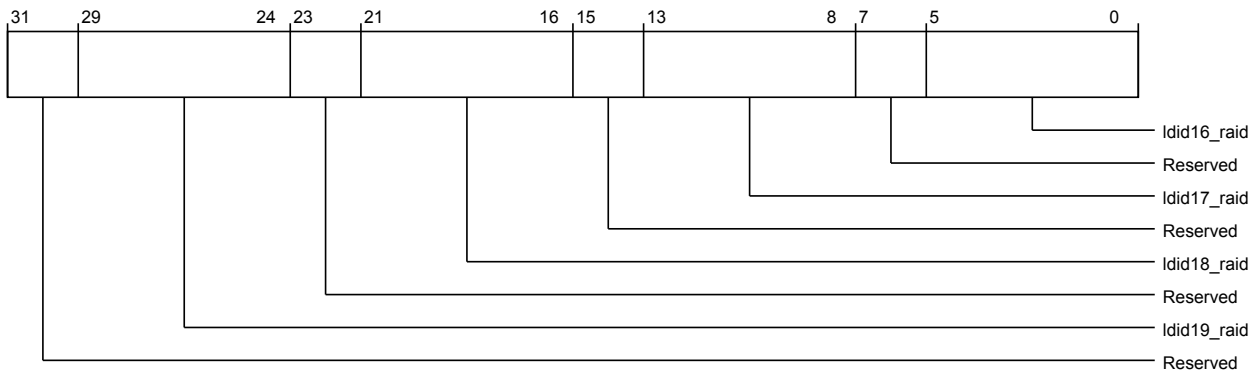


Figure 4-1209 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg2` (low)

The following table shows the `por_cxg_ra_rnd_ldid_to_raid_reg2` lower register bit assignments.

Table 4-1226 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg2` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>ldid19_raid</code>	Specifies the RAID for LDID 19	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	<code>ldid18_raid</code>	Specifies the RAID for LDID 18	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	<code>ldid17_raid</code>	Specifies the RAID for LDID 17	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	<code>ldid16_raid</code>	Specifies the RAID for LDID 16	RW	6'h0

por_cxg_ra_rnd_ldid_to_raid_reg3

Specifies the mapping of RN-D LDID to RAID for LDIDs 24 to 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF18
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

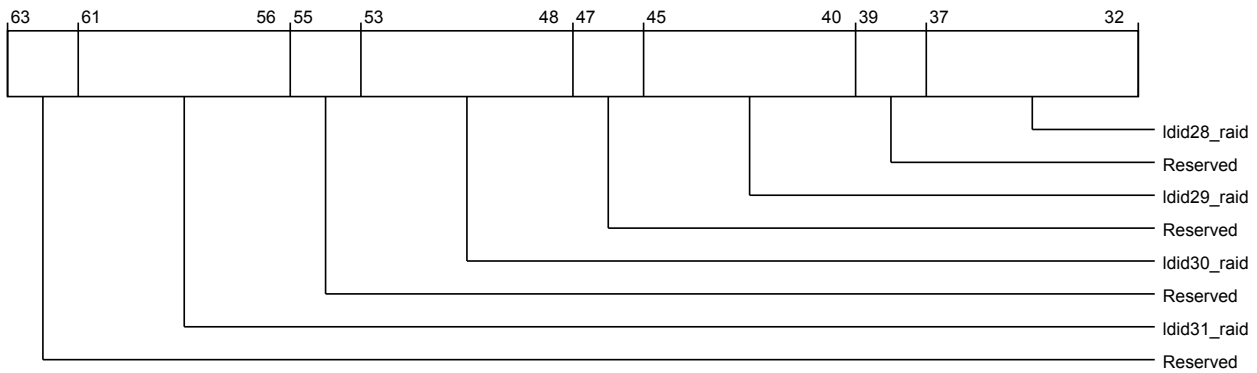


Figure 4-1210 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg3 (high)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_reg3 higher register bit assignments.

Table 4-1227 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid31_raid	Specifies the RAID for LDID 31	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid30_raid	Specifies the RAID for LDID 30	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid29_raid	Specifies the RAID for LDID 29	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid28_raid	Specifies the RAID for LDID 28	RW	6'h0

The following image shows the lower register bit assignments.

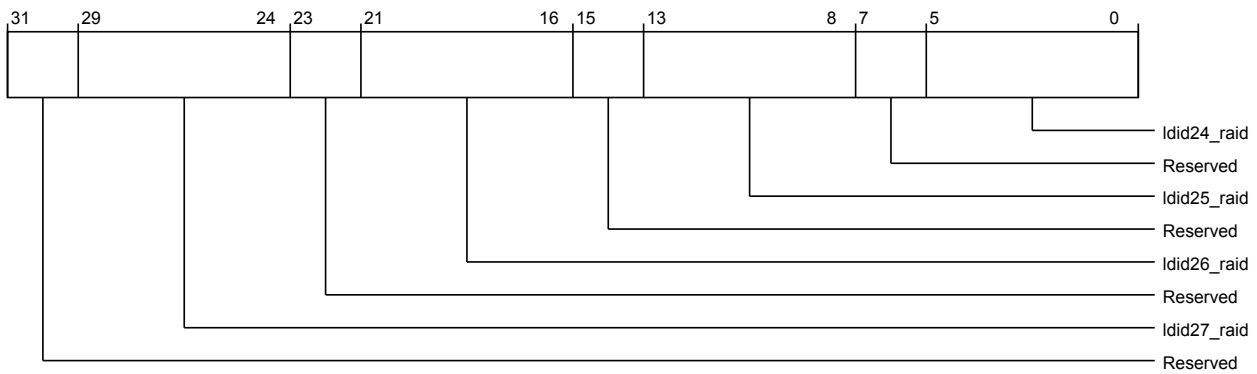


Figure 4-1211 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg3` (low)

The following table shows the `por_cxg_ra_rnd_ldid_to_raid_reg3` lower register bit assignments.

Table 4-1228 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg3` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid27_raid	Specifies the RAID for LDID 27	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid26_raid	Specifies the RAID for LDID 26	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid25_raid	Specifies the RAID for LDID 25	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid24_raid	Specifies the RAID for LDID 24	RW	6'h0

`por_cxg_ra_agentid_to_linkid_val`

Specifies which Agent ID to Link ID mappings are valid.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF20
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.linkid_ctl</code>

The following image shows the higher register bit assignments.

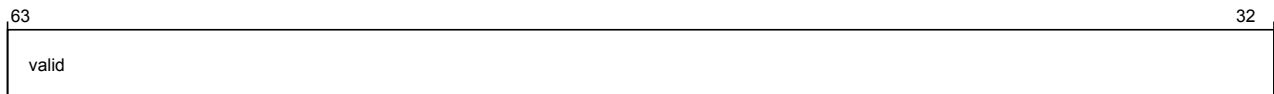


Figure 4-1212 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_val` (high)

The following table shows the `por_cxg_ra_agentid_to_linkid_val` higher register bit assignments.

Table 4-1229 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_val` (high)

Bits	Field name	Description	Type	Reset
63:32	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

The following image shows the lower register bit assignments.



Figure 4-1213 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_val` (low)

The following table shows the `por_cxg_ra_agentid_to_linkid_val` lower register bit assignments.

Table 4-1230 `por_cxg_ra_por_cxg_ra_agentid_to_linkid_val` (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

`por_cxg_ra_rnf_ldid_to_raid_val`

Specifies which RN-F LDID to RAID mappings are valid.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF28
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

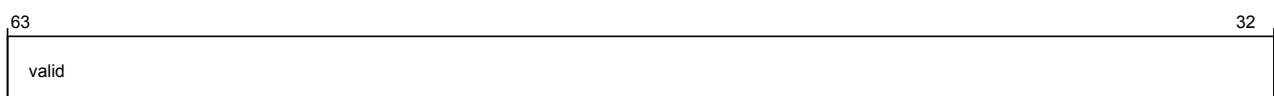


Figure 4-1214 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_val` (high)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_val` higher register bit assignments.

Table 4-1231 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_val` (high)

Bits	Field name	Description	Type	Reset
63:32	valid	Specifies whether the RAID is valid; bit number corresponds to logical RN-F LDID number (from 0 to 63)	RW	63'h0

The following image shows the lower register bit assignments.

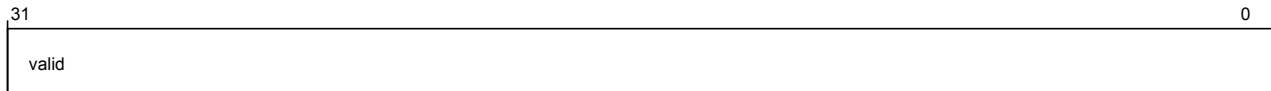


Figure 4-1215 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_val` (low)

The following table shows the `por_cxg_ra_rnf_ldid_to_raid_val` lower register bit assignments.

Table 4-1232 `por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_val` (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the RAID is valid; bit number corresponds to logical RN-F LDID number (from 0 to 63)	RW	63'h0

`por_cxg_ra_rni_ldid_to_raid_val`

Specifies which RN-I LDID to RAID mappings are valid.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF30
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

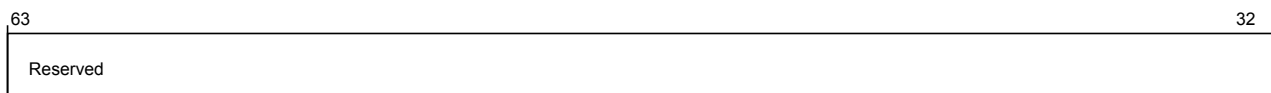


Figure 4-1216 `por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_val` (high)

The following table shows the `por_cxg_ra_rni_ldid_to_raid_val` higher register bit assignments.

Table 4-1233 `por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_val` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.



Figure 4-1217 `por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_val` (low)

The following table shows the `por_cxg_ra_rni_ldid_to_raid_val` lower register bit assignments.

Table 4-1234 `por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_val` (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the RAID is valid; bit number corresponds to logical RN-I LDID number (from 0 to 31)	RW	32'h0

`por_cxg_ra_rnd_ldid_to_raid_val`

Specifies which RN-D LDID to RAID mappings are valid.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hF38
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxg_ra_secure_register_groups_override.ldid_ctl</code>

The following image shows the higher register bit assignments.

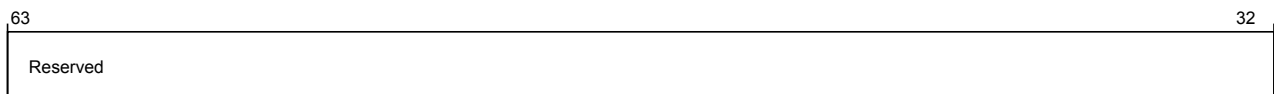


Figure 4-1218 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_val` (high)

The following table shows the `por_cxg_ra_rnd_ldid_to_raid_val` higher register bit assignments.

Table 4-1235 `por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_val` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

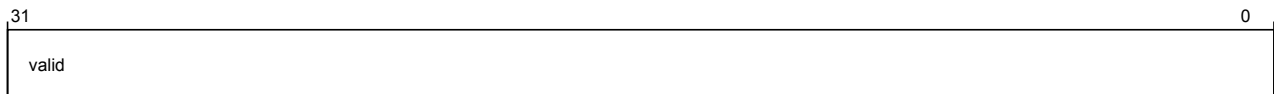


Figure 4-1219 por_cxg_ra_rnd_lidid_to_raid_val (low)

The following table shows the por_cxg_ra_rnd_lidid_to_raid_val lower register bit assignments.

Table 4-1236 por_cxg_ra_rnd_lidid_to_raid_val (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the RAID is valid; bit number corresponds to logical RN-D LDID number (from 0 to 31)	RW	32'h0

por_cxg_ra_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2000
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

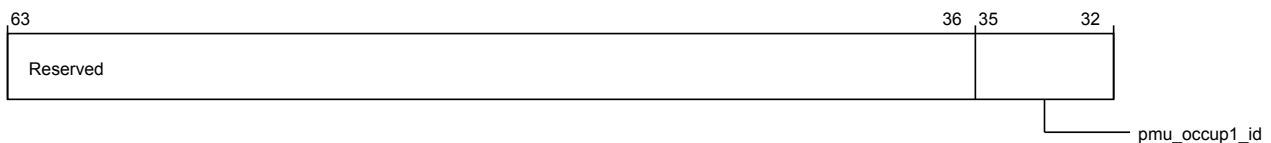


Figure 4-1220 por_cxg_ra_pmu_event_sel (high)

The following table shows the por_cxg_ra_pmu_event_sel higher register bit assignments.

Table 4-1237 por_cxg_ra_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:36	Reserved	Reserved	RO	-
35:32	pmu_occup1_id	PMU occupancy event selector ID	RW	4'b0

The following image shows the lower register bit assignments.

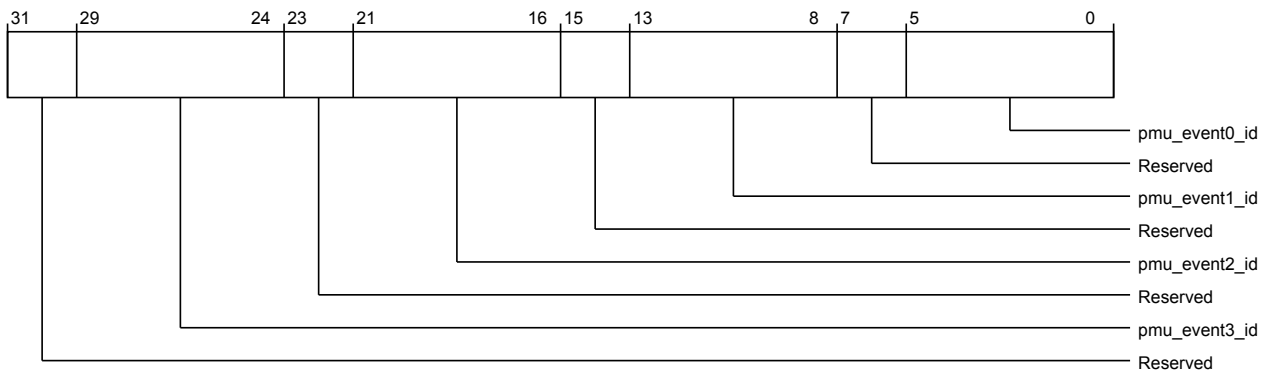


Figure 4-1221 `por_cxg_ra_por_cxg_ra_pmu_event_sel` (low)

The following table shows the `por_cxg_ra_pmu_event_sel` lower register bit assignments.

Table 4-1238 `por_cxg_ra_por_cxg_ra_pmu_event_sel` (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	<code>pmu_event3_id</code>	CXRA PMU Event 3 ID; see <code>pmu_event0_id</code> for encodings	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	<code>pmu_event2_id</code>	CXRA PMU Event 2 ID; see <code>pmu_event0_id</code> for encodings	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	<code>pmu_event1_id</code>	CXRA PMU Event 1 ID; see <code>pmu_event0_id</code> for encodings	RW	6'b0

Table 4-1238 `por_cxg_ra_por_cxg_ra_pmu_event_sel` (low) (continued)

Bits	Field name	Description	Type	Reset
7:6	Reserved	Reserved	RO	-
5:0	<code>pmu_event0_id</code>	CXRA PMU Event 0 ID 6'h00: No event 6'h01: Request Tracker (RHT) occupancy count overflow 6'h02: Snoop Tracker (SHT) occupancy count overflow 6'h03: Read Data Buffer (RDB) occupancy count overflow 6'h04: Write Data Buffer (WDB) occupancy count overflow 6'h05: Snoop Sink Buffer (SSB) occupancy count overflow 6'h06: CCIX RX broadcast snoops 6'h07: CCIX TX request chain 6'h08: CCIX TX request chain average length 6'h09: CHI internal RSP stall 6'h0A: CHI internal DAT stall 6'h0B: CCIX REQ Protocol credit Link 0 stall 6'h0C: CCIX REQ Protocol credit Link 1 stall 6'h0D: CCIX REQ Protocol credit Link 2 stall 6'h0E: CCIX DAT Protocol credit Link 0 stall 6'h0F: CCIX DAT Protocol credit Link 1 stall 6'h10: CCIX DAT Protocol credit Link 2 stall 6'h11: CHI external RSP stall 6'h12: CHI external DAT stall	RW	6'b0

`por_cxg_ra_cxprtcl_link0_ctl`

Functions as the CXRA CCIX Protocol Link 0 control register. Works with `por_cxg_ra_cxprtcl_link0_status`.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1000
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

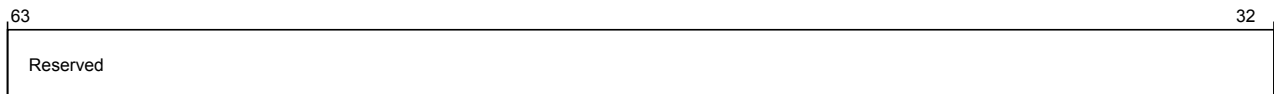


Figure 4-1222 por_cxg_ra_por_cxg_ra_cxprtcl_link0_ctl (high)

The following table shows the por_cxg_ra_cxprtcl_link0_ctl higher register bit assignments.

Table 4-1239 por_cxg_ra_por_cxg_ra_cxprtcl_link0_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

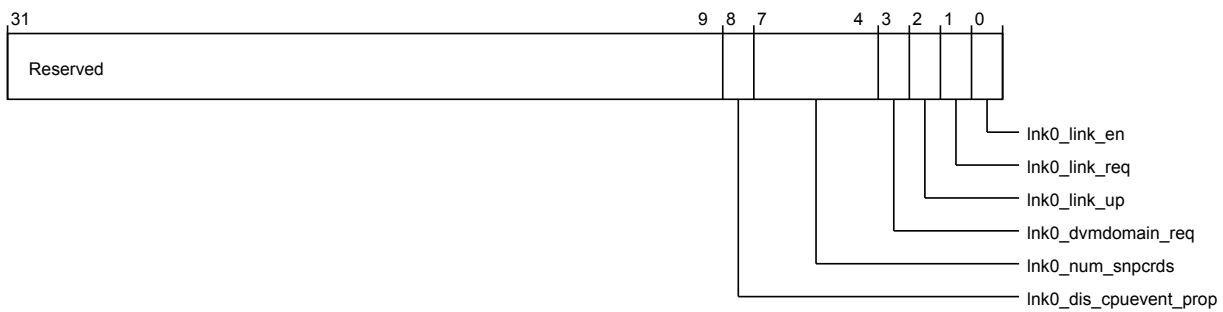


Figure 4-1223 por_cxg_ra_por_cxg_ra_cxprtcl_link0_ctl (low)

The following table shows the por_cxg_ra_cxprtcl_link0_ctl lower register bit assignments.

Table 4-1240 por_cxg_ra_por_cxg_ra_cxprtcl_link0_ctl (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	Ink0_dis_cpuevent_prop	When set, disables the propagation of CPU Events on CCIX Link 0 NOTE: This field is applicable only when SMP Mode enable parameter is set.	RW	1'b0
7:4	Ink0_num_snp crds	Controls the number of CCIX snoop credits assigned to Link 0 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	Ink0_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for CCIX Link 0	RW	1'b0

Table 4-1240 `por_cxg_ra_por_cxg_ra_cxprtcl_link0_ctl` (low) (continued)

Bits	Field name	Description	Type	Reset
2	<code>lnk0_link_up</code>	Link Up status. Software writes this register bit to indicate Link status after polling <code>Link_ACK</code> and <code>Link_DN</code> status in the remote agent 1'b0: Link is not Up. Software clears <code>Link_UP</code> when <code>Link_ACK</code> status is clear and <code>Link_DN</code> status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when <code>Link_UP</code> is clear 1'b1: Link is Up. Software sets <code>Link_UP</code> when <code>Link_ACK</code> status is set and <code>Link_DN</code> status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
1	<code>lnk0_link_req</code>	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in <code>Link_UP</code> state. 1'b1: Link Up request	RW	1'b0
0	<code>lnk0_link_en</code>	Enables CCIX Link 0 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

`por_cxg_ra_cxprtcl_link0_status`

Functions as the CXRA CCIX Protocol Link 0 status register. Works with `por_cxg_ra_cxprtcl_link0_ctl`.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h1008
Register reset	64'b0010
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

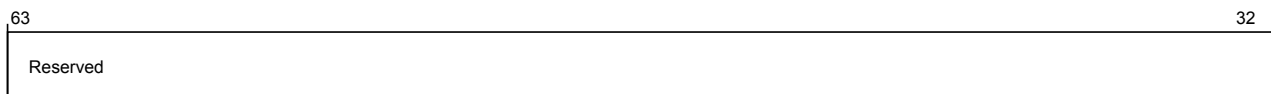


Figure 4-1224 `por_cxg_ra_por_cxg_ra_cxprtcl_link0_status` (high)

The following table shows the `por_cxg_ra_cxprtcl_link0_status` higher register bit assignments.

Table 4-1241 `por_cxg_ra_por_cxg_ra_cxprtcl_link0_status` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

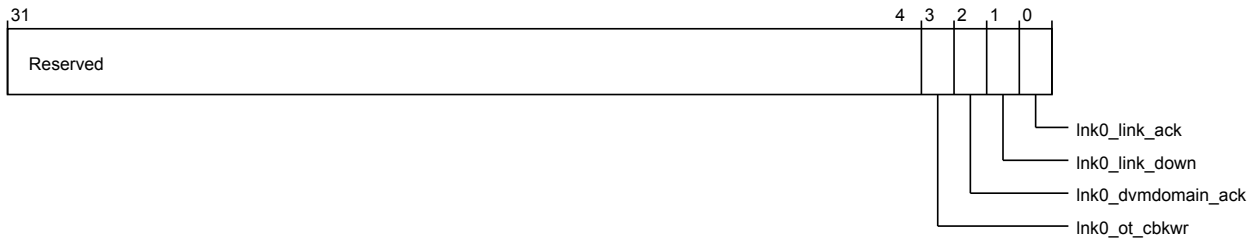


Figure 4-1225 por_cxg_ra_por_cxg_ra_cxprtcl_link0_status (low)

The following table shows the por_cxg_ra_cxprtcl_link0_status lower register bit assignments.

Table 4-1242 por_cxg_ra_por_cxg_ra_cxprtcl_link0_status (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	lnk0_ot_cbkwr	Provides status for outstanding CopyBack Write for CCIX Link0	RO	1'b0
2	lnk0_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for CCIX Link 0	RO	1'b0
1	lnk0_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk0_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops granting protocol credits and starts returning protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

por_cxg_ra_cxprtcl_link1_ctl

Functions as the CXRA CCIX Protocol Link 1 control register. Works with por_cxg_ra_cxprtcl_link1_status.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1010
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

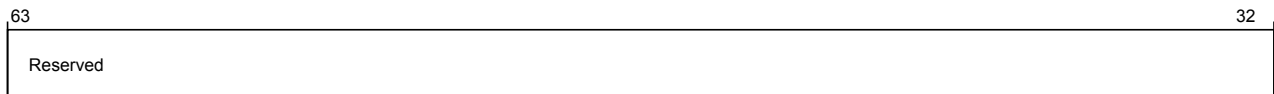


Figure 4-1226 por_cxg_ra_por_cxg_ra_cxprtcl_link1_ctl (high)

The following table shows the por_cxg_ra_cxprtcl_link1_ctl higher register bit assignments.

Table 4-1243 por_cxg_ra_por_cxg_ra_cxprtcl_link1_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

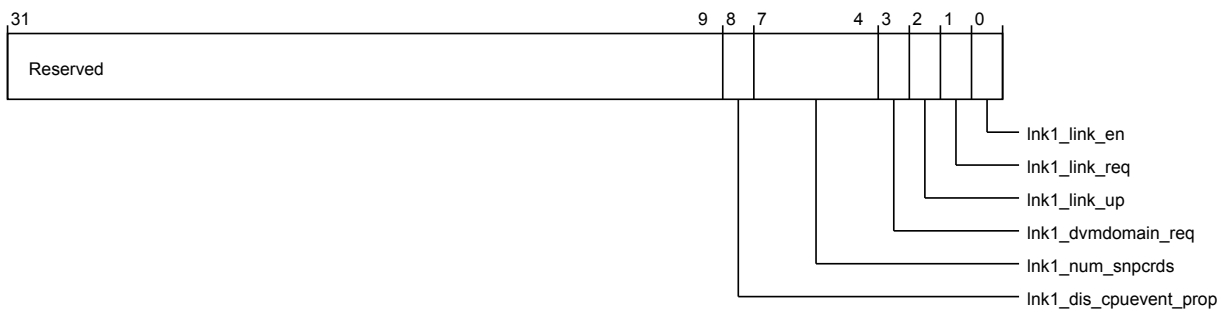


Figure 4-1227 por_cxg_ra_por_cxg_ra_cxprtcl_link1_ctl (low)

The following table shows the por_cxg_ra_cxprtcl_link1_ctl lower register bit assignments.

Table 4-1244 por_cxg_ra_por_cxg_ra_cxprtcl_link1_ctl (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	Inl1_dis_cpuevent_prop	When set, disables the propagation of CPU Events on CCIX Link 1 NOTE: This field is applicable only when SMP Mode enable parameter is set.	RW	1'b0
7:4	Inl1_num_snpdrds	Controls the number of CCIX snoop credits assigned to Link 1 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	Inl1_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for CCIX Link 1	RW	1'b0

Table 4-1244 `por_cxg_ra_por_cxg_ra_cxprtcl_link1_ctl` (low) (continued)

Bits	Field name	Description	Type	Reset
2	<code>lnk1_link_up</code>	Link Up status. Software writes this register bit to indicate Link status after polling <code>Link_ACK</code> and <code>Link_DN</code> status in the remote agent 1'b0: Link is not Up. Software clears <code>Link_UP</code> when <code>Link_ACK</code> status is clear and <code>Link_DN</code> status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when <code>Link_UP</code> is clear 1'b1: Link is Up. Software sets <code>Link_UP</code> when <code>Link_ACK</code> status is set and <code>Link_DN</code> status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
1	<code>lnk1_link_req</code>	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in <code>Link_UP</code> state. 1'b1: Link Up request	RW	1'b0
0	<code>lnk1_link_en</code>	Enables CCIX Link 1 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

`por_cxg_ra_cxprtcl_link1_status`

Functions as the CXRA CCIX Protocol Link 1 status register. Works with `por_cxg_ra_cxprtcl_link1_ctl`.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h1018
Register reset	64'b0010
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

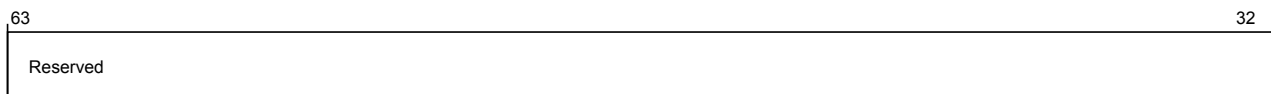


Figure 4-1228 `por_cxg_ra_por_cxg_ra_cxprtcl_link1_status` (high)

The following table shows the `por_cxg_ra_cxprtcl_link1_status` higher register bit assignments.

Table 4-1245 `por_cxg_ra_por_cxg_ra_cxprtcl_link1_status` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

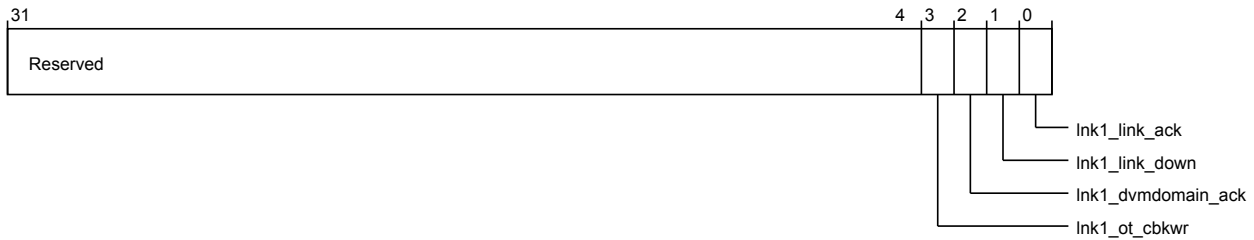


Figure 4-1229 por_cxg_ra_por_cxg_ra_cxprtcl_link1_status (low)

The following table shows the por_cxg_ra_cxprtcl_link1_status lower register bit assignments.

Table 4-1246 por_cxg_ra_por_cxg_ra_cxprtcl_link1_status (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	lnk1_ot_cbkwr	Provides status for outstanding CopyBack Write for CCIX Link 1	RO	1'b0
2	lnk1_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for CCIX Link 1	RO	1'b0
1	lnk1_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk1_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

por_cxg_ra_cxprtcl_link2_ctl

Functions as the CXRA CCIX Protocol Link 2 control register. Works with por_cxg_ra_cxprtcl_link2_status.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1020
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

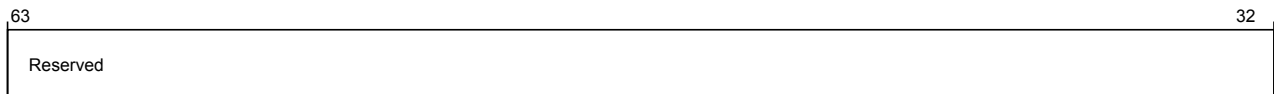


Figure 4-1230 por_cxg_ra_por_cxg_ra_cxprtcl_link2_ctl (high)

The following table shows the por_cxg_ra_cxprtcl_link2_ctl higher register bit assignments.

Table 4-1247 por_cxg_ra_por_cxg_ra_cxprtcl_link2_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

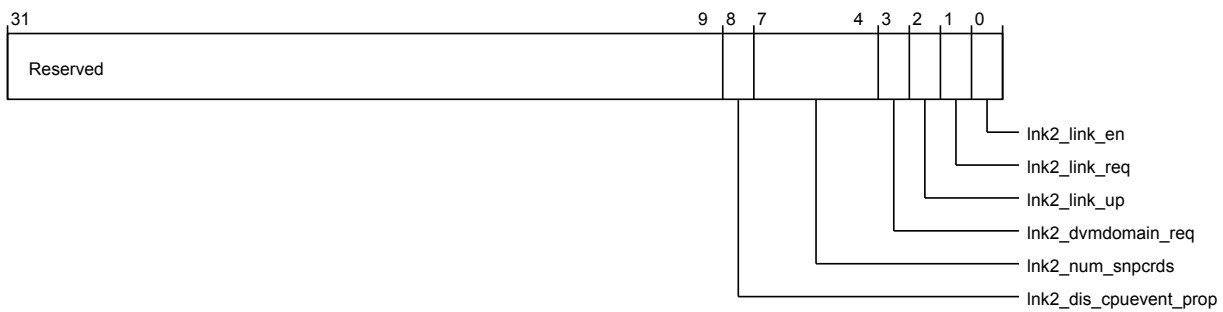


Figure 4-1231 por_cxg_ra_por_cxg_ra_cxprtcl_link2_ctl (low)

The following table shows the por_cxg_ra_cxprtcl_link2_ctl lower register bit assignments.

Table 4-1248 por_cxg_ra_por_cxg_ra_cxprtcl_link2_ctl (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	Inlk2_dis_cpuevent_prop	When set, disables the propagation of CPU Events on CCIX Link 2 NOTE: This field is applicable only when SMP Mode enable parameter is set.	RW	1'b0
7:4	Inlk2_num_snp crds	Controls the number of CCIX snoop credits assigned to Link 2 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	Inlk2_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for CCIX Link 2	RW	1'b0

Table 4-1248 `por_cxg_ra_por_cxg_ra_cxprtcl_link2_ctl` (low) (continued)

Bits	Field name	Description	Type	Reset
2	<code>lnk2_link_up</code>	Link Up status. Software writes this register bit to indicate Link status after polling <code>Link_ACK</code> and <code>Link_DN</code> status in the remote agent 1'b0: Link is not Up. Software clears <code>Link_UP</code> when <code>Link_ACK</code> status is clear and <code>Link_DN</code> status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when <code>Link_UP</code> is clear 1'b1: Link is Up. Software sets <code>Link_UP</code> when <code>Link_ACK</code> status is set and <code>Link_DN</code> status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
1	<code>lnk2_link_req</code>	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in <code>Link_UP</code> state. 1'b1: Link Up request	RW	1'b0
0	<code>lnk2_link_en</code>	Enables CCIX Link 2 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

`por_cxg_ra_cxprtcl_link2_status`

Functions as the CXRA CCIX Protocol Link 2 status register. Works with `por_cxg_ra_cxprtcl_link2_ctl`.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h1028
Register reset	64'b0010
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1232 `por_cxg_ra_por_cxg_ra_cxprtcl_link2_status` (high)

The following table shows the `por_cxg_ra_cxprtcl_link2_status` higher register bit assignments.

Table 4-1249 `por_cxg_ra_por_cxg_ra_cxprtcl_link2_status` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

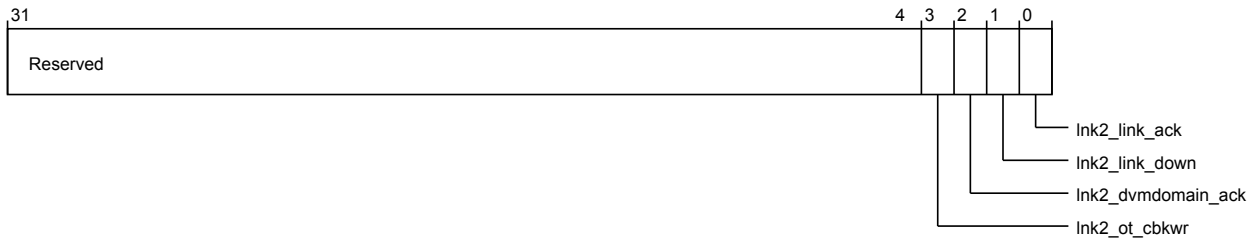


Figure 4-1233 por_cxg_ra_por_cxg_ra_cxprtcl_link2_status (low)

The following table shows the por_cxg_ra_cxprtcl_link2_status lower register bit assignments.

Table 4-1250 por_cxg_ra_por_cxg_ra_cxprtcl_link2_status (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	lnk2_ot_cbkwr	Provides status for outstanding CopyBack Write for CCIX Link2	RO	1'b0
2	lnk2_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for CCIX Link 2	RO	1'b0
1	lnk2_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk2_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

4.3.13 CXLA configuration registers

This section lists the CXLA configuration registers.

por_cxla_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

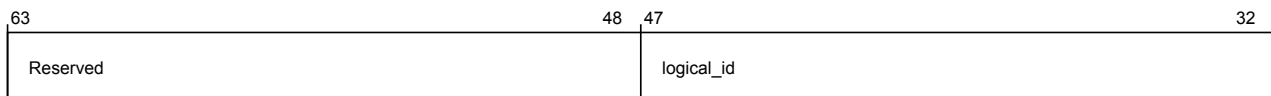


Figure 4-1234 por_cxla_por_cxla_node_info (high)

The following table shows the por_cxla_node_info higher register bit assignments.

Table 4-1251 por_cxla_por_cxla_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

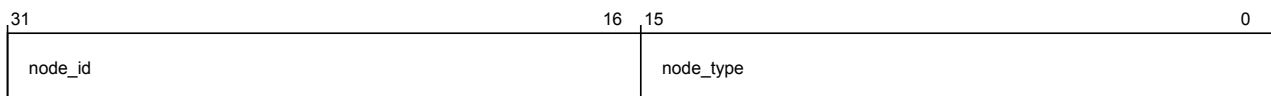


Figure 4-1235 por_cxla_por_cxla_node_info (low)

The following table shows the por_cxla_node_info lower register bit assignments.

Table 4-1252 por_cxla_por_cxla_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0102

por_cxla_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-1236 por_cxla_por_cxla_child_info (high)

The following table shows the por_cxla_child_info higher register bit assignments.

Table 4-1253 por_cxla_por_cxla_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

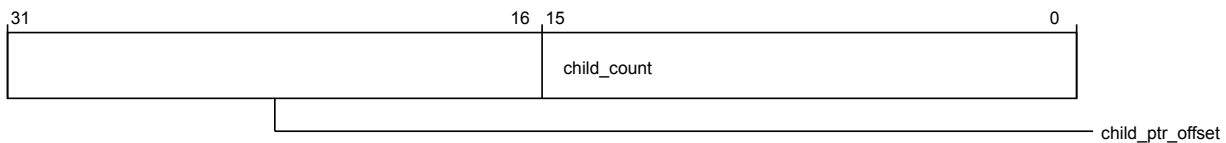


Figure 4-1237 por_cxla_por_cxla_child_info (low)

The following table shows the por_cxla_child_info lower register bit assignments.

Table 4-1254 por_cxla_por_cxla_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_cxla_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type	RW
Register width (Bits)	64

Address offset	14'h980
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

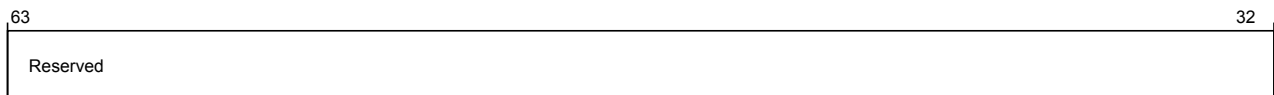


Figure 4-1238 por_cxla_secure_register_groups_override (high)

The following table shows the por_cxla_secure_register_groups_override higher register bit assignments.

Table 4-1255 por_cxla_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

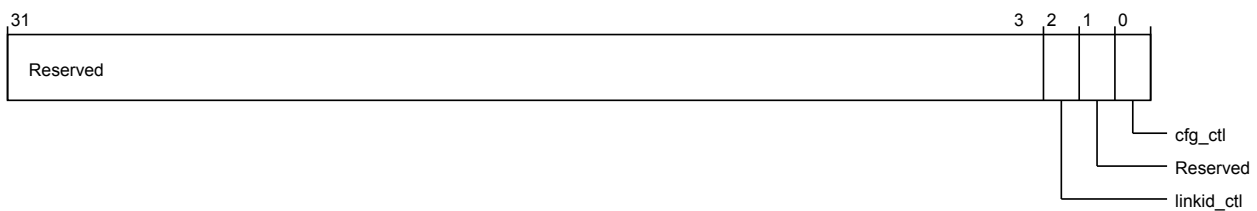


Figure 4-1239 por_cxla_secure_register_groups_override (low)

The following table shows the por_cxla_secure_register_groups_override lower register bit assignments.

Table 4-1256 por_cxla_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	linkid_ctl	Allows non-secure access to secure LA Link ID registers	RW	1'b0
1	Reserved	Reserved	RO	-
0	cfg_ctl	Allows non-secure access to secure configuration control register	RW	1'b0

por_cxla_unit_info

Provides component identification information for CXLA.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-1240 por_cxla_por_cxla_unit_info (high)

The following table shows the por_cxla_unit_info higher register bit assignments.

Table 4-1257 por_cxla_por_cxla_unit_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

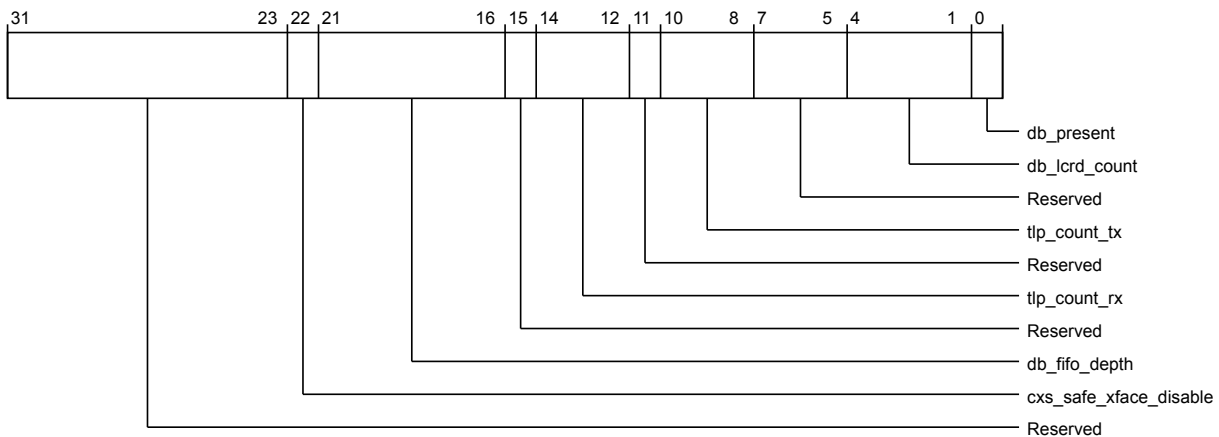


Figure 4-1241 por_cxla_por_cxla_unit_info (low)

The following table shows the por_cxla_unit_info lower register bit assignments.

Table 4-1258 por_cxla_por_cxla_unit_info (low)

Bits	Field name	Description	Type	Reset
31:23	Reserved	Reserved	RO	-
22	cxs_safe_xface_disable	CXS safe interface disable	RO	Configuration dependent
21:16	db_fifo_depth	FIFO Depth in CXLA Domain Bridges - CXDB, PDB	RO	Configuration dependent
15	Reserved	Reserved	RO	-
14:12	tlp_count_rx	Maximum number of TLPs supported by RX TLP buffer	RO	Configuration dependent

Table 4-1258 `por_cxla_por_cxla_unit_info` (low) (continued)

Bits	Field name	Description	Type	Reset
11	Reserved	Reserved	RO	-
10:8	tlp_count_tx	Maximum number of TLPs supported by TX TLP buffer	RO	Configuration dependent
7:5	Reserved	Reserved	RO	-
4:1	db_lcrd_count	Number of flit credits between CXG and CXLA	RO	Configuration dependent
0	db_present	DB present in CXLA	RO	Configuration dependent

por_cxla_aux_ctl

Functions as the auxiliary control register for CXLA.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

[illegible]

Usage constraints	Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.
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The following image shows the higher register bit assignments.

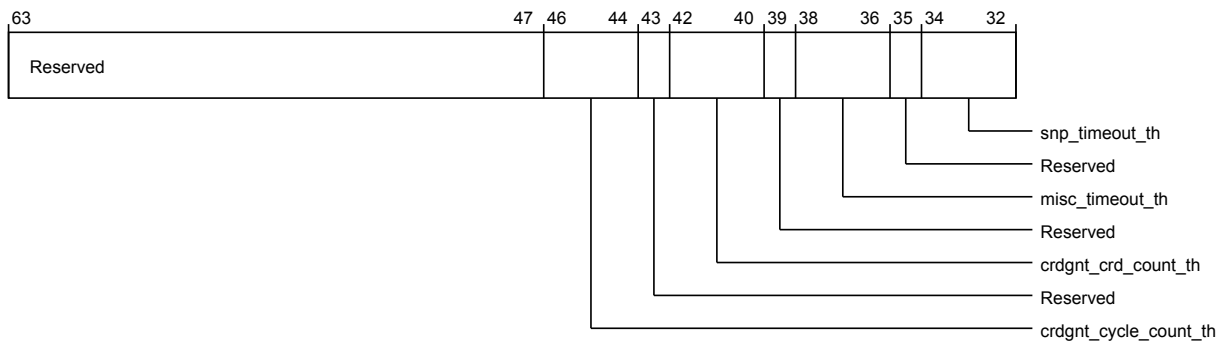


Figure 4-1242 `por_cxla_por_cxla_aux_ctl` (high)

The following table shows the `por_cxla_aux_ctl` higher register bit assignments.

Table 4-1259 **por_cxla_por_cxla_aux_ctl** (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:44	crdgnt_cycle_count_th	Maximum number of cycles that need to be elapsed since the end of previous TLP to send a credit grant message 3'b000: 32 cycles 3'b001: 64 cycles 3'b010: 128 cycles 3'b011: 256 cycles	RW	3'b010
43	Reserved	Reserved	RO	-
42:40	crdgnt_crd_count_th	Maximum number of credits that need to be accumulated to send a credit grant message 3'b000: 16 credits 3'b001: 32 credits 3'b010: 64 credits 3'b011: 128 credits	RW	3'b010
39	Reserved	Reserved	RO	-
38:36	misc_timeout_th	Maximum number of cycles a MISC message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
35	Reserved	Reserved	RO	-
34:32	snp_timeout_th	Maximum number of cycles a SNP message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000

The following image shows the lower register bit assignments.

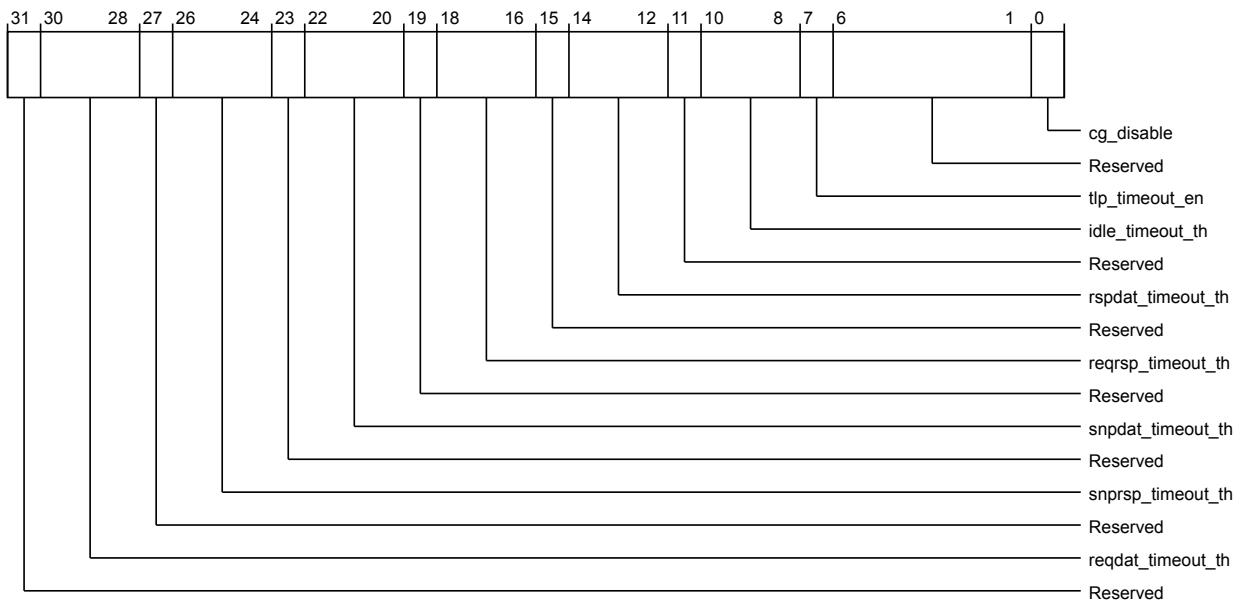


Figure 4-1243 por_cxla_por_cxla_aux_ctl (low)

The following table shows the por_cxla_aux_ctl lower register bit assignments.

Table 4-1260 por_cxla_por_cxla_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	reqdat_timeout_th	Maximum number of cycles a REQDAT message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
27	Reserved	Reserved	RO	-
26:24	snprsp_timeout_th	Maximum number of cycles a SNPRSP message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
23	Reserved	Reserved	RO	-

Table 4-1260 `por_cxla_por_cxla_aux_ctl` (low) (continued)

Bits	Field name	Description	Type	Reset
22:20	<code>snpdattimeout_th</code>	Maximum number of cycles a SNPDAT message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as <code>idle_timeout_th</code> 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
19	Reserved	Reserved	RO	-
18:16	<code>reqrsp_timeout_th</code>	Maximum number of cycles a REQRSP message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as <code>idle_timeout_th</code> 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
15	Reserved	Reserved	RO	-
14:12	<code>rspdat_timeout_th</code>	Maximum number of cycles a RSPDAT message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as <code>idle_timeout_th</code> 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
11	Reserved	Reserved	RO	-
10:8	<code>idle_timeout_th</code>	Maximum number of idle cycles a TLP waits for a message to pack to complete/end the TLP; applies for message packing 3'b000: 4 cycles 3'b001: 8 cycles 3'b010: 16 cycles 3'b011: 32 cycles	RW	3'b001
7	<code>tlp_timeout_en</code>	Enables TLP timeout based on thresholds set for each message type; doesn't apply for idle timeout; applies for message packing	RW	1'b1
6:1	Reserved	Reserved	RO	-
0	<code>cg_disable</code>	Disables CXLA architectural clock gates	RW	1'b0

por_cxla_ccix_prop_capabilities

Contains CCIX-supported properties.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'hC00
Register reset	Configuration dependent
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

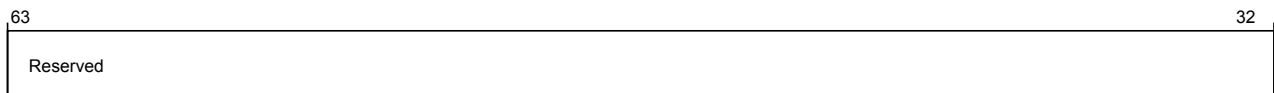


Figure 4-1244 por_cxla_por_cxla_ccix_prop_capabilities (high)

The following table shows the por_cxla_ccix_prop_capabilities higher register bit assignments.

Table 4-1261 por_cxla_por_cxla_ccix_prop_capabilities (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

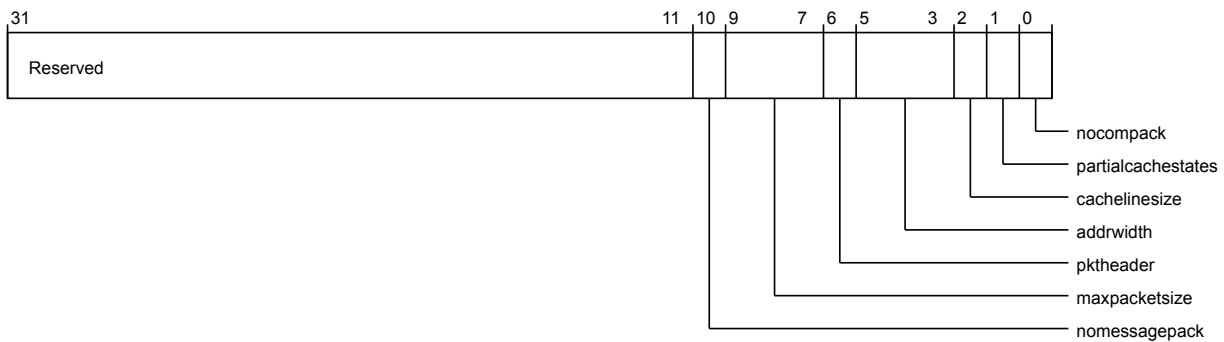


Figure 4-1245 por_cxla_por_cxla_ccix_prop_capabilities (low)

The following table shows the por_cxla_ccix_prop_capabilities lower register bit assignments.

Table 4-1262 por_cxla_por_cxla_ccix_prop_capabilities (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10	nomessagepack	No message packing only supported 1'b0: False 1'b1: True	RO	Configuration dependent
9:7	maxpacketsize	Maximum packet size supported 3'b000: 128B 3'b001: 256B 3'b010: 512B	RO	Configuration dependent
6	pkthead	Packet header supported 1'b0: PCIe compatible header 1'b1: Optimized header	RO	Configuration dependent
5:3	addrwidth	Address width supported 3'b000: 48b 3'b001: 52b 3'b010: 56b 3'b011: 60b 3'b100: 64b	RO	Configuration dependent
2	cachelinesize	Cache line size supported 1'b0: 64B 1'b1: 128B	RO	Configuration dependent
1	partialcachestates	Partial cache states supported 1'b0: False 1'b1: True	RO	Configuration dependent
0	nocompack	No CompAck supported 1'b0: False 1'b1: True	RO	Configuration dependent

por_cxla_ccix_prop_configured

Contains CCIX-configured properties.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC08
Register reset	64'b100000000000

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1246 por_cxla_por_cxla_ccix_prop_configured (high)

The following table shows the por_cxla_ccix_prop_configured higher register bit assignments.

Table 4-1263 por_cxla_por_cxla_ccix_prop_configured (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

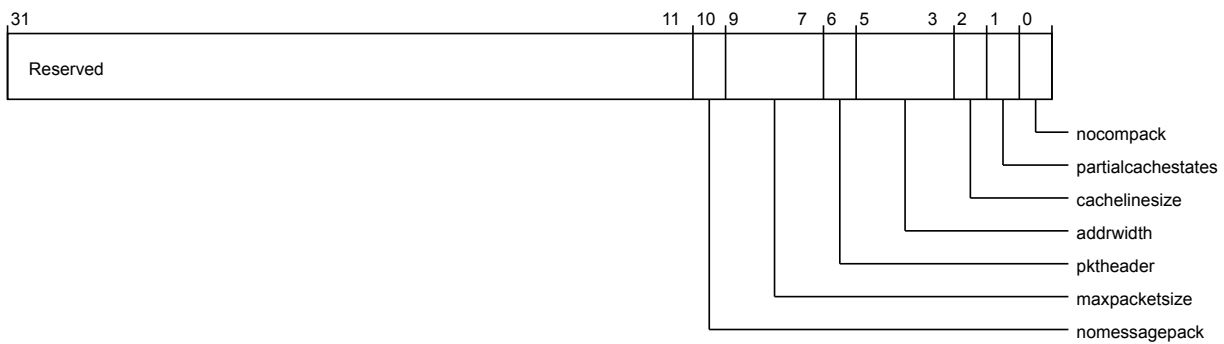


Figure 4-1247 por_cxla_por_cxla_ccix_prop_configured (low)

The following table shows the por_cxla_ccix_prop_configured lower register bit assignments.

Table 4-1264 por_cxla_por_cxla_ccix_prop_configured (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10	nomessagepack	No message packing configured 1'b0: False 1'b1: True	RW	1'b1
9:7	maxpacketsize	Maximum packet size configured 3'b000: 128B 3'b001: 256B 3'b010: 512B	RW	3'b000

Table 4-1264 `por_cxla_por_cxla_ccix_prop_configured (low)` (continued)

Bits	Field name	Description	Type	Reset
6	pktheaderr	Packet header configured 1'b0: PCIe compatible header 1'b1: Optimized header	RW	1'b0
5:3	addrwidth	Address width configured 3'b000: 48b 3'b001: 52b 3'b010: 56b 3'b011: 60b 3'b100: 64b	RW	3'b000
2	cachelinesize	Cache line size configured 1'b0: 64B 1'b1: 128B	RW	1'b0
1	partialcachestates	Partial cache states configured 1'b0: False 1'b1: True	RW	1'b0
0	nocompack	No CompAck configured 1'b0: False 1'b1: True	RW	1'b0

`por_cxla_tx_cxs_attr_capabilities`

Contains TX CXS supported attributes.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'hC10
Register reset	Configuration dependent
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

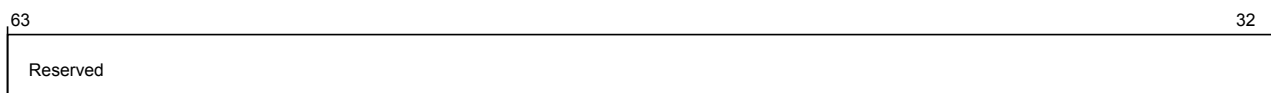


Figure 4-1248 `por_cxla_por_cxla_tx_cxs_attr_capabilities (high)`

The following table shows the `por_cxla_tx_cxs_attr_capabilities` higher register bit assignments.

Table 4-1265 por_cxla_por_cxla_tx_cxs_attr_capabilities (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

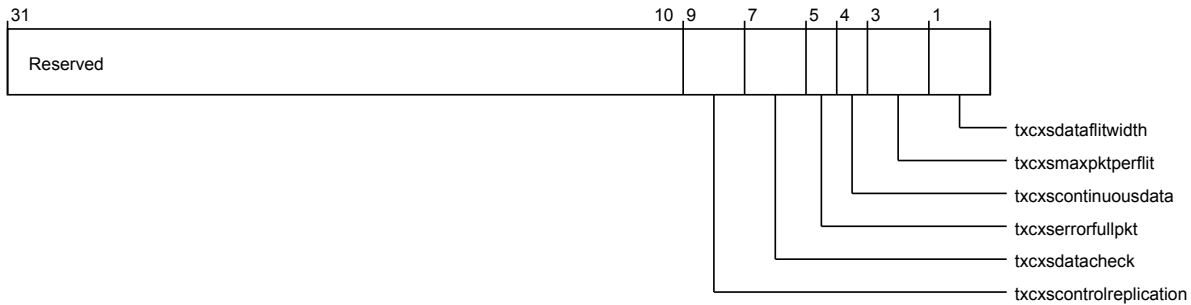


Figure 4-1249 por_cxla_por_cxla_tx_cxs_attr_capabilities (low)

The following table shows the `por_cxla_tx_cxs_attr_capabilities` lower register bit assignments.

Table 4-1266 por_cxla_por_cxla_tx_cxs_attr_capabilities (low)

Bits	Field name	Description	Type	Reset
31:10	Reserved	Reserved	RO	-
9:8	<code>txcscontrolreplication</code>	TX CXS control replication supported 2'b00: None 2'b01: Duplicate 2'b10: Triplicate	RO	Configuration dependent
7:6	<code>txcsdatacheck</code>	TX CXS datacheck supported 2'b00: None 2'b01: Parity 2'b10: SECEDED	RO	Configuration dependent
5	<code>txcserrorfullpkt</code>	TX CXS error full packet supported 1'b0: False 1'b1: True	RO	Configuration dependent
4	<code>txcscontinuousdata</code>	TX CXS continuous data supported 1'b0: False 1'b1: True	RO	Configuration dependent

Table 4-1266 por_cxla_por_cxla_tx_cxs_attr_capabilities (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	txcxsmxpktperflit	TX CXS maximum packets per flit supported 2'b00: 2 2'b01: 3 2'b10: 4	RO	Configuration dependent
1:0	txcxldataflitwidth	TX CXS data flit width supported 2'b00: 256b 2'b01: 512b 2'b10: 1024b	RO	Configuration dependent

por_cxla_rx_cxs_attr_capabilities

Contains RX CXS supported attributes.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'hC18

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

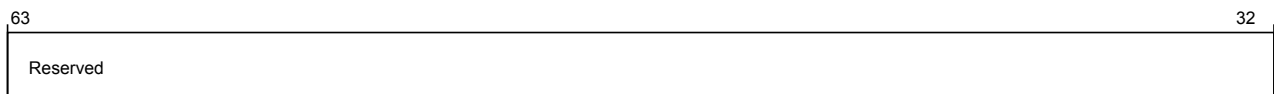


Figure 4-1250 por_cxla_por_cxla_rx_cxs_attr_capabilities (high)

The following table shows the por_cxla_rx_cxs_attr_capabilities higher register bit assignments.

Table 4-1267 por_cxla_por_cxla_rx_cxs_attr_capabilities (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

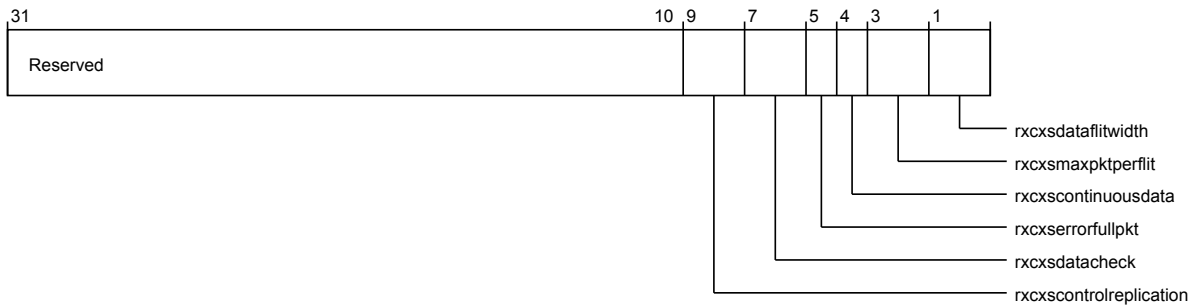


Figure 4-1251 `por_cxla_por_cxla_rx_cxs_attr_capabilities (low)`

The following table shows the `por_cxla_rx_cxs_attr_capabilities` lower register bit assignments.

Table 4-1268 `por_cxla_por_cxla_rx_cxs_attr_capabilities (low)`

Bits	Field name	Description	Type	Reset
31:10	Reserved	Reserved	RO	-
9:8	<code>rxcscontrolreplication</code>	RX CXS control replication supported 2'b00: None 2'b01: Duplicate 2'b10: Triplicate	RO	Configuration dependent
7:6	<code>rxcsdatacheck</code>	RX CXS datacheck supported 2'b00: None 2'b01: Parity 2'b10: SECEDED	RO	Configuration dependent
5	<code>rxcserrorfullpkt</code>	RX CXS error full packet supported 1'b0: False 1'b1: True	RO	Configuration dependent
4	<code>rxcscontinuousdata</code>	RX CXS continuous data supported 1'b0: False 1'b1: True	RO	Configuration dependent
3:2	<code>rxcsmaxpktperflit</code>	RX CXS maximum packets per flit supported 2'b00: 2 2'b01: 3 2'b10: 4	RO	Configuration dependent
1:0	<code>rxcsdataflitwidth</code>	RX CXS data flit width supported 2'b00: 256b 2'b01: 512b 2'b10: 1024b	RO	Configuration dependent

por_cxla_agentid_to_linkid_reg0

Specifies the mapping of Agent ID to Link ID for Agent IDs 0 to 7.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC30
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

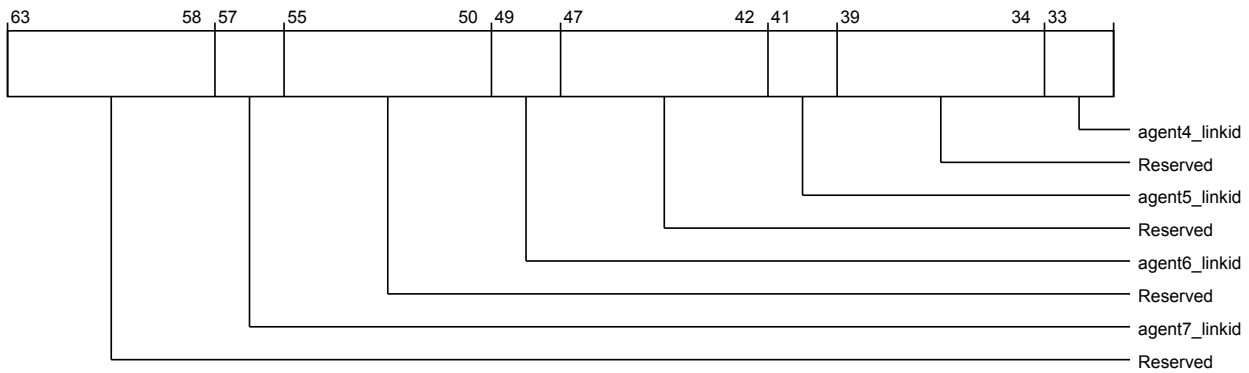


Figure 4-1252 por_cxla_por_cxla_agentid_to_linkid_reg0 (high)

The following table shows the por_cxla_agentid_to_linkid_reg0 higher register bit assignments.

Table 4-1269 por_cxla_por_cxla_agentid_to_linkid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent7_linkid	Specifies the Link ID for Agent ID 7	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent6_linkid	Specifies the Link ID for Agent ID 6	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent5_linkid	Specifies the Link ID for Agent ID 5	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent4_linkid	Specifies the Link ID for Agent ID 4	RW	2'h0

The following image shows the lower register bit assignments.

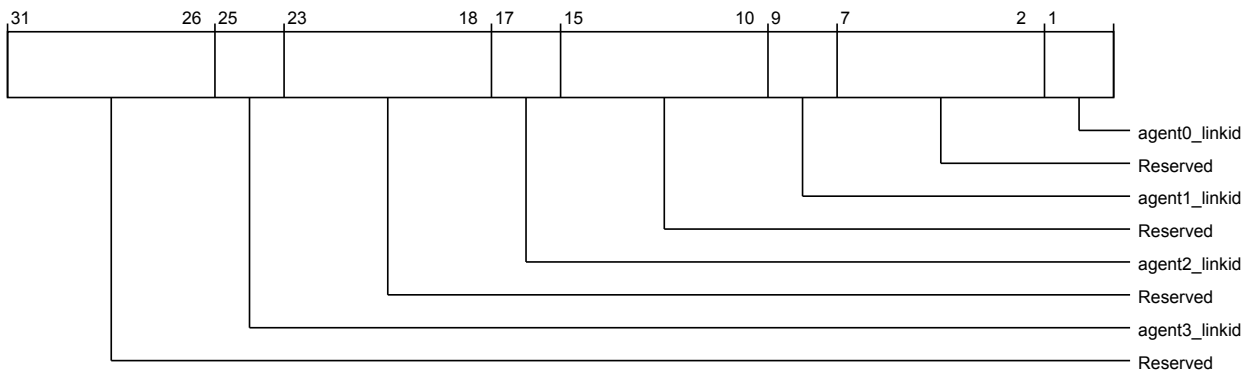


Figure 4-1253 por_cxla_por_cxla_agentid_to_linkid_reg0 (low)

The following table shows the por_cxla_agentid_to_linkid_reg0 lower register bit assignments.

Table 4-1270 por_cxla_por_cxla_agentid_to_linkid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent3_linkid	Specifies the Link ID for Agent ID 3	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent2_linkid	Specifies the Link ID for Agent ID 2	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent1_linkid	Specifies the Link ID for Agent ID 1	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent0_linkid	Specifies the Link ID for Agent ID 0	RW	2'h0

por_cxla_agentid_to_linkid_reg1

Specifies the mapping of Agent ID to Link ID for Agent IDs 8 to 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC38
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

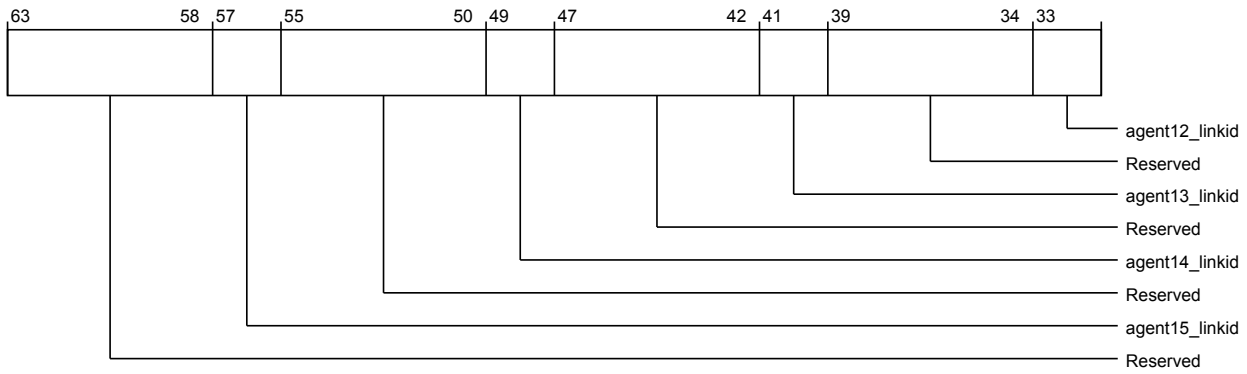


Figure 4-1254 por_cxla_por_cxla_agentid_to_linkid_reg1 (high)

The following table shows the por_cxla_agentid_to_linkid_reg1 higher register bit assignments.

Table 4-1271 por_cxla_por_cxla_agentid_to_linkid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent15_linkid	Specifies the Link ID for Agent ID 15	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent14_linkid	Specifies the Link ID for Agent ID 14	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent13_linkid	Specifies the Link ID for Agent ID 13	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent12_linkid	Specifies the Link ID for Agent ID 12	RW	2'h0

The following image shows the lower register bit assignments.

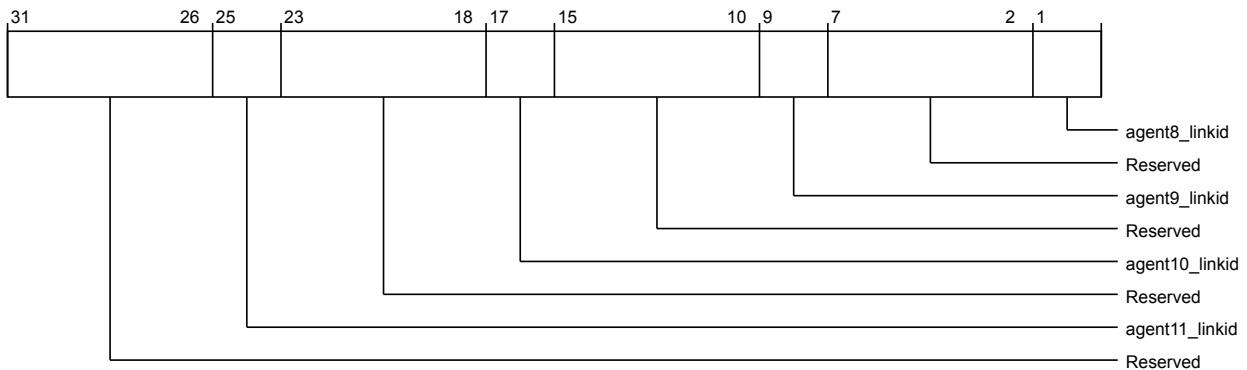


Figure 4-1255 por_cxla_por_cxla_agentid_to_linkid_reg1 (low)

The following table shows the por_cxla_agentid_to_linkid_reg1 lower register bit assignments.

Table 4-1272 `por_cxla_por_cxla_agentid_to_linkid_reg1` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent11_linkid	Specifies the Link ID for Agent ID 11	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent10_linkid	Specifies the Link ID for Agent ID 10	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent9_linkid	Specifies the Link ID for Agent ID 9	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent8_linkid	Specifies the Link ID for Agent ID 8	RW	2'h0

`por_cxla_agentid_to_linkid_reg2`

Specifies the mapping of Agent ID to Link ID for Agent IDs 16 to 23.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC40
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxla_secure_register_groups_override.linkid_ctl</code>

The following image shows the higher register bit assignments.

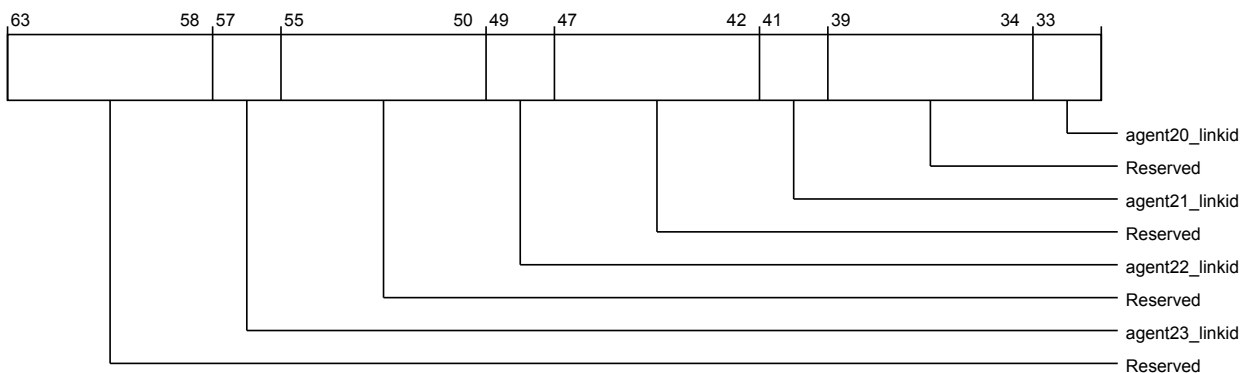


Figure 4-1256 `por_cxla_por_cxla_agentid_to_linkid_reg2` (high)

The following table shows the `por_cxla_agentid_to_linkid_reg2` higher register bit assignments.

Table 4-1273 por_cxla_por_cxla_agentid_to_linkid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent23_linkid	Specifies the Link ID for Agent ID 23	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent22_linkid	Specifies the Link ID for Agent ID 22	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent21_linkid	Specifies the Link ID for Agent ID 21	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent20_linkid	Specifies the Link ID for Agent ID 20	RW	2'h0

The following image shows the lower register bit assignments.

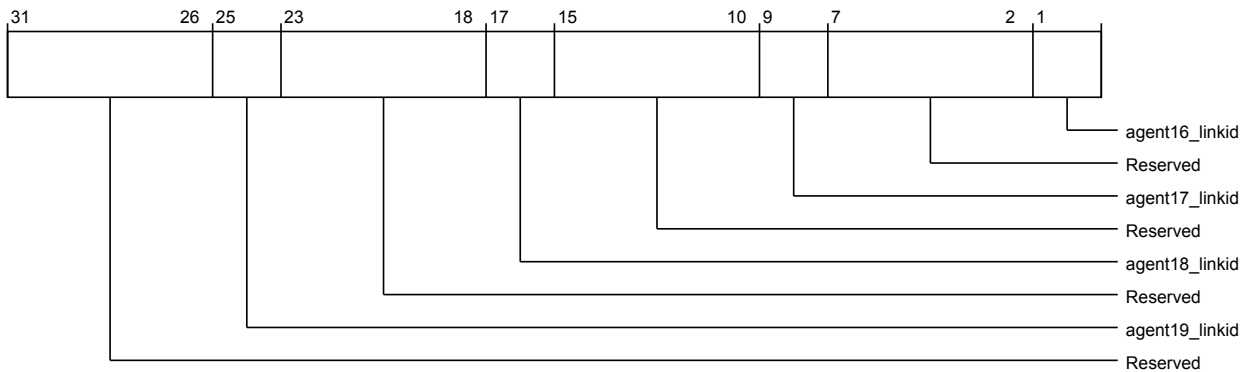


Figure 4-1257 por_cxla_por_cxla_agentid_to_linkid_reg2 (low)

The following table shows the `por_cxla_agentid_to_linkid_reg2` lower register bit assignments.

Table 4-1274 por_cxla_por_cxla_agentid_to_linkid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent19_linkid	Specifies the Link ID for Agent ID 19	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent18_linkid	Specifies the Link ID for Agent ID 18	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent17_linkid	Specifies the Link ID for Agent ID 17	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent16_linkid	Specifies the Link ID for Agent ID 16	RW	2'h0

por_cxla_agentid_to_linkid_reg3

Specifies the mapping of Agent ID to Link ID for Agent IDs 24 to 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC48
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

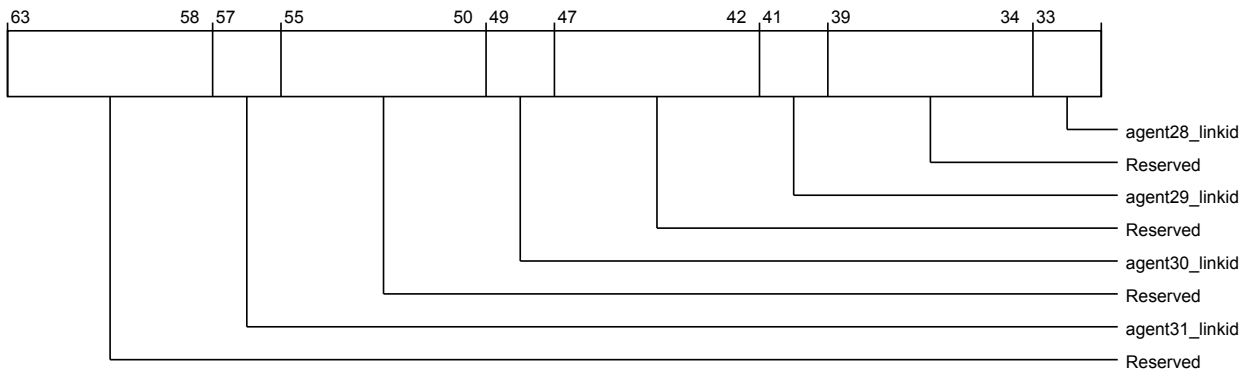


Figure 4-1258 por_cxla_por_cxla_agentid_to_linkid_reg3 (high)

The following table shows the por_cxla_agentid_to_linkid_reg3 higher register bit assignments.

Table 4-1275 por_cxla_por_cxla_agentid_to_linkid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent31_linkid	Specifies the Link ID for Agent ID 31	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent30_linkid	Specifies the Link ID for Agent ID 30	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent29_linkid	Specifies the Link ID for Agent ID 29	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent28_linkid	Specifies the Link ID for Agent ID 28	RW	2'h0

The following image shows the lower register bit assignments.

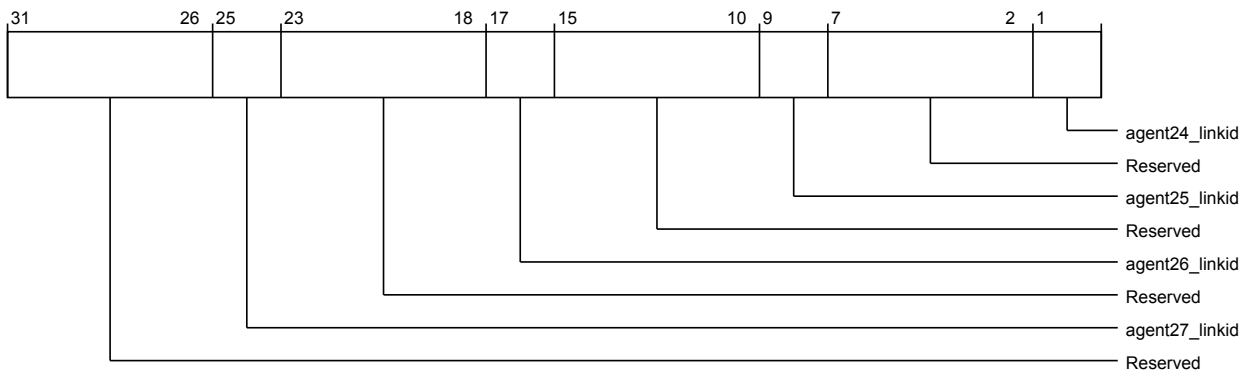


Figure 4-1259 por_cxla_por_cxla_agentid_to_linkid_reg3 (low)

The following table shows the por_cxla_agentid_to_linkid_reg3 lower register bit assignments.

Table 4-1276 por_cxla_por_cxla_agentid_to_linkid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent27_linkid	Specifies the Link ID for Agent ID 27	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent26_linkid	Specifies the Link ID for Agent ID 26	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent25_linkid	Specifies the Link ID for Agent ID 25	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent24_linkid	Specifies the Link ID for Agent ID 24	RW	2'h0

por_cxla_agentid_to_linkid_reg4

Specifies the mapping of Agent ID to Link ID for Agent IDs 32 to 39.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC50
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

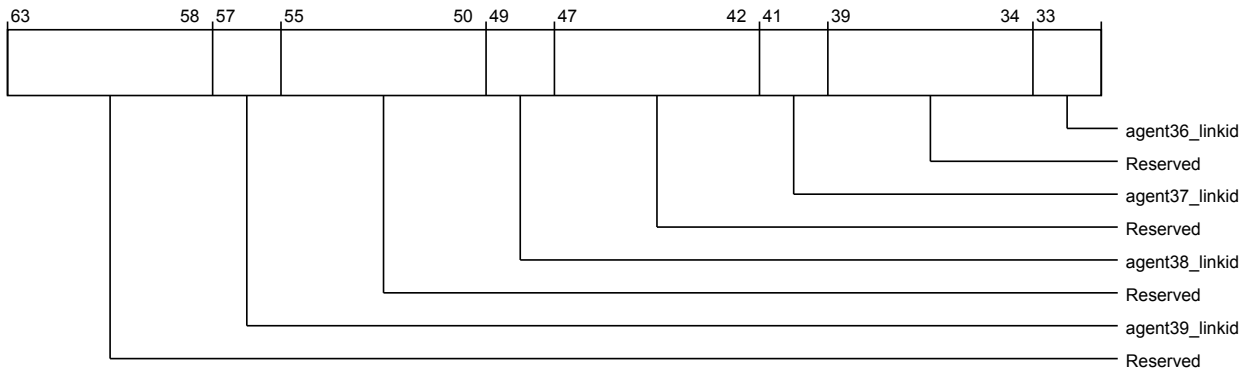


Figure 4-1260 por_cxla_por_cxla_agentid_to_linkid_reg4 (high)

The following table shows the por_cxla_agentid_to_linkid_reg4 higher register bit assignments.

Table 4-1277 por_cxla_por_cxla_agentid_to_linkid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent39_linkid	Specifies the Link ID for Agent ID 39	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent38_linkid	Specifies the Link ID for Agent ID 38	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent37_linkid	Specifies the Link ID for Agent ID 37	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent36_linkid	Specifies the Link ID for Agent ID 36	RW	2'h0

The following image shows the lower register bit assignments.

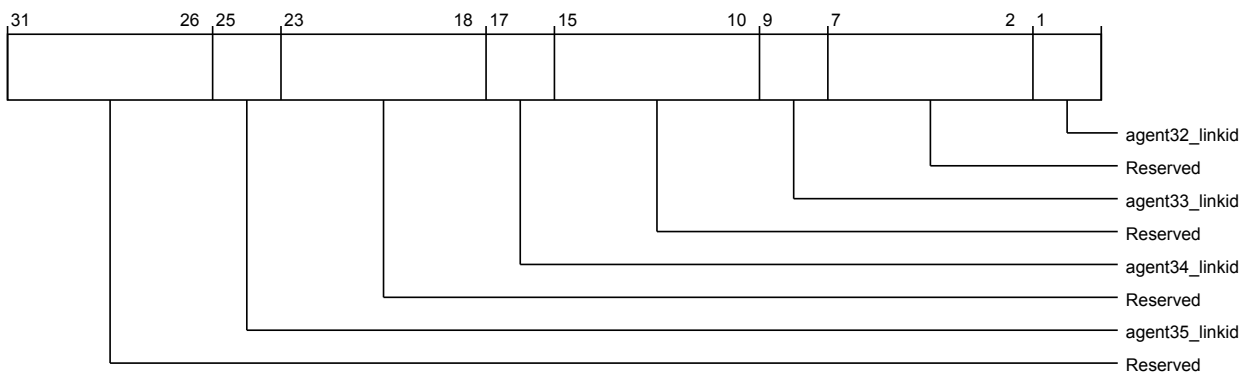


Figure 4-1261 por_cxla_por_cxla_agentid_to_linkid_reg4 (low)

The following table shows the por_cxla_agentid_to_linkid_reg4 lower register bit assignments.

Table 4-1278 `por_cxla_por_cxla_agentid_to_linkid_reg4` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent35_linkid	Specifies the Link ID for Agent ID 35	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent34_linkid	Specifies the Link ID for Agent ID 34	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent33_linkid	Specifies the Link ID for Agent ID 33	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent32_linkid	Specifies the Link ID for Agent ID 32	RW	2'h0

`por_cxla_agentid_to_linkid_reg5`

Specifies the mapping of Agent ID to Link ID for Agent IDs 40 to 47.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC58
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	<code>por_cxla_secure_register_groups_override.linkid_ctl</code>

The following image shows the higher register bit assignments.

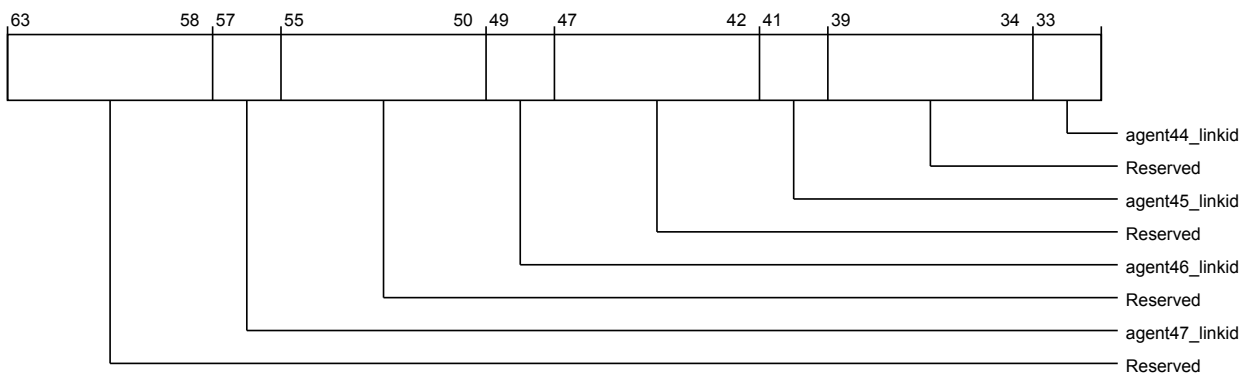


Figure 4-1262 `por_cxla_por_cxla_agentid_to_linkid_reg5` (high)

The following table shows the `por_cxla_agentid_to_linkid_reg5` higher register bit assignments.

Table 4-1279 `por_cxla_por_cxla_agentid_to_linkid_reg5` (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent47_linkid	Specifies the Link ID for Agent ID 47	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent46_linkid	Specifies the Link ID for Agent ID 46	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent45_linkid	Specifies the Link ID for Agent ID 45	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent44_linkid	Specifies the Link ID for Agent ID 44	RW	2'h0

The following image shows the lower register bit assignments.

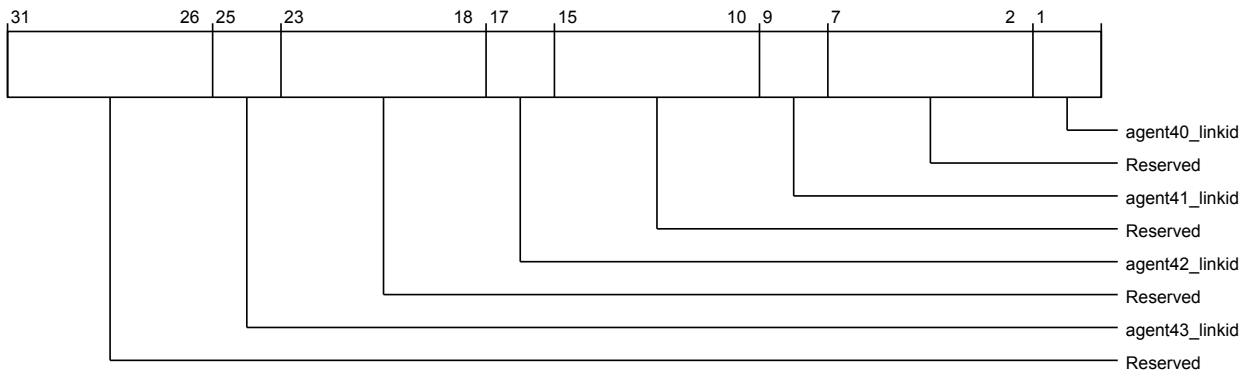


Figure 4-1263 `por_cxla_por_cxla_agentid_to_linkid_reg5` (low)

The following table shows the `por_cxla_agentid_to_linkid_reg5` lower register bit assignments.

Table 4-1280 `por_cxla_por_cxla_agentid_to_linkid_reg5` (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent43_linkid	Specifies the Link ID for Agent ID 43	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent42_linkid	Specifies the Link ID for Agent ID 42	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent41_linkid	Specifies the Link ID for Agent ID 41	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent40_linkid	Specifies the Link ID for Agent ID 40	RW	2'h0

por_cxla_agentid_to_linkid_reg6

Specifies the mapping of Agent ID to Link ID for Agent IDs 48 to 55.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC60
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

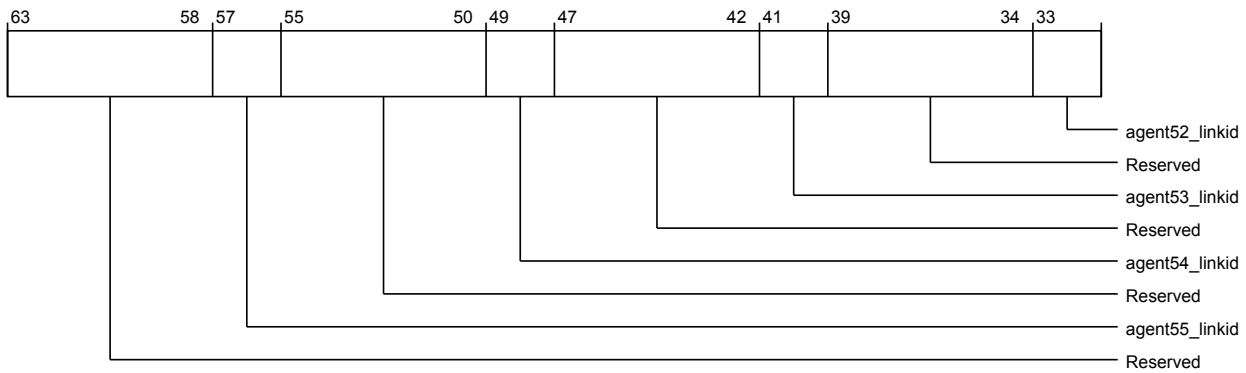


Figure 4-1264 por_cxla_por_cxla_agentid_to_linkid_reg6 (high)

The following table shows the por_cxla_agentid_to_linkid_reg6 higher register bit assignments.

Table 4-1281 por_cxla_por_cxla_agentid_to_linkid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent55_linkid	Specifies the Link ID for Agent ID 55	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent54_linkid	Specifies the Link ID for Agent ID 54	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent53_linkid	Specifies the Link ID for Agent ID 53	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent52_linkid	Specifies the Link ID for Agent ID 52	RW	2'h0

The following image shows the lower register bit assignments.

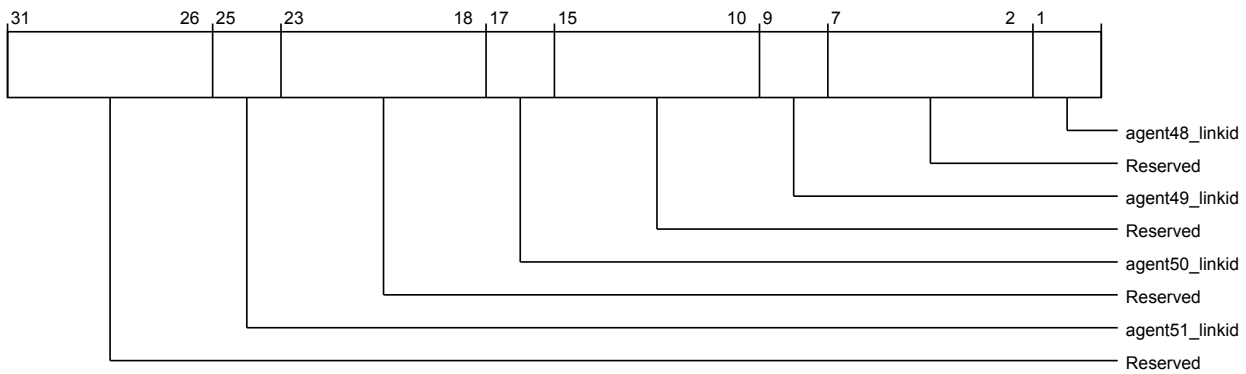


Figure 4-1265 por_cxla_por_cxla_agentid_to_linkid_reg6 (low)

The following table shows the por_cxla_agentid_to_linkid_reg6 lower register bit assignments.

Table 4-1282 por_cxla_por_cxla_agentid_to_linkid_reg6 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent51_linkid	Specifies the Link ID for Agent ID 51	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent50_linkid	Specifies the Link ID for Agent ID 50	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent49_linkid	Specifies the Link ID for Agent ID 49	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent48_linkid	Specifies the Link ID for Agent ID 48	RW	2'h0

por_cxla_agentid_to_linkid_reg7

Specifies the mapping of Agent ID to Link ID for Agent IDs 56 to 63.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC68
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

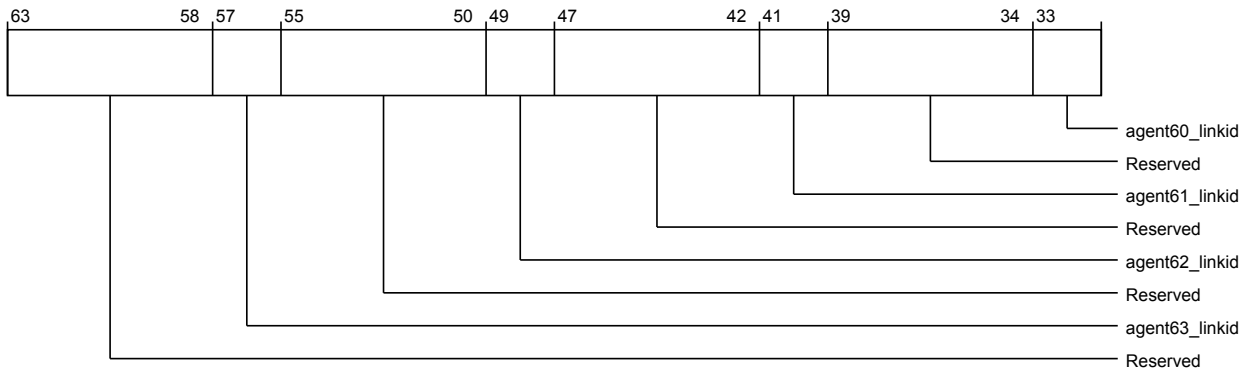


Figure 4-1266 por_cxla_por_cxla_agentid_to_linkid_reg7 (high)

The following table shows the por_cxla_agentid_to_linkid_reg7 higher register bit assignments.

Table 4-1283 por_cxla_por_cxla_agentid_to_linkid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent63_linkid	Specifies the Link ID for Agent ID 63	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent62_linkid	Specifies the Link ID for Agent ID 62	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent61_linkid	Specifies the Link ID for Agent ID 61	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent60_linkid	Specifies the Link ID for Agent ID 60	RW	2'h0

The following image shows the lower register bit assignments.

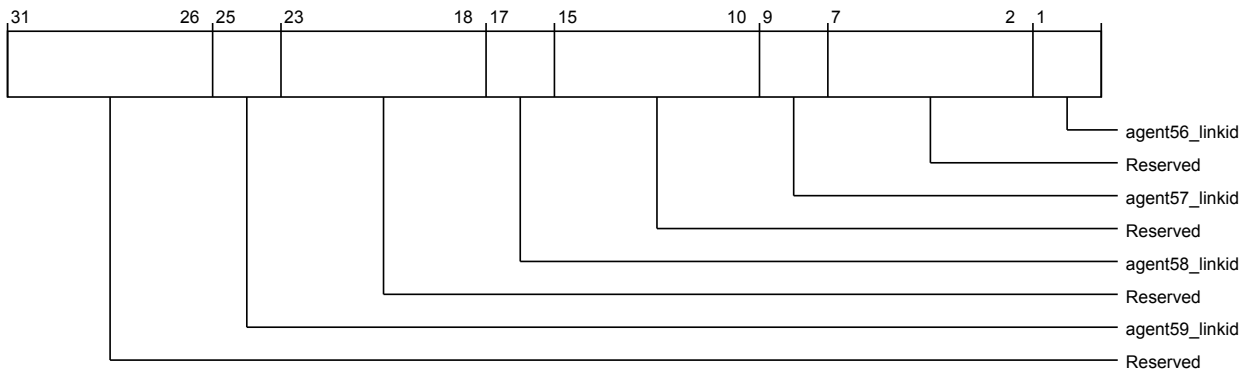


Figure 4-1267 por_cxla_por_cxla_agentid_to_linkid_reg7 (low)

The following table shows the por_cxla_agentid_to_linkid_reg7 lower register bit assignments.

Table 4-1284 por_cxla_por_cxla_agentid_to_linkid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent59_linkid	Specifies the Link ID for Agent ID 59	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent58_linkid	Specifies the Link ID for Agent ID 58	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent57_linkid	Specifies the Link ID for Agent ID 57	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent56_linkid	Specifies the Link ID for Agent ID 56	RW	2'h0

por_cxla_agentid_to_linkid_val

Specifies which Agent ID to Link ID mappings are valid.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC70
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

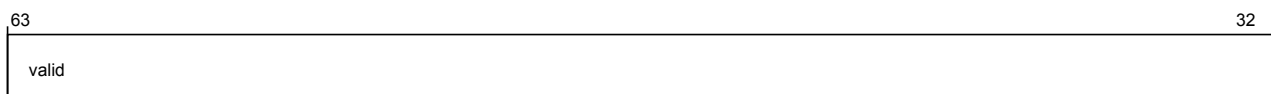


Figure 4-1268 por_cxla_por_cxla_agentid_to_linkid_val (high)

The following table shows the por_cxla_agentid_to_linkid_val higher register bit assignments.

Table 4-1285 por_cxla_por_cxla_agentid_to_linkid_val (high)

Bits	Field name	Description	Type	Reset
63:32	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

The following image shows the lower register bit assignments.

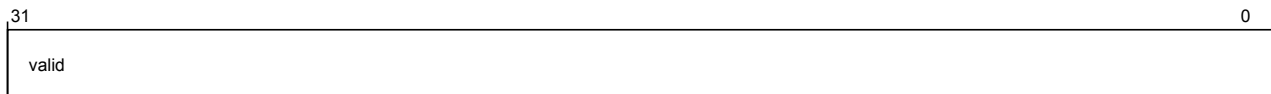


Figure 4-1269 por_cxla_por_cxla_agentid_to_linkid_val (low)

The following table shows the por_cxla_agentid_to_linkid_val lower register bit assignments.

Table 4-1286 por_cxla_por_cxla_agentid_to_linkid_val (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

por_cxla_linkid_to_pcie_bus_num

Specifies the mapping of CCIX Link ID to PCIe bus number.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

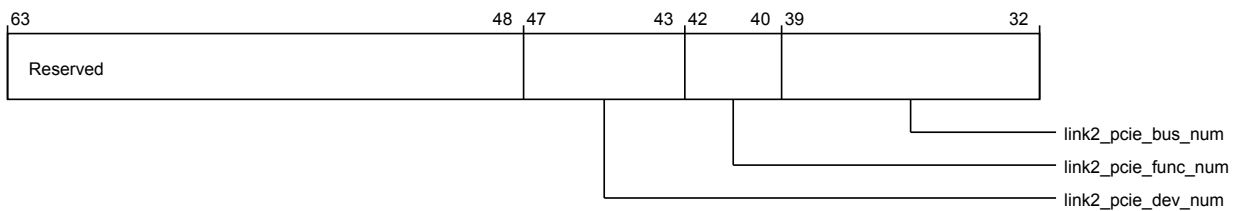


Figure 4-1270 por_cxla_por_cxla_linkid_to_pcie_bus_num (high)

The following table shows the por_cxla_linkid_to_pcie_bus_num higher register bit assignments.

Table 4-1287 por_cxla_por_cxla_linkid_to_pcie_bus_num (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:43	link2_pcie_dev_num	PCIe Device number for Link ID 2	RW	5'h00
42:40	link2_pcie_func_num	PCIe Function number for Link ID 2	RW	3'h0
39:32	link2_pcie_bus_num	PCIe bus number for Link ID 2	RW	8'h00

The following image shows the lower register bit assignments.

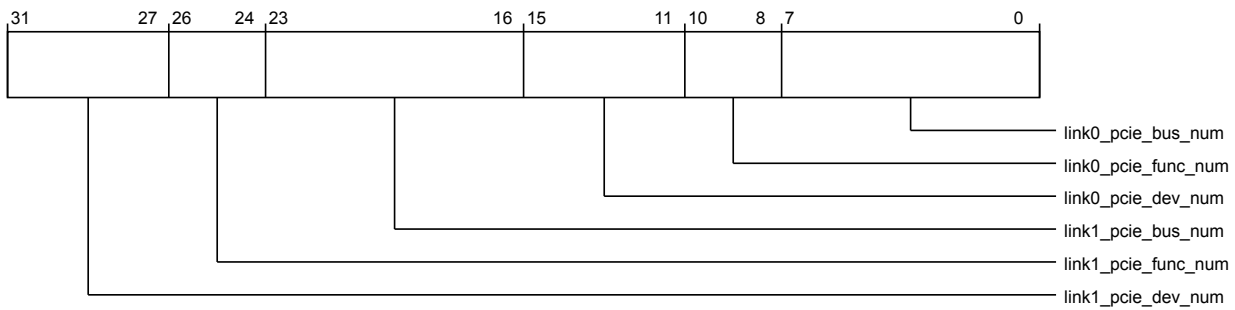


Figure 4-1271 por_cxla_por_cxla_linkid_to_pcie_bus_num (low)

The following table shows the por_cxla_linkid_to_pcie_bus_num lower register bit assignments.

Table 4-1288 por_cxla_por_cxla_linkid_to_pcie_bus_num (low)

Bits	Field name	Description	Type	Reset
31:27	link1_pcie_dev_num	PCIe Device number for Link ID 1	RW	5'h00
26:24	link1_pcie_func_num	PCIe Function number for Link ID 1	RW	3'h0
23:16	link1_pcie_bus_num	PCIe bus number for Link ID 1	RW	8'h00
15:11	link0_pcie_dev_num	PCIe Device number for Link ID 0	RW	5'h00
10:8	link0_pcie_func_num	PCIe Function number for Link ID 0	RW	3'h0
7:0	link0_pcie_bus_num	PCIe bus number for Link ID 0	RW	8'h00

por_cxla_permmsg_pyld_0_63

Contains bits[63:0] of CCIX Protocol Error (PER) Message payload.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD00
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

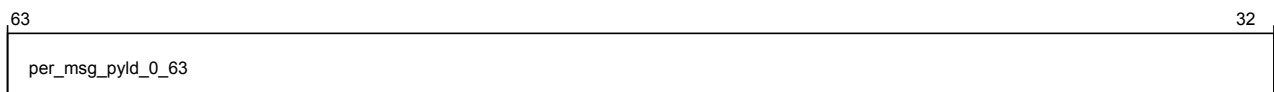


Figure 4-1272 por_cxla_por_cxla_permmsg_pyld_0_63 (high)

The following table shows the por_cxla_permmsg_pyld_0_63 higher register bit assignments.

Table 4-1289 por_cxla_por_cxla_permsg_pyld_0_63 (high)

Bits	Field name	Description	Type	Reset
63:32	per_msg_pyld_0_63	Protocol Error Msg Payload[63:0]	RW	64'b0

The following image shows the lower register bit assignments.



Figure 4-1273 por_cxla_por_cxla_permsg_pyld_0_63 (low)

The following table shows the por_cxla_permsg_pyld_0_63 lower register bit assignments.

Table 4-1290 por_cxla_por_cxla_permsg_pyld_0_63 (low)

Bits	Field name	Description	Type	Reset
31:0	per_msg_pyld_0_63	Protocol Error Msg Payload[63:0]	RW	64'b0

por_cxla_permsg_pyld_64_127

Contains bits[127:64] of CCIX Protocol Error (PER) Message payload.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD08
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

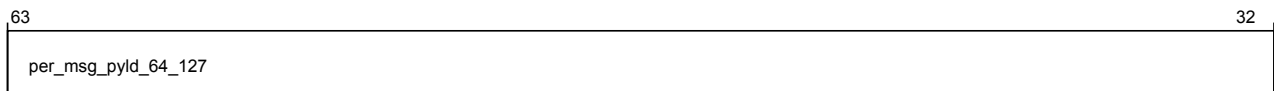


Figure 4-1274 por_cxla_por_cxla_permsg_pyld_64_127 (high)

The following table shows the por_cxla_permsg_pyld_64_127 higher register bit assignments.

Table 4-1291 por_cxla_por_cxla_permsg_pyld_64_127 (high)

Bits	Field name	Description	Type	Reset
63:32	per_msg_pyld_64_127	Protocol Error Msg Payload[127:64]	RW	64'b0

The following image shows the lower register bit assignments.

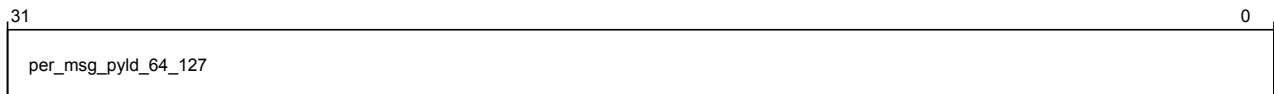


Figure 4-1275 por_cxla_por_cxla_permsg_pyld_64_127 (low)

The following table shows the por_cxla_permsg_pyld_64_127 lower register bit assignments.

Table 4-1292 por_cxla_por_cxla_permsg_pyld_64_127 (low)

Bits	Field name	Description	Type	Reset
31:0	per_msg_pyld_64_127	Protocol Error Msg Payload[127:64]	RW	64'b0

por_cxla_permsg_pyld_128_191

Contains bits[192:128] of CCIX Protocol Error (PER) Message payload.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD10
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

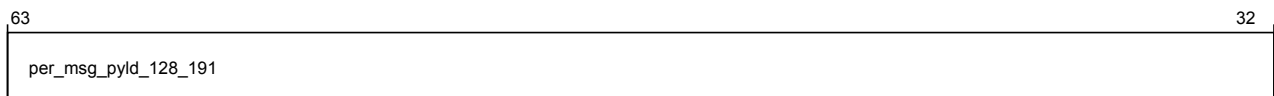


Figure 4-1276 por_cxla_por_cxla_permsg_pyld_128_191 (high)

The following table shows the por_cxla_permsg_pyld_128_191 higher register bit assignments.

Table 4-1293 por_cxla_por_cxla_permsg_pyld_128_191 (high)

Bits	Field name	Description	Type	Reset
63:32	per_msg_pyld_128_191	Protocol Error Msg Payload[191:128]	RW	64'b0

The following image shows the lower register bit assignments.

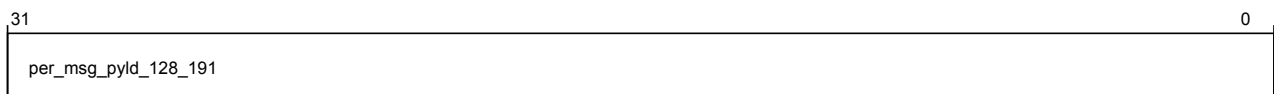


Figure 4-1277 por_cxla_por_cxla_permsg_pyld_128_191 (low)

The following table shows the por_cxla_permsg_pyld_128_191 lower register bit assignments.

Table 4-1294 por_cxla_por_cxla_permmsg_pyld_128_191 (low)

Bits	Field name	Description	Type	Reset
31:0	per_msg_pyld_128_191	Protocol Error Msg Payload[191:128]	RW	64'b0

por_cxla_permmsg_pyld_192_255

Contains bits[255:192] of CCIX Protocol Error (PER) Message payload.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD18
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

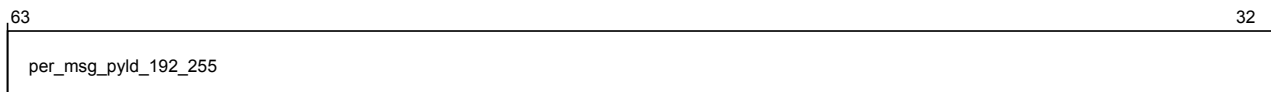


Figure 4-1278 por_cxla_por_cxla_permmsg_pyld_192_255 (high)

The following table shows the por_cxla_permmsg_pyld_192_255 higher register bit assignments.

Table 4-1295 por_cxla_por_cxla_permmsg_pyld_192_255 (high)

Bits	Field name	Description	Type	Reset
63:32	per_msg_pyld_192_255	Protocol Error Msg Payload[255:192]	RW	64'b0

The following image shows the lower register bit assignments.

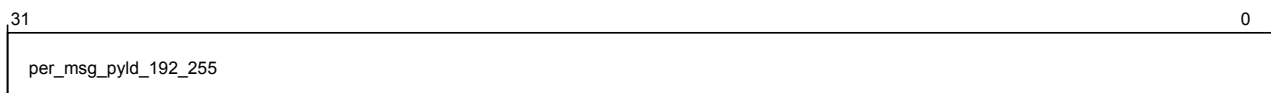


Figure 4-1279 por_cxla_por_cxla_permmsg_pyld_192_255 (low)

The following table shows the por_cxla_permmsg_pyld_192_255 lower register bit assignments.

Table 4-1296 por_cxla_por_cxla_permmsg_pyld_192_255 (low)

Bits	Field name	Description	Type	Reset
31:0	per_msg_pyld_192_255	Protocol Error Msg Payload[255:192]	RW	64'b0

por_cxla_permmsg_ctl

Contains Control bits to trigger CCIX Protocol Error (PER) Message.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD20
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.



Figure 4-1280 por_cxla_por_cxla_permmsg_ctl (high)

The following table shows the por_cxla_permmsg_ctl higher register bit assignments.

Table 4-1297 por_cxla_por_cxla_permmsg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

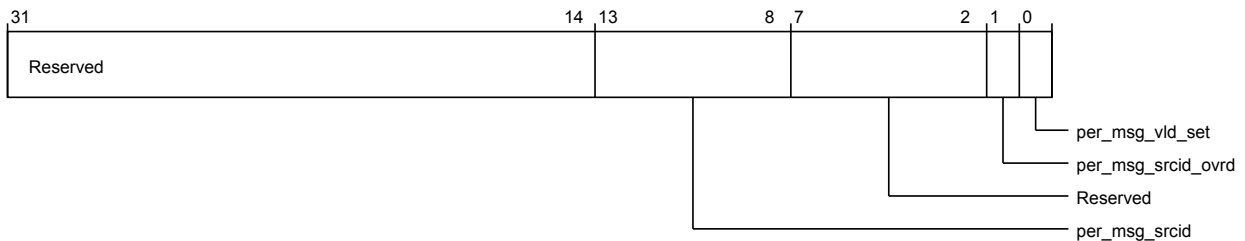


Figure 4-1281 por_cxla_por_cxla_permmsg_ctl (low)

The following table shows the por_cxla_permmsg_ctl lower register bit assignments.

Table 4-1298 por_cxla_por_cxla_permmsg_ctl (low)

Bits	Field name	Description	Type	Reset
31:14	Reserved	Reserved	RO	-
13:8	per_msg_srcid	Contains Source ID used on CCIX Protocol Error Msg. Used when per_msg_srcid_ovrd is set.	RW	6'b0
7:2	Reserved	Reserved	RO	-
1	per_msg_srcid_ovrd	When set, overrides the Source ID on Protocol Error Msg by value specified in this register. Or else the source ID from payload[55:48] is used.	RW	1'b0
0	per_msg_vld_set	When set, sends CCIX Protocol Error Msg. Must be cleared after the current error is processed and before a new error message is triggered	RW	1'b0

por_cxla_err_agent_id

Contains Error Agent ID. Must be programmed by CCIX discovery s/w. Used as TargetID on CCIX Protocol Error (PER) Message.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD28
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

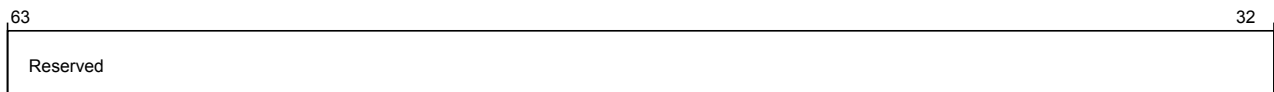


Figure 4-1282 por_cxla_err_agent_id (high)

The following table shows the por_cxla_err_agent_id higher register bit assignments.

Table 4-1299 por_cxla_err_agent_id (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

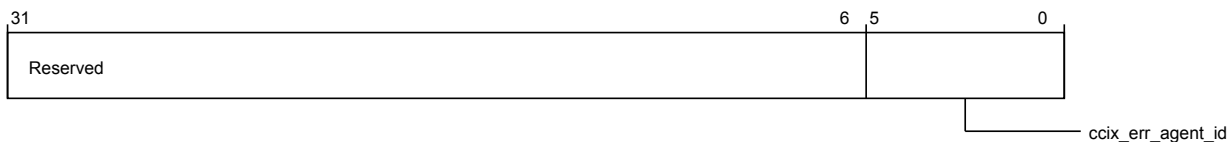


Figure 4-1283 por_cxla_err_agent_id (low)

The following table shows the por_cxla_err_agent_id lower register bit assignments.

Table 4-1300 por_cxla_err_agent_id (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5:0	ccix_err_agent_id	CCIX Error AgentID	RW	6'b0

por_cxla_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type	RW
-------------	----

Register width (Bits) 64
Address offset 14'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

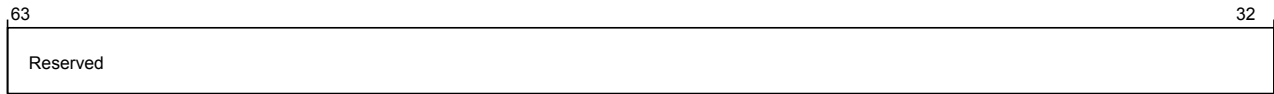


Figure 4-1284 `por_cxla_por_cxla_pmu_event_sel` (high)

The following table shows the `por_cxla_pmu_event_sel` higher register bit assignments.

Table 4-1301 `por_cxla_por_cxla_pmu_event_sel` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

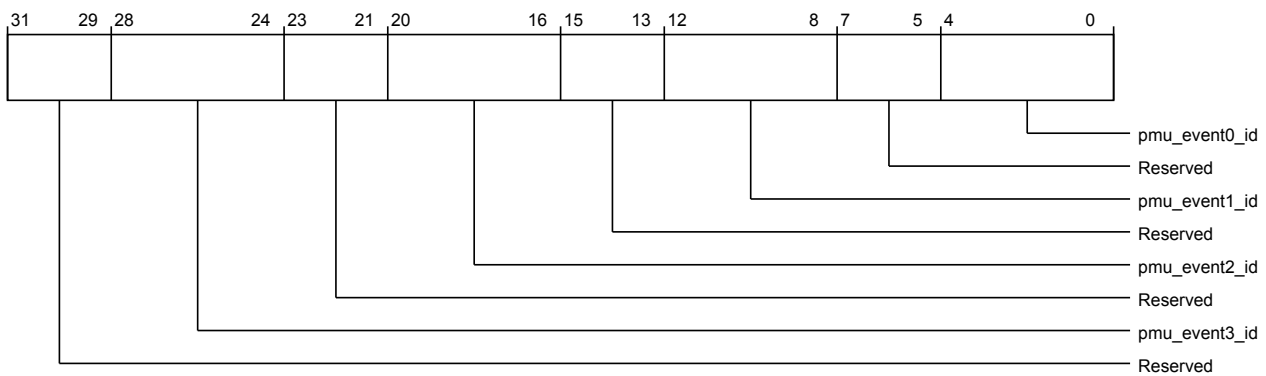


Figure 4-1285 `por_cxla_por_cxla_pmu_event_sel` (low)

The following table shows the `por_cxla_pmu_event_sel` lower register bit assignments.

Table 4-1302 `por_cxla_por_cxla_pmu_event_sel` (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	<code>pmu_event3_id</code>	CXLA PMU Event 3 ID; see <code>pmu_event0_id</code> for encodings	RW	5'b0
23:21	Reserved	Reserved	RO	-
20:16	<code>pmu_event2_id</code>	CXLA PMU Event 2 ID; see <code>pmu_event0_id</code> for encodings	RW	5'b0
15:13	Reserved	Reserved	RO	-
12:8	<code>pmu_event1_id</code>	CXLA PMU Event 1 ID; see <code>pmu_event0_id</code> for encodings	RW	5'b0

Table 4-1302 por_cxla_por_cxla_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
7:5	Reserved	Reserved	RO	-
4:0	pmu_event0_id	CXLA PMU Event 0 ID 5'h00: No event 5'h01: RX TLP for Link 0 5'h02: RX TLP for Link 1 5'h03: RX TLP for Link 2 5'h04: TX TLP for Link 0 5'h05: TX TLP for Link 1 5'h06: TX TLP for Link 2 5'h07: RX CXS for Link 0 5'h08: RX CXS for Link 1 5'h09: RX CXS for Link 2 5'h0A: TX CXS for Link 0 5'h0B: TX CXS for Link 1 5'h0B: TX CXS for Link 2 5'h0D: Average RX TLP size in DWs 5'h0E: Average TX TLP size in DWs 5'h0F: Average RX TLP size in CCIX messages 5'h10: Average TX TLP size in CCIX messages 5'h11: Average size of RX CXS in DWs within a beat 5'h12: Average size of TX CXS in DWs within a beat 5'h13: TX CXS link credit backpressure 5'h14: RX TLP buffer full and backpressured 5'h15: TX TLP buffer full and backpressured 5'h16: Average latency to process an RX TLP 5'h17: Average latency to form a TX TLP	RW	5'b0

por_cxla_pmu_config

Configures the CXLA PMU.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2210
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

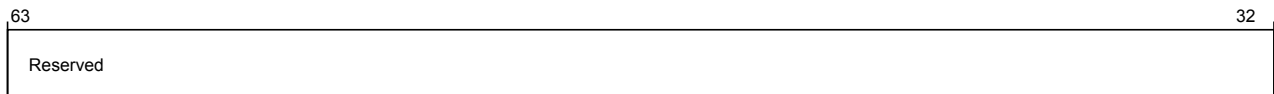


Figure 4-1286 por_cxla_por_cxla_pmu_config (high)

The following table shows the por_cxla_pmu_config higher register bit assignments.

Table 4-1303 por_cxla_por_cxla_pmu_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

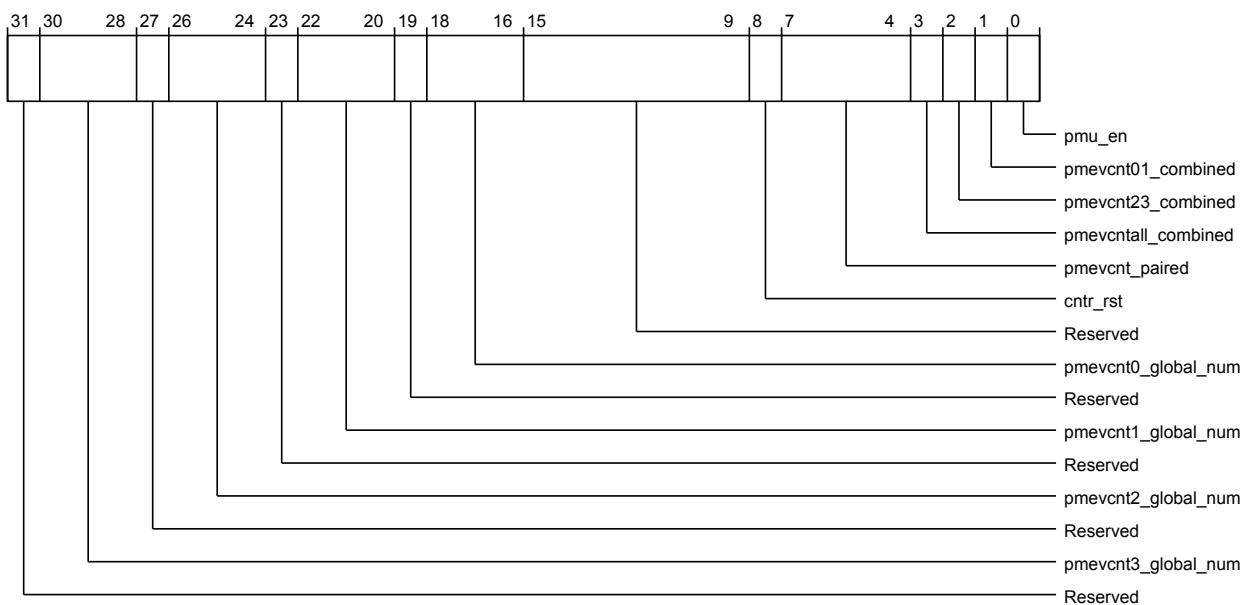


Figure 4-1287 por_cxla_por_cxla_pmu_config (low)

The following table shows the por_cxla_pmu_config lower register bit assignments.

Table 4-1304 por_cxla_por_cxla_pmu_config (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	pmevcnt3_global_num	Global counter to pair with PMU counter 3; see pmevcnt0_global_num for encodings	RW	3'b0
27	Reserved	Reserved	RO	-
26:24	pmevcnt2_global_num	Global counter to pair with PMU counter 2; see pmevcnt0_global_num for encodings	RW	3'b0
23	Reserved	Reserved	RO	-
22:20	pmevcnt1_global_num	Global counter to pair with PMU counter 1; see pmevcnt0_global_num for encodings	RW	3'b0

Table 4-1304 por_cxla_por_cxla_pmu_config (low) (continued)

Bits	Field name	Description	Type	Reset
19	Reserved	Reserved	RO	-
18:16	pmevcnt0_global_num	Global counter to pair with PMU counter 0 3'b000: Global PMU event counter A 3'b001: Global PMU event counter B 3'b010: Global PMU event counter C 3'b011: Global PMU event counter D 3'b100: Global PMU event counter E 3'b101: Global PMU event counter F 3'b110: Global PMU event counter G 3'b111: Global PMU event counter H	RW	3'b0
15:9	Reserved	Reserved	RO	-
8	cntr_rst	Enables clearing of live counters upon assertion of snapshot	RW	1'b0
7:4	pmevcnt_paired	PMU local counter paired with global counter	RW	4'b0
3	pmevcntall_combined	Enables combination of all PMU counters (0, 1, 2, 3) NOTE: When set, pmevcnt01_combined and pmevcnt23_combined have no effect.	RW	1'b0
2	pmevcnt23_combined	Enables combination of PMU counters 2 and 3	RW	1'b0
1	pmevcnt01_combined	Enables combination of PMU counters 0 and 1	RW	1'b0
0	pmu_en	CXLA PMU enable NOTE: All other fields in this register are valid only if this bit is set.	RW	1'b0

por_cxla_pmevcnt

Contains all PMU event counters (0, 1, 2, 3).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2220

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

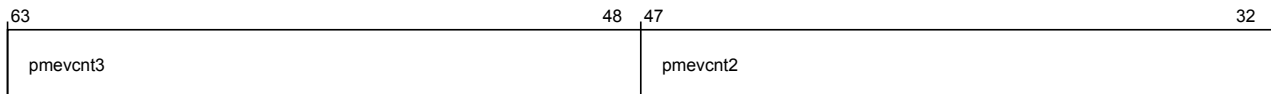


Figure 4-1288 por_cxla_por_cxla_pmevcnt (high)

The following table shows the por_cxla_pmevnt higher register bit assignments.

Table 4-1305 por_cxla_por_cxla_pmevcnt (high)

Bits	Field name	Description	Type	Reset
63:48	pmevnt3	PMU event counter 3	RW	16'h0000
47:32	pmevnt2	PMU event counter 2	RW	16'h0000

The following image shows the lower register bit assignments.

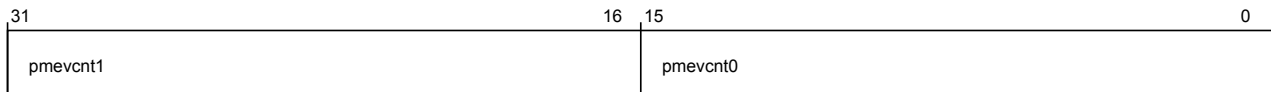


Figure 4-1289 por_cxla_por_cxla_pmevcnt (low)

The following table shows the por_cxla_pmevnt lower register bit assignments.

Table 4-1306 por_cxla_por_cxla_pmevcnt (low)

Bits	Field name	Description	Type	Reset
31:16	pmevnt1	PMU event counter 1	RW	16'h0000
15:0	pmevnt0	PMU event counter 0	RW	16'h0000

por_cxla_pmevntsr

Functions as the PMU event counter shadow register for all counters (0, 1, 2, 3).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2240
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

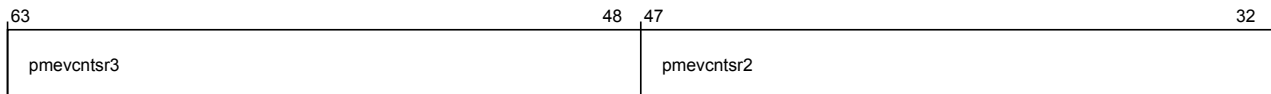


Figure 4-1290 por_cxla_por_cxla_pmevcntrs (high)

The following table shows the por_cxla_pmevcntrs higher register bit assignments.

Table 4-1307 por_cxla_por_cxla_pmevcntrs (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcntrs3	PMU event counter 3 shadow register	RW	16'h0000
47:32	pmevcntrs2	PMU event counter 2 shadow register	RW	16'h0000

The following image shows the lower register bit assignments.

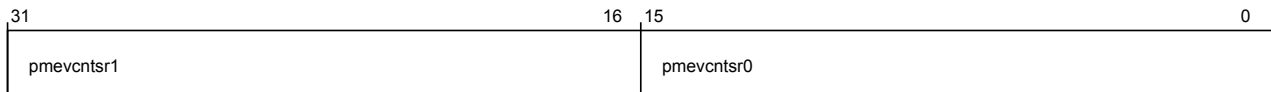


Figure 4-1291 por_cxla_por_cxla_pmevcntrs (low)

The following table shows the por_cxla_pmevcntrs lower register bit assignments.

Table 4-1308 por_cxla_por_cxla_pmevcntrs (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcntrs1	PMU event counter 1 shadow register	RW	16'h0000
15:0	pmevcntrs0	PMU event counter 0 shadow register	RW	16'h0000

4.3.14 FMU register descriptions

This section lists the FMU configuration registers.

por_fmu_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

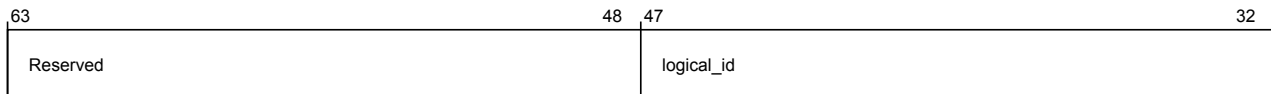


Figure 4-1292 por_fmu_por_fmu_node_info (high)

The following table shows the por_fmu_node_info higher register bit assignments.

Table 4-1309 por_fmu_por_fmu_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID NOTE: FMU logical ID is always set to 16'b0.	RO	16'h0

The following image shows the lower register bit assignments.

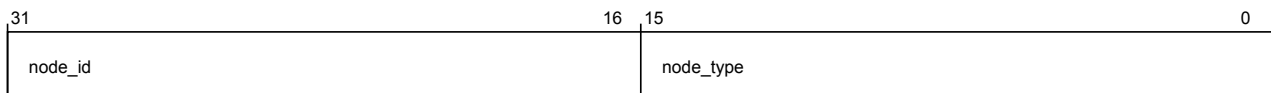


Figure 4-1293 por_fmu_por_fmu_node_info (low)

The following table shows the por_fmu_node_info lower register bit assignments.

Table 4-1310 por_fmu_por_fmu_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0200

por_fmu_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

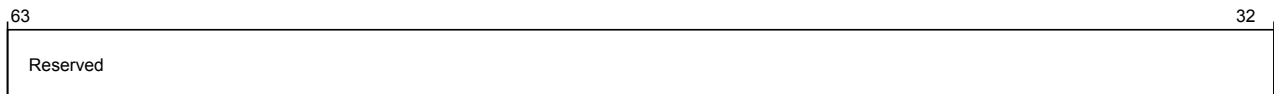


Figure 4-1294 por_fmu_por_fmu_child_info (high)

The following table shows the por_fmu_child_info higher register bit assignments.

Table 4-1311 por_fmu_por_fmu_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

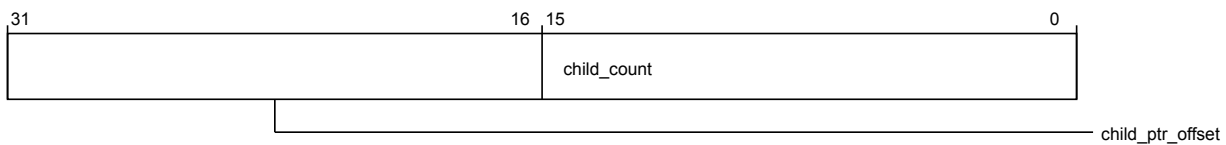


Figure 4-1295 por_fmu_por_fmu_child_info (low)

The following table shows the por_fmu_child_info lower register bit assignments.

Table 4-1312 por_fmu_por_fmu_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_fmu_ctl

Functions as the FMU control register.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC10

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

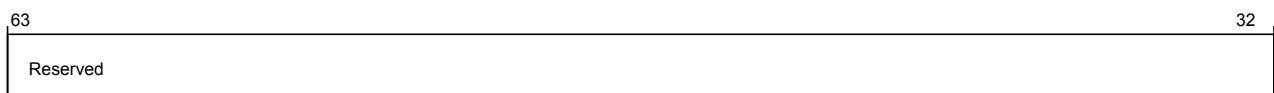


Figure 4-1296 por_fmu_por_fmu_ctl (high)

The following table shows the por_fmu_ctl higher register bit assignments.

Table 4-1313 por_fmu_por_fmu_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

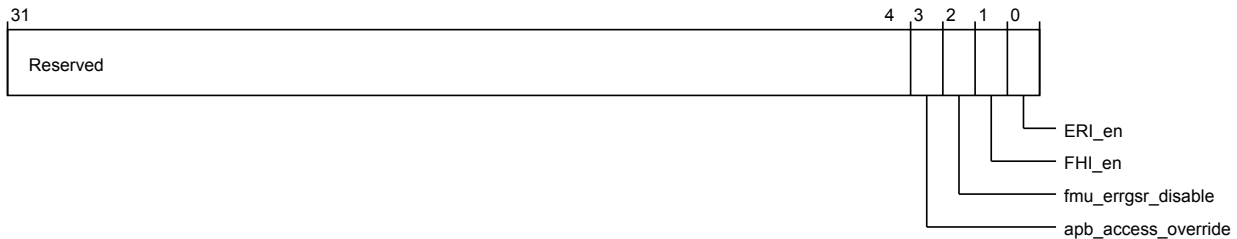


Figure 4-1297 por_fmu_por_fmu_ctl (low)

The following table shows the por_fmu_ctl lower register bit assignments.

Table 4-1314 por_fmu_por_fmu_ctl (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	apb_access_override	To give RN* access to FMU/FDC/MPU config registers 1'b0: no access 1'b1: access override	RW	1'b0
2	fmu_errgsr_disable	Disable updating FMU error group status, should be turned on before warm reset. 1'b0: not disable 1'b1: disable	RW	1'b0
1	FHI_en	Enable FMU_FHI interrupt 1'b0: not enable 1'b1: enable	RW	1'b0
0	ERI_en	Enable FMU_ERI interrupt 1'b0: not enable 1'b1: enable	RW	1'b0

por_fmu_key

FMU write key

Its characteristics are:

Type WO

Register width (Bits) 64

Address offset 14'hC18
Register reset 64'b10111110
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

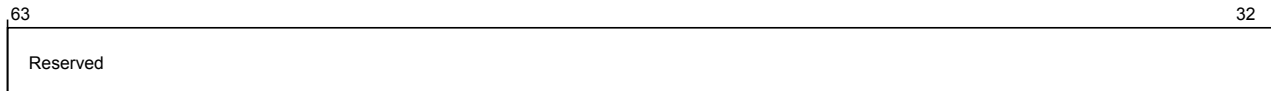


Figure 4-1298 por_fmu_por_fmu_key (high)

The following table shows the por_fmu_key higher register bit assignments.

Table 4-1315 por_fmu_por_fmu_key (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

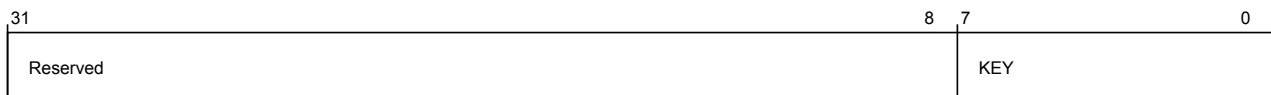


Figure 4-1299 por_fmu_por_fmu_key (low)

The following table shows the por_fmu_key lower register bit assignments.

Table 4-1316 por_fmu_por_fmu_key (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	KEY	The write protection key. Only writing of correct value will enable subsequent write to other FMU registers.	WO	8'hBE

por_fmu_errgsr_clk_mxp

Provides XP <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3008
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

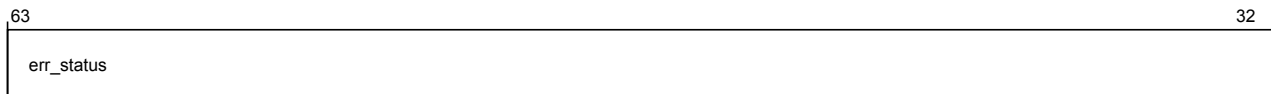


Figure 4-1300 por_fmu_por_fmu_errgsr_clk_mxp (high)

The following table shows the por_fmu_errgsr_clk_mxp higher register bit assignments.

Table 4-1317 por_fmu_por_fmu_errgsr_clk_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

The following image shows the lower register bit assignments.

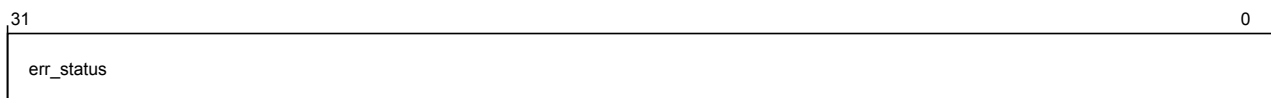


Figure 4-1301 por_fmu_por_fmu_errgsr_clk_mxp (low)

The following table shows the por_fmu_errgsr_clk_mxp lower register bit assignments.

Table 4-1318 por_fmu_por_fmu_errgsr_clk_mxp (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

por_fmu_errgsr_rst_mxp

Provides XP <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3010

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

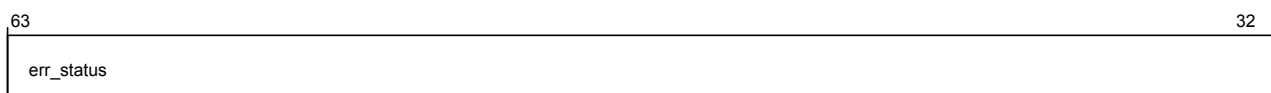


Figure 4-1302 por_fmu_por_fmu_errgsr_rst_mxp (high)

The following table shows the por_fmu_errgsr_rst_mxp higher register bit assignments.

Table 4-1319 por_fmu_por_fmu_errgsr_rst_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1303 por_fmu_por_fmu_errgsr_rst_mxp (low)

The following table shows the por_fmu_errgsr_rst_mxp lower register bit assignments.

Table 4-1320 por_fmu_por_fmu_errgsr_rst_mxp (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

por_fmu_errgsr_lsc_mxp

Provides XP <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3018

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

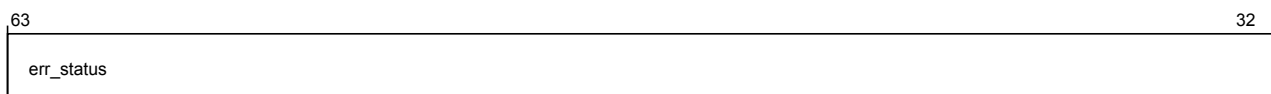


Figure 4-1304 por_fmu_por_fmu_errgsr_lsc_mxp (high)

The following table shows the por_fmu_errgsr_lsc_mxp higher register bit assignments.

Table 4-1321 por_fmu_por_fmu_errgsr_lsc_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

The following image shows the lower register bit assignments.

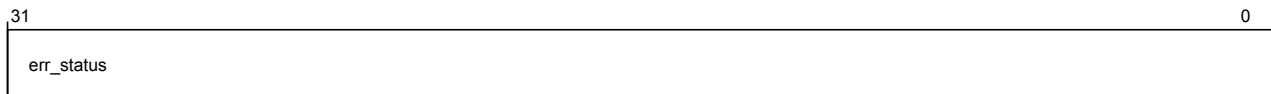


Figure 4-1305 por_fmu_por_fmu_errgsr_lsc_mxp (low)

The following table shows the por_fmu_errgsr_lsc_mxp lower register bit assignments.

Table 4-1322 por_fmu_por_fmu_errgsr_lsc_mxp (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

por_fmu_errgsr_ioc_mxp

Provides XP <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3020

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

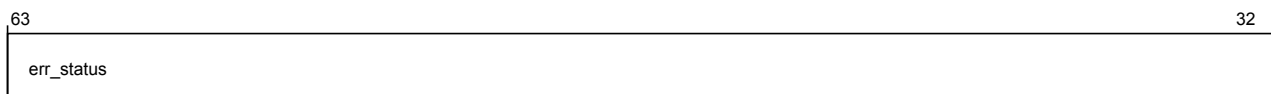


Figure 4-1306 por_fmu_por_fmu_errgsr_ioc_mxp (high)

The following table shows the por_fmu_errgsr_ioc_mxp higher register bit assignments.

Table 4-1323 por_fmu_por_fmu_errgsr_ioc_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

The following image shows the lower register bit assignments.

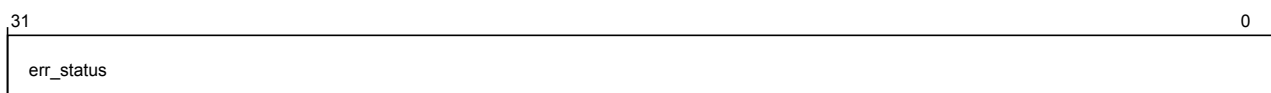


Figure 4-1307 por_fmu_por_fmu_errgsr_ioc_mxp (low)

The following table shows the por_fmu_errgsr_ioc_mxp lower register bit assignments.

Table 4-1324 por_fmu_por_fmu_errgsr_ioc_mxp (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

por_fmu_errgsr_async_mxp

Provides XP <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3028

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1308 por_fmu_por_fmu_errgsr_async_mxp (high)

The following table shows the por_fmu_errgsr_async_mxp higher register bit assignments.

Table 4-1325 por_fmu_por_fmu_errgsr_async_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

The following image shows the lower register bit assignments.

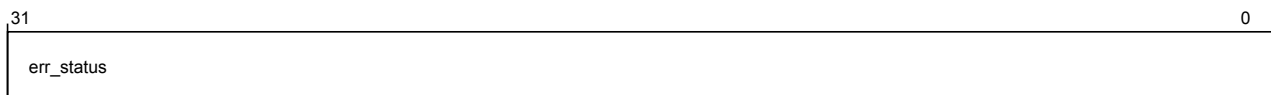


Figure 4-1309 por_fmu_por_fmu_errgsr_async_mxp (low)

The following table shows the por_fmu_errgsr_async_mxp lower register bit assignments.

Table 4-1326 por_fmu_por_fmu_errgsr_async_mxp (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

por_fmu_errgsr_hang_mxp

Provides XP <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3030
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

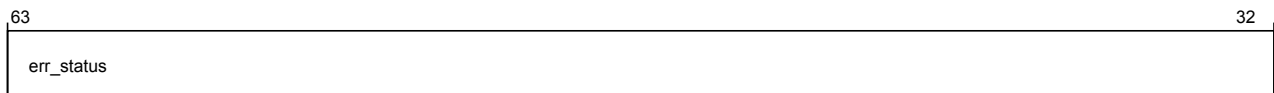


Figure 4-1310 por_fmu_por_fmu_errgsr_hang_mxp (high)

The following table shows the por_fmu_errgsr_hang_mxp higher register bit assignments.

Table 4-1327 por_fmu_por_fmu_errgsr_hang_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

The following image shows the lower register bit assignments.

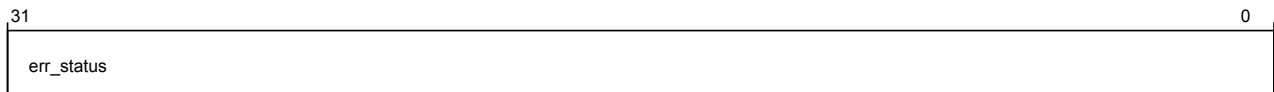


Figure 4-1311 por_fmu_por_fmu_errgsr_hang_mxp (low)

The following table shows the por_fmu_errgsr_hang_mxp lower register bit assignments.

Table 4-1328 por_fmu_por_fmu_errgsr_hang_mxp (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

por_fmu_errgsr_mpu_mxp

Provides XP <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3038

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1312 por_fmu_por_fmu_errgsr_mpu_mxp (high)

The following table shows the por_fmu_errgsr_mpu_mxp higher register bit assignments.

Table 4-1329 por_fmu_por_fmu_errgsr_mpu_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

The following image shows the lower register bit assignments.

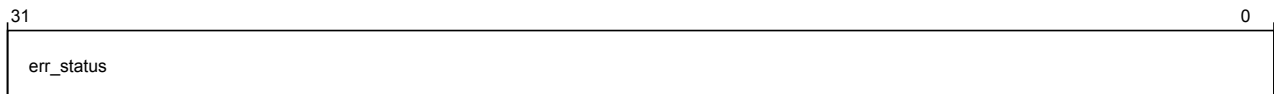


Figure 4-1313 por_fmu_por_fmu_errgsr_mpu_mxp (low)

The following table shows the por_fmu_errgsr_mpu_mxp lower register bit assignments.

Table 4-1330 por_fmu_por_fmu_errgsr_mpu_mxp (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

por_fmu_errgsr_eccue_mxp

Provides XP <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3040
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

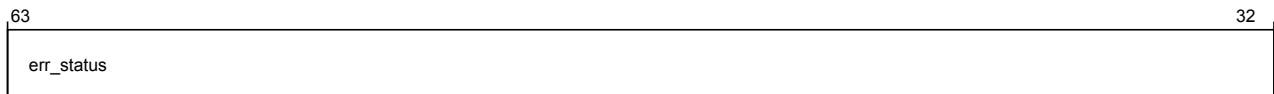


Figure 4-1314 por_fmu_por_fmu_errgsr_eccue_mxp (high)

The following table shows the por_fmu_errgsr_eccue_mxp higher register bit assignments.

Table 4-1331 por_fmu_por_fmu_errgsr_eccue_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

The following image shows the lower register bit assignments.

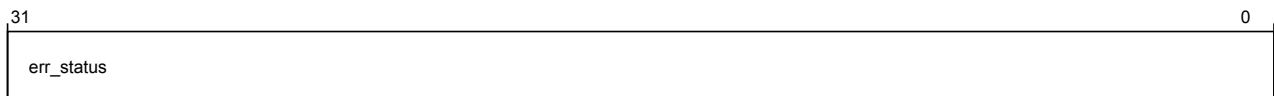


Figure 4-1315 por_fmu_por_fmu_errgsr_eccue_mxp (low)

The following table shows the por_fmu_errgsr_eccue_mxp lower register bit assignments.

Table 4-1332 por_fmu_por_fmu_errgsr_eccue_mxp (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

por_fmu_errgsr_eccce_mxp

Provides XP <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3048

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1316 por_fmu_por_fmu_errgsr_eccce_mxp (high)

The following table shows the por_fmu_errgsr_eccce_mxp higher register bit assignments.

Table 4-1333 por_fmu_por_fmu_errgsr_eccce_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1317 por_fmu_por_fmu_errgsr_eccce_mxp (low)

The following table shows the por_fmu_errgsr_eccce_mxp lower register bit assignments.

Table 4-1334 por_fmu_por_fmu_errgsr_eccce_mxp (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_mxp<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_mxp'	RO	64'h0

por_fmu_errgsr_clk_p0_d0

Provides device connected to p0_d0 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3050

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

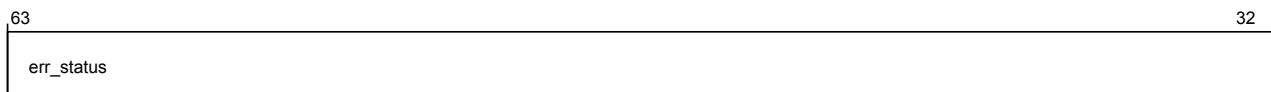


Figure 4-1318 por_fmu_por_fmu_errgsr_clk_p0_d0 (high)

The following table shows the por_fmu_errgsr_clk_p0_d0 higher register bit assignments.

Table 4-1335 por_fmu_por_fmu_errgsr_clk_p0_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

The following image shows the lower register bit assignments.

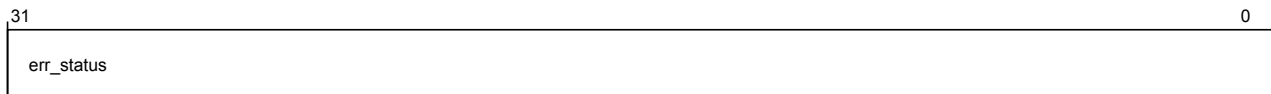


Figure 4-1319 por_fmu_por_fmu_errgsr_clk_p0_d0 (low)

The following table shows the por_fmu_errgsr_clk_p0_d0 lower register bit assignments.

Table 4-1336 por_fmu_por_fmu_errgsr_clk_p0_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

por_fmu_errgsr_rst_p0_d0

Provides device connected to p0_d0 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3058

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

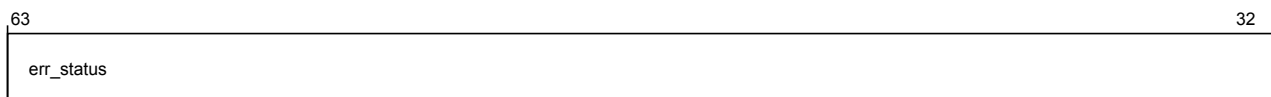


Figure 4-1320 por_fmu_por_fmu_errgsr_rst_p0_d0 (high)

The following table shows the por_fmu_errgsr_rst_p0_d0 higher register bit assignments.

Table 4-1337 por_fmu_por_fmu_errgsr_rst_p0_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

The following image shows the lower register bit assignments.

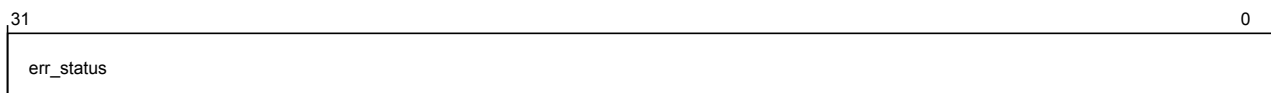


Figure 4-1321 por_fmu_por_fmu_errgsr_rst_p0_d0 (low)

The following table shows the por_fmu_errgsr_rst_p0_d0 lower register bit assignments.

Table 4-1338 `por_fmu_por_fmu_errgsr_rst_p0_d0` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>err_status</code>	Read-only copy of <code>por_errstatus_p0_d0<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

`por_fmu_errgsr_lsc_p0_d0`

Provides device connected to `p0_d0` port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3060

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

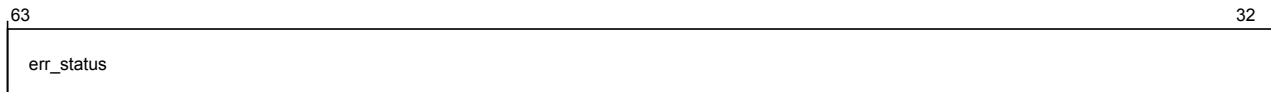


Figure 4-1322 `por_fmu_por_fmu_errgsr_lsc_p0_d0` (high)

The following table shows the `por_fmu_errgsr_lsc_p0_d0` higher register bit assignments.

Table 4-1339 `por_fmu_por_fmu_errgsr_lsc_p0_d0` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p0_d0<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

The following image shows the lower register bit assignments.

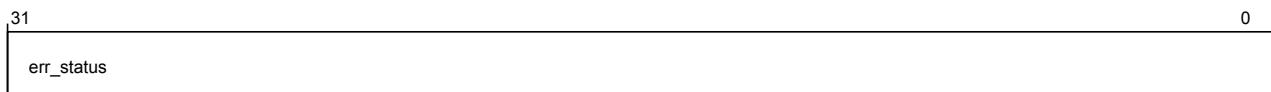


Figure 4-1323 `por_fmu_por_fmu_errgsr_lsc_p0_d0` (low)

The following table shows the `por_fmu_errgsr_lsc_p0_d0` lower register bit assignments.

Table 4-1340 `por_fmu_por_fmu_errgsr_lsc_p0_d0` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>err_status</code>	Read-only copy of <code>por_errstatus_p0_d0<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

por_fmu_errgsr_ioc_p0_d0

Provides device connected to p0_d0 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3068
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

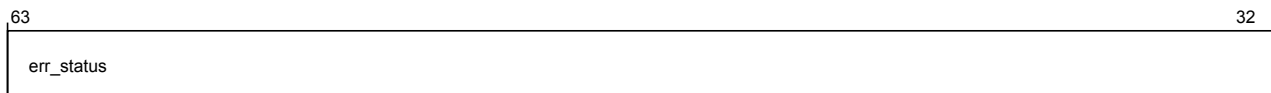


Figure 4-1324 por_fmu_por_fmu_errgsr_ioc_p0_d0 (high)

The following table shows the por_fmu_errgsr_ioc_p0_d0 higher register bit assignments.

Table 4-1341 por_fmu_por_fmu_errgsr_ioc_p0_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

The following image shows the lower register bit assignments.

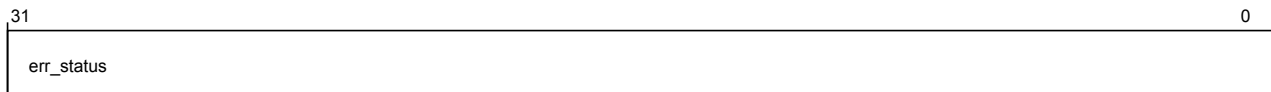


Figure 4-1325 por_fmu_por_fmu_errgsr_ioc_p0_d0 (low)

The following table shows the por_fmu_errgsr_ioc_p0_d0 lower register bit assignments.

Table 4-1342 por_fmu_por_fmu_errgsr_ioc_p0_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

por_fmu_errgsr_async_p0_d0

Provides device connected to p0_d0 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3070

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1326 por_fmu_por_fmu_errgsr_async_p0_d0 (high)

The following table shows the por_fmu_errgsr_async_p0_d0 higher register bit assignments.

Table 4-1343 por_fmu_por_fmu_errgsr_async_p0_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

The following image shows the lower register bit assignments.

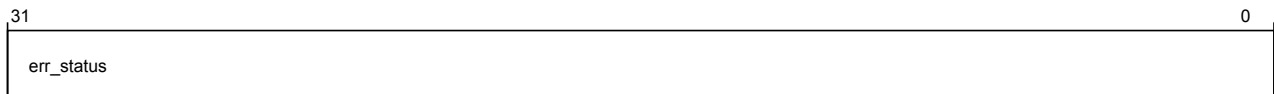


Figure 4-1327 por_fmu_por_fmu_errgsr_async_p0_d0 (low)

The following table shows the por_fmu_errgsr_async_p0_d0 lower register bit assignments.

Table 4-1344 por_fmu_por_fmu_errgsr_async_p0_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

por_fmu_errgsr_hang_p0_d0

Provides device connected to p0_d0 port <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3078
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

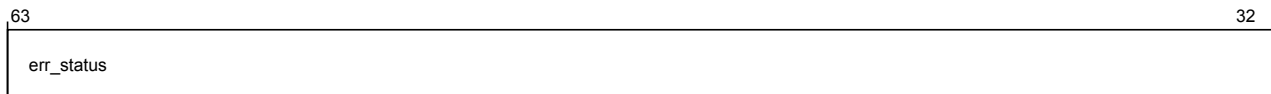


Figure 4-1328 por_fmu_por_fmu_errgsr_hang_p0_d0 (high)

The following table shows the por_fmu_errgsr_hang_p0_d0 higher register bit assignments.

Table 4-1345 por_fmu_por_fmu_errgsr_hang_p0_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1329 por_fmu_por_fmu_errgsr_hang_p0_d0 (low)

The following table shows the por_fmu_errgsr_hang_p0_d0 lower register bit assignments.

Table 4-1346 por_fmu_por_fmu_errgsr_hang_p0_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

por_fmu_errgsr_mpu_p0_d0

Provides device connected to p0_d0 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3080

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

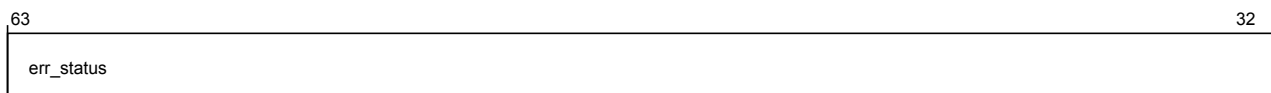


Figure 4-1330 por_fmu_por_fmu_errgsr_mpu_p0_d0 (high)

The following table shows the por_fmu_errgsr_mpu_p0_d0 higher register bit assignments.

Table 4-1347 `por_fmu_por_fmu_errgsr_mpu_p0_d0` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p0_d0<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1331 `por_fmu_por_fmu_errgsr_mpu_p0_d0` (low)

The following table shows the `por_fmu_errgsr_mpu_p0_d0` lower register bit assignments.

Table 4-1348 `por_fmu_por_fmu_errgsr_mpu_p0_d0` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>err_status</code>	Read-only copy of <code>por_errstatus_p0_d0<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

`por_fmu_errgsr_eccue_p0_d0`

Provides device connected to `p0_d0` port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3088

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

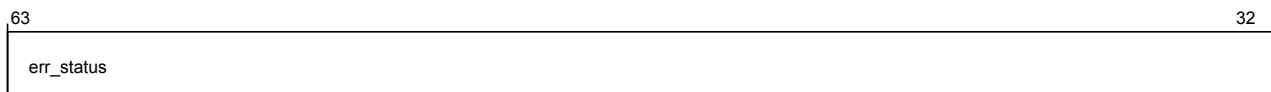


Figure 4-1332 `por_fmu_por_fmu_errgsr_eccue_p0_d0` (high)

The following table shows the `por_fmu_errgsr_eccue_p0_d0` higher register bit assignments.

Table 4-1349 `por_fmu_por_fmu_errgsr_eccue_p0_d0` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p0_d0<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

The following image shows the lower register bit assignments.

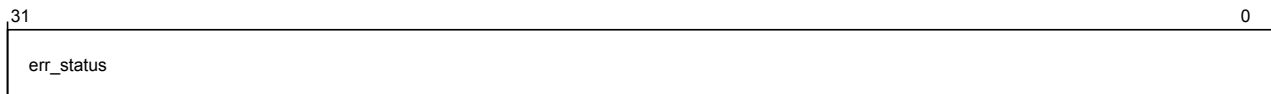


Figure 4-1333 por_fmu_por_fmu_errgsr_eccue_p0_d0 (low)

The following table shows the por_fmu_errgsr_eccue_p0_d0 lower register bit assignments.

Table 4-1350 por_fmu_por_fmu_errgsr_eccue_p0_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

por_fmu_errgsr_eccce_p0_d0

Provides device connected to p0_d0 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3090

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

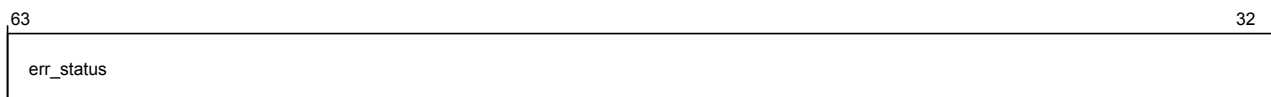


Figure 4-1334 por_fmu_por_fmu_errgsr_eccce_p0_d0 (high)

The following table shows the por_fmu_errgsr_eccce_p0_d0 higher register bit assignments.

Table 4-1351 por_fmu_por_fmu_errgsr_eccce_p0_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

The following image shows the lower register bit assignments.

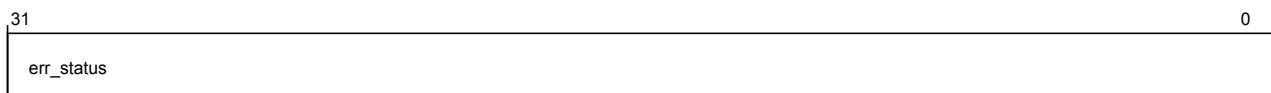


Figure 4-1335 por_fmu_por_fmu_errgsr_eccce_p0_d0 (low)

The following table shows the por_fmu_errgsr_eccce_p0_d0 lower register bit assignments.

Table 4-1352 por_fmu_por_fmu_errgsr_eccce_p0_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d0'	RO	64'h0

por_fmu_errgsr_clk_p0_d1

Provides device connected to p0_d1 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3098

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

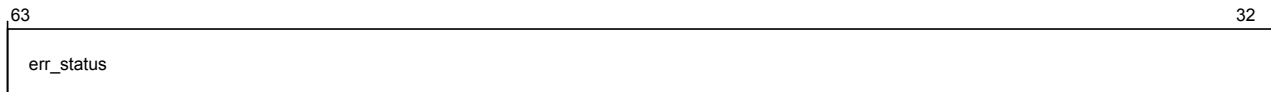


Figure 4-1336 por_fmu_por_fmu_errgsr_clk_p0_d1 (high)

The following table shows the por_fmu_errgsr_clk_p0_d1 higher register bit assignments.

Table 4-1353 por_fmu_por_fmu_errgsr_clk_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

The following image shows the lower register bit assignments.

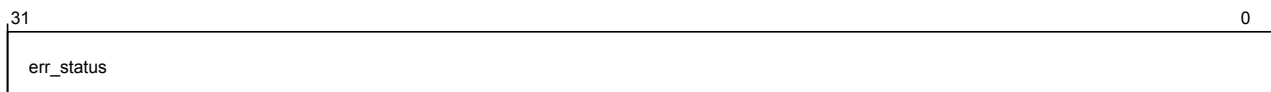


Figure 4-1337 por_fmu_por_fmu_errgsr_clk_p0_d1 (low)

The following table shows the por_fmu_errgsr_clk_p0_d1 lower register bit assignments.

Table 4-1354 por_fmu_por_fmu_errgsr_clk_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

por_fmu_errgsr_rst_p0_d1

Provides device connected to p0_d1 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h30A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1338 por_fmu_errgsr_rst_p0_d1 (high)

The following table shows the por_fmu_errgsr_rst_p0_d1 higher register bit assignments.

Table 4-1355 por_fmu_errgsr_rst_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

The following image shows the lower register bit assignments.

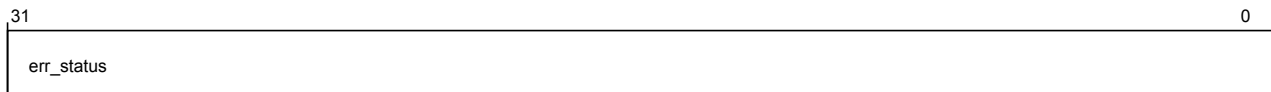


Figure 4-1339 por_fmu_errgsr_rst_p0_d1 (low)

The following table shows the por_fmu_errgsr_rst_p0_d1 lower register bit assignments.

Table 4-1356 por_fmu_errgsr_rst_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

por_fmu_errgsr_lsc_p0_d1

Provides device connected to p0_d1 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h30A8

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1340 por_fmu_por_fmu_errgsr_lsc_p0_d1 (high)

The following table shows the por_fmu_errgsr_lsc_p0_d1 higher register bit assignments.

Table 4-1357 por_fmu_por_fmu_errgsr_lsc_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

The following image shows the lower register bit assignments.

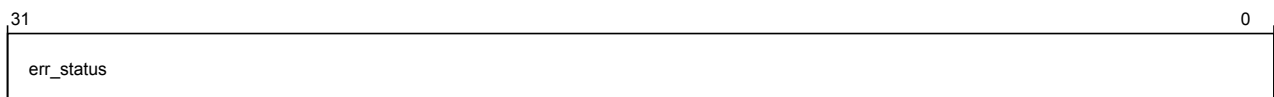


Figure 4-1341 por_fmu_por_fmu_errgsr_lsc_p0_d1 (low)

The following table shows the por_fmu_errgsr_lsc_p0_d1 lower register bit assignments.

Table 4-1358 por_fmu_por_fmu_errgsr_lsc_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

por_fmu_errgsr_ioc_p0_d1

Provides device connected to p0_d1 port <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h30B0
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

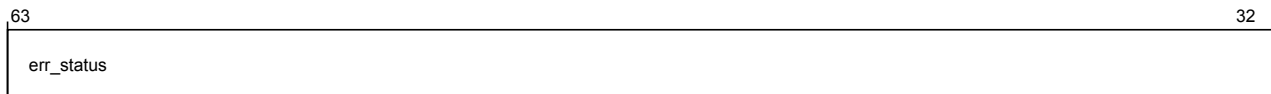


Figure 4-1342 por_fmu_por_fmu_errgsr_ioc_p0_d1 (high)

The following table shows the por_fmu_errgsr_ioc_p0_d1 higher register bit assignments.

Table 4-1359 por_fmu_por_fmu_errgsr_ioc_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1343 por_fmu_por_fmu_errgsr_ioc_p0_d1 (low)

The following table shows the por_fmu_errgsr_ioc_p0_d1 lower register bit assignments.

Table 4-1360 por_fmu_por_fmu_errgsr_ioc_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

por_fmu_errgsr_async_p0_d1

Provides device connected to p0_d1 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h30B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

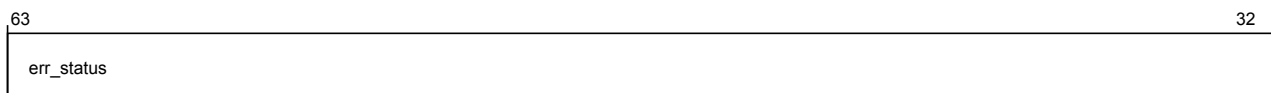


Figure 4-1344 por_fmu_por_fmu_errgsr_async_p0_d1 (high)

The following table shows the por_fmu_errgsr_async_p0_d1 higher register bit assignments.

Table 4-1361 por_fmu_por_fmu_errgsr_async_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1345 por_fmu_por_fmu_errgsr_async_p0_d1 (low)

The following table shows the por_fmu_errgsr_async_p0_d1 lower register bit assignments.

Table 4-1362 por_fmu_por_fmu_errgsr_async_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

por_fmu_errgsr_hang_p0_d1

Provides device connected to p0_d1 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h30C0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

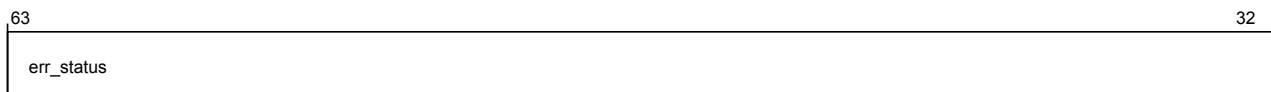


Figure 4-1346 por_fmu_por_fmu_errgsr_hang_p0_d1 (high)

The following table shows the por_fmu_errgsr_hang_p0_d1 higher register bit assignments.

Table 4-1363 por_fmu_por_fmu_errgsr_hang_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

The following image shows the lower register bit assignments.

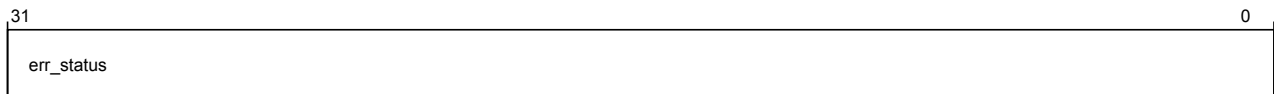


Figure 4-1347 por_fmu_por_fmu_errgsr_hang_p0_d1 (low)

The following table shows the por_fmu_errgsr_hang_p0_d1 lower register bit assignments.

Table 4-1364 por_fmu_por_fmu_errgsr_hang_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

por_fmu_errgsr_mpu_p0_d1

Provides device connected to p0_d1 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h30C8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

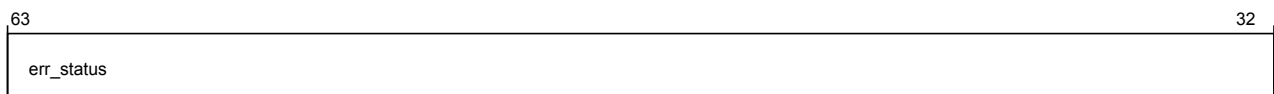


Figure 4-1348 por_fmu_por_fmu_errgsr_mpu_p0_d1 (high)

The following table shows the por_fmu_errgsr_mpu_p0_d1 higher register bit assignments.

Table 4-1365 por_fmu_por_fmu_errgsr_mpu_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

The following image shows the lower register bit assignments.

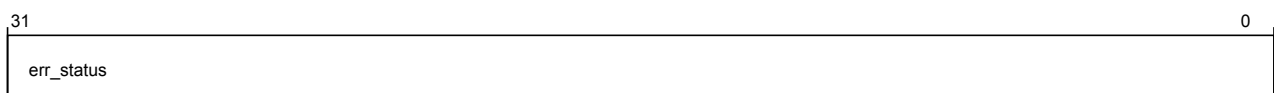


Figure 4-1349 por_fmu_por_fmu_errgsr_mpu_p0_d1 (low)

The following table shows the por_fmu_errgsr_mpu_p0_d1 lower register bit assignments.

Table 4-1366 por_fmu_por_fmu_errgsr_mpu_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

por_fmu_errgsr_eccue_p0_d1

Provides device connected to p0_d1 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h30D0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

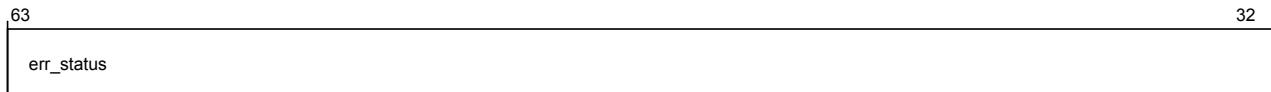


Figure 4-1350 por_fmu_por_fmu_errgsr_eccue_p0_d1 (high)

The following table shows the por_fmu_errgsr_eccue_p0_d1 higher register bit assignments.

Table 4-1367 por_fmu_por_fmu_errgsr_eccue_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

The following image shows the lower register bit assignments.

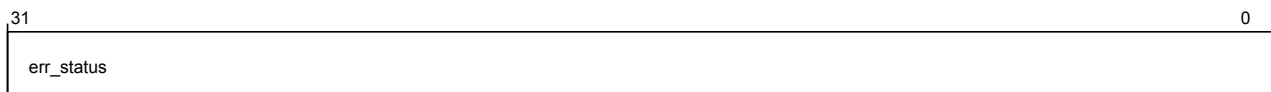


Figure 4-1351 por_fmu_por_fmu_errgsr_eccue_p0_d1 (low)

The following table shows the por_fmu_errgsr_eccue_p0_d1 lower register bit assignments.

Table 4-1368 por_fmu_por_fmu_errgsr_eccue_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

por_fmu_errgsr_eccce_p0_d1

Provides device connected to p0_d1 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h30D8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1352 por_fmu_errgsr_eccce_p0_d1 (high)

The following table shows the por_fmu_errgsr_eccce_p0_d1 higher register bit assignments.

Table 4-1369 por_fmu_errgsr_eccce_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

The following image shows the lower register bit assignments.

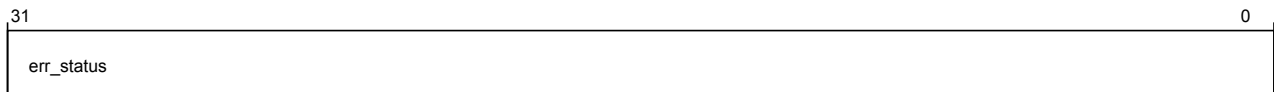


Figure 4-1353 por_fmu_errgsr_eccce_p0_d1 (low)

The following table shows the por_fmu_errgsr_eccce_p0_d1 lower register bit assignments.

Table 4-1370 por_fmu_errgsr_eccce_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d1'	RO	64'h0

por_fmu_errgsr_clk_p0_d2

Provides device connected to p0_d2 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h30E0

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1354 por_fmu_por_fmu_errgsr_clk_p0_d2 (high)

The following table shows the por_fmu_errgsr_clk_p0_d2 higher register bit assignments.

Table 4-1371 por_fmu_por_fmu_errgsr_clk_p0_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

The following image shows the lower register bit assignments.

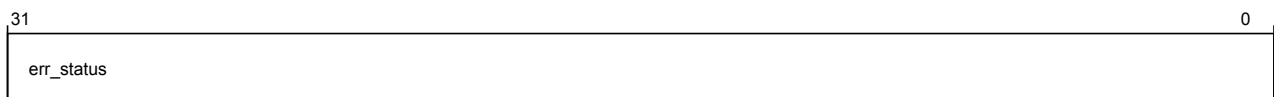


Figure 4-1355 por_fmu_por_fmu_errgsr_clk_p0_d2 (low)

The following table shows the por_fmu_errgsr_clk_p0_d2 lower register bit assignments.

Table 4-1372 por_fmu_por_fmu_errgsr_clk_p0_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

por_fmu_errgsr_rst_p0_d2

Provides device connected to p0_d2 port <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h30E8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

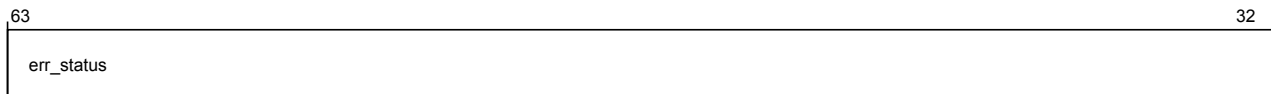


Figure 4-1356 por_fmu_por_fmu_errgsr_rst_p0_d2 (high)

The following table shows the por_fmu_errgsr_rst_p0_d2 higher register bit assignments.

Table 4-1373 por_fmu_por_fmu_errgsr_rst_p0_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1357 por_fmu_por_fmu_errgsr_rst_p0_d2 (low)

The following table shows the por_fmu_errgsr_rst_p0_d2 lower register bit assignments.

Table 4-1374 por_fmu_por_fmu_errgsr_rst_p0_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

por_fmu_errgsr_lsc_p0_d2

Provides device connected to p0_d2 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h30F0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

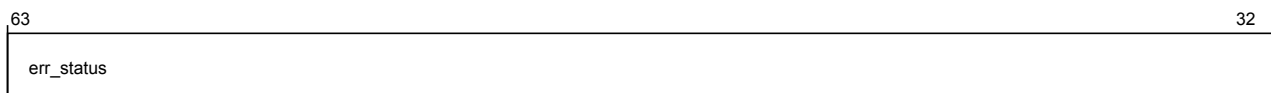


Figure 4-1358 por_fmu_por_fmu_errgsr_lsc_p0_d2 (high)

The following table shows the por_fmu_errgsr_lsc_p0_d2 higher register bit assignments.

Table 4-1375 `por_fmu_por_fmu_errgsr_lsc_p0_d2` (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of <code>por_errstatus_p0_d2<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1359 `por_fmu_por_fmu_errgsr_lsc_p0_d2` (low)

The following table shows the `por_fmu_errgsr_lsc_p0_d2` lower register bit assignments.

Table 4-1376 `por_fmu_por_fmu_errgsr_lsc_p0_d2` (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of <code>por_errstatus_p0_d2<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

`por_fmu_errgsr_ioc_p0_d2`

Provides device connected to `p0_d2` port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h30F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

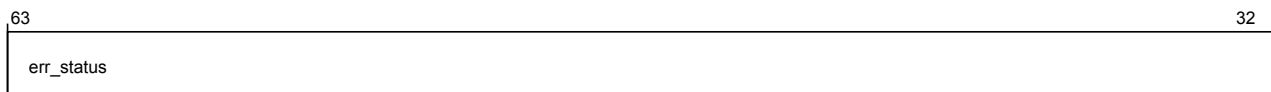


Figure 4-1360 `por_fmu_por_fmu_errgsr_ioc_p0_d2` (high)

The following table shows the `por_fmu_errgsr_ioc_p0_d2` higher register bit assignments.

Table 4-1377 `por_fmu_por_fmu_errgsr_ioc_p0_d2` (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of <code>por_errstatus_p0_d2<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

The following image shows the lower register bit assignments.

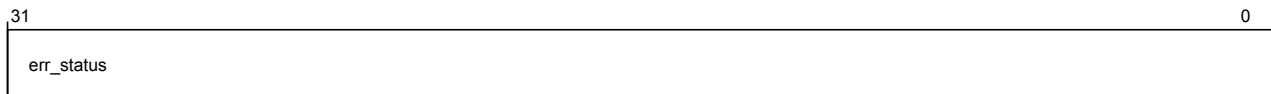


Figure 4-1361 por_fmu_por_fmu_errgsr_ioc_p0_d2 (low)

The following table shows the por_fmu_errgsr_ioc_p0_d2 lower register bit assignments.

Table 4-1378 por_fmu_por_fmu_errgsr_ioc_p0_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

por_fmu_errgsr_async_p0_d2

Provides device connected to p0_d2 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3100

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

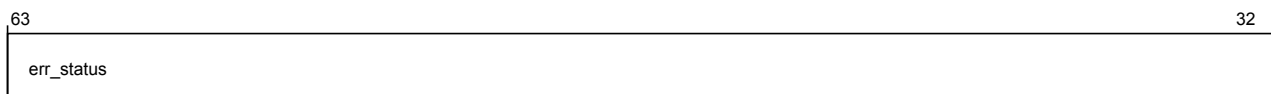


Figure 4-1362 por_fmu_por_fmu_errgsr_async_p0_d2 (high)

The following table shows the por_fmu_errgsr_async_p0_d2 higher register bit assignments.

Table 4-1379 por_fmu_por_fmu_errgsr_async_p0_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

The following image shows the lower register bit assignments.

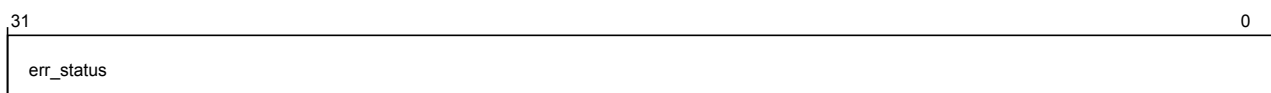


Figure 4-1363 por_fmu_por_fmu_errgsr_async_p0_d2 (low)

The following table shows the por_fmu_errgsr_async_p0_d2 lower register bit assignments.

Table 4-1380 por_fmu_por_fmu_errgsr_async_p0_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

por_fmu_errgsr_hang_p0_d2

Provides device connected to p0_d2 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3108

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

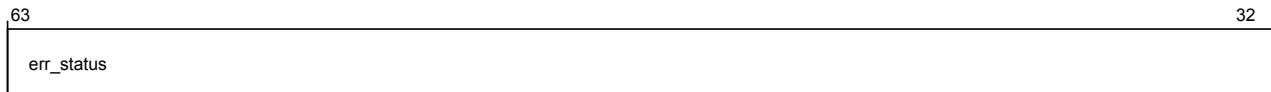


Figure 4-1364 por_fmu_por_fmu_errgsr_hang_p0_d2 (high)

The following table shows the por_fmu_errgsr_hang_p0_d2 higher register bit assignments.

Table 4-1381 por_fmu_por_fmu_errgsr_hang_p0_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

The following image shows the lower register bit assignments.

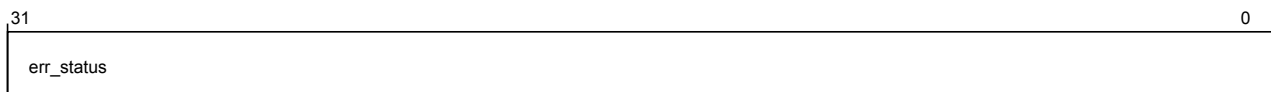


Figure 4-1365 por_fmu_por_fmu_errgsr_hang_p0_d2 (low)

The following table shows the por_fmu_errgsr_hang_p0_d2 lower register bit assignments.

Table 4-1382 por_fmu_por_fmu_errgsr_hang_p0_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

por_fmu_errgsr_mpu_p0_d2

Provides device connected to p0_d2 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3110
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

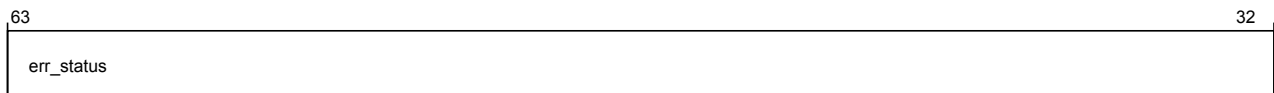


Figure 4-1366 por_fmu_errgsr_mpu_p0_d2 (high)

The following table shows the por_fmu_errgsr_mpu_p0_d2 higher register bit assignments.

Table 4-1383 por_fmu_errgsr_mpu_p0_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

The following image shows the lower register bit assignments.

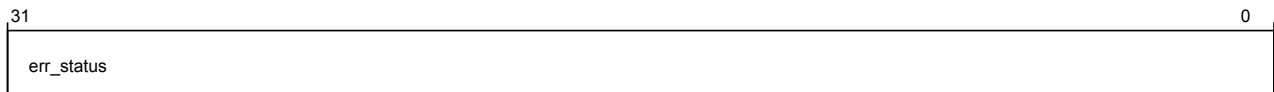


Figure 4-1367 por_fmu_errgsr_mpu_p0_d2 (low)

The following table shows the por_fmu_errgsr_mpu_p0_d2 lower register bit assignments.

Table 4-1384 por_fmu_errgsr_mpu_p0_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

por_fmu_errgsr_eccue_p0_d2

Provides device connected to p0_d2 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3118

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1368 por_fmu_por_fmu_errgsr_eccue_p0_d2 (high)

The following table shows the por_fmu_errgsr_eccue_p0_d2 higher register bit assignments.

Table 4-1385 por_fmu_por_fmu_errgsr_eccue_p0_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

The following image shows the lower register bit assignments.

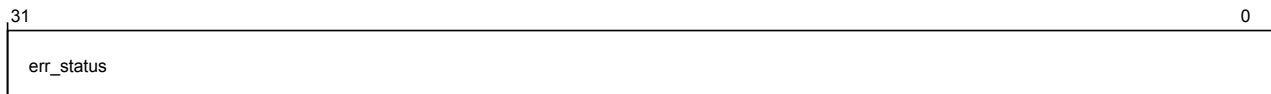


Figure 4-1369 por_fmu_por_fmu_errgsr_eccue_p0_d2 (low)

The following table shows the por_fmu_errgsr_eccue_p0_d2 lower register bit assignments.

Table 4-1386 por_fmu_por_fmu_errgsr_eccue_p0_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

por_fmu_errgsr_eccue_p0_d2

Provides device connected to p0_d2 port <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3120
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

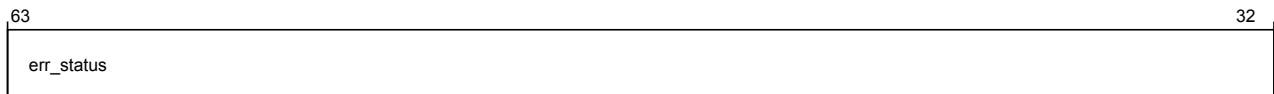


Figure 4-1370 por_fmu_por_fmu_errgsr_eccce_p0_d2 (high)

The following table shows the por_fmu_errgsr_eccce_p0_d2 higher register bit assignments.

Table 4-1387 por_fmu_por_fmu_errgsr_eccce_p0_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

The following image shows the lower register bit assignments.

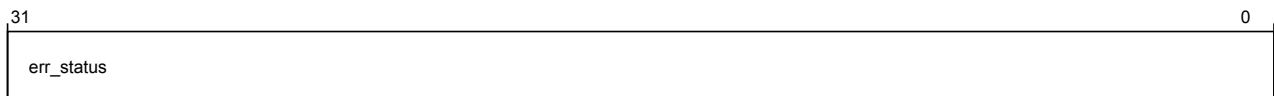


Figure 4-1371 por_fmu_por_fmu_errgsr_eccce_p0_d2 (low)

The following table shows the por_fmu_errgsr_eccce_p0_d2 lower register bit assignments.

Table 4-1388 por_fmu_por_fmu_errgsr_eccce_p0_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d2'	RO	64'h0

por_fmu_errgsr_clk_p0_d3

Provides device connected to p0_d3 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3128

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

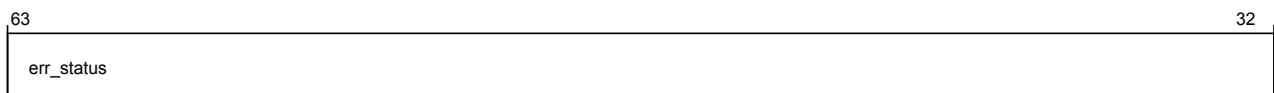


Figure 4-1372 por_fmu_por_fmu_errgsr_clk_p0_d3 (high)

The following table shows the por_fmu_errgsr_clk_p0_d3 higher register bit assignments.

Table 4-1389 `por_fmu_por_fmu_errgsr_clk_p0_d3` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p0_d3<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1373 `por_fmu_por_fmu_errgsr_clk_p0_d3` (low)

The following table shows the `por_fmu_errgsr_clk_p0_d3` lower register bit assignments.

Table 4-1390 `por_fmu_por_fmu_errgsr_clk_p0_d3` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>err_status</code>	Read-only copy of <code>por_errstatus_p0_d3<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

`por_fmu_errgsr_rst_p0_d3`

Provides device connected to p0_d3 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3130

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

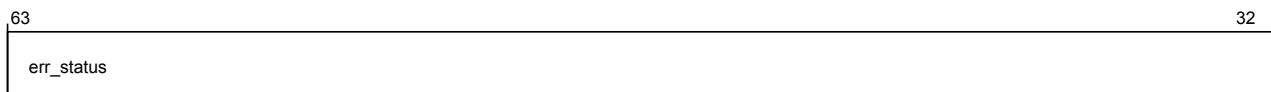


Figure 4-1374 `por_fmu_por_fmu_errgsr_rst_p0_d3` (high)

The following table shows the `por_fmu_errgsr_rst_p0_d3` higher register bit assignments.

Table 4-1391 `por_fmu_por_fmu_errgsr_rst_p0_d3` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p0_d3<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

The following image shows the lower register bit assignments.

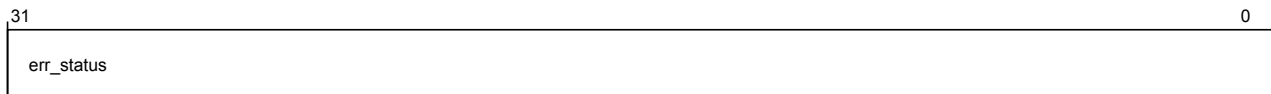


Figure 4-1375 por_fmu_errgsr_rst_p0_d3 (low)

The following table shows the por_fmu_errgsr_rst_p0_d3 lower register bit assignments.

Table 4-1392 por_fmu_errgsr_rst_p0_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

por_fmu_errgsr_lsc_p0_d3

Provides device connected to p0_d3 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3138

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

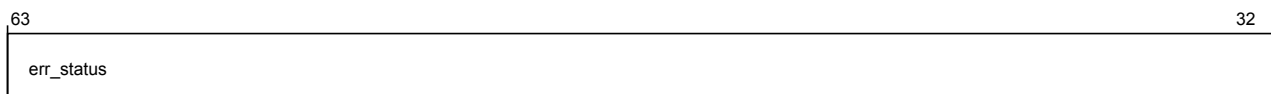


Figure 4-1376 por_fmu_errgsr_lsc_p0_d3 (high)

The following table shows the por_fmu_errgsr_lsc_p0_d3 higher register bit assignments.

Table 4-1393 por_fmu_errgsr_lsc_p0_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

The following image shows the lower register bit assignments.

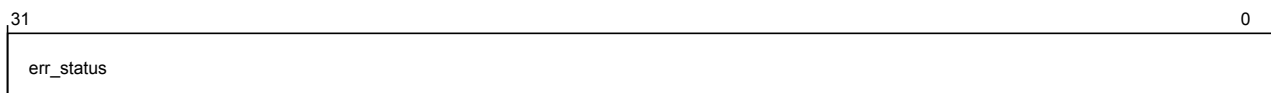


Figure 4-1377 por_fmu_errgsr_lsc_p0_d3 (low)

The following table shows the por_fmu_errgsr_lsc_p0_d3 lower register bit assignments.

Table 4-1394 por_fmu_por_fmu_errgsr_lsc_p0_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

por_fmu_errgsr_ioc_p0_d3

Provides device connected to p0_d3 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3140

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

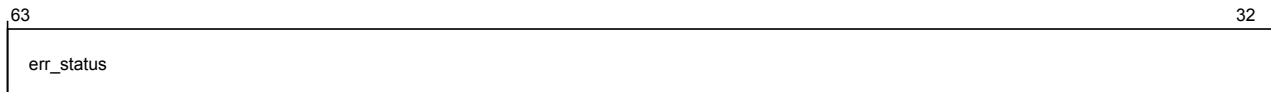


Figure 4-1378 por_fmu_por_fmu_errgsr_ioc_p0_d3 (high)

The following table shows the por_fmu_errgsr_ioc_p0_d3 higher register bit assignments.

Table 4-1395 por_fmu_por_fmu_errgsr_ioc_p0_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

The following image shows the lower register bit assignments.

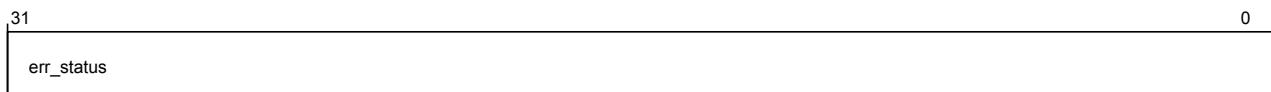


Figure 4-1379 por_fmu_por_fmu_errgsr_ioc_p0_d3 (low)

The following table shows the por_fmu_errgsr_ioc_p0_d3 lower register bit assignments.

Table 4-1396 por_fmu_por_fmu_errgsr_ioc_p0_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

por_fmu_errgsr_async_p0_d3

Provides device connected to p0_d3 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3148
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

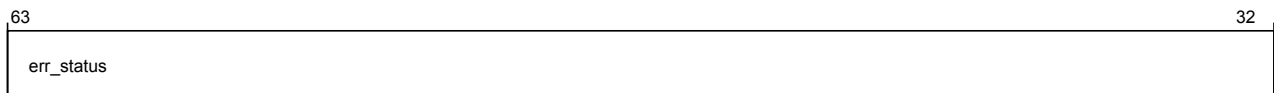


Figure 4-1380 por_fmu_errgsr_async_p0_d3 (high)

The following table shows the por_fmu_errgsr_async_p0_d3 higher register bit assignments.

Table 4-1397 por_fmu_errgsr_async_p0_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

The following image shows the lower register bit assignments.

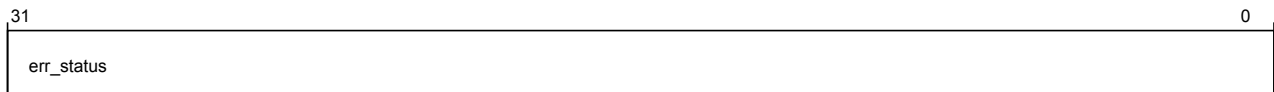


Figure 4-1381 por_fmu_errgsr_async_p0_d3 (low)

The following table shows the por_fmu_errgsr_async_p0_d3 lower register bit assignments.

Table 4-1398 por_fmu_errgsr_async_p0_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

por_fmu_errgsr_hang_p0_d3

Provides device connected to p0_d3 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3150

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1382 por_fmu_por_fmu_errgsr_hang_p0_d3 (high)

The following table shows the por_fmu_errgsr_hang_p0_d3 higher register bit assignments.

Table 4-1399 por_fmu_por_fmu_errgsr_hang_p0_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

The following image shows the lower register bit assignments.

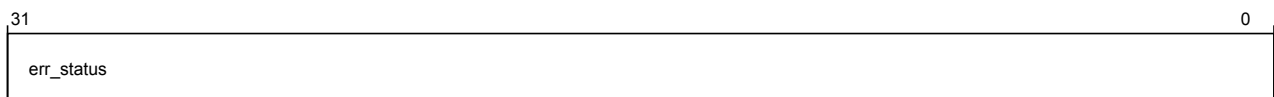


Figure 4-1383 por_fmu_por_fmu_errgsr_hang_p0_d3 (low)

The following table shows the por_fmu_errgsr_hang_p0_d3 lower register bit assignments.

Table 4-1400 por_fmu_por_fmu_errgsr_hang_p0_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

por_fmu_errgsr_mpu_p0_d3

Provides device connected to p0_d3 port <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3158
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

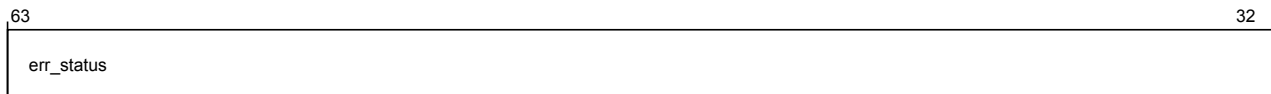


Figure 4-1384 por_fmu_por_fmu_errgsr_mpu_p0_d3 (high)

The following table shows the por_fmu_errgsr_mpu_p0_d3 higher register bit assignments.

Table 4-1401 por_fmu_por_fmu_errgsr_mpu_p0_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1385 por_fmu_por_fmu_errgsr_mpu_p0_d3 (low)

The following table shows the por_fmu_errgsr_mpu_p0_d3 lower register bit assignments.

Table 4-1402 por_fmu_por_fmu_errgsr_mpu_p0_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

por_fmu_errgsr_eccue_p0_d3

Provides device connected to p0_d3 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3160

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

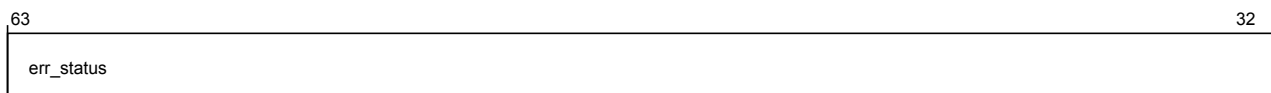


Figure 4-1386 por_fmu_por_fmu_errgsr_eccue_p0_d3 (high)

The following table shows the por_fmu_errgsr_eccue_p0_d3 higher register bit assignments.

Table 4-1403 por_fmu_por_fmu_errgsr_eccue_p0_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1387 por_fmu_por_fmu_errgsr_eccue_p0_d3 (low)

The following table shows the por_fmu_errgsr_eccue_p0_d3 lower register bit assignments.

Table 4-1404 por_fmu_por_fmu_errgsr_eccue_p0_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

por_fmu_errgsr_eccce_p0_d3

Provides device connected to p0_d3 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3168

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

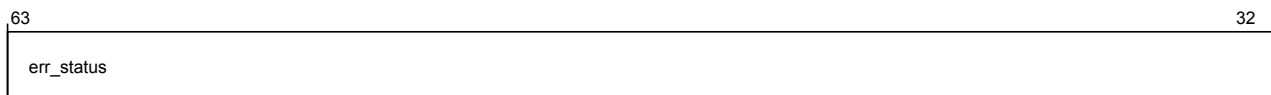


Figure 4-1388 por_fmu_por_fmu_errgsr_eccce_p0_d3 (high)

The following table shows the por_fmu_errgsr_eccce_p0_d3 higher register bit assignments.

Table 4-1405 por_fmu_por_fmu_errgsr_eccce_p0_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

The following image shows the lower register bit assignments.

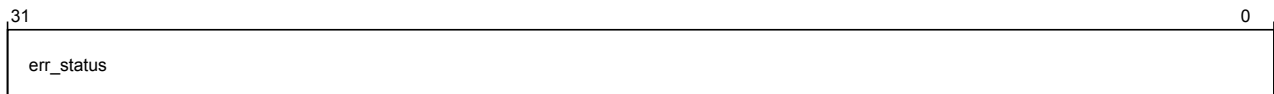


Figure 4-1389 por_fmu_por_fmu_errgsr_eccce_p0_d3 (low)

The following table shows the por_fmu_errgsr_eccce_p0_d3 lower register bit assignments.

Table 4-1406 por_fmu_por_fmu_errgsr_eccce_p0_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p0_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p0_d3'	RO	64'h0

por_fmu_errgsr_clk_p1_d0

Provides device connected to p1_d0 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3170

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

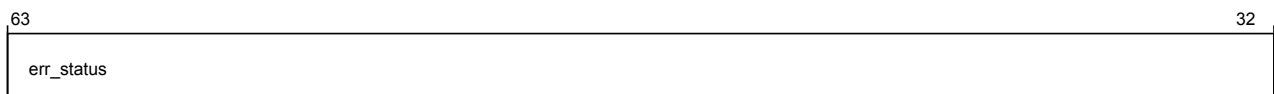


Figure 4-1390 por_fmu_por_fmu_errgsr_clk_p1_d0 (high)

The following table shows the por_fmu_errgsr_clk_p1_d0 higher register bit assignments.

Table 4-1407 por_fmu_por_fmu_errgsr_clk_p1_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

The following image shows the lower register bit assignments.

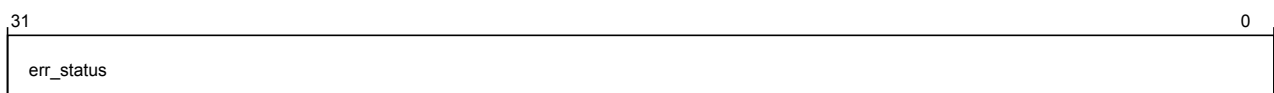


Figure 4-1391 por_fmu_por_fmu_errgsr_clk_p1_d0 (low)

The following table shows the por_fmu_errgsr_clk_p1_d0 lower register bit assignments.

Table 4-1408 por_fmu_por_fmu_errgsr_clk_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

por_fmu_errgsr_rst_p1_d0

Provides device connected to p1_d0 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3178

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

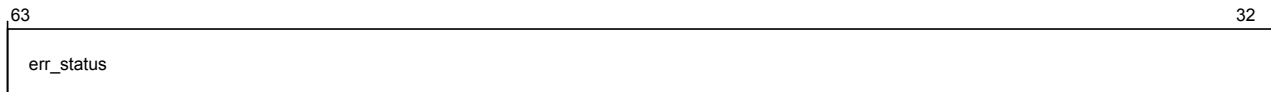


Figure 4-1392 por_fmu_por_fmu_errgsr_rst_p1_d0 (high)

The following table shows the por_fmu_errgsr_rst_p1_d0 higher register bit assignments.

Table 4-1409 por_fmu_por_fmu_errgsr_rst_p1_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

The following image shows the lower register bit assignments.

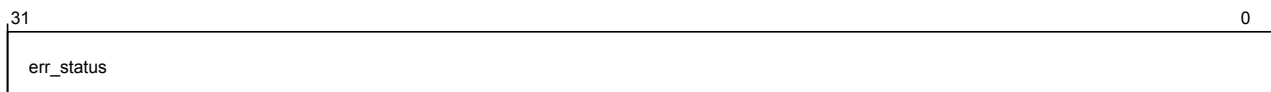


Figure 4-1393 por_fmu_por_fmu_errgsr_rst_p1_d0 (low)

The following table shows the por_fmu_errgsr_rst_p1_d0 lower register bit assignments.

Table 4-1410 por_fmu_por_fmu_errgsr_rst_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

por_fmu_errgsr_lsc_p1_d0

Provides device connected to p1_d0 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3180
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

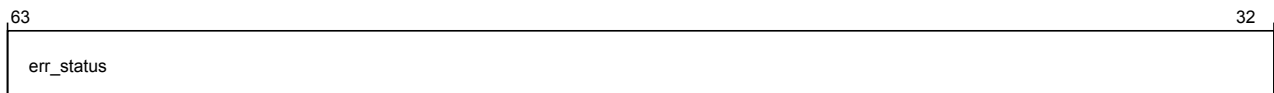


Figure 4-1394 por_fmu_por_fmu_errgsr_lsc_p1_d0 (high)

The following table shows the por_fmu_errgsr_lsc_p1_d0 higher register bit assignments.

Table 4-1411 por_fmu_por_fmu_errgsr_lsc_p1_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

The following image shows the lower register bit assignments.

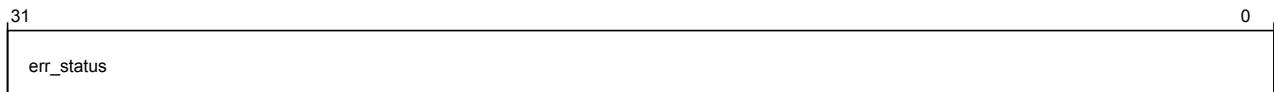


Figure 4-1395 por_fmu_por_fmu_errgsr_lsc_p1_d0 (low)

The following table shows the por_fmu_errgsr_lsc_p1_d0 lower register bit assignments.

Table 4-1412 por_fmu_por_fmu_errgsr_lsc_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

por_fmu_errgsr_ioc_p1_d0

Provides device connected to p1_d0 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3188

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1396 por_fmu_por_fmu_errgsr_ioc_p1_d0 (high)

The following table shows the por_fmu_errgsr_ioc_p1_d0 higher register bit assignments.

Table 4-1413 por_fmu_por_fmu_errgsr_ioc_p1_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

The following image shows the lower register bit assignments.

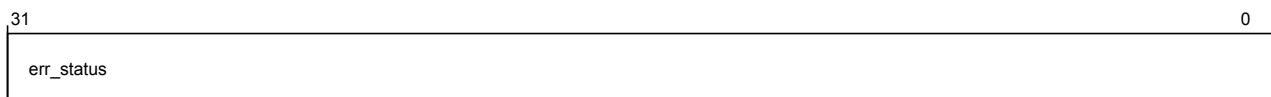


Figure 4-1397 por_fmu_por_fmu_errgsr_ioc_p1_d0 (low)

The following table shows the por_fmu_errgsr_ioc_p1_d0 lower register bit assignments.

Table 4-1414 por_fmu_por_fmu_errgsr_ioc_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

por_fmu_errgsr_async_p1_d0

Provides device connected to p1_d0 port <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3190
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

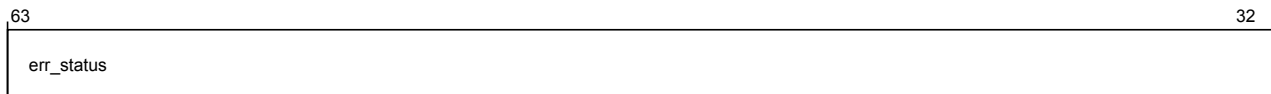


Figure 4-1398 por_fmu_por_fmu_errgsr_async_p1_d0 (high)

The following table shows the por_fmu_errgsr_async_p1_d0 higher register bit assignments.

Table 4-1415 por_fmu_por_fmu_errgsr_async_p1_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1399 por_fmu_por_fmu_errgsr_async_p1_d0 (low)

The following table shows the por_fmu_errgsr_async_p1_d0 lower register bit assignments.

Table 4-1416 por_fmu_por_fmu_errgsr_async_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

por_fmu_errgsr_hang_p1_d0

Provides device connected to p1_d0 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3198

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

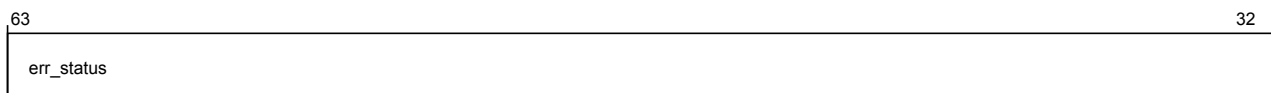


Figure 4-1400 por_fmu_por_fmu_errgsr_hang_p1_d0 (high)

The following table shows the por_fmu_errgsr_hang_p1_d0 higher register bit assignments.

Table 4-1417 `por_fmu_por_fmu_errgsr_hang_p1_d0` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p1_d0<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1401 `por_fmu_por_fmu_errgsr_hang_p1_d0` (low)

The following table shows the `por_fmu_errgsr_hang_p1_d0` lower register bit assignments.

Table 4-1418 `por_fmu_por_fmu_errgsr_hang_p1_d0` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>err_status</code>	Read-only copy of <code>por_errstatus_p1_d0<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

`por_fmu_errgsr_mpu_p1_d0`

Provides device connected to p1_d0 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h31A0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

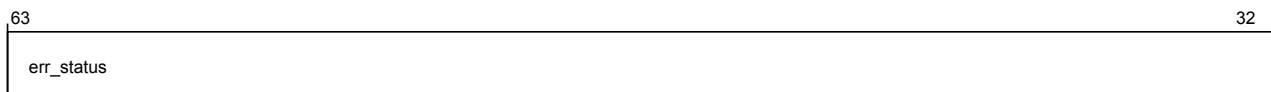


Figure 4-1402 `por_fmu_por_fmu_errgsr_mpu_p1_d0` (high)

The following table shows the `por_fmu_errgsr_mpu_p1_d0` higher register bit assignments.

Table 4-1419 `por_fmu_por_fmu_errgsr_mpu_p1_d0` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p1_d0<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

The following image shows the lower register bit assignments.

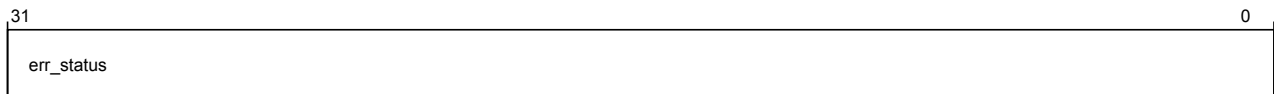


Figure 4-1403 por_fmu_por_fmu_errgsr_mpu_p1_d0 (low)

The following table shows the por_fmu_errgsr_mpu_p1_d0 lower register bit assignments.

Table 4-1420 por_fmu_por_fmu_errgsr_mpu_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

por_fmu_errgsr_eccue_p1_d0

Provides device connected to p1_d0 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h31A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

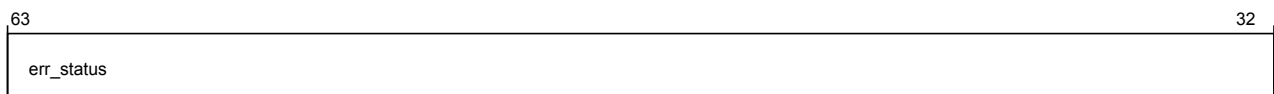


Figure 4-1404 por_fmu_por_fmu_errgsr_eccue_p1_d0 (high)

The following table shows the por_fmu_errgsr_eccue_p1_d0 higher register bit assignments.

Table 4-1421 por_fmu_por_fmu_errgsr_eccue_p1_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

The following image shows the lower register bit assignments.

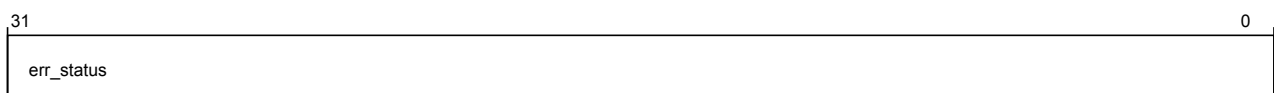


Figure 4-1405 por_fmu_por_fmu_errgsr_eccue_p1_d0 (low)

The following table shows the por_fmu_errgsr_eccue_p1_d0 lower register bit assignments.

Table 4-1422 por_fmu_por_fmu_errgsr_eccue_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

por_fmu_errgsr_eccce_p1_d0

Provides device connected to p1_d0 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h31B0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

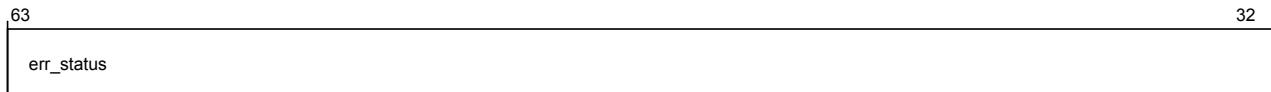


Figure 4-1406 por_fmu_por_fmu_errgsr_eccce_p1_d0 (high)

The following table shows the por_fmu_errgsr_eccce_p1_d0 higher register bit assignments.

Table 4-1423 por_fmu_por_fmu_errgsr_eccce_p1_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

The following image shows the lower register bit assignments.

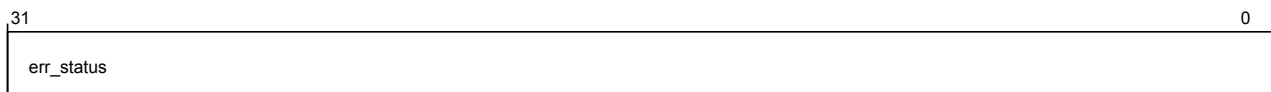


Figure 4-1407 por_fmu_por_fmu_errgsr_eccce_p1_d0 (low)

The following table shows the por_fmu_errgsr_eccce_p1_d0 lower register bit assignments.

Table 4-1424 por_fmu_por_fmu_errgsr_eccce_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d0<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d0'	RO	64'h0

por_fmu_errgsr_clk_p1_d1

Provides device connected to p1_d1 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h31B8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1408 por_fmu_por_fmu_errgsr_clk_p1_d1 (high)

The following table shows the por_fmu_errgsr_clk_p1_d1 higher register bit assignments.

Table 4-1425 por_fmu_por_fmu_errgsr_clk_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

The following image shows the lower register bit assignments.

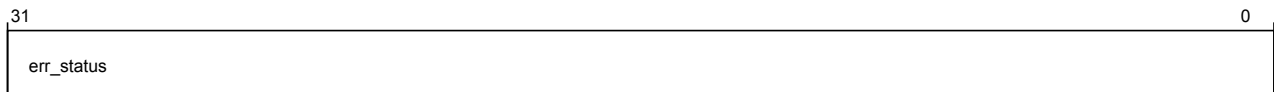


Figure 4-1409 por_fmu_por_fmu_errgsr_clk_p1_d1 (low)

The following table shows the por_fmu_errgsr_clk_p1_d1 lower register bit assignments.

Table 4-1426 por_fmu_por_fmu_errgsr_clk_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

por_fmu_errgsr_rst_p1_d1

Provides device connected to p1_d1 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h31C0

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1410 por_fmu_por_fmu_errgsr_rst_p1_d1 (high)

The following table shows the por_fmu_errgsr_rst_p1_d1 higher register bit assignments.

Table 4-1427 por_fmu_por_fmu_errgsr_rst_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

The following image shows the lower register bit assignments.

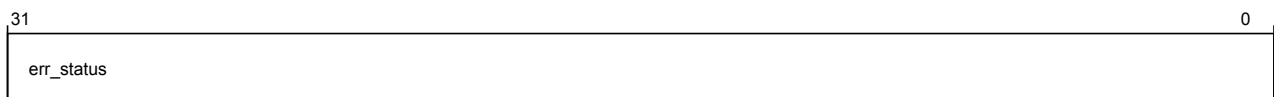


Figure 4-1411 por_fmu_por_fmu_errgsr_rst_p1_d1 (low)

The following table shows the por_fmu_errgsr_rst_p1_d1 lower register bit assignments.

Table 4-1428 por_fmu_por_fmu_errgsr_rst_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

por_fmu_errgsr_lsc_p1_d1

Provides device connected to p1_d1 port <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h31C8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

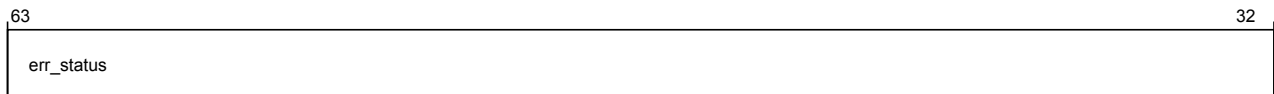


Figure 4-1412 por_fmu_por_fmu_errgsr_lsc_p1_d1 (high)

The following table shows the por_fmu_errgsr_lsc_p1_d1 higher register bit assignments.

Table 4-1429 por_fmu_por_fmu_errgsr_lsc_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

The following image shows the lower register bit assignments.

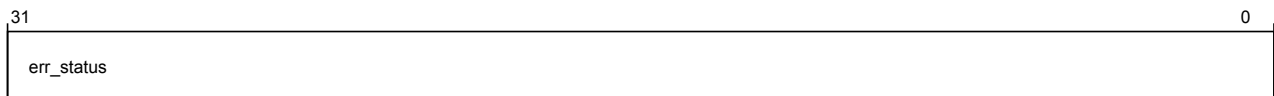


Figure 4-1413 por_fmu_por_fmu_errgsr_lsc_p1_d1 (low)

The following table shows the por_fmu_errgsr_lsc_p1_d1 lower register bit assignments.

Table 4-1430 por_fmu_por_fmu_errgsr_lsc_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

por_fmu_errgsr_ioc_p1_d1

Provides device connected to p1_d1 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h31D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

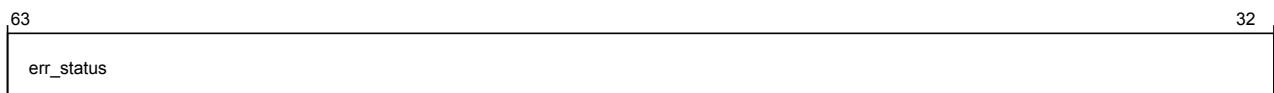


Figure 4-1414 por_fmu_por_fmu_errgsr_ioc_p1_d1 (high)

The following table shows the por_fmu_errgsr_ioc_p1_d1 higher register bit assignments.

Table 4-1431 por_fmu_por_fmu_errgsr_ioc_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1415 por_fmu_por_fmu_errgsr_ioc_p1_d1 (low)

The following table shows the por_fmu_errgsr_ioc_p1_d1 lower register bit assignments.

Table 4-1432 por_fmu_por_fmu_errgsr_ioc_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

por_fmu_errgsr_async_p1_d1

Provides device connected to p1_d1 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h31D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

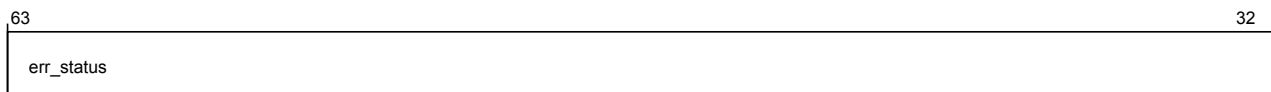


Figure 4-1416 por_fmu_por_fmu_errgsr_async_p1_d1 (high)

The following table shows the por_fmu_errgsr_async_p1_d1 higher register bit assignments.

Table 4-1433 por_fmu_por_fmu_errgsr_async_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

The following image shows the lower register bit assignments.

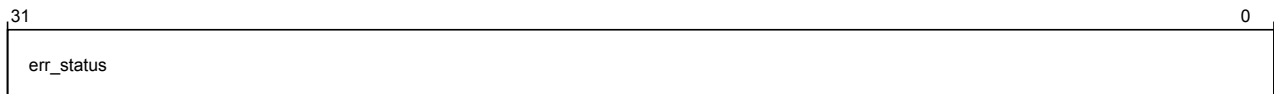


Figure 4-1417 por_fmu_por_fmu_errgsr_async_p1_d1 (low)

The following table shows the por_fmu_errgsr_async_p1_d1 lower register bit assignments.

Table 4-1434 por_fmu_por_fmu_errgsr_async_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

por_fmu_errgsr_hang_p1_d1

Provides device connected to p1_d1 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h31E0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

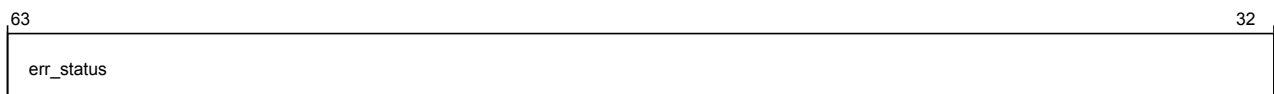


Figure 4-1418 por_fmu_por_fmu_errgsr_hang_p1_d1 (high)

The following table shows the por_fmu_errgsr_hang_p1_d1 higher register bit assignments.

Table 4-1435 por_fmu_por_fmu_errgsr_hang_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

The following image shows the lower register bit assignments.

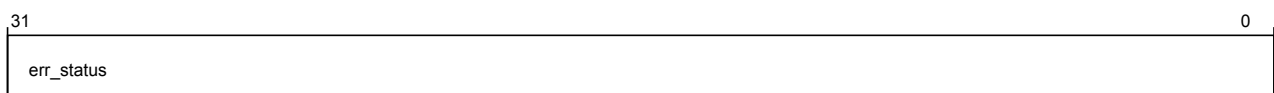


Figure 4-1419 por_fmu_por_fmu_errgsr_hang_p1_d1 (low)

The following table shows the por_fmu_errgsr_hang_p1_d1 lower register bit assignments.

Table 4-1436 por_fmu_por_fmu_errgsr_hang_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

por_fmu_errgsr_mpu_p1_d1

Provides device connected to p1_d1 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h31E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

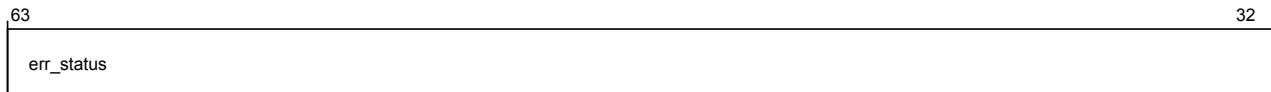


Figure 4-1420 por_fmu_por_fmu_errgsr_mpu_p1_d1 (high)

The following table shows the por_fmu_errgsr_mpu_p1_d1 higher register bit assignments.

Table 4-1437 por_fmu_por_fmu_errgsr_mpu_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

The following image shows the lower register bit assignments.

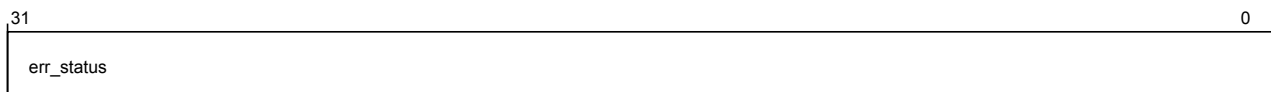


Figure 4-1421 por_fmu_por_fmu_errgsr_mpu_p1_d1 (low)

The following table shows the por_fmu_errgsr_mpu_p1_d1 lower register bit assignments.

Table 4-1438 por_fmu_por_fmu_errgsr_mpu_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

por_fmu_errgsr_eccue_p1_d1

Provides device connected to p1_d1 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h31F0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1422 por_fmu_por_fmu_errgsr_eccue_p1_d1 (high)

The following table shows the por_fmu_errgsr_eccue_p1_d1 higher register bit assignments.

Table 4-1439 por_fmu_por_fmu_errgsr_eccue_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

The following image shows the lower register bit assignments.

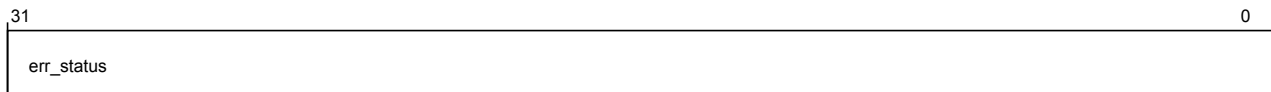


Figure 4-1423 por_fmu_por_fmu_errgsr_eccue_p1_d1 (low)

The following table shows the por_fmu_errgsr_eccue_p1_d1 lower register bit assignments.

Table 4-1440 por_fmu_por_fmu_errgsr_eccue_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

por_fmu_errgsr_eccce_p1_d1

Provides device connected to p1_d1 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h31F8

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1424 por_fmu_por_fmu_errgsr_eccce_p1_d1 (high)

The following table shows the por_fmu_errgsr_eccce_p1_d1 higher register bit assignments.

Table 4-1441 por_fmu_por_fmu_errgsr_eccce_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

The following image shows the lower register bit assignments.

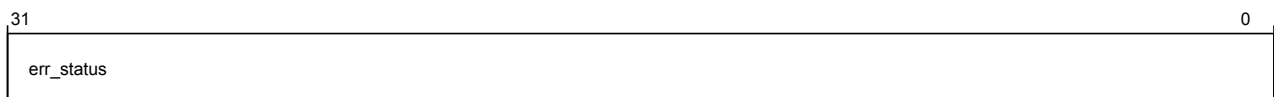


Figure 4-1425 por_fmu_por_fmu_errgsr_eccce_p1_d1 (low)

The following table shows the por_fmu_errgsr_eccce_p1_d1 lower register bit assignments.

Table 4-1442 por_fmu_por_fmu_errgsr_eccce_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d1<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d1'	RO	64'h0

por_fmu_errgsr_clk_p1_d2

Provides device connected to p1_d2 port <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3200
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

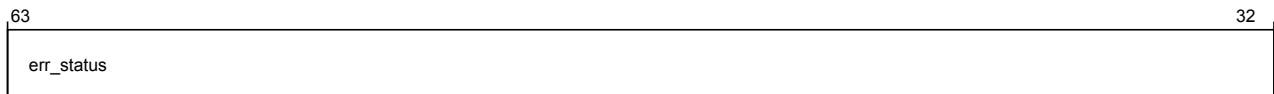


Figure 4-1426 por_fmu_por_fmu_errgsr_clk_p1_d2 (high)

The following table shows the por_fmu_errgsr_clk_p1_d2 higher register bit assignments.

Table 4-1443 por_fmu_por_fmu_errgsr_clk_p1_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

The following image shows the lower register bit assignments.

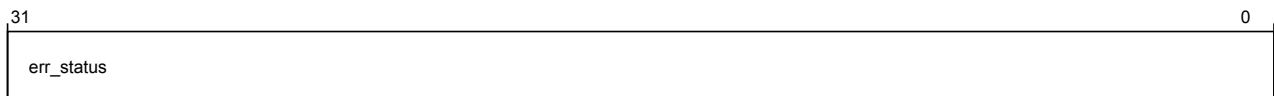


Figure 4-1427 por_fmu_por_fmu_errgsr_clk_p1_d2 (low)

The following table shows the por_fmu_errgsr_clk_p1_d2 lower register bit assignments.

Table 4-1444 por_fmu_por_fmu_errgsr_clk_p1_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

por_fmu_errgsr_rst_p1_d2

Provides device connected to p1_d2 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3208

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

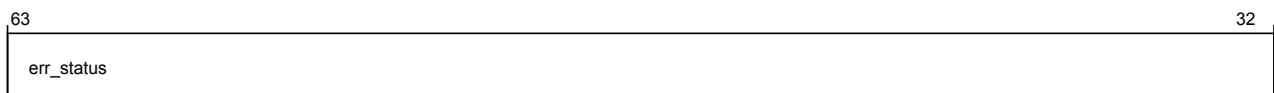


Figure 4-1428 por_fmu_por_fmu_errgsr_rst_p1_d2 (high)

The following table shows the por_fmu_errgsr_rst_p1_d2 higher register bit assignments.

Table 4-1445 `por_fmu_por_fmu_errgsr_rst_p1_d2` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p1_d2<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1429 `por_fmu_por_fmu_errgsr_rst_p1_d2` (low)

The following table shows the `por_fmu_errgsr_rst_p1_d2` lower register bit assignments.

Table 4-1446 `por_fmu_por_fmu_errgsr_rst_p1_d2` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>err_status</code>	Read-only copy of <code>por_errstatus_p1_d2<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

`por_fmu_errgsr_lsc_p1_d2`

Provides device connected to p1_d2 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3210

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

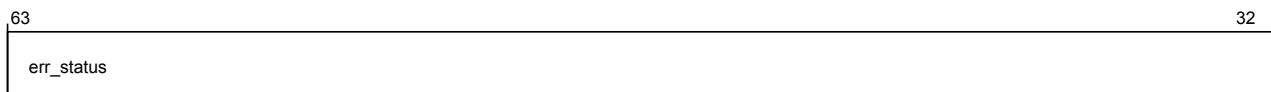


Figure 4-1430 `por_fmu_por_fmu_errgsr_lsc_p1_d2` (high)

The following table shows the `por_fmu_errgsr_lsc_p1_d2` higher register bit assignments.

Table 4-1447 `por_fmu_por_fmu_errgsr_lsc_p1_d2` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p1_d2<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

The following image shows the lower register bit assignments.

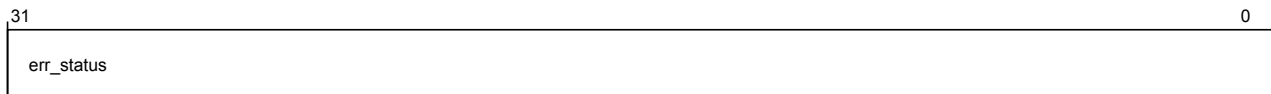


Figure 4-1431 por_fmu_por_fmu_errgsr_lsc_p1_d2 (low)

The following table shows the por_fmu_errgsr_lsc_p1_d2 lower register bit assignments.

Table 4-1448 por_fmu_por_fmu_errgsr_lsc_p1_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

por_fmu_errgsr_ioc_p1_d2

Provides device connected to p1_d2 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3218

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

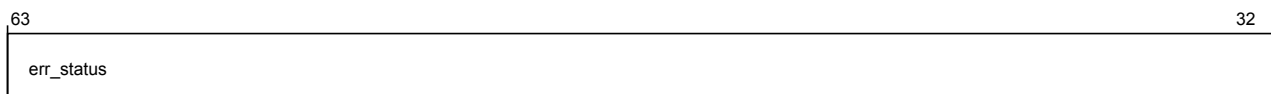


Figure 4-1432 por_fmu_por_fmu_errgsr_ioc_p1_d2 (high)

The following table shows the por_fmu_errgsr_ioc_p1_d2 higher register bit assignments.

Table 4-1449 por_fmu_por_fmu_errgsr_ioc_p1_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

The following image shows the lower register bit assignments.

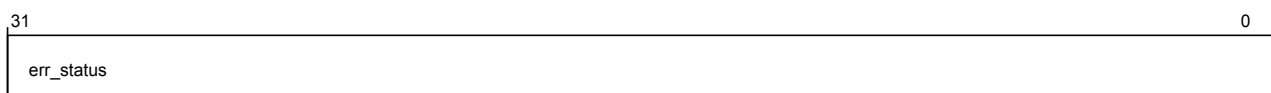


Figure 4-1433 por_fmu_por_fmu_errgsr_ioc_p1_d2 (low)

The following table shows the por_fmu_errgsr_ioc_p1_d2 lower register bit assignments.

Table 4-1450 por_fmu_por_fmu_errgsr_ioc_p1_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

por_fmu_errgsr_async_p1_d2

Provides device connected to p1_d2 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3220

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

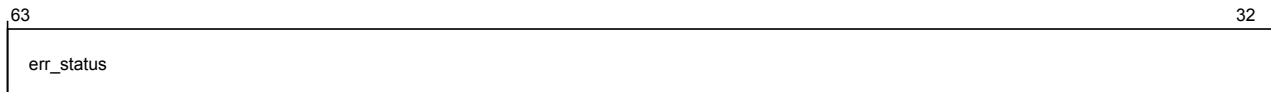


Figure 4-1434 por_fmu_por_fmu_errgsr_async_p1_d2 (high)

The following table shows the por_fmu_errgsr_async_p1_d2 higher register bit assignments.

Table 4-1451 por_fmu_por_fmu_errgsr_async_p1_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

The following image shows the lower register bit assignments.

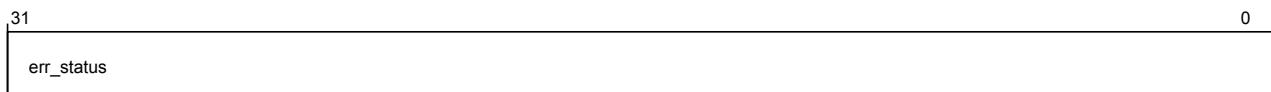


Figure 4-1435 por_fmu_por_fmu_errgsr_async_p1_d2 (low)

The following table shows the por_fmu_errgsr_async_p1_d2 lower register bit assignments.

Table 4-1452 por_fmu_por_fmu_errgsr_async_p1_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

por_fmu_errgsr_hang_p1_d2

Provides device connected to p1_d2 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3228
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

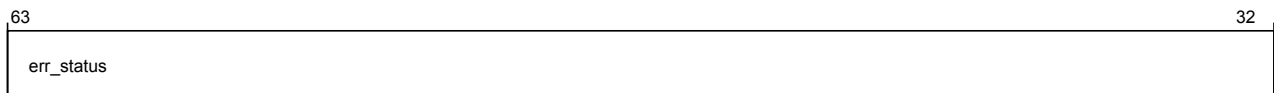


Figure 4-1436 por_fmu_por_fmu_errgsr_hang_p1_d2 (high)

The following table shows the por_fmu_errgsr_hang_p1_d2 higher register bit assignments.

Table 4-1453 por_fmu_por_fmu_errgsr_hang_p1_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

The following image shows the lower register bit assignments.

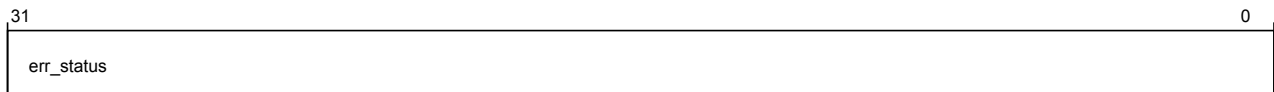


Figure 4-1437 por_fmu_por_fmu_errgsr_hang_p1_d2 (low)

The following table shows the por_fmu_errgsr_hang_p1_d2 lower register bit assignments.

Table 4-1454 por_fmu_por_fmu_errgsr_hang_p1_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

por_fmu_errgsr_mpu_p1_d2

Provides device connected to p1_d2 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3230

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1438 por_fmu_por_fmu_errgsr_mpu_p1_d2 (high)

The following table shows the por_fmu_errgsr_mpu_p1_d2 higher register bit assignments.

Table 4-1455 por_fmu_por_fmu_errgsr_mpu_p1_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

The following image shows the lower register bit assignments.

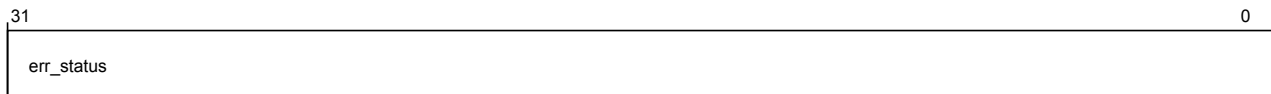


Figure 4-1439 por_fmu_por_fmu_errgsr_mpu_p1_d2 (low)

The following table shows the por_fmu_errgsr_mpu_p1_d2 lower register bit assignments.

Table 4-1456 por_fmu_por_fmu_errgsr_mpu_p1_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

por_fmu_errgsr_eccue_p1_d2

Provides device connected to p1_d2 port <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3238
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

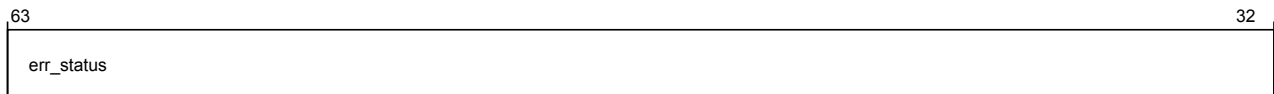


Figure 4-1440 por_fmu_por_fmu_errgsr_eccue_p1_d2 (high)

The following table shows the por_fmu_errgsr_eccue_p1_d2 higher register bit assignments.

Table 4-1457 por_fmu_por_fmu_errgsr_eccue_p1_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

The following image shows the lower register bit assignments.

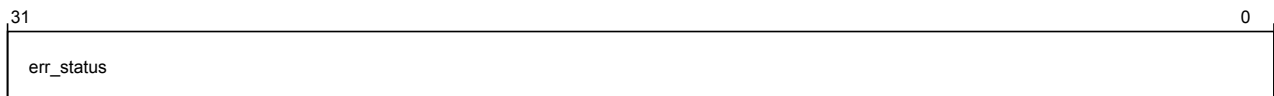


Figure 4-1441 por_fmu_por_fmu_errgsr_eccue_p1_d2 (low)

The following table shows the por_fmu_errgsr_eccue_p1_d2 lower register bit assignments.

Table 4-1458 por_fmu_por_fmu_errgsr_eccue_p1_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

por_fmu_errgsr_eccce_p1_d2

Provides device connected to p1_d2 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3240

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

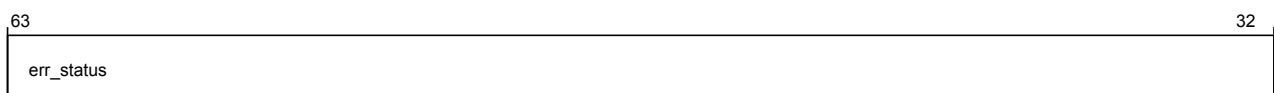


Figure 4-1442 por_fmu_por_fmu_errgsr_eccce_p1_d2 (high)

The following table shows the por_fmu_errgsr_eccce_p1_d2 higher register bit assignments.

Table 4-1459 por_fmu_por_fmu_errgsr_eccce_p1_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

The following image shows the lower register bit assignments.



Figure 4-1443 por_fmu_por_fmu_errgsr_eccce_p1_d2 (low)

The following table shows the por_fmu_errgsr_eccce_p1_d2 lower register bit assignments.

Table 4-1460 por_fmu_por_fmu_errgsr_eccce_p1_d2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d2<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d2'	RO	64'h0

por_fmu_errgsr_clk_p1_d3

Provides device connected to p1_d3 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3248

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

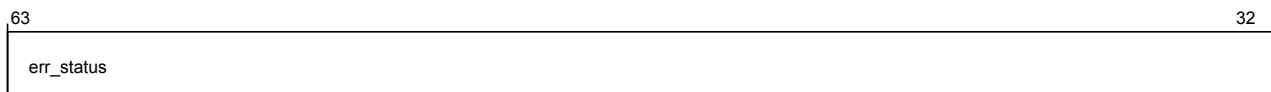


Figure 4-1444 por_fmu_por_fmu_errgsr_clk_p1_d3 (high)

The following table shows the por_fmu_errgsr_clk_p1_d3 higher register bit assignments.

Table 4-1461 por_fmu_por_fmu_errgsr_clk_p1_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

The following image shows the lower register bit assignments.

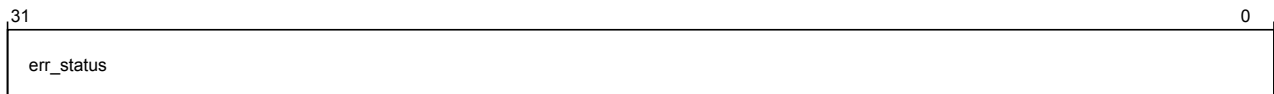


Figure 4-1445 `por_fmu_por_fmu_errgsr_clk_p1_d3` (low)

The following table shows the `por_fmu_errgsr_clk_p1_d3` lower register bit assignments.

Table 4-1462 `por_fmu_por_fmu_errgsr_clk_p1_d3` (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of <code>por_errstatus_p1_d3<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

`por_fmu_errgsr_rst_p1_d3`

Provides device connected to `p1_d3` port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3250

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

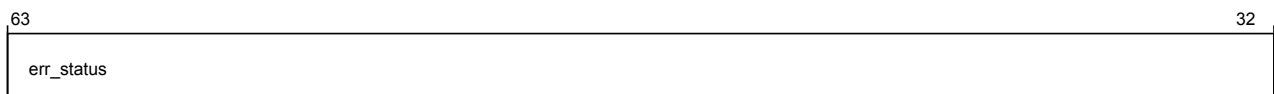


Figure 4-1446 `por_fmu_por_fmu_errgsr_rst_p1_d3` (high)

The following table shows the `por_fmu_errgsr_rst_p1_d3` higher register bit assignments.

Table 4-1463 `por_fmu_por_fmu_errgsr_rst_p1_d3` (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of <code>por_errstatus_p1_d3<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

The following image shows the lower register bit assignments.

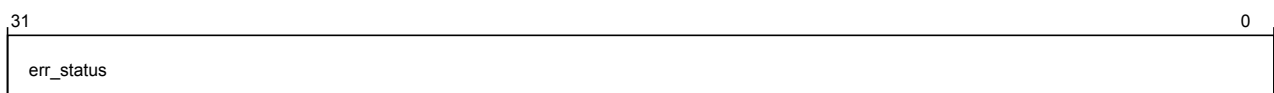


Figure 4-1447 `por_fmu_por_fmu_errgsr_rst_p1_d3` (low)

The following table shows the `por_fmu_errgsr_rst_p1_d3` lower register bit assignments.

Table 4-1464 por_fmu_por_fmu_errgsr_rst_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

por_fmu_errgsr_lsc_p1_d3

Provides device connected to p1_d3 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3258

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

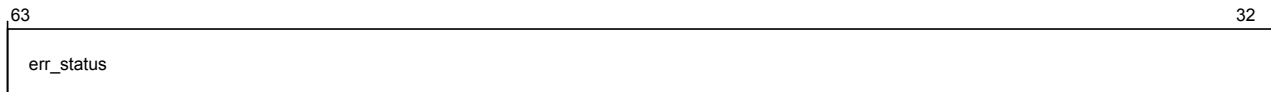


Figure 4-1448 por_fmu_por_fmu_errgsr_lsc_p1_d3 (high)

The following table shows the por_fmu_errgsr_lsc_p1_d3 higher register bit assignments.

Table 4-1465 por_fmu_por_fmu_errgsr_lsc_p1_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

The following image shows the lower register bit assignments.

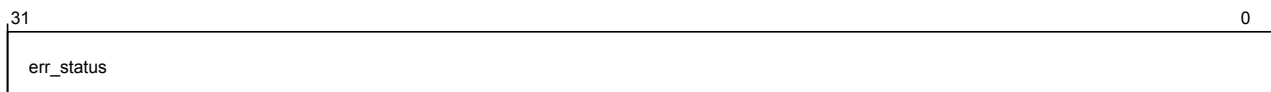


Figure 4-1449 por_fmu_por_fmu_errgsr_lsc_p1_d3 (low)

The following table shows the por_fmu_errgsr_lsc_p1_d3 lower register bit assignments.

Table 4-1466 por_fmu_por_fmu_errgsr_lsc_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

por_fmu_errgsr_ioc_p1_d3

Provides device connected to p1_d3 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3260
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

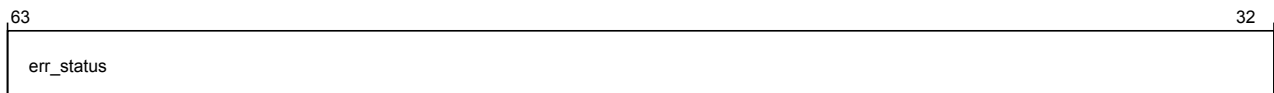


Figure 4-1450 por_fmu_por_fmu_errgsr_ioc_p1_d3 (high)

The following table shows the por_fmu_errgsr_ioc_p1_d3 higher register bit assignments.

Table 4-1467 por_fmu_por_fmu_errgsr_ioc_p1_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

The following image shows the lower register bit assignments.

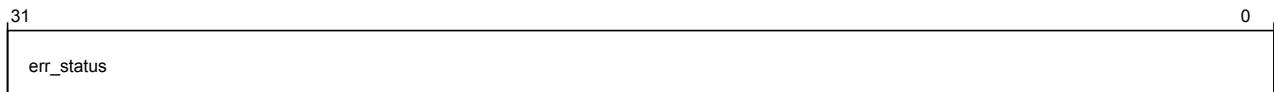


Figure 4-1451 por_fmu_por_fmu_errgsr_ioc_p1_d3 (low)

The following table shows the por_fmu_errgsr_ioc_p1_d3 lower register bit assignments.

Table 4-1468 por_fmu_por_fmu_errgsr_ioc_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

por_fmu_errgsr_async_p1_d3

Provides device connected to p1_d3 port <n> error status.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3268

Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1452 por_fmu_por_fmu_errgsr_async_p1_d3 (high)

The following table shows the por_fmu_errgsr_async_p1_d3 higher register bit assignments.

Table 4-1469 por_fmu_por_fmu_errgsr_async_p1_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

The following image shows the lower register bit assignments.

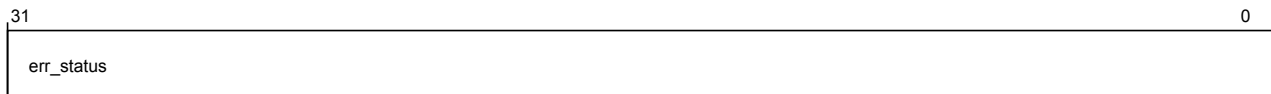


Figure 4-1453 por_fmu_por_fmu_errgsr_async_p1_d3 (low)

The following table shows the por_fmu_errgsr_async_p1_d3 lower register bit assignments.

Table 4-1470 por_fmu_por_fmu_errgsr_async_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

por_fmu_errgsr_hang_p1_d3

Provides device connected to p1_d3 port <n> error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3270
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

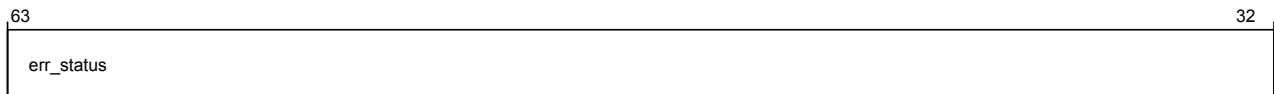


Figure 4-1454 por_fmu_por_fmu_errgsr_hang_p1_d3 (high)

The following table shows the por_fmu_errgsr_hang_p1_d3 higher register bit assignments.

Table 4-1471 por_fmu_por_fmu_errgsr_hang_p1_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

The following image shows the lower register bit assignments.

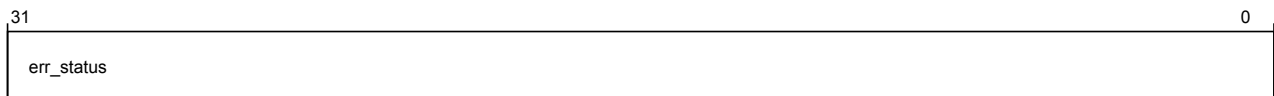


Figure 4-1455 por_fmu_por_fmu_errgsr_hang_p1_d3 (low)

The following table shows the por_fmu_errgsr_hang_p1_d3 lower register bit assignments.

Table 4-1472 por_fmu_por_fmu_errgsr_hang_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

por_fmu_errgsr_mpu_p1_d3

Provides device connected to p1_d3 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3278

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-1456 por_fmu_por_fmu_errgsr_mpu_p1_d3 (high)

The following table shows the por_fmu_errgsr_mpu_p1_d3 higher register bit assignments.

Table 4-1473 `por_fmu_por_fmu_errgsr_mpu_p1_d3` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p1_d3<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

The following image shows the lower register bit assignments.

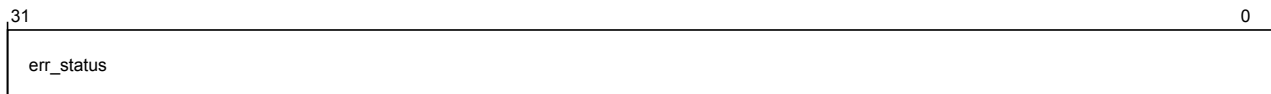


Figure 4-1457 `por_fmu_por_fmu_errgsr_mpu_p1_d3` (low)

The following table shows the `por_fmu_errgsr_mpu_p1_d3` lower register bit assignments.

Table 4-1474 `por_fmu_por_fmu_errgsr_mpu_p1_d3` (low)

Bits	Field name	Description	Type	Reset
31:0	<code>err_status</code>	Read-only copy of <code>por_errstatus_p1_d3<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

`por_fmu_errgsr_eccue_p1_d3`

Provides device connected to `p1_d3` port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3280

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

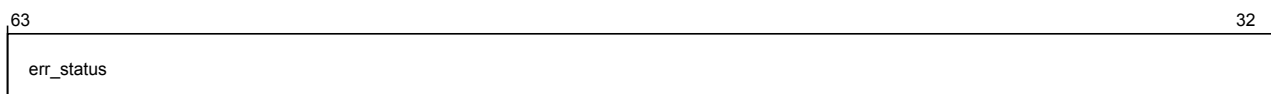


Figure 4-1458 `por_fmu_por_fmu_errgsr_eccue_p1_d3` (high)

The following table shows the `por_fmu_errgsr_eccue_p1_d3` higher register bit assignments.

Table 4-1475 `por_fmu_por_fmu_errgsr_eccue_p1_d3` (high)

Bits	Field name	Description	Type	Reset
63:32	<code>err_status</code>	Read-only copy of <code>por_errstatus_p1_d3<n>.V_ERR_TYPE</code> , where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

The following image shows the lower register bit assignments.

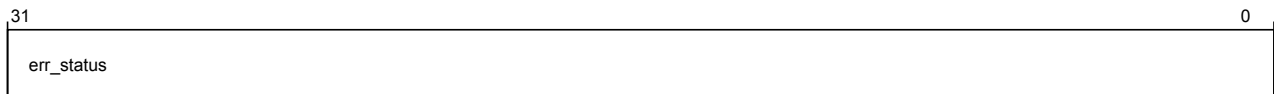


Figure 4-1459 por_fmu_por_fmu_errgsr_eccue_p1_d3 (low)

The following table shows the por_fmu_errgsr_eccue_p1_d3 lower register bit assignments.

Table 4-1476 por_fmu_por_fmu_errgsr_eccue_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

por_fmu_errgsr_eccce_p1_d3

Provides device connected to p1_d3 port <n> error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3288

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

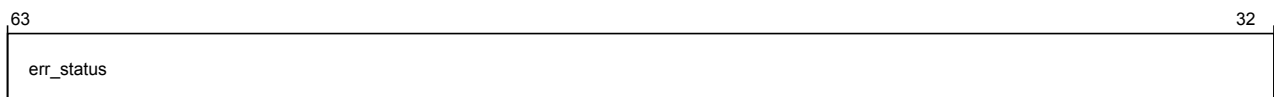


Figure 4-1460 por_fmu_por_fmu_errgsr_eccce_p1_d3 (high)

The following table shows the por_fmu_errgsr_eccce_p1_d3 higher register bit assignments.

Table 4-1477 por_fmu_por_fmu_errgsr_eccce_p1_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

The following image shows the lower register bit assignments.

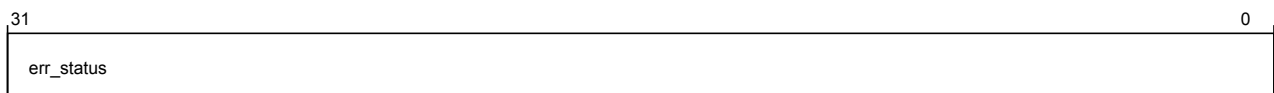


Figure 4-1461 por_fmu_por_fmu_errgsr_eccce_p1_d3 (low)

The following table shows the por_fmu_errgsr_eccce_p1_d3 lower register bit assignments.

Table 4-1478 por_fmu_por_fmu_errgsr_eccce_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status	Read-only copy of por_errstatus_p1_d3<n>.V_ERR_TYPE, where 'n' represents the logical id of the MXP that includes the FDC containing the 'por_errstatus_p1_d3'	RO	64'h0

4.3.15 MPU register descriptions

This section lists the MPU configuration registers.

por_mpu_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

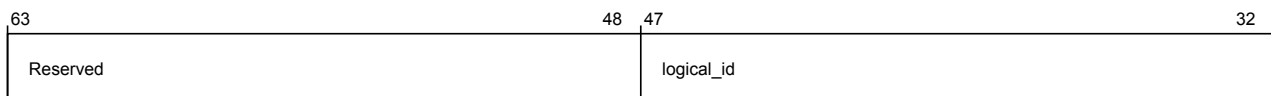


Figure 4-1462 por_mpu_por_mpu_node_info (high)

The following table shows the por_mpu_node_info higher register bit assignments.

Table 4-1479 por_mpu_por_mpu_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID NOTE: MPU logical ID is always set to 16'b0.	RO	16'h0

The following image shows the lower register bit assignments.

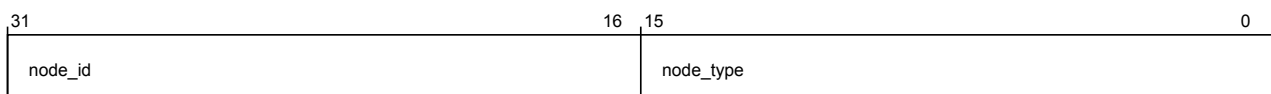


Figure 4-1463 por_mpu_por_mpu_node_info (low)

The following table shows the por_mpu_node_info lower register bit assignments.

Table 4-1480 por_mpu_por_mpu_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0202

por_mpu_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

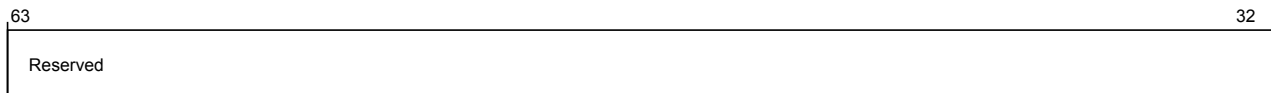


Figure 4-1464 por_mpu_por_mpu_child_info (high)

The following table shows the por_mpu_child_info higher register bit assignments.

Table 4-1481 por_mpu_por_mpu_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

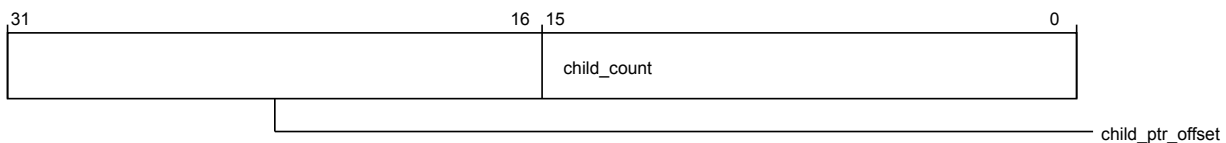


Figure 4-1465 por_mpu_por_mpu_child_info (low)

The following table shows the por_mpu_child_info lower register bit assignments.

Table 4-1482 por_mpu_por_mpu_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_mpu_unit_info

Provides component identification information for MPU.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h900
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

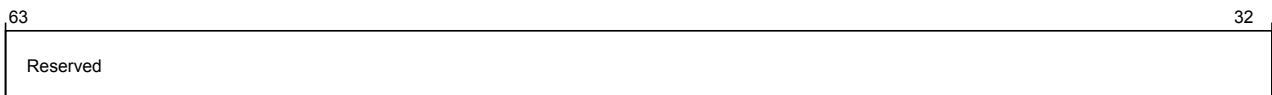


Figure 4-1466 por_mpu_por_mpu_unit_info (high)

The following table shows the por_mpu_unit_info higher register bit assignments.

Table 4-1483 por_mpu_por_mpu_unit_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

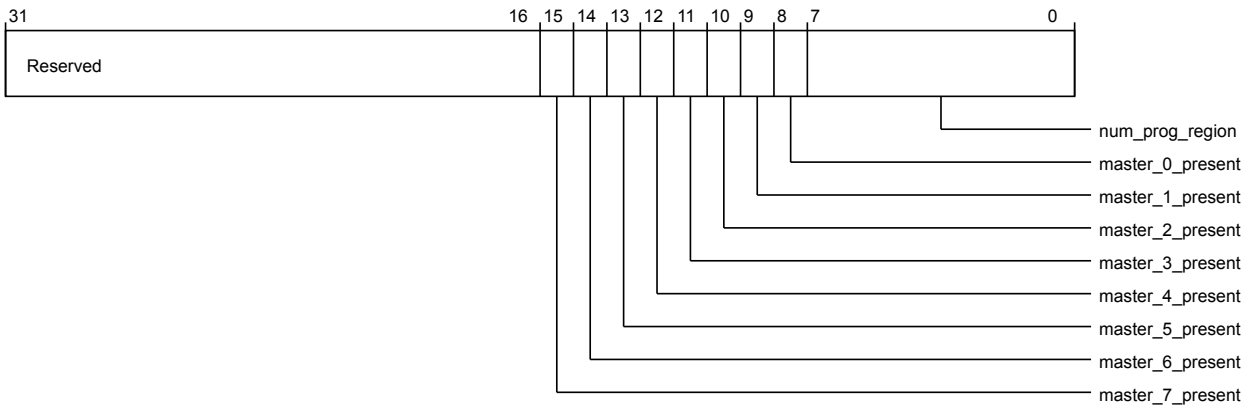


Figure 4-1467 por_mpu_por_mpu_unit_info (low)

The following table shows the por_mpu_unit_info lower register bit assignments.

Table 4-1484 por_mpu_por_mpu_unit_info (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15	master_7_present	Indicates whether the master 7 is present - 1'b0: not present 1'b1: present	RO	Configuration dependent
14	master_6_present	Indicates whether the master 6 is present - 1'b0: not present 1'b1: present	RO	Configuration dependent
13	master_5_present	Indicates whether the master 5 is present - 1'b0: not present 1'b1: present	RO	Configuration dependent
12	master_4_present	Indicates whether the master 4 is present - 1'b0: not present 1'b1: present	RO	Configuration dependent
11	master_3_present	Indicates whether the master 3 is present - 1'b0: not present 1'b1: present	RO	Configuration dependent
10	master_2_present	Indicates whether the master 2 is present - 1'b0: not present 1'b1: present	RO	Configuration dependent
9	master_1_present	Indicates whether the master 1 is present - 1'b0: not present 1'b1: present	RO	Configuration dependent
8	master_0_present	Indicates whether the master 0 is present - 1'b0: not present 1'b1: present	RO	Configuration dependent
7:0	num_prog_region	Indicates total of MPU programmable regions. The following are supported - 8'd0: 0 programmable regions (No MPU present) 8'd8: 8 programmable regions 8'd16: 16 programmable regions 8'd24: 24 programmable regions 8'd32: 32 programmable regions	RO	Configuration dependent

por_mpu_m0_ctl

Functions as the MPU Master 0 control register.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1000
Register reset	64'b010
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.



Figure 4-1468 por_mpu_por_mpu_m0_ctl (high)

The following table shows the por_mpu_m0_ctl higher register bit assignments.

Table 4-1485 por_mpu_por_mpu_m0_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

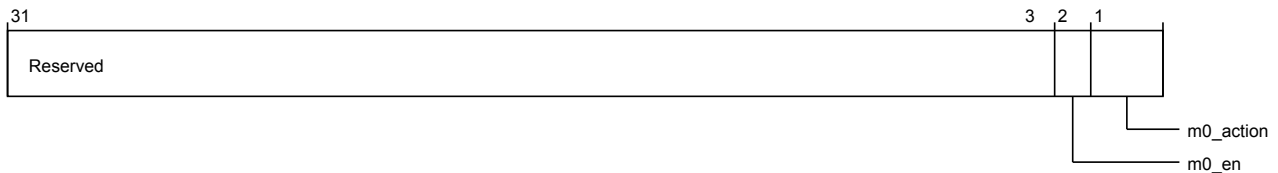


Figure 4-1469 por_mpu_por_mpu_m0_ctl (low)

The following table shows the por_mpu_m0_ctl lower register bit assignments.

Table 4-1486 por_mpu_por_mpu_m0_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	m0_en	MPU master 0 enable.	RW	1'b0
1:0	m0_action	Indicates action HN* should take if no access permission is granted 2'b00: FUSA interrupt 2'b01: Bus error to the originating bus master 2'b10: Both FUSA interrupt and bus error.	RW	2'b10

por_mpu_m0_prbar0

MPU master 0 programmable base address register 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1010

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

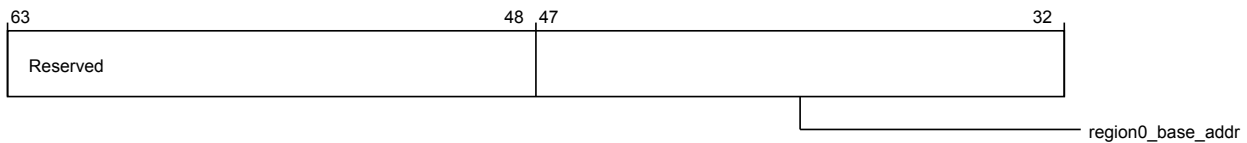


Figure 4-1470 por_mpu_por_mpu_m0_prbar0 (high)

The following table shows the `por_mpu_m0_prbar0` higher register bit assignments.

Table 4-1487 por_mpu_por_mpu_m0_prbar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

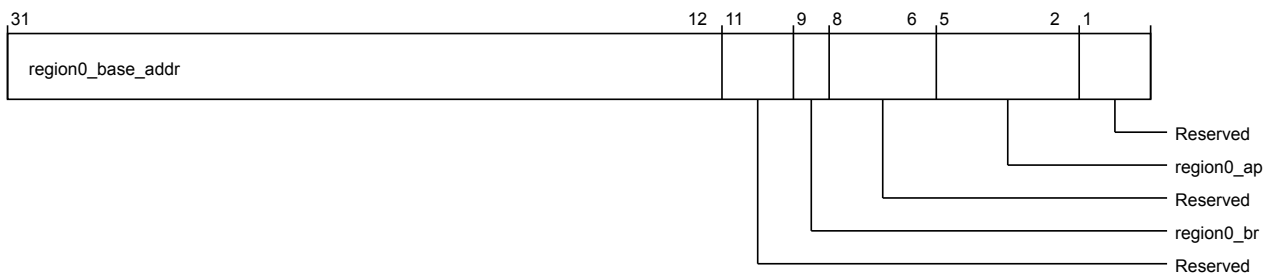


Figure 4-1471 por_mpu_por_mpu_m0_prbar0 (low)

The following table shows the `por_mpu_m0_prbar0` lower register bit assignments.

Table 4-1488 por_mpu_por_mpu_m0_prbar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1488 por_mpu_por_mpu_m0_prbar0 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region0_br	Region 0 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region0_ap	Region 0 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar0

MPU master 0 programmable limit address register 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1018

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

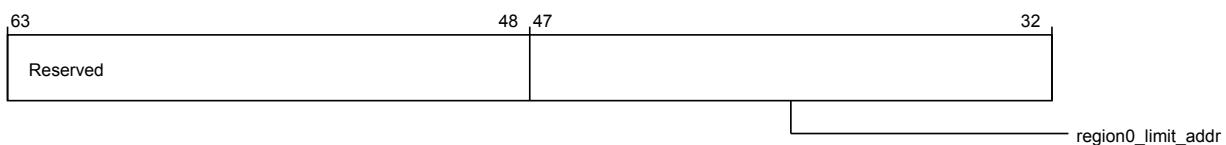


Figure 4-1472 por_mpu_por_mpu_m0_prlar0 (high)

The following table shows the por_mpu_m0_prlar0 higher register bit assignments.

Table 4-1489 por_mpu_por_mpu_m0_prlar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

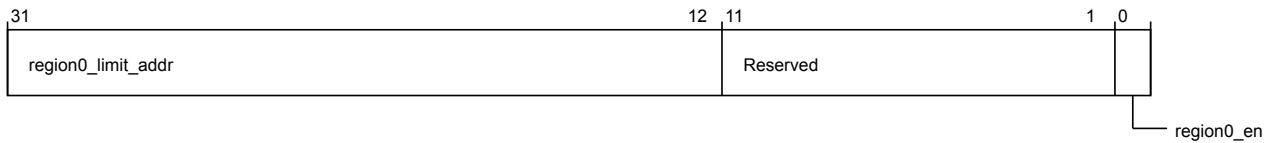


Figure 4-1473 `por_mpu_por_mpu_m0_prlar0` (low)

The following table shows the `por_mpu_m0_prlar0` lower register bit assignments.

Table 4-1490 `por_mpu_por_mpu_m0_prlar0` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region0_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region0_en</code>	Region 0 enable.	RW	1'b0

`por_mpu_m0_prbar1`

MPU master 0 programmable base address register 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1020

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

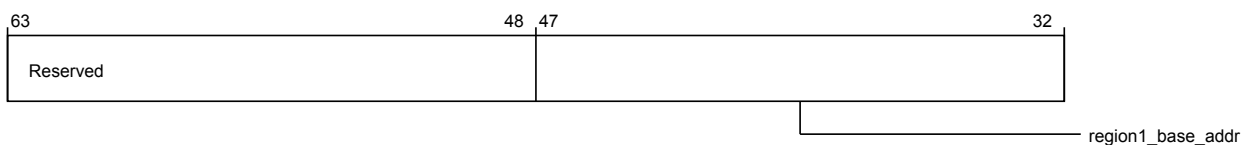


Figure 4-1474 `por_mpu_por_mpu_m0_prbar1` (high)

The following table shows the `por_mpu_m0_prbar1` higher register bit assignments.

Table 4-1491 `por_mpu_por_mpu_m0_prbar1` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region1_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

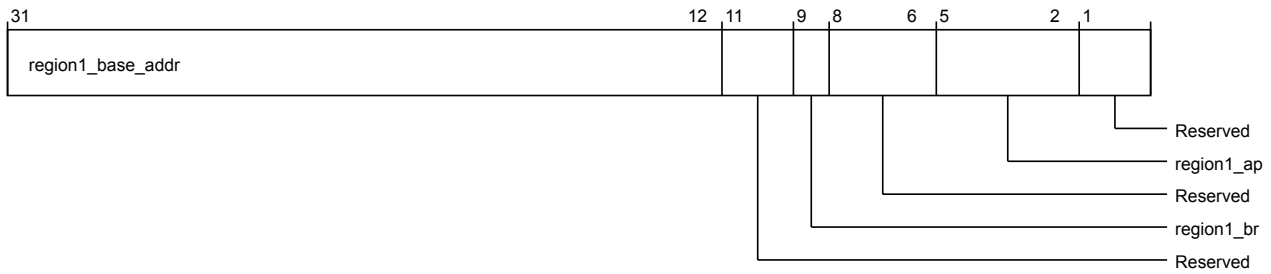


Figure 4-1475 por_mpu_por_mpu_m0_prbar1 (low)

The following table shows the por_mpu_m0_prbar1 lower register bit assignments.

Table 4-1492 por_mpu_por_mpu_m0_prbar1 (low)

Bits	Field name	Description	Type	Reset
31:12	region1_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region1_br	Region 1 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region1_ap	Region 1 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar1

MPU master 0 programmable limit address register 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1028

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

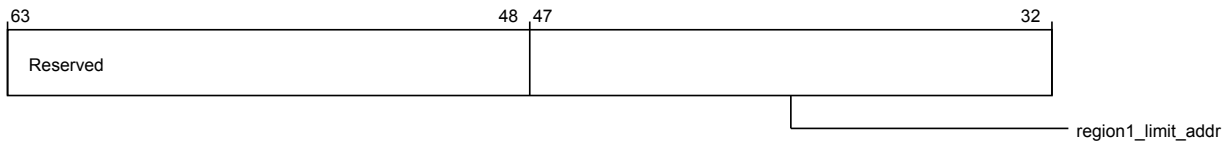


Figure 4-1476 `por_mpu_m0_prlar1` (high)

The following table shows the `por_mpu_m0_prlar1` higher register bit assignments.

Table 4-1493 `por_mpu_m0_prlar1` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region1_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

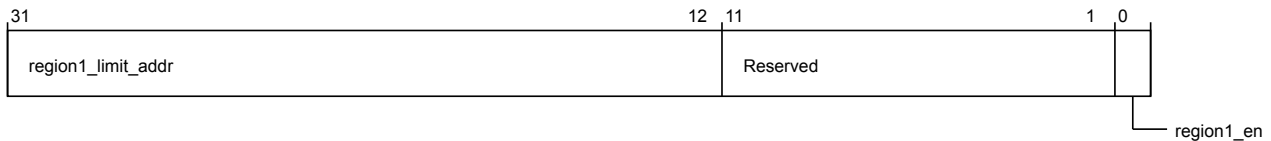


Figure 4-1477 `por_mpu_m0_prlar1` (low)

The following table shows the `por_mpu_m0_prlar1` lower register bit assignments.

Table 4-1494 `por_mpu_m0_prlar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region1_en</code>	Region 1 enable.	RW	1'b0

`por_mpu_m0_prbar2`

MPU master 0 programmable base address register 2.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1030
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

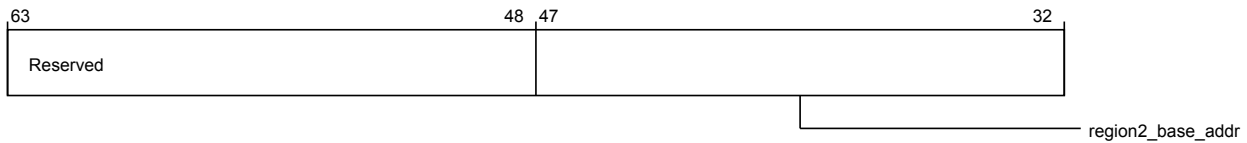


Figure 4-1478 por_mpu_por_mpu_m0_prbar2 (high)

The following table shows the por_mpu_m0_prbar2 higher register bit assignments.

Table 4-1495 por_mpu_por_mpu_m0_prbar2 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region2_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

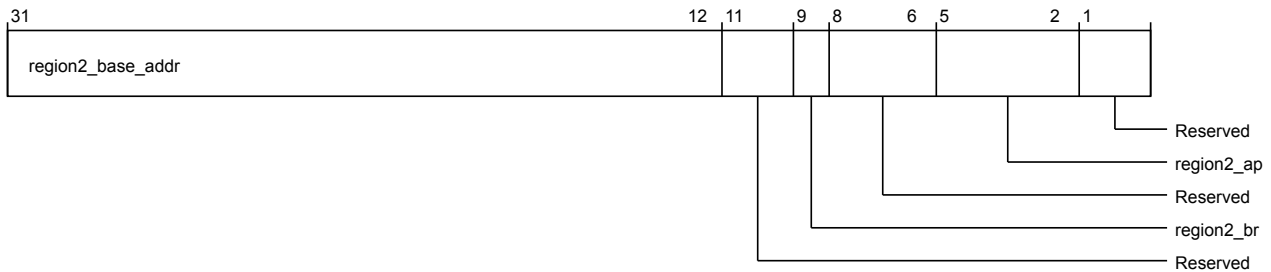


Figure 4-1479 por_mpu_por_mpu_m0_prbar2 (low)

The following table shows the por_mpu_m0_prbar2 lower register bit assignments.

Table 4-1496 por_mpu_por_mpu_m0_prbar2 (low)

Bits	Field name	Description	Type	Reset
31:12	region2_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region2_br	Region 2 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region2_ap	Region 2 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar2

MPU master 0 programmable limit address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1038

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

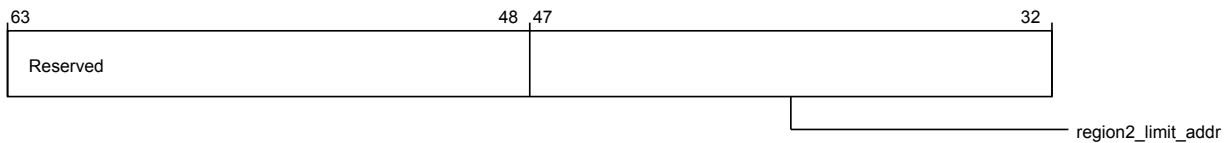


Figure 4-1480 por_mpu_por_mpu_m0_prlar2 (high)

The following table shows the por_mpu_m0_prlar2 higher register bit assignments.

Table 4-1497 por_mpu_por_mpu_m0_prlar2 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region2_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

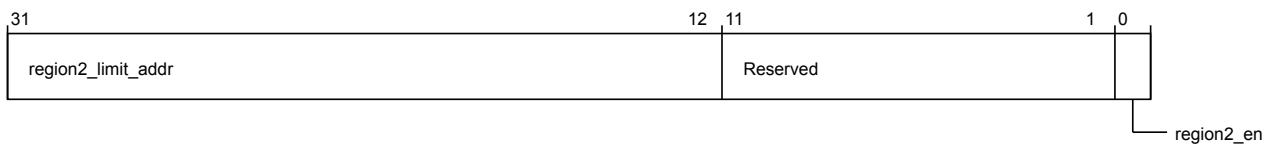


Figure 4-1481 por_mpu_por_mpu_m0_prlar2 (low)

The following table shows the por_mpu_m0_prlar2 lower register bit assignments.

Table 4-1498 por_mpu_por_mpu_m0_prlar2 (low)

Bits	Field name	Description	Type	Reset
31:12	region2_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region2_en	Region 2 enable.	RW	1'b0

por_mpu_m0_prbar3

MPU master 0 programmable base address register 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1040

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

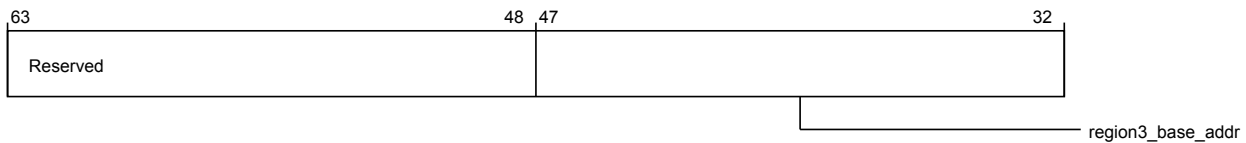


Figure 4-1482 por_mpu_por_mpu_m0_prbar3 (high)

The following table shows the por_mpu_m0_prbar3 higher register bit assignments.

Table 4-1499 por_mpu_por_mpu_m0_prbar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

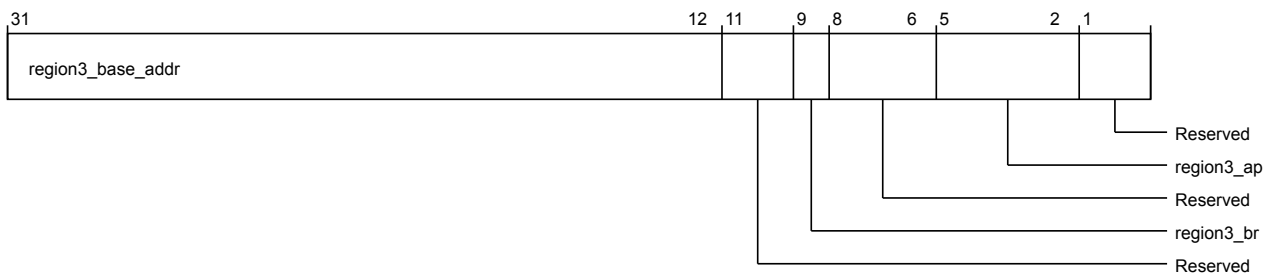


Figure 4-1483 por_mpu_por_mpu_m0_prbar3 (low)

The following table shows the por_mpu_m0_prbar3 lower register bit assignments.

Table 4-1500 por_mpu_por_mpu_m0_prbar3 (low)

Bits	Field name	Description	Type	Reset
31:12	region3_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1500 por_mpu_por_mpu_m0_prbar3 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region3_br	Region 3 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region3_ap	Region 3 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar3

MPU master 0 programmable limit address register 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1048

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

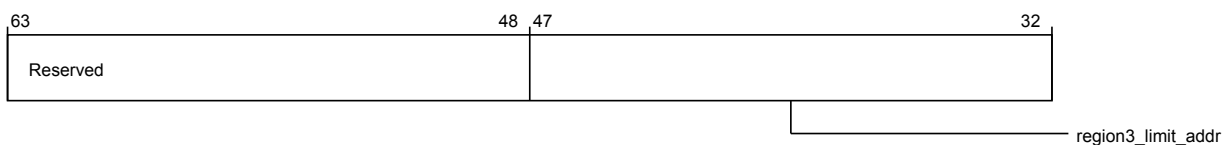


Figure 4-1484 por_mpu_por_mpu_m0_prlar3 (high)

The following table shows the por_mpu_m0_prlar3 higher register bit assignments.

Table 4-1501 por_mpu_por_mpu_m0_prlar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

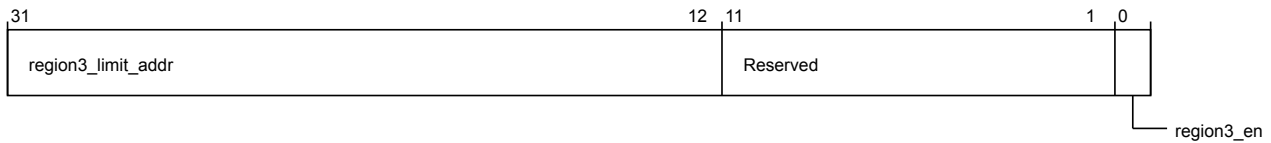


Figure 4-1485 `por_mpu_por_mpu_m0_prlar3` (low)

The following table shows the `por_mpu_m0_prlar3` lower register bit assignments.

Table 4-1502 `por_mpu_por_mpu_m0_prlar3` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region3_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region3_en</code>	Region 3 enable.	RW	1'b0

`por_mpu_m0_prbar4`

MPU master 0 programmable base address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1050

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

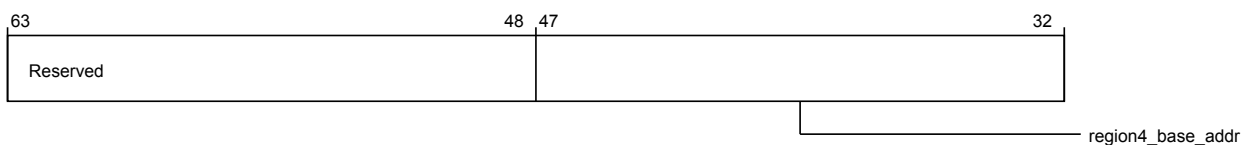


Figure 4-1486 `por_mpu_por_mpu_m0_prbar4` (high)

The following table shows the `por_mpu_m0_prbar4` higher register bit assignments.

Table 4-1503 `por_mpu_por_mpu_m0_prbar4` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region4_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

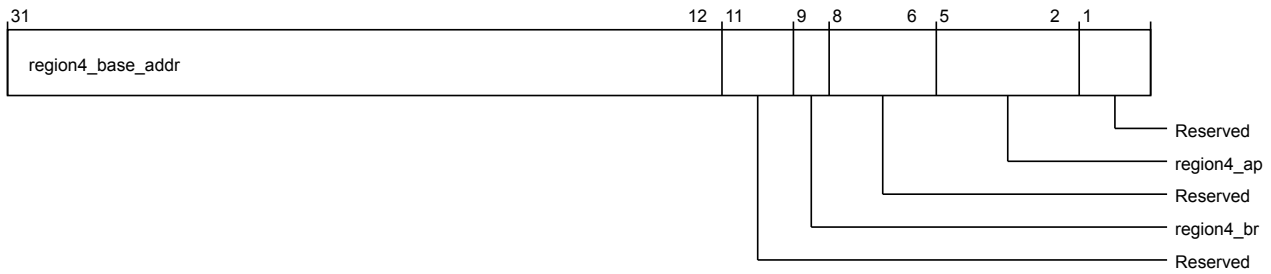


Figure 4-1487 por_mpu_por_mpu_m0_prbar4 (low)

The following table shows the por_mpu_m0_prbar4 lower register bit assignments.

Table 4-1504 por_mpu_por_mpu_m0_prbar4 (low)

Bits	Field name	Description	Type	Reset
31:12	region4_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region4_br	Region 4 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region4_ap	Region 4 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar4

MPU master 0 programmable limit address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1058

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

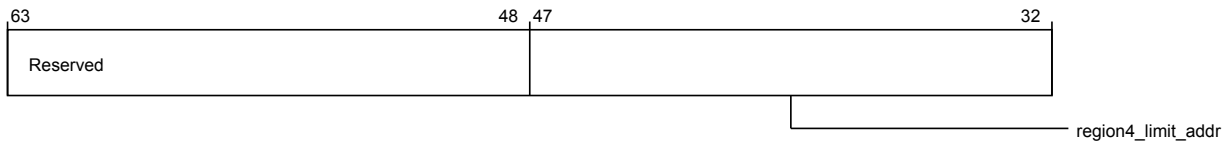


Figure 4-1488 `por_mpu_m0_prlar4` (high)

The following table shows the `por_mpu_m0_prlar4` higher register bit assignments.

Table 4-1505 `por_mpu_m0_prlar4` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region4_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

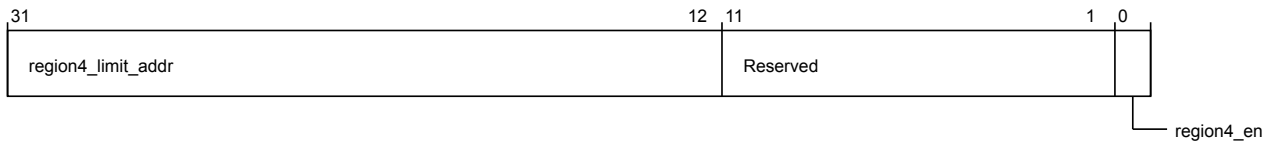


Figure 4-1489 `por_mpu_m0_prlar4` (low)

The following table shows the `por_mpu_m0_prlar4` lower register bit assignments.

Table 4-1506 `por_mpu_m0_prlar4` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region4_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region4_en</code>	Region 4 enable.	RW	1'b0

`por_mpu_m0_prbar5`

MPU master 0 programmable base address register 5.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1060
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

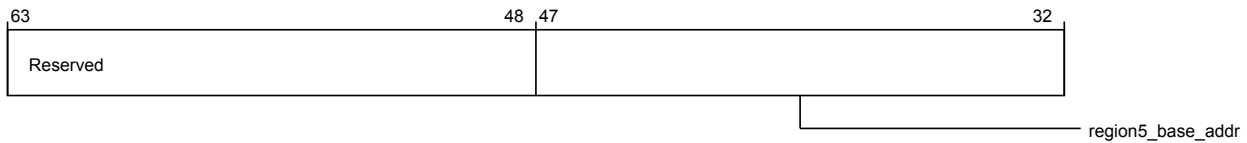


Figure 4-1490 `por_mpu_m0_prbar5` (high)

The following table shows the `por_mpu_m0_prbar5` higher register bit assignments.

Table 4-1507 `por_mpu_m0_prbar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region5_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

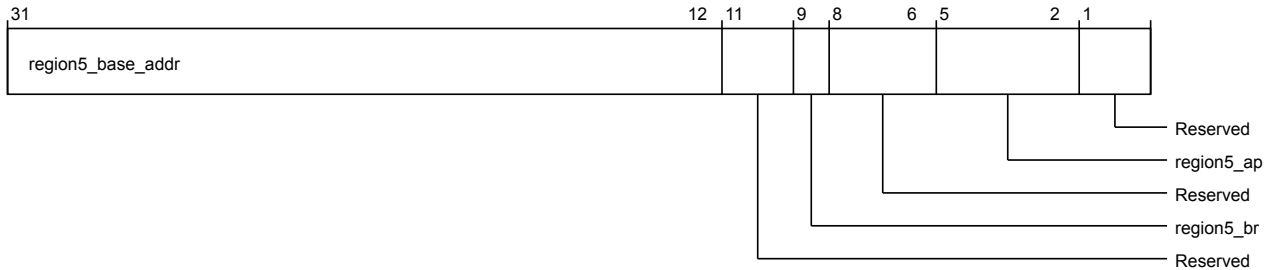


Figure 4-1491 `por_mpu_m0_prbar5` (low)

The following table shows the `por_mpu_m0_prbar5` lower register bit assignments.

Table 4-1508 `por_mpu_m0_prbar5` (low)

Bits	Field name	Description	Type	Reset
31:12	region5_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region5_br	Region 5 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region5_ap	Region 5 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar5

MPU master 0 programmable limit address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1068

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

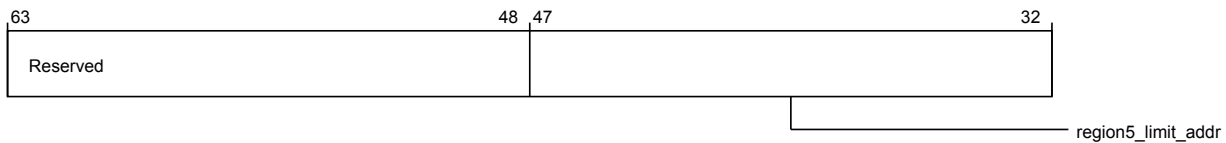


Figure 4-1492 por_mpu_por_mpu_m0_prlar5 (high)

The following table shows the por_mpu_m0_prlar5 higher register bit assignments.

Table 4-1509 por_mpu_por_mpu_m0_prlar5 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region5_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

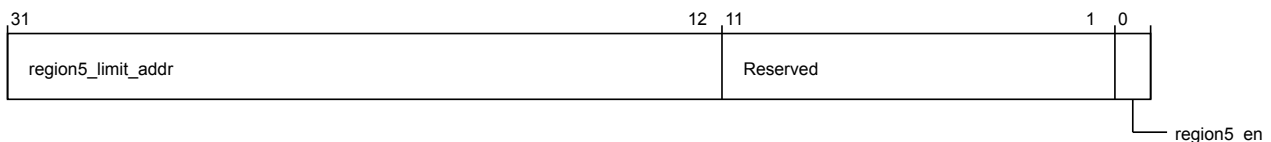


Figure 4-1493 por_mpu_por_mpu_m0_prlar5 (low)

The following table shows the por_mpu_m0_prlar5 lower register bit assignments.

Table 4-1510 por_mpu_por_mpu_m0_prlar5 (low)

Bits	Field name	Description	Type	Reset
31:12	region5_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region5_en	Region 5 enable.	RW	1'b0

por_mpu_m0_prbar6

MPU master 0 programmable base address register 6.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1070

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

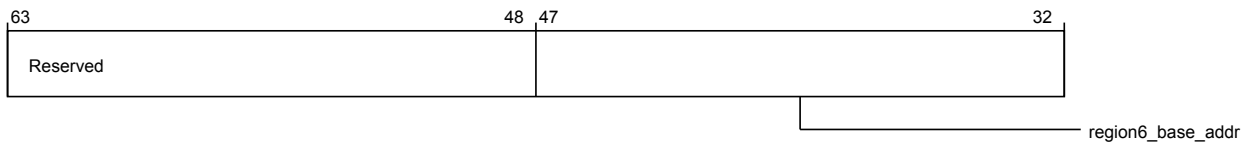


Figure 4-1494 por_mpu_por_mpu_m0_prbar6 (high)

The following table shows the por_mpu_m0_prbar6 higher register bit assignments.

Table 4-1511 por_mpu_por_mpu_m0_prbar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

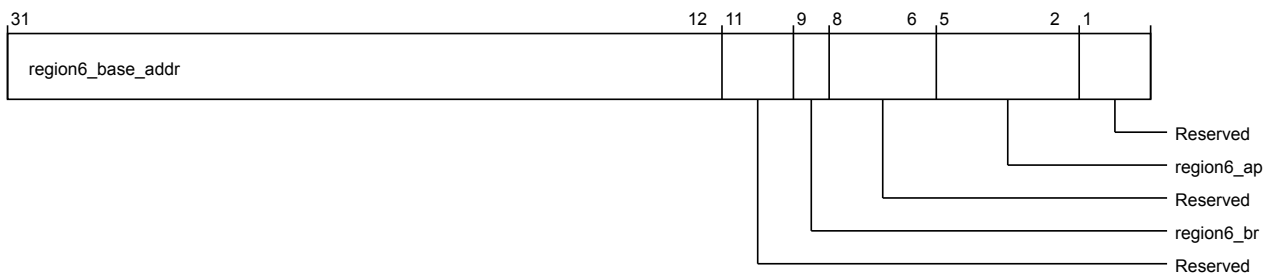


Figure 4-1495 por_mpu_por_mpu_m0_prbar6 (low)

The following table shows the por_mpu_m0_prbar6 lower register bit assignments.

Table 4-1512 por_mpu_por_mpu_m0_prbar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1512 por_mpu_por_mpu_m0_prbar6 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region6_br	Region 6 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region6_ap	Region 6 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar6

MPU master 0 programmable limit address register 6.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1078

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

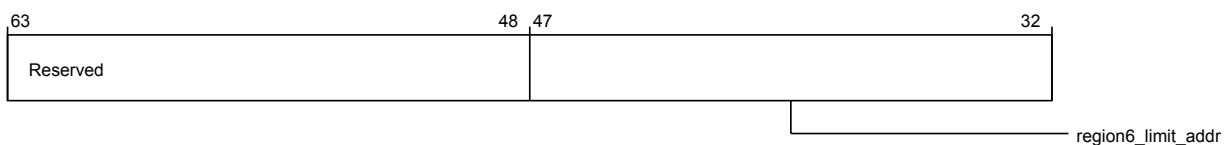


Figure 4-1496 por_mpu_por_mpu_m0_prlar6 (high)

The following table shows the por_mpu_m0_prlar6 higher register bit assignments.

Table 4-1513 por_mpu_por_mpu_m0_prlar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_limit_addr	Bits [47:32] of limit address of the range.	RW	20'b0

The following image shows the lower register bit assignments.

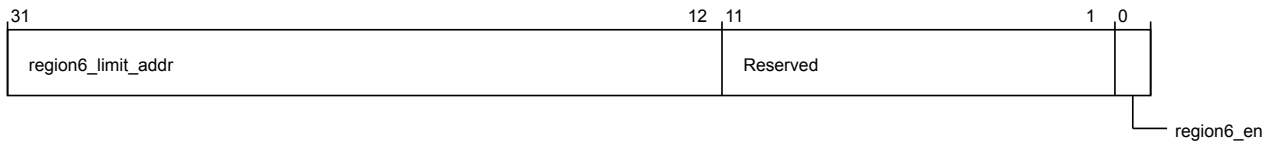


Figure 4-1497 `por_mpu_por_mpu_m0_prlar6` (low)

The following table shows the `por_mpu_m0_prlar6` lower register bit assignments.

Table 4-1514 `por_mpu_por_mpu_m0_prlar6` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region6_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region6_en</code>	Region 6 enable.	RW	1'b0

`por_mpu_m0_prbar7`

MPU master 0 programmable base address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1080

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

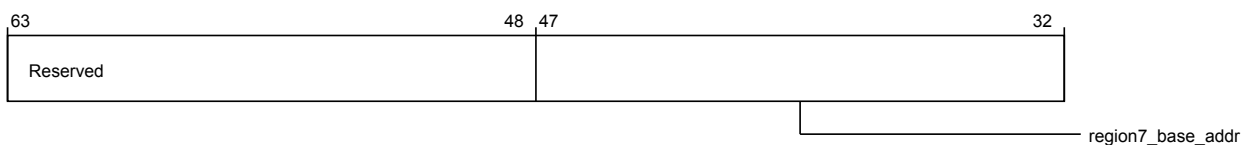


Figure 4-1498 `por_mpu_por_mpu_m0_prbar7` (high)

The following table shows the `por_mpu_m0_prbar7` higher register bit assignments.

Table 4-1515 `por_mpu_por_mpu_m0_prbar7` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region7_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

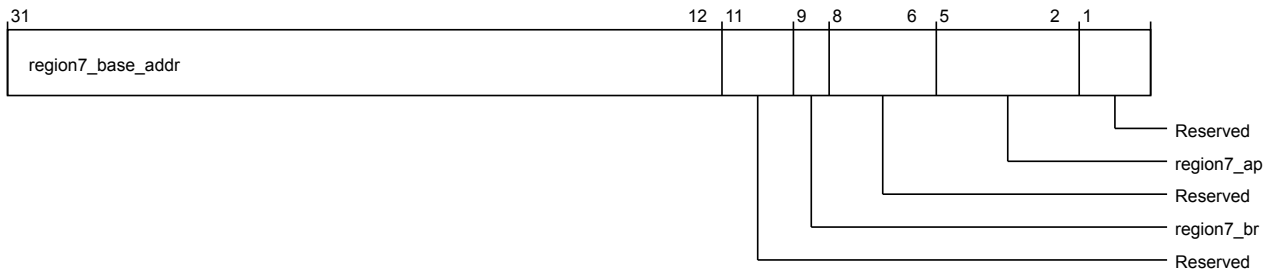


Figure 4-1499 por_mpu_por_mpu_m0_prbar7 (low)

The following table shows the por_mpu_m0_prbar7 lower register bit assignments.

Table 4-1516 por_mpu_por_mpu_m0_prbar7 (low)

Bits	Field name	Description	Type	Reset
31:12	region7_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region7_br	Region 7 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region7_ap	Region 7 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar7

MPU master 0 programmable limit address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1088

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

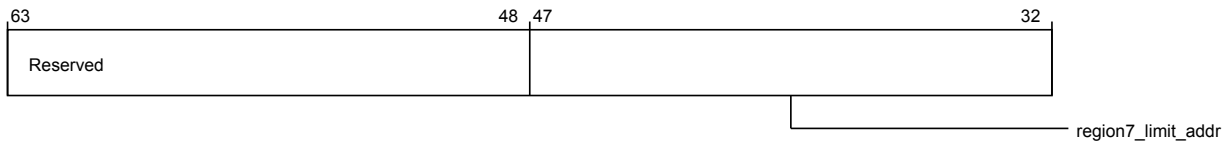


Figure 4-1500 `por_mpu_m0_prlar7` (high)

The following table shows the `por_mpu_m0_prlar7` higher register bit assignments.

Table 4-1517 `por_mpu_m0_prlar7` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region7_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

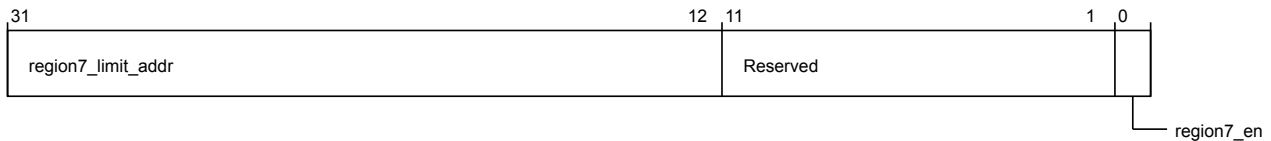


Figure 4-1501 `por_mpu_m0_prlar7` (low)

The following table shows the `por_mpu_m0_prlar7` lower register bit assignments.

Table 4-1518 `por_mpu_m0_prlar7` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region7_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region7_en</code>	Region 7 enable.	RW	1'b0

`por_mpu_m0_prbar8`

MPU master 0 programmable base address register 8.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1090
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

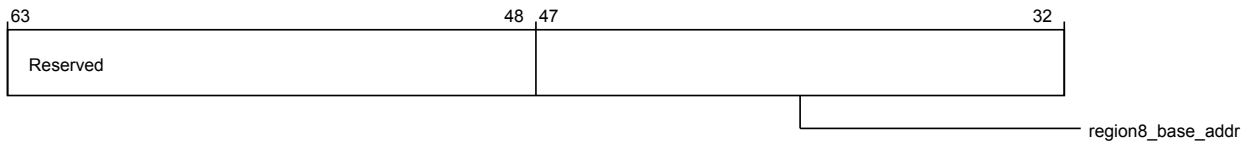


Figure 4-1502 `por_mpu_m0_prbar8` (high)

The following table shows the `por_mpu_m0_prbar8` higher register bit assignments.

Table 4-1519 `por_mpu_m0_prbar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region8_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

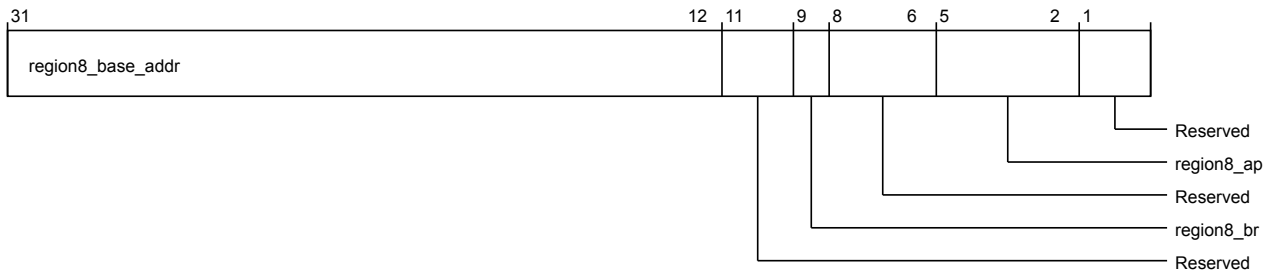


Figure 4-1503 `por_mpu_m0_prbar8` (low)

The following table shows the `por_mpu_m0_prbar8` lower register bit assignments.

Table 4-1520 `por_mpu_m0_prbar8` (low)

Bits	Field name	Description	Type	Reset
31:12	region8_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region8_br	Region 8 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region8_ap	Region 8 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar8

MPU master 0 programmable limit address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1098

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

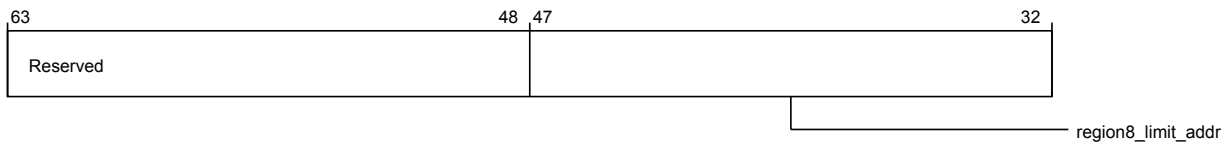


Figure 4-1504 por_mpu_por_mpu_m0_prlar8 (high)

The following table shows the por_mpu_m0_prlar8 higher register bit assignments.

Table 4-1521 por_mpu_por_mpu_m0_prlar8 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region8_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

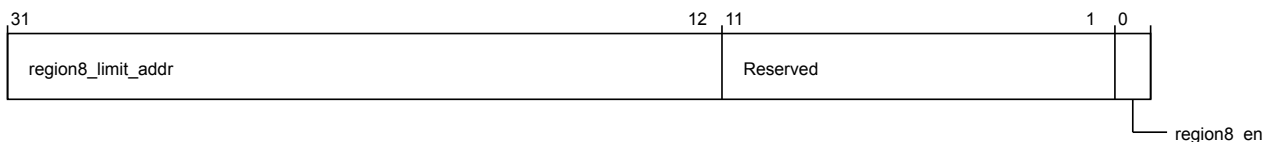


Figure 4-1505 por_mpu_por_mpu_m0_prlar8 (low)

The following table shows the por_mpu_m0_prlar8 lower register bit assignments.

Table 4-1522 por_mpu_por_mpu_m0_prlar8 (low)

Bits	Field name	Description	Type	Reset
31:12	region8_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region8_en	Region 8 enable.	RW	1'b0

por_mpu_m0_prbar9

MPU master 0 programmable base address register 9.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h10A0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

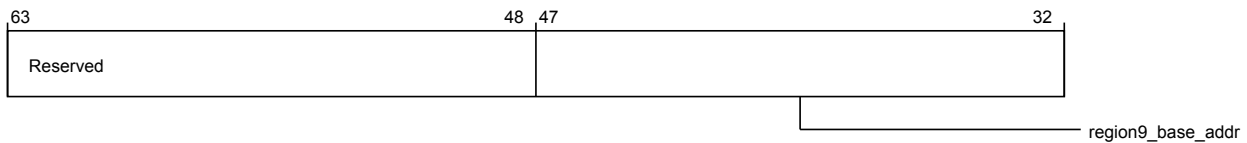


Figure 4-1506 por_mpu_por_mpu_m0_prbar9 (high)

The following table shows the `por_mpu_m0_prbar9` higher register bit assignments.

Table 4-1523 por_mpu_por_mpu_m0_prbar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

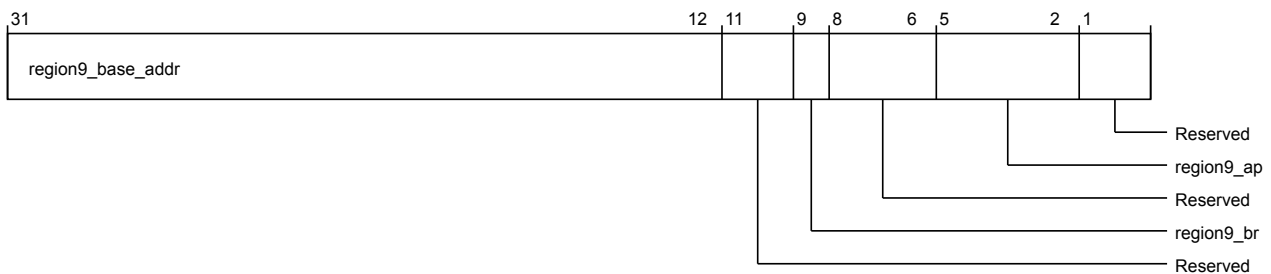


Figure 4-1507 por_mpu_por_mpu_m0_prbar9 (low)

The following table shows the `por_mpu_m0_prbar9` lower register bit assignments.

Table 4-1524 por_mpu_por_mpu_m0_prbar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1524 por_mpu_por_mpu_m0_prbar9 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region9_br	Region 9 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region9_ap	Region 9 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar9

MPU master 0 programmable limit address register 9.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h10A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

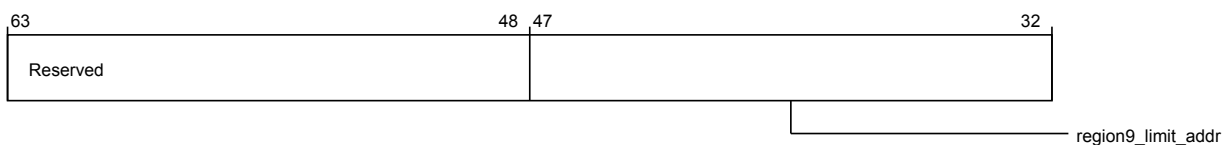


Figure 4-1508 por_mpu_por_mpu_m0_prlar9 (high)

The following table shows the por_mpu_m0_prlar9 higher register bit assignments.

Table 4-1525 por_mpu_por_mpu_m0_prlar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

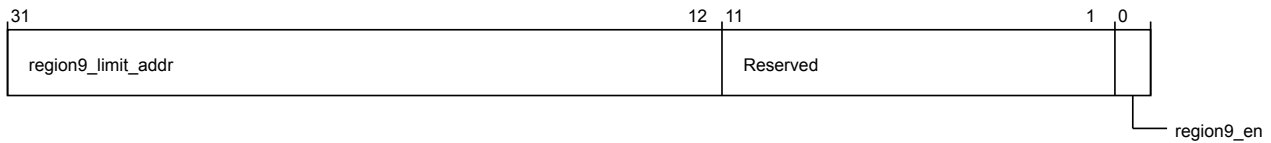


Figure 4-1509 `por_mpu_por_mpu_m0_prlar9` (low)

The following table shows the `por_mpu_m0_prlar9` lower register bit assignments.

Table 4-1526 `por_mpu_por_mpu_m0_prlar9` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region9_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region9_en</code>	Region 9 enable.	RW	1'b0

`por_mpu_m0_prbar10`

MPU master 0 programmable base address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h10B0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

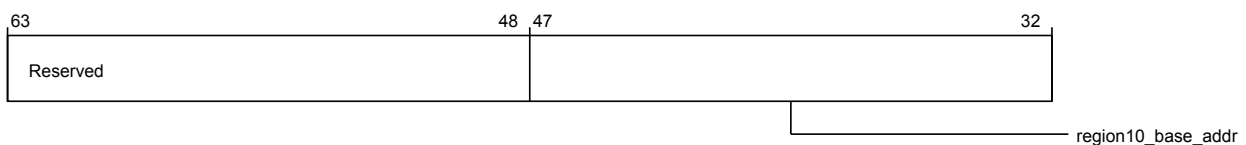


Figure 4-1510 `por_mpu_por_mpu_m0_prbar10` (high)

The following table shows the `por_mpu_m0_prbar10` higher register bit assignments.

Table 4-1527 `por_mpu_por_mpu_m0_prbar10` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region10_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

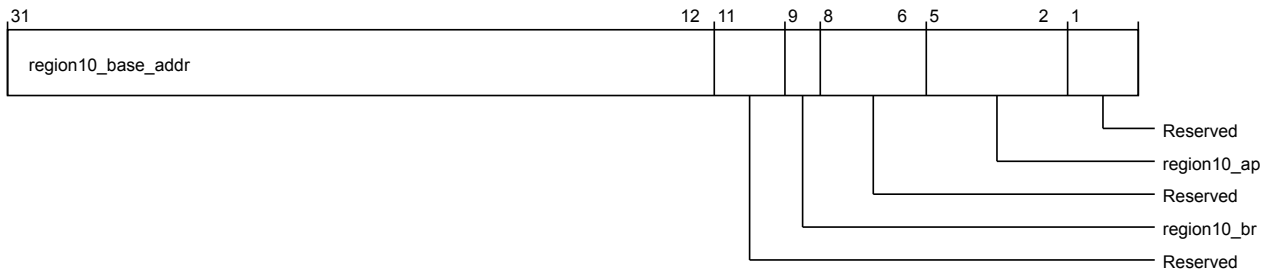


Figure 4-1511 por_mpu_por_mpu_m0_prbar10 (low)

The following table shows the por_mpu_m0_prbar10 lower register bit assignments.

Table 4-1528 por_mpu_por_mpu_m0_prbar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region10_br	Region 10 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region10_ap	Region 10 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar10

MPU master 0 programmable limit address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h10B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

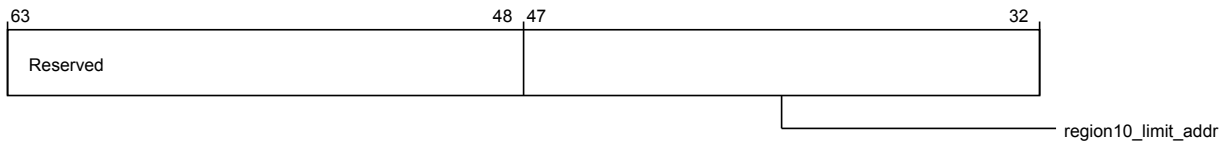


Figure 4-1512 por_mpu_m0_prlar10 (high)

The following table shows the por_mpu_m0_prlar10 higher register bit assignments.

Table 4-1529 por_mpu_m0_prlar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

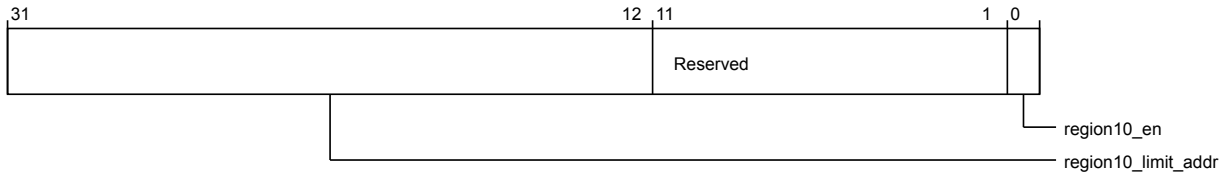


Figure 4-1513 por_mpu_m0_prlar10 (low)

The following table shows the por_mpu_m0_prlar10 lower register bit assignments.

Table 4-1530 por_mpu_m0_prlar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region10_en	Region 10 enable.	RW	1'b0

por_mpu_m0_prbar11

MPU master 0 programmable base address register 11.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h10C0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

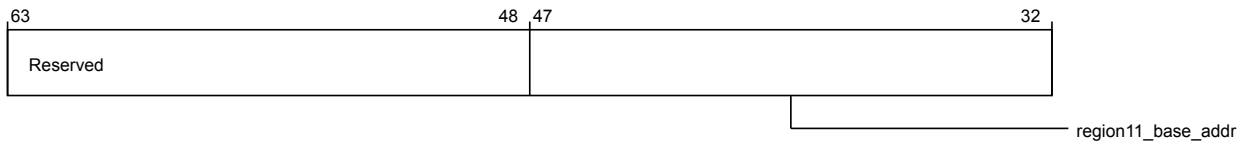


Figure 4-1514 por_mpu_por_mpu_m0_prbar11 (high)

The following table shows the por_mpu_m0_prbar11 higher register bit assignments.

Table 4-1531 por_mpu_por_mpu_m0_prbar11 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

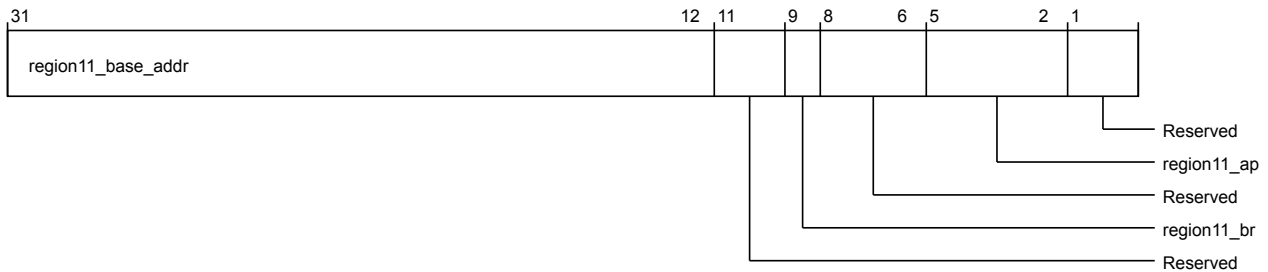


Figure 4-1515 por_mpu_por_mpu_m0_prbar11 (low)

The following table shows the por_mpu_m0_prbar11 lower register bit assignments.

Table 4-1532 por_mpu_por_mpu_m0_prbar11 (low)

Bits	Field name	Description	Type	Reset
31:12	region11_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region11_br	Region 11 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region11_ap	Region 11 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar11

MPU master 0 programmable limit address register 11.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h10C8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

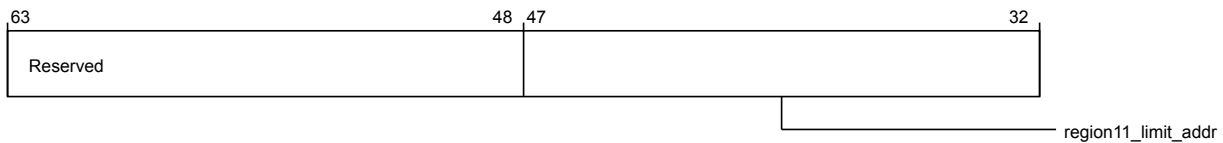


Figure 4-1516 por_mpu_por_mpu_m0_prlar11 (high)

The following table shows the por_mpu_m0_prlar11 higher register bit assignments.

Table 4-1533 por_mpu_por_mpu_m0_prlar11 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

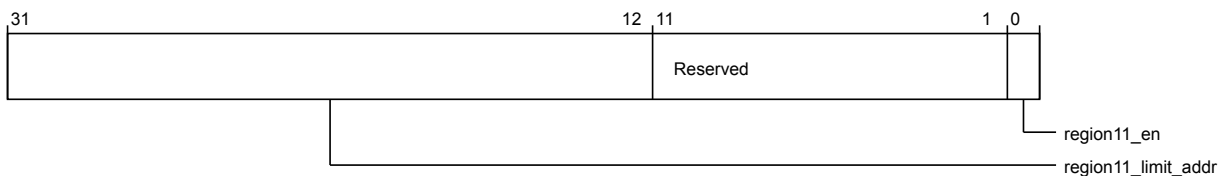


Figure 4-1517 por_mpu_por_mpu_m0_prlar11 (low)

The following table shows the por_mpu_m0_prlar11 lower register bit assignments.

Table 4-1534 por_mpu_por_mpu_m0_prlar11 (low)

Bits	Field name	Description	Type	Reset
31:12	region11_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region11_en	Region 11 enable.	RW	1'b0

por_mpu_m0_prbar12

MPU master 0 programmable base address register 12.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h10D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

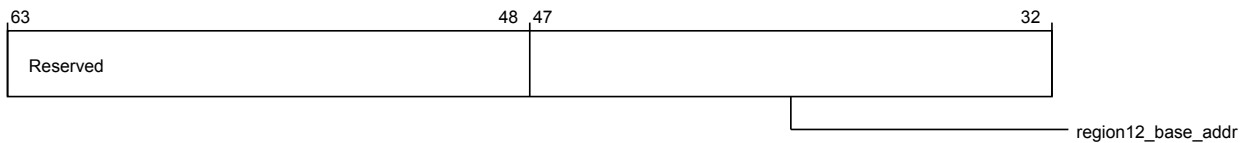


Figure 4-1518 por_mpu_por_mpu_m0_prbar12 (high)

The following table shows the por_mpu_m0_prbar12 higher register bit assignments.

Table 4-1535 por_mpu_por_mpu_m0_prbar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

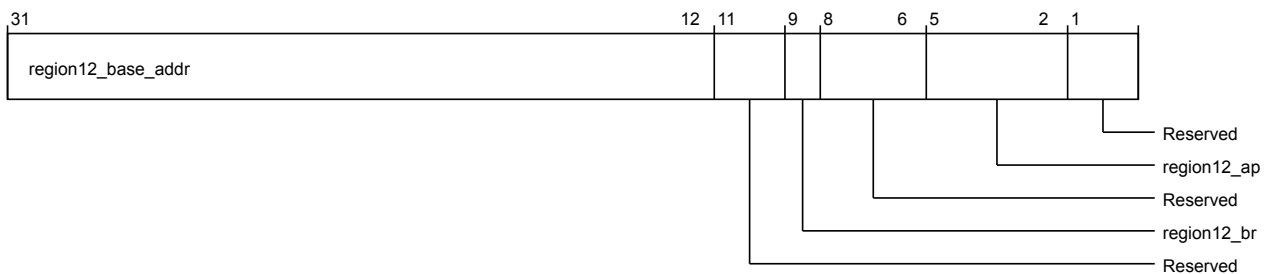


Figure 4-1519 por_mpu_por_mpu_m0_prbar12 (low)

The following table shows the por_mpu_m0_prbar12 lower register bit assignments.

Table 4-1536 por_mpu_por_mpu_m0_prbar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1536 por_mpu_por_mpu_m0_prbar12 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region12_br	Region 12 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region12_ap	Region 12 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar12

MPU master 0 programmable limit address register 12.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h10D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

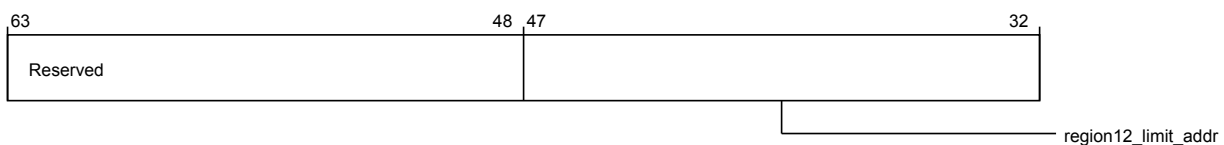


Figure 4-1520 por_mpu_por_mpu_m0_prlar12 (high)

The following table shows the por_mpu_m0_prlar12 higher register bit assignments.

Table 4-1537 por_mpu_por_mpu_m0_prlar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

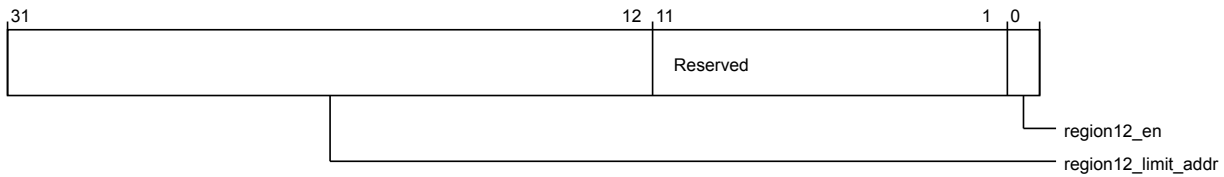


Figure 4-1521 por_mpu_por_mpu_m0_prlar12 (low)

The following table shows the por_mpu_m0_prlar12 lower register bit assignments.

Table 4-1538 por_mpu_por_mpu_m0_prlar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region12_en	Region 12 enable.	RW	1'b0

por_mpu_m0_prbar13

MPU master 0 programmable base address register 13.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h10E0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

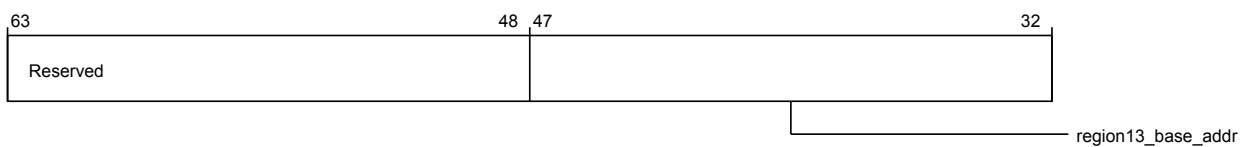


Figure 4-1522 por_mpu_por_mpu_m0_prbar13 (high)

The following table shows the por_mpu_m0_prbar13 higher register bit assignments.

Table 4-1539 por_mpu_por_mpu_m0_prbar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

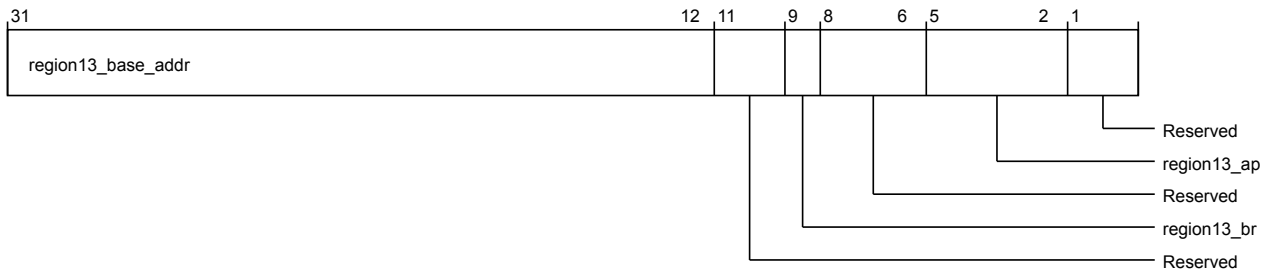


Figure 4-1523 `por_mpu_m0_prbar13` (low)

The following table shows the `por_mpu_m0_prbar13` lower register bit assignments.

Table 4-1540 `por_mpu_m0_prbar13` (low)

Bits	Field name	Description	Type	Reset
31:12	region13_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region13_br	Region 13 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region13_ap	Region 13 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m0_prlar13`

MPU master 0 programmable limit address register 13.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h10E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

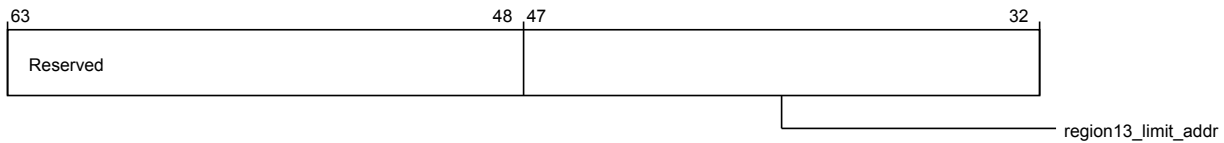


Figure 4-1524 por_mpu_m0_prlar13 (high)

The following table shows the por_mpu_m0_prlar13 higher register bit assignments.

Table 4-1541 por_mpu_m0_prlar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

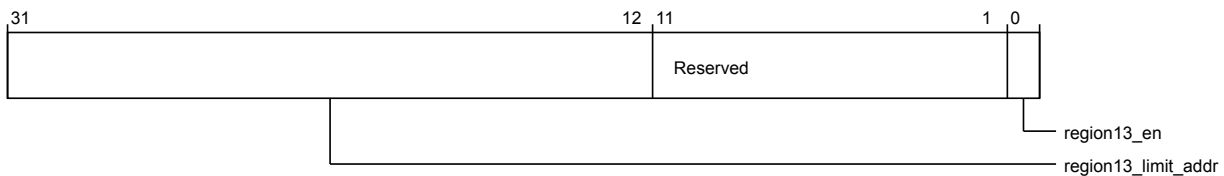


Figure 4-1525 por_mpu_m0_prlar13 (low)

The following table shows the por_mpu_m0_prlar13 lower register bit assignments.

Table 4-1542 por_mpu_m0_prlar13 (low)

Bits	Field name	Description	Type	Reset
31:12	region13_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region13_en	Region 13 enable.	RW	1'b0

por_mpu_m0_prbar14

MPU master 0 programmable base address register 14.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h10F0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

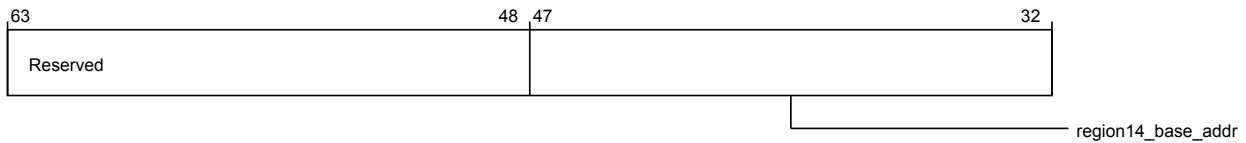


Figure 4-1526 `por_mpu_por_mpu_m0_prbar14` (high)

The following table shows the `por_mpu_m0_prbar14` higher register bit assignments.

Table 4-1543 `por_mpu_por_mpu_m0_prbar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region14_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

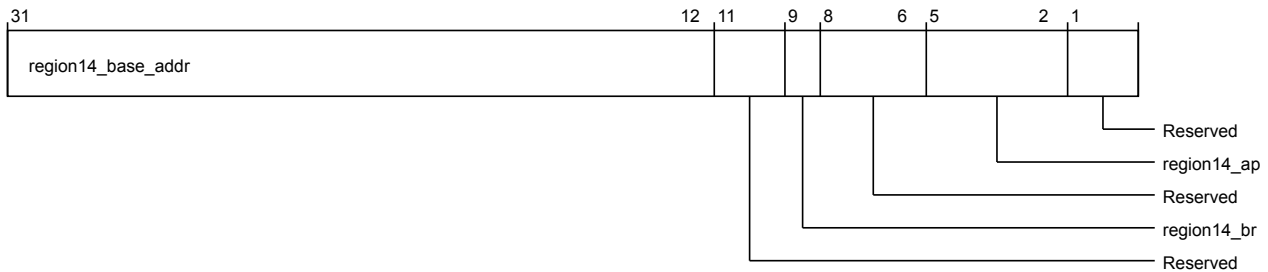


Figure 4-1527 `por_mpu_por_mpu_m0_prbar14` (low)

The following table shows the `por_mpu_m0_prbar14` lower register bit assignments.

Table 4-1544 `por_mpu_por_mpu_m0_prbar14` (low)

Bits	Field name	Description	Type	Reset
31:12	region14_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region14_br	Region 14 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region14_ap	Region 14 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar14

MPU master 0 programmable limit address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h10F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

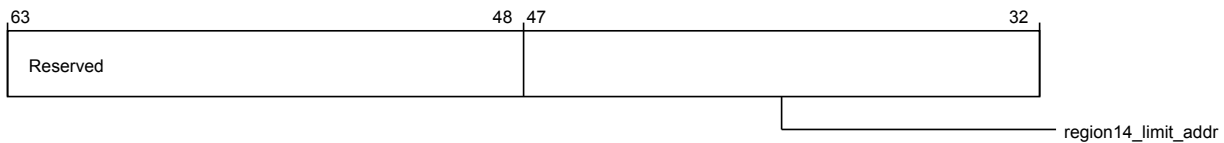


Figure 4-1528 `por_mpu_m0_prlar14` (high)

The following table shows the `por_mpu_m0_prlar14` higher register bit assignments.

Table 4-1545 `por_mpu_m0_prlar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region14_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

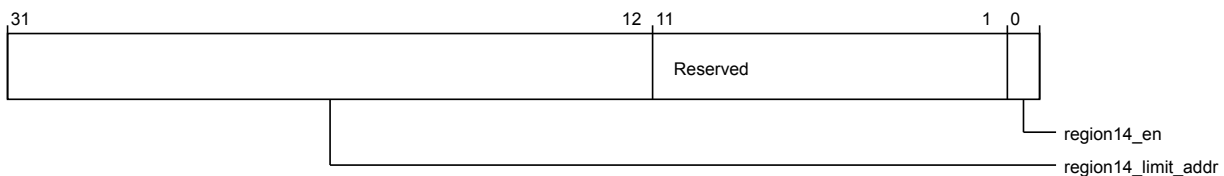


Figure 4-1529 `por_mpu_m0_prlar14` (low)

The following table shows the `por_mpu_m0_prlar14` lower register bit assignments.

Table 4-1546 `por_mpu_m0_prlar14` (low)

Bits	Field name	Description	Type	Reset
31:12	region14_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region14_en	Region 14 enable.	RW	1'b0

por_mpu_m0_prbar15

MPU master 0 programmable base address register 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1100
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

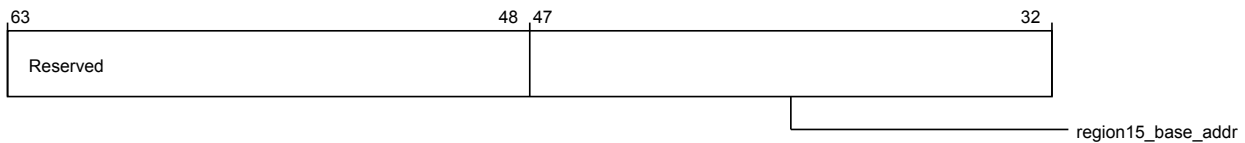


Figure 4-1530 por_mpu_m0_prbar15 (high)

The following table shows the por_mpu_m0_prbar15 higher register bit assignments.

Table 4-1547 por_mpu_m0_prbar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

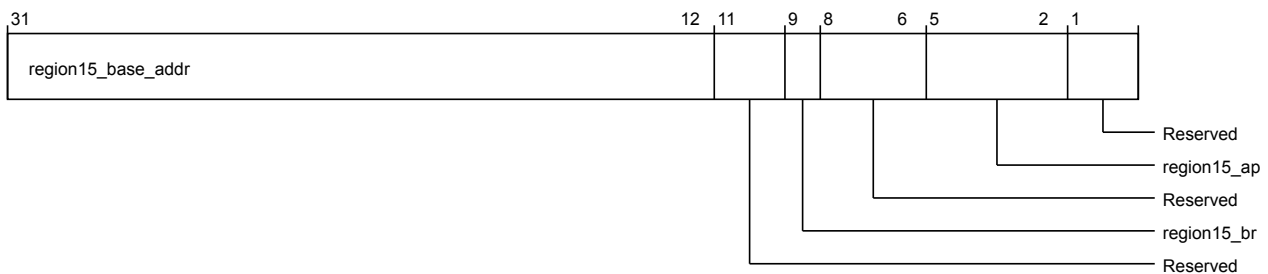


Figure 4-1531 por_mpu_m0_prbar15 (low)

The following table shows the por_mpu_m0_prbar15 lower register bit assignments.

Table 4-1548 por_mpu_m0_prbar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1548 `por_mpu_por_mpu_m0_prbar15` (low) (continued)

Bits	Field name	Description	Type	Reset
9	region15_br	Region 15 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region15_ap	Region 15 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m0_prlar15`

MPU master 0 programmable limit address register 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1108

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

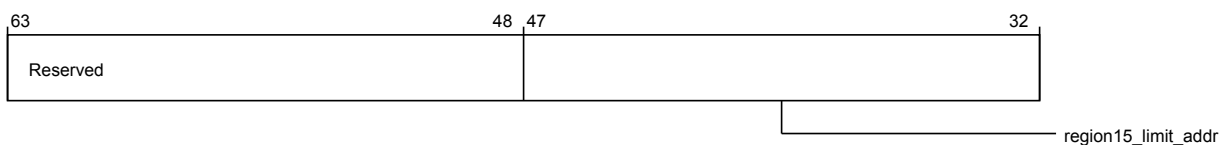


Figure 4-1532 `por_mpu_por_mpu_m0_prlar15` (high)

The following table shows the `por_mpu_m0_prlar15` higher register bit assignments.

Table 4-1549 `por_mpu_por_mpu_m0_prlar15` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

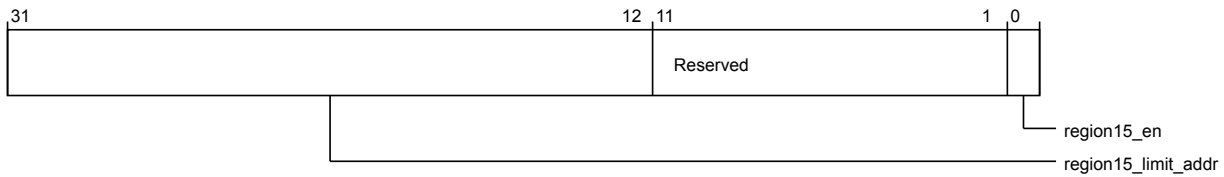


Figure 4-1533 por_mpu_por_mpu_m0_prlar15 (low)

The following table shows the por_mpu_m0_prlar15 lower register bit assignments.

Table 4-1550 por_mpu_por_mpu_m0_prlar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region15_en	Region 15 enable.	RW	1'b0

por_mpu_m0_prbar16

MPU master 0 programmable base address register 16.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1110

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

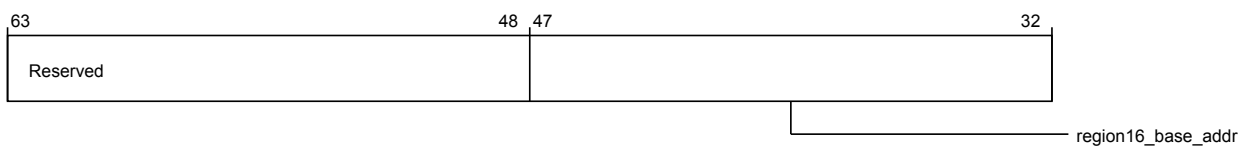


Figure 4-1534 por_mpu_por_mpu_m0_prbar16 (high)

The following table shows the por_mpu_m0_prbar16 higher register bit assignments.

Table 4-1551 por_mpu_por_mpu_m0_prbar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

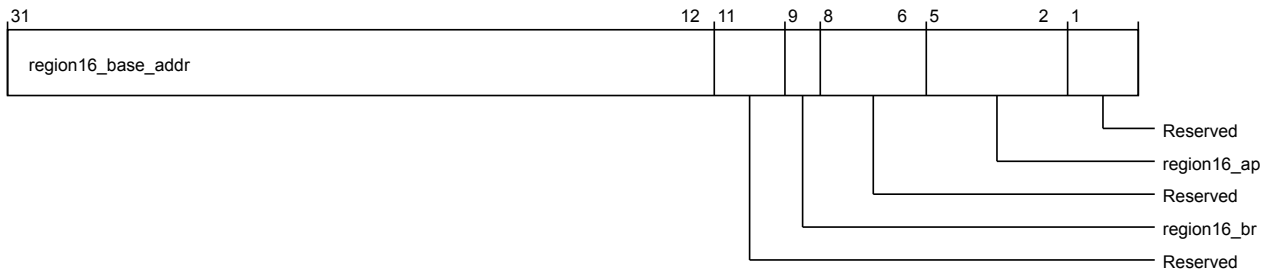


Figure 4-1535 `por_mpu_m0_prbar16` (low)

The following table shows the `por_mpu_m0_prbar16` lower register bit assignments.

Table 4-1552 `por_mpu_m0_prbar16` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region16_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region16_br</code>	Region 16 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region16_ap</code>	Region 16 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m0_prlar16`

MPU master 0 programmable limit address register 16.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1118

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

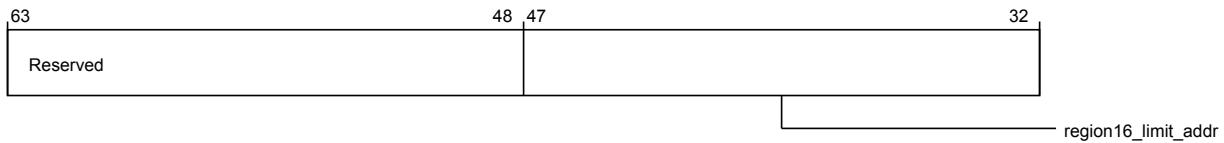


Figure 4-1536 por_mpu_m0_prlar16 (high)

The following table shows the por_mpu_m0_prlar16 higher register bit assignments.

Table 4-1553 por_mpu_m0_prlar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

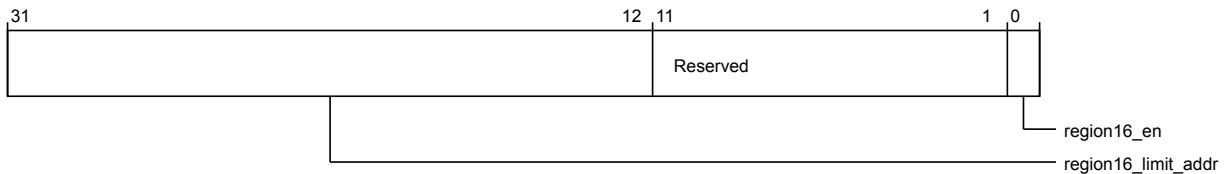


Figure 4-1537 por_mpu_m0_prlar16 (low)

The following table shows the por_mpu_m0_prlar16 lower register bit assignments.

Table 4-1554 por_mpu_m0_prlar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region16_en	Region 16 enable.	RW	1'b0

por_mpu_m0_prbar17

MPU master 0 programmable base address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1120

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

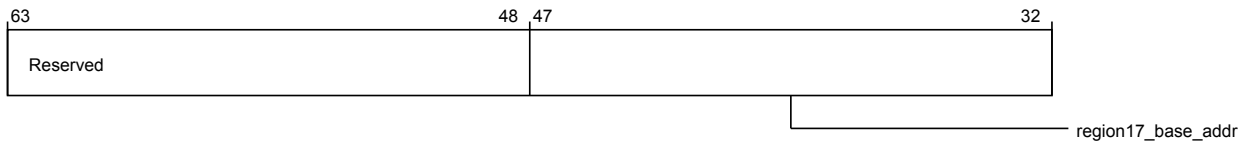


Figure 4-1538 `por_mpu_por_mpu_m0_prbar17` (high)

The following table shows the `por_mpu_m0_prbar17` higher register bit assignments.

Table 4-1555 `por_mpu_por_mpu_m0_prbar17` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region17_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

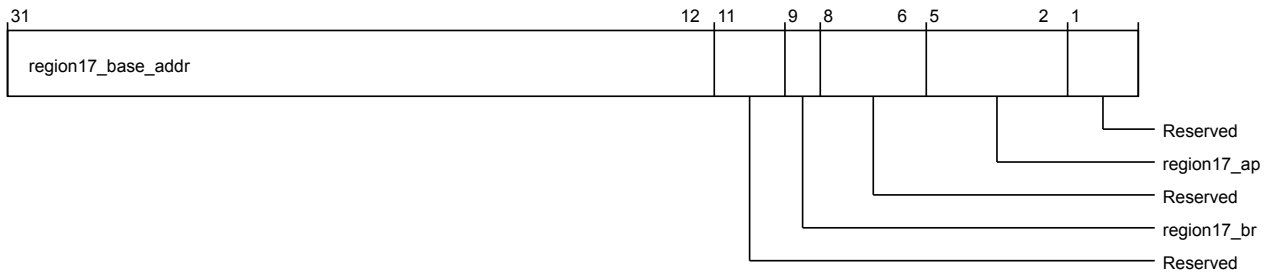


Figure 4-1539 `por_mpu_por_mpu_m0_prbar17` (low)

The following table shows the `por_mpu_m0_prbar17` lower register bit assignments.

Table 4-1556 `por_mpu_por_mpu_m0_prbar17` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region17_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region17_br</code>	Region 17 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region17_ap</code>	Region 17 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar17

MPU master 0 programmable limit address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1128

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

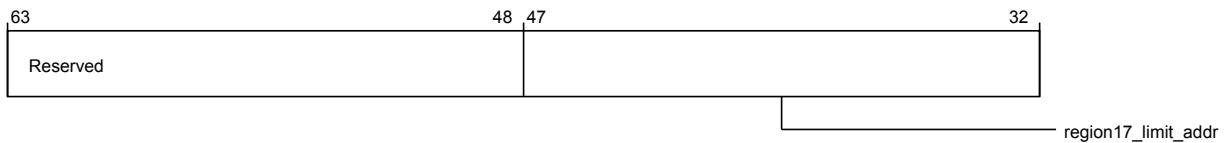


Figure 4-1540 `por_mpu_m0_prlar17` (high)

The following table shows the `por_mpu_m0_prlar17` higher register bit assignments.

Table 4-1557 `por_mpu_m0_prlar17` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

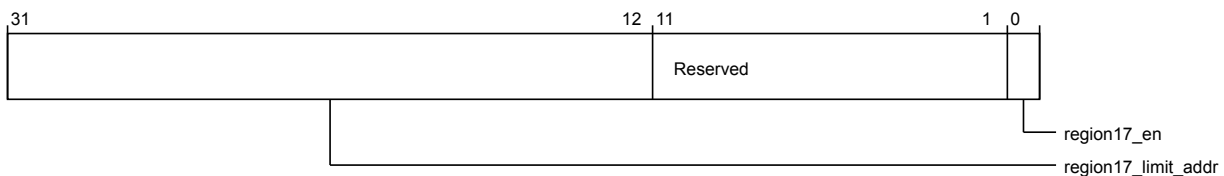


Figure 4-1541 `por_mpu_m0_prlar17` (low)

The following table shows the `por_mpu_m0_prlar17` lower register bit assignments.

Table 4-1558 `por_mpu_m0_prlar17` (low)

Bits	Field name	Description	Type	Reset
31:12	region17_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region17_en	Region 17 enable.	RW	1'b0

por_mpu_m0_prbar18

MPU master 0 programmable base address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1130
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

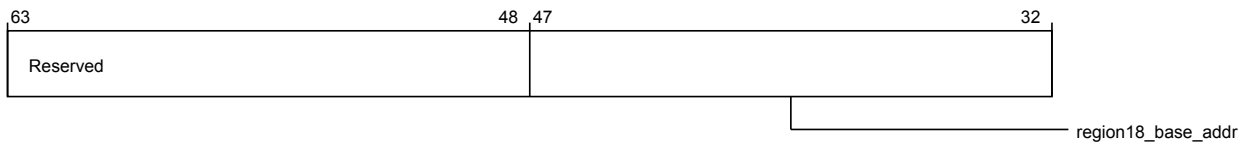


Figure 4-1542 por_mpu_por_mpu_m0_prbar18 (high)

The following table shows the por_mpu_m0_prbar18 higher register bit assignments.

Table 4-1559 por_mpu_por_mpu_m0_prbar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

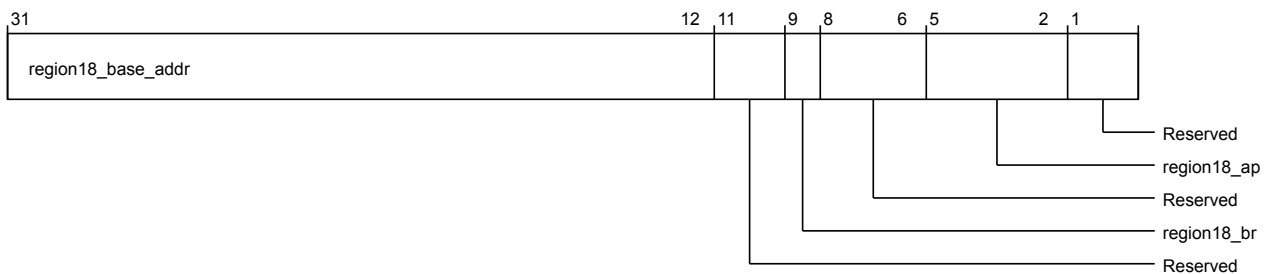


Figure 4-1543 por_mpu_por_mpu_m0_prbar18 (low)

The following table shows the por_mpu_m0_prbar18 lower register bit assignments.

Table 4-1560 por_mpu_por_mpu_m0_prbar18 (low)

Bits	Field name	Description	Type	Reset
31:12	region18_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1560 por_mpu_por_mpu_m0_prbar18 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region18_br	Region 18 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region18_ap	Region 18 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar18

MPU master 0 programmable limit address register 18.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1138

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

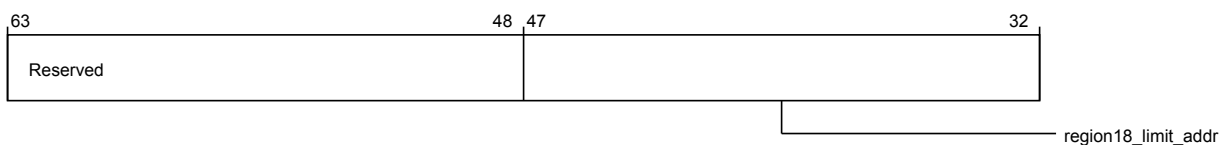


Figure 4-1544 por_mpu_por_mpu_m0_prlar18 (high)

The following table shows the por_mpu_m0_prlar18 higher register bit assignments.

Table 4-1561 por_mpu_por_mpu_m0_prlar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

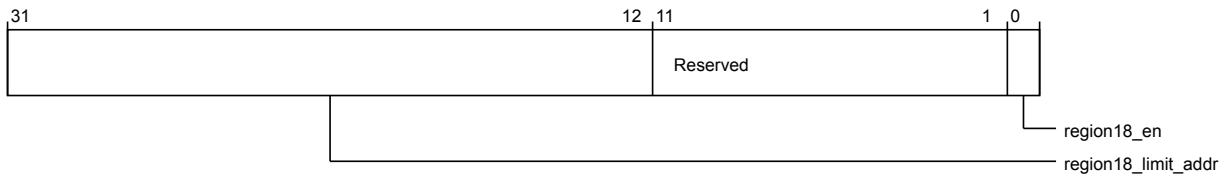


Figure 4-1545 `por_mpu_por_mpu_m0_prlar18` (low)

The following table shows the `por_mpu_m0_prlar18` lower register bit assignments.

Table 4-1562 `por_mpu_por_mpu_m0_prlar18` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region18_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region18_en</code>	Region 18 enable.	RW	1'b0

`por_mpu_m0_prbar19`

MPU master 0 programmable base address register 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1140

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

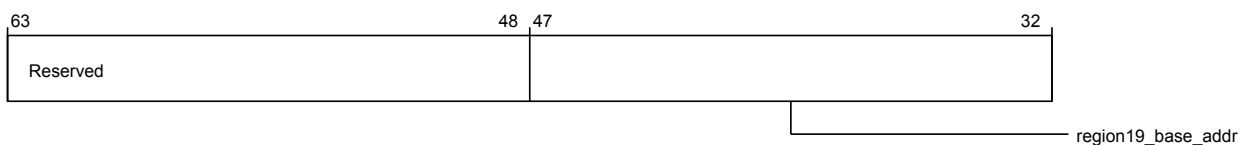


Figure 4-1546 `por_mpu_por_mpu_m0_prbar19` (high)

The following table shows the `por_mpu_m0_prbar19` higher register bit assignments.

Table 4-1563 `por_mpu_por_mpu_m0_prbar19` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region19_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

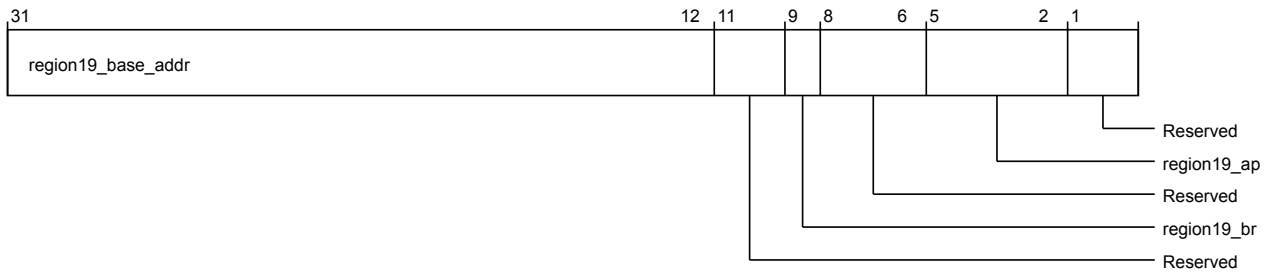


Figure 4-1547 `por_mpu_por_mpu_m0_prbar19` (low)

The following table shows the `por_mpu_m0_prbar19` lower register bit assignments.

Table 4-1564 `por_mpu_por_mpu_m0_prbar19` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region19_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region19_br</code>	Region 19 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region19_ap</code>	Region 19 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m0_prlar19`

MPU master 0 programmable limit address register 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1148

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

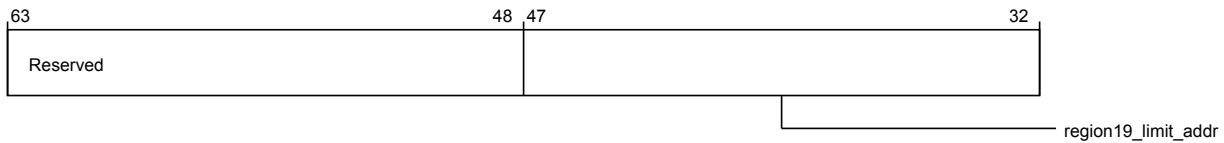


Figure 4-1548 por_mpu_m0_prlar19 (high)

The following table shows the por_mpu_m0_prlar19 higher register bit assignments.

Table 4-1565 por_mpu_m0_prlar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

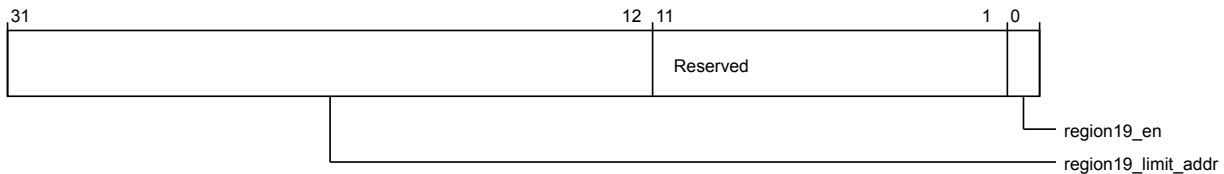


Figure 4-1549 por_mpu_m0_prlar19 (low)

The following table shows the por_mpu_m0_prlar19 lower register bit assignments.

Table 4-1566 por_mpu_m0_prlar19 (low)

Bits	Field name	Description	Type	Reset
31:12	region19_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region19_en	Region 19 enable.	RW	1'b0

por_mpu_m0_prbar20

MPU master 0 programmable base address register 20.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1150
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

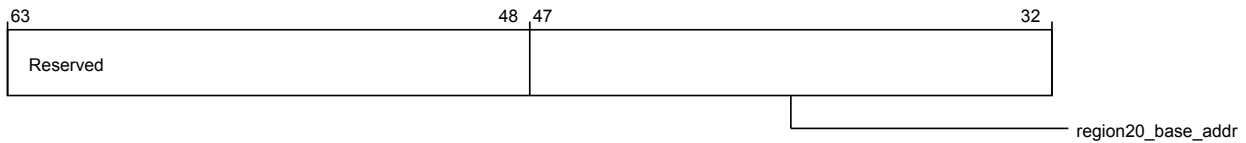


Figure 4-1550 por_mpu_por_mpu_m0_prbar20 (high)

The following table shows the por_mpu_m0_prbar20 higher register bit assignments.

Table 4-1567 por_mpu_por_mpu_m0_prbar20 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region20_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

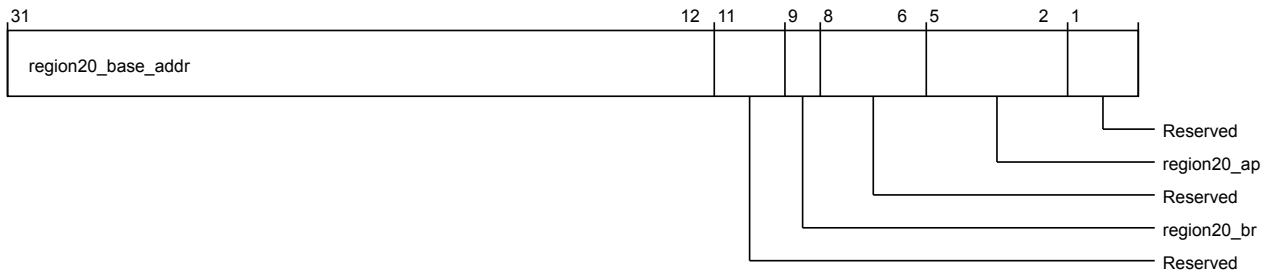


Figure 4-1551 por_mpu_por_mpu_m0_prbar20 (low)

The following table shows the por_mpu_m0_prbar20 lower register bit assignments.

Table 4-1568 por_mpu_por_mpu_m0_prbar20 (low)

Bits	Field name	Description	Type	Reset
31:12	region20_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region20_br	Region 20 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region20_ap	Region 20 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar20

MPU master 0 programmable limit address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1158

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

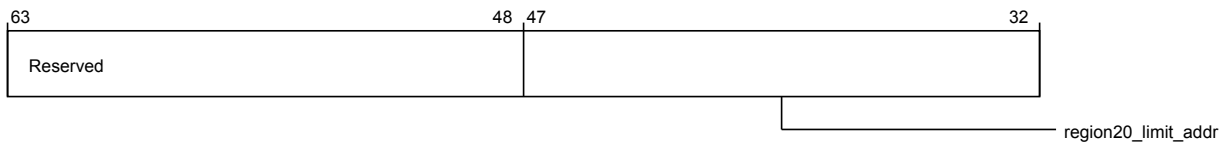


Figure 4-1552 por_mpu_por_mpu_m0_prlar20 (high)

The following table shows the por_mpu_m0_prlar20 higher register bit assignments.

Table 4-1569 por_mpu_por_mpu_m0_prlar20 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region20_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

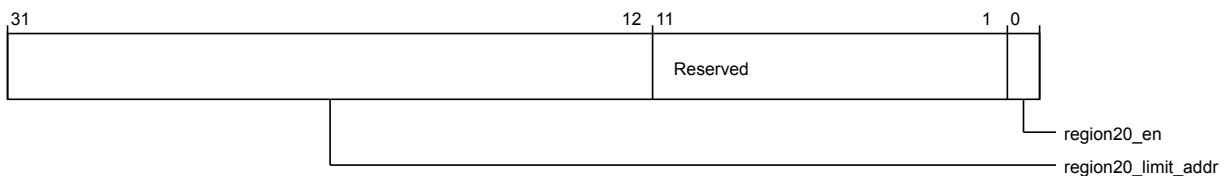


Figure 4-1553 por_mpu_por_mpu_m0_prlar20 (low)

The following table shows the por_mpu_m0_prlar20 lower register bit assignments.

Table 4-1570 por_mpu_por_mpu_m0_prlar20 (low)

Bits	Field name	Description	Type	Reset
31:12	region20_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region20_en	Region 20 enable.	RW	1'b0

por_mpu_m0_prbar21

MPU master 0 programmable base address register 21.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1160
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

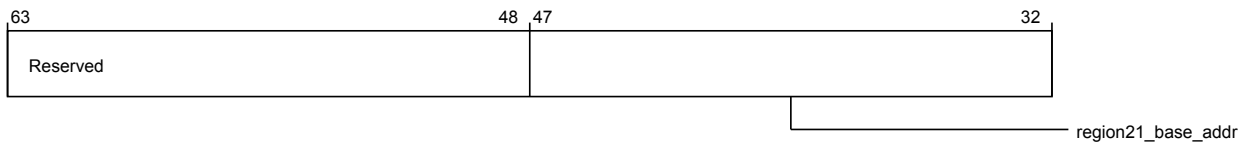


Figure 4-1554 por_mpu_por_mpu_m0_prbar21 (high)

The following table shows the por_mpu_m0_prbar21 higher register bit assignments.

Table 4-1571 por_mpu_por_mpu_m0_prbar21 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

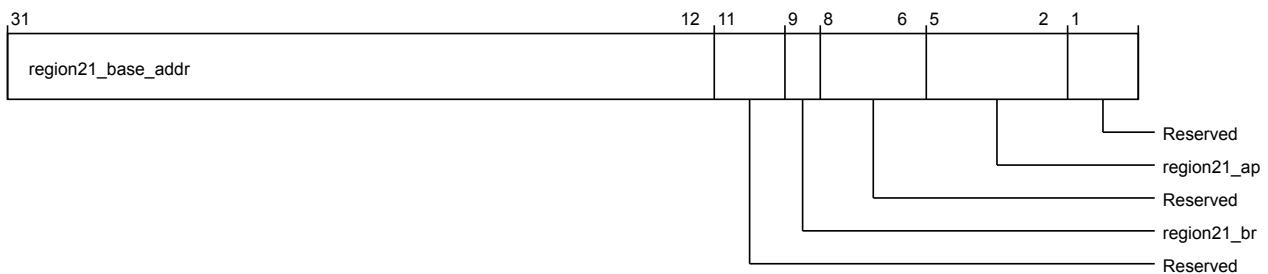


Figure 4-1555 por_mpu_por_mpu_m0_prbar21 (low)

The following table shows the por_mpu_m0_prbar21 lower register bit assignments.

Table 4-1572 por_mpu_por_mpu_m0_prbar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1572 `por_mpu_por_mpu_m0_prbar21` (low) (continued)

Bits	Field name	Description	Type	Reset
9	region21_br	Region 21 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region21_ap	Region 21 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m0_prlar21`

MPU master 0 programmable limit address register 21.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1168

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

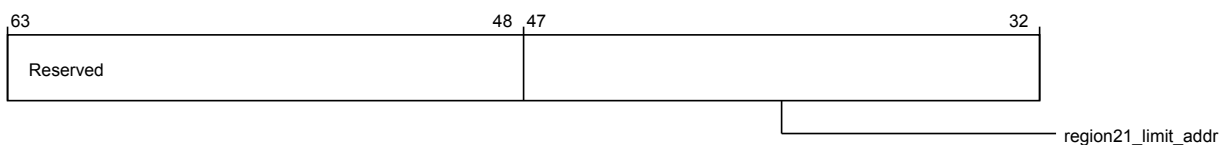


Figure 4-1556 `por_mpu_por_mpu_m0_prlar21` (high)

The following table shows the `por_mpu_m0_prlar21` higher register bit assignments.

Table 4-1573 `por_mpu_por_mpu_m0_prlar21` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

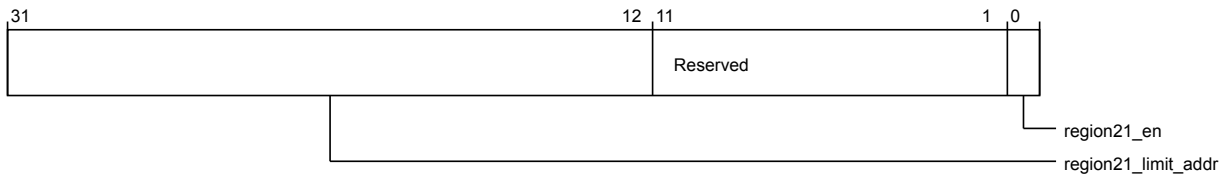


Figure 4-1557 por_mpu_m0_prbar21 (low)

The following table shows the por_mpu_m0_prbar21 lower register bit assignments.

Table 4-1574 por_mpu_m0_prbar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region21_en	Region 21 enable.	RW	1'b0

por_mpu_m0_prbar22

MPU master 0 programmable base address register 22.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1170

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

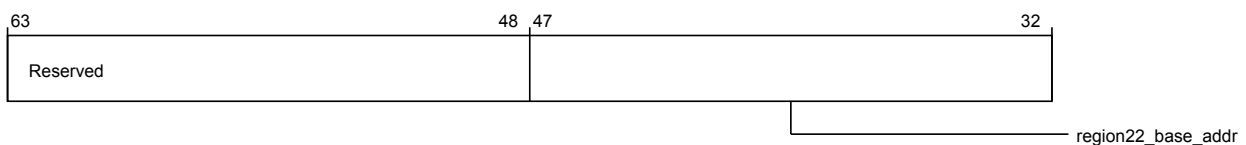


Figure 4-1558 por_mpu_m0_prbar22 (high)

The following table shows the por_mpu_m0_prbar22 higher register bit assignments.

Table 4-1575 por_mpu_m0_prbar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

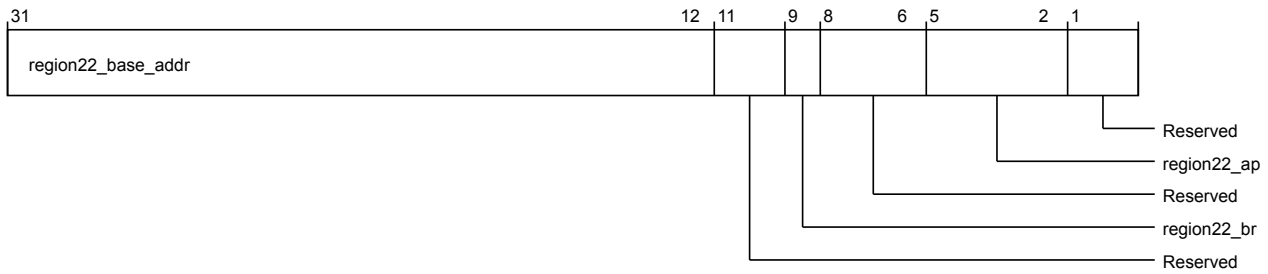


Figure 4-1559 por_mpu_por_mpu_m0_prbar22 (low)

The following table shows the por_mpu_m0_prbar22 lower register bit assignments.

Table 4-1576 por_mpu_por_mpu_m0_prbar22 (low)

Bits	Field name	Description	Type	Reset
31:12	region22_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region22_br	Region 22 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region22_ap	Region 22 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar22

MPU master 0 programmable limit address register 22.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1178

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

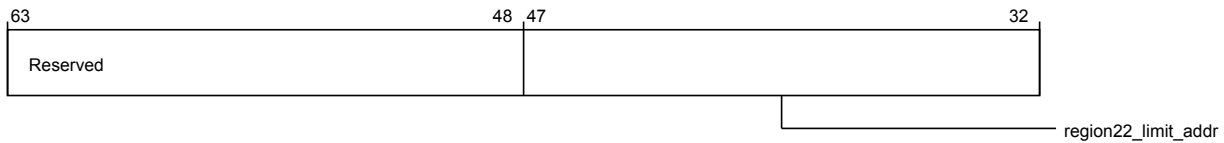


Figure 4-1560 `por_mpu_m0_prlar22` (high)

The following table shows the `por_mpu_m0_prlar22` higher register bit assignments.

Table 4-1577 `por_mpu_m0_prlar22` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

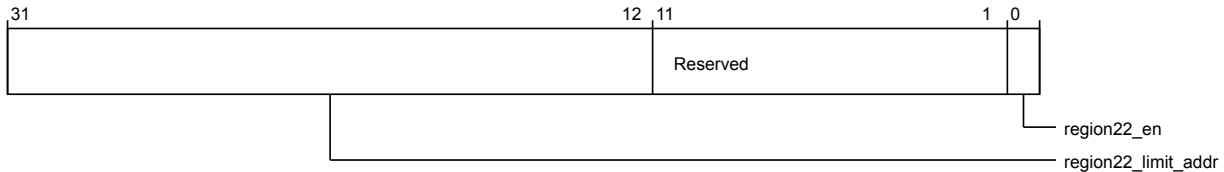


Figure 4-1561 `por_mpu_m0_prlar22` (low)

The following table shows the `por_mpu_m0_prlar22` lower register bit assignments.

Table 4-1578 `por_mpu_m0_prlar22` (low)

Bits	Field name	Description	Type	Reset
31:12	region22_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region22_en	Region 22 enable.	RW	1'b0

`por_mpu_m0_prbar23`

MPU master 0 programmable base address register 23.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1180
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

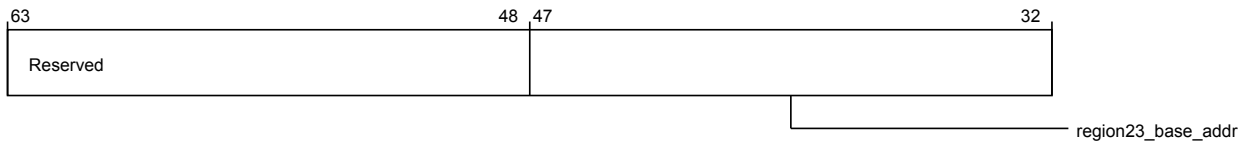


Figure 4-1562 por_mpu_por_mpu_m0_prbar23 (high)

The following table shows the por_mpu_m0_prbar23 higher register bit assignments.

Table 4-1579 por_mpu_por_mpu_m0_prbar23 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region23_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

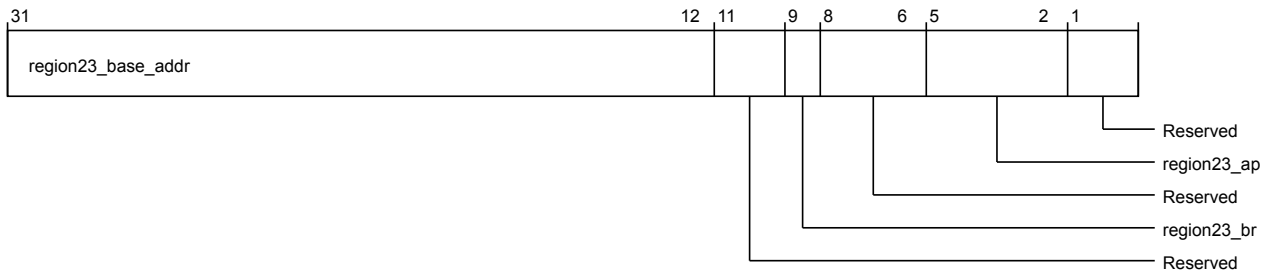


Figure 4-1563 por_mpu_por_mpu_m0_prbar23 (low)

The following table shows the por_mpu_m0_prbar23 lower register bit assignments.

Table 4-1580 por_mpu_por_mpu_m0_prbar23 (low)

Bits	Field name	Description	Type	Reset
31:12	region23_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region23_br	Region 23 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region23_ap	Region 23 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar23

MPU master 0 programmable limit address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1188

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

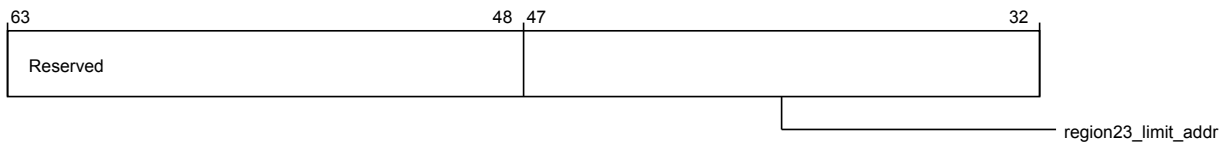


Figure 4-1564 por_mpu_por_mpu_m0_prlar23 (high)

The following table shows the `por_mpu_m0_prlar23` higher register bit assignments.

Table 4-1581 por_mpu_por_mpu_m0_prlar23 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region23_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

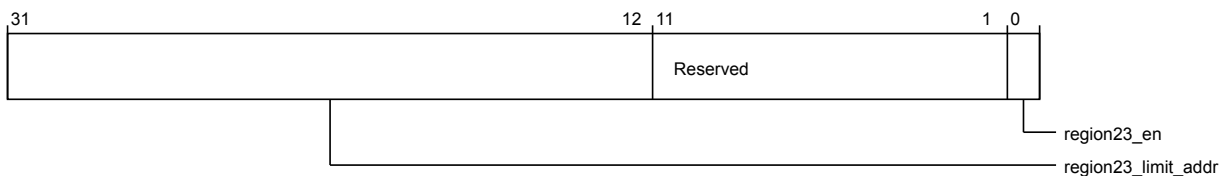


Figure 4-1565 por_mpu_por_mpu_m0_prlar23 (low)

The following table shows the `por_mpu_m0_prlar23` lower register bit assignments.

Table 4-1582 por_mpu_por_mpu_m0_prlar23 (low)

Bits	Field name	Description	Type	Reset
31:12	region23_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region23_en	Region 23 enable.	RW	1'b0

por_mpu_m0_prbar24

MPU master 0 programmable base address register 24.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1190

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

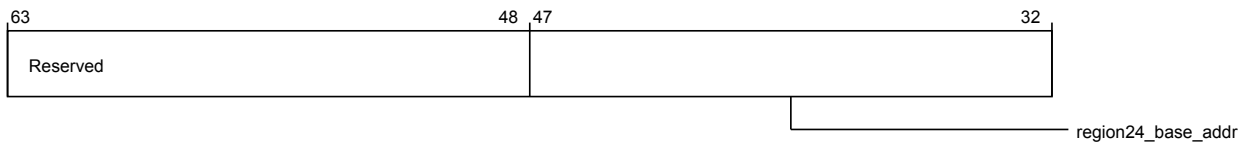


Figure 4-1566 por_mpu_por_mpu_m0_prbar24 (high)

The following table shows the por_mpu_m0_prbar24 higher register bit assignments.

Table 4-1583 por_mpu_por_mpu_m0_prbar24 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

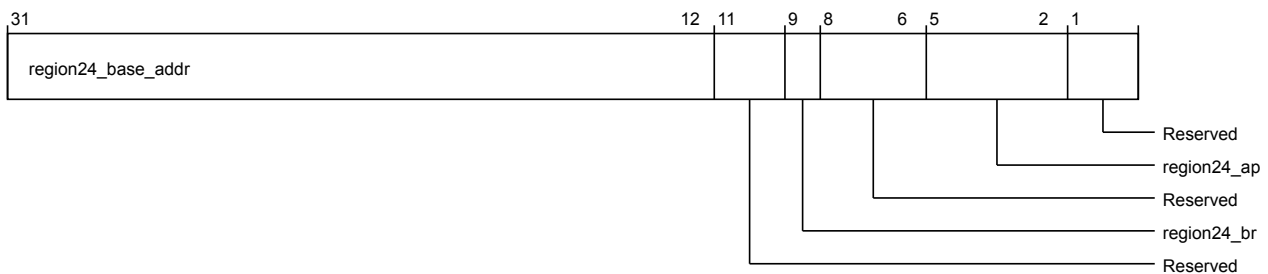


Figure 4-1567 por_mpu_por_mpu_m0_prbar24 (low)

The following table shows the por_mpu_m0_prbar24 lower register bit assignments.

Table 4-1584 por_mpu_por_mpu_m0_prbar24 (low)

Bits	Field name	Description	Type	Reset
31:12	region24_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1584 por_mpu_por_mpu_m0_prbar24 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region24_br	Region 24 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region24_ap	Region 24 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar24

MPU master 0 programmable limit address register 24.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1198

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

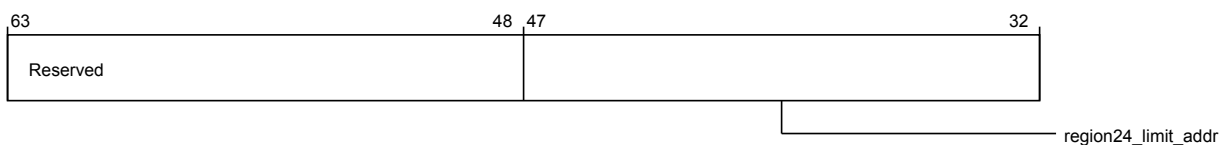


Figure 4-1568 por_mpu_por_mpu_m0_prlar24 (high)

The following table shows the por_mpu_m0_prlar24 higher register bit assignments.

Table 4-1585 por_mpu_por_mpu_m0_prlar24 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

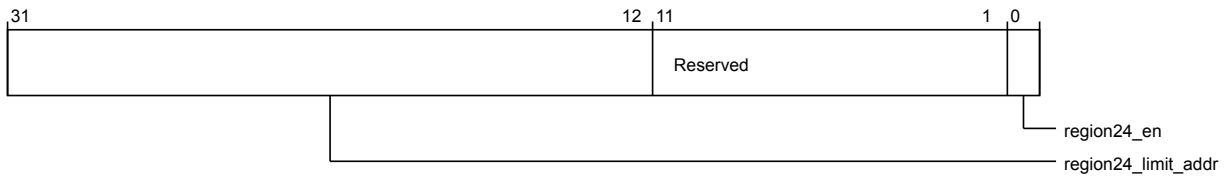


Figure 4-1569 `por_mpu_m0_prlar24` (low)

The following table shows the `por_mpu_m0_prlar24` lower register bit assignments.

Table 4-1586 `por_mpu_m0_prlar24` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region24_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region24_en</code>	Region 24 enable.	RW	1'b0

`por_mpu_m0_prbar25`

MPU master 0 programmable base address register 25.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h11A0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

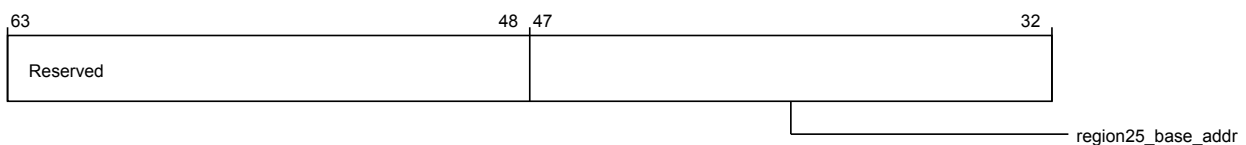


Figure 4-1570 `por_mpu_m0_prbar25` (high)

The following table shows the `por_mpu_m0_prbar25` higher register bit assignments.

Table 4-1587 `por_mpu_m0_prbar25` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region25_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

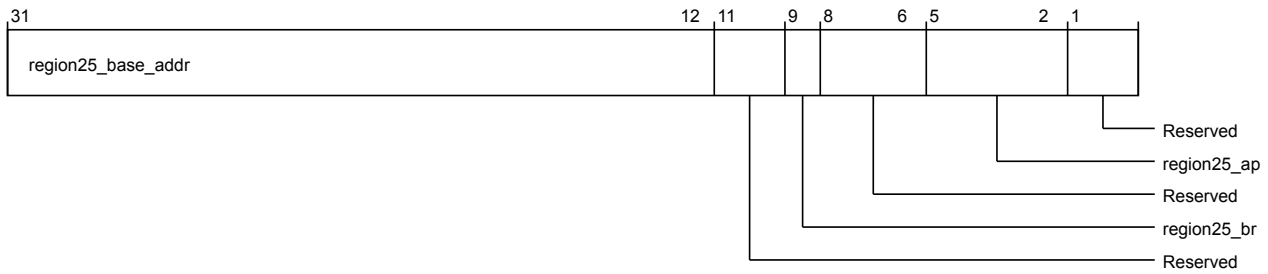


Figure 4-1571 por_mpu_m0_prbar25 (low)

The following table shows the por_mpu_m0_prbar25 lower register bit assignments.

Table 4-1588 por_mpu_m0_prbar25 (low)

Bits	Field name	Description	Type	Reset
31:12	region25_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region25_br	Region 25 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region25_ap	Region 25 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar25

MPU master 0 programmable limit address register 25.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h11A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

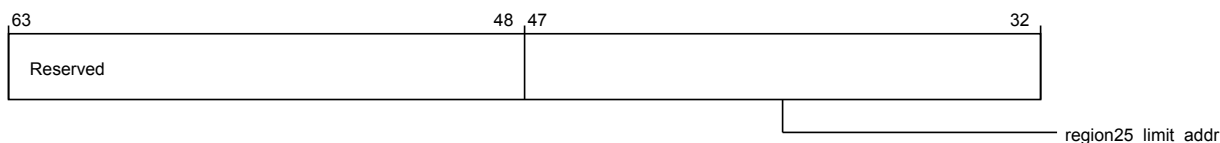


Figure 4-1572 por_mpu_m0_prlar25 (high)

The following table shows the por_mpu_m0_prlar25 higher register bit assignments.

Table 4-1589 por_mpu_m0_prlar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

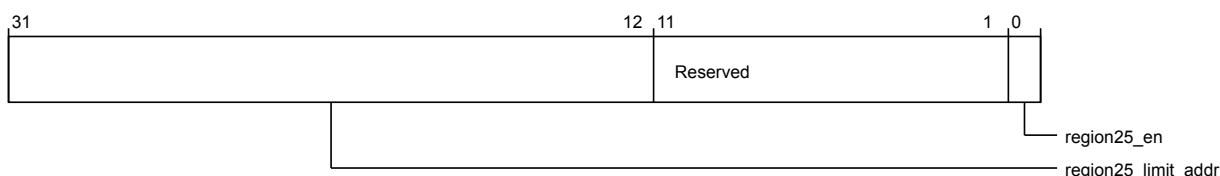


Figure 4-1573 por_mpu_m0_prlar25 (low)

The following table shows the por_mpu_m0_prlar25 lower register bit assignments.

Table 4-1590 por_mpu_m0_prlar25 (low)

Bits	Field name	Description	Type	Reset
31:12	region25_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region25_en	Region 25 enable.	RW	1'b0

por_mpu_m0_prbar26

MPU master 0 programmable base address register 26.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h11B0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

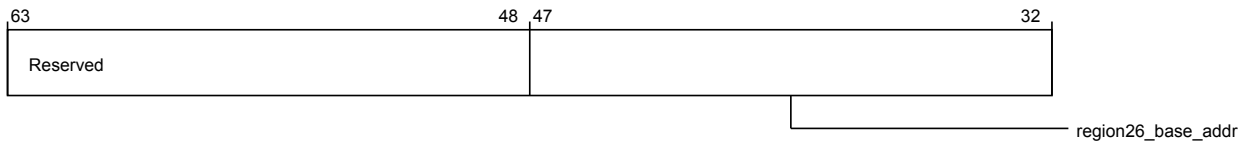


Figure 4-1574 por_mpu_por_mpu_m0_prbar26 (high)

The following table shows the por_mpu_m0_prbar26 higher register bit assignments.

Table 4-1591 por_mpu_por_mpu_m0_prbar26 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region26_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

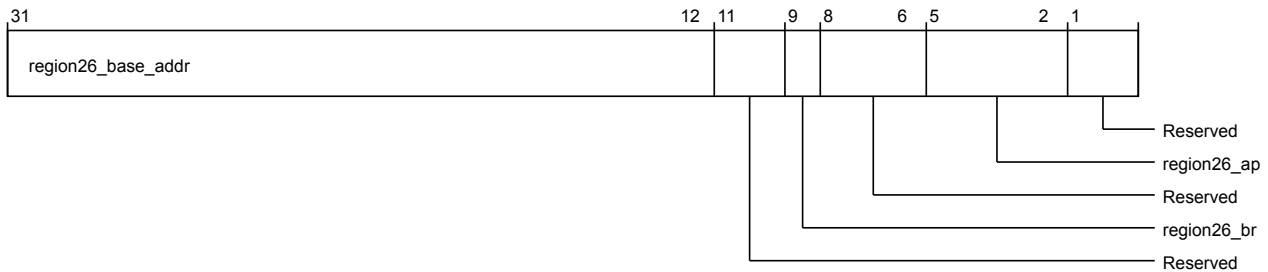


Figure 4-1575 por_mpu_por_mpu_m0_prbar26 (low)

The following table shows the por_mpu_m0_prbar26 lower register bit assignments.

Table 4-1592 por_mpu_por_mpu_m0_prbar26 (low)

Bits	Field name	Description	Type	Reset
31:12	region26_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region26_br	Region 26 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region26_ap	Region 26 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar26

MPU master 0 programmable limit address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h11B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

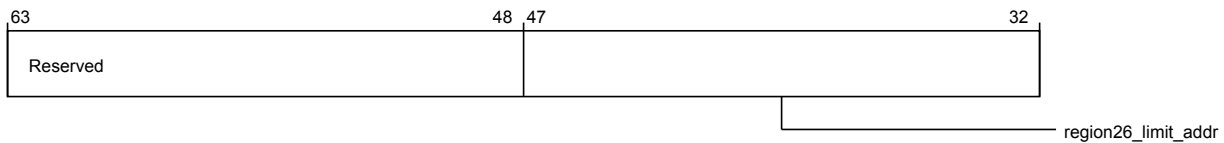


Figure 4-1576 por_mpu_por_mpu_m0_prlar26 (high)

The following table shows the `por_mpu_m0_prlar26` higher register bit assignments.

Table 4-1593 por_mpu_por_mpu_m0_prlar26 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region26_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

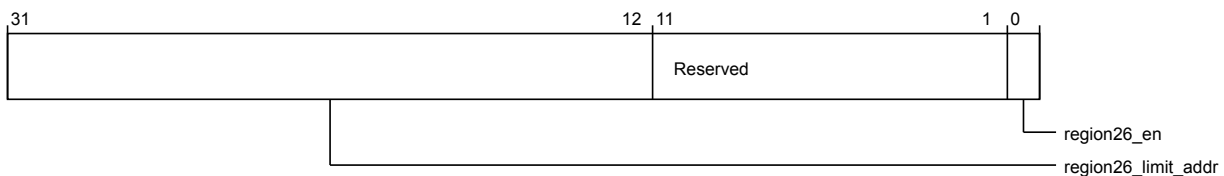


Figure 4-1577 por_mpu_por_mpu_m0_prlar26 (low)

The following table shows the `por_mpu_m0_prlar26` lower register bit assignments.

Table 4-1594 por_mpu_por_mpu_m0_prlar26 (low)

Bits	Field name	Description	Type	Reset
31:12	region26_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region26_en	Region 26 enable.	RW	1'b0

por_mpu_m0_prbar27

MPU master 0 programmable base address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h11C0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

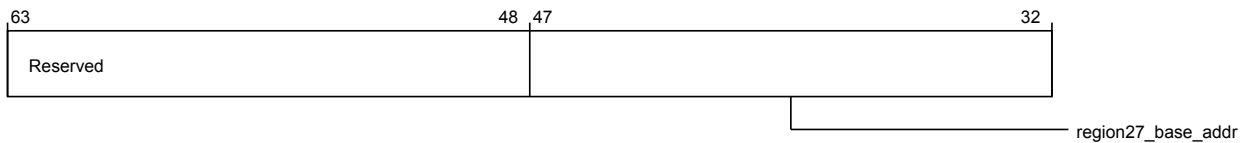


Figure 4-1578 por_mpu_por_mpu_m0_prbar27 (high)

The following table shows the por_mpu_m0_prbar27 higher register bit assignments.

Table 4-1595 por_mpu_por_mpu_m0_prbar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

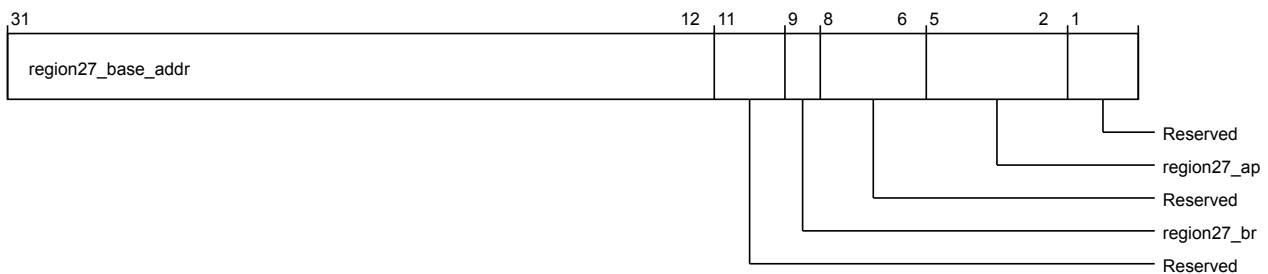


Figure 4-1579 por_mpu_por_mpu_m0_prbar27 (low)

The following table shows the por_mpu_m0_prbar27 lower register bit assignments.

Table 4-1596 por_mpu_por_mpu_m0_prbar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1596 por_mpu_por_mpu_m0_prbar27 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region27_br	Region 27 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region27_ap	Region 27 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar27

MPU master 0 programmable limit address register 27.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h11C8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

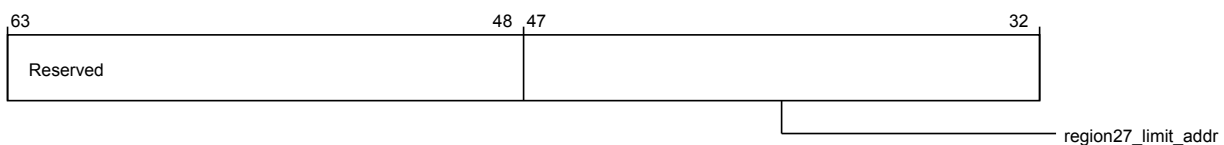


Figure 4-1580 por_mpu_por_mpu_m0_prlar27 (high)

The following table shows the por_mpu_m0_prlar27 higher register bit assignments.

Table 4-1597 por_mpu_por_mpu_m0_prlar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

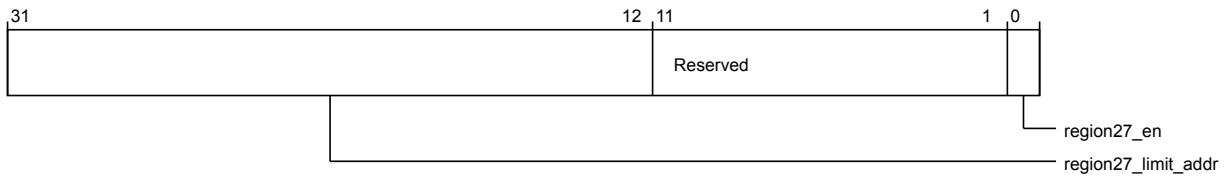


Figure 4-1581 `por_mpu_por_mpu_m0_prlar27` (low)

The following table shows the `por_mpu_m0_prlar27` lower register bit assignments.

Table 4-1598 `por_mpu_por_mpu_m0_prlar27` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region27_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region27_en</code>	Region 27 enable.	RW	1'b0

`por_mpu_m0_prbar28`

MPU master 0 programmable base address register 28.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h11D0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

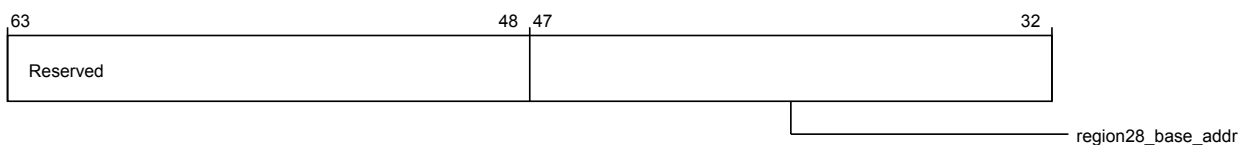


Figure 4-1582 `por_mpu_por_mpu_m0_prbar28` (high)

The following table shows the `por_mpu_m0_prbar28` higher register bit assignments.

Table 4-1599 `por_mpu_por_mpu_m0_prbar28` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region28_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

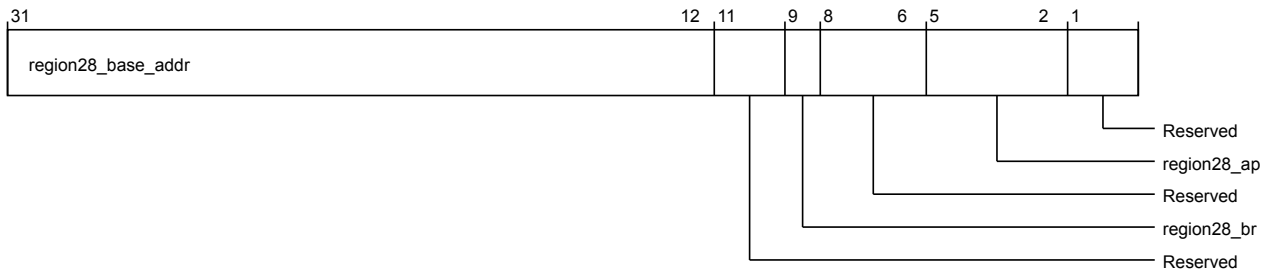


Figure 4-1583 `por_mpu_por_mpu_m0_prbar28` (low)

The following table shows the `por_mpu_m0_prbar28` lower register bit assignments.

Table 4-1600 `por_mpu_por_mpu_m0_prbar28` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region28_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region28_br</code>	Region 28 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region28_ap</code>	Region 28 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m0_prlar28`

MPU master 0 programmable limit address register 28.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h11D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

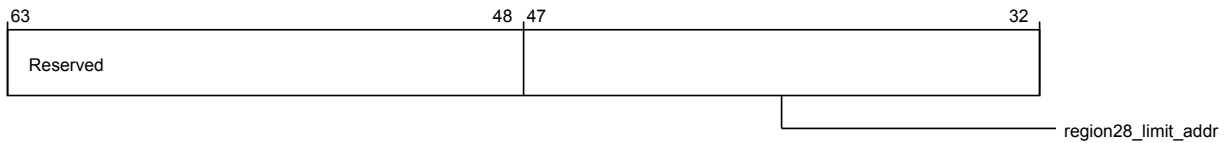


Figure 4-1584 por_mpu_m0_prlar28 (high)

The following table shows the por_mpu_m0_prlar28 higher register bit assignments.

Table 4-1601 por_mpu_m0_prlar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

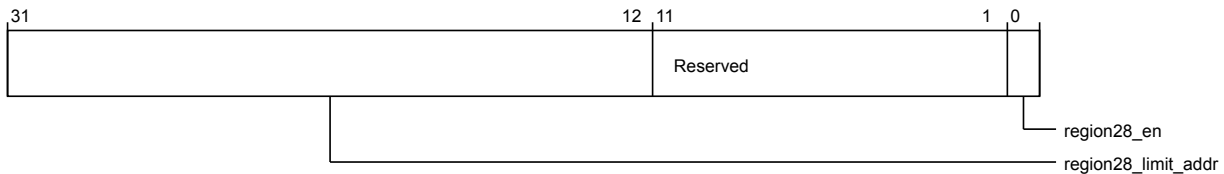


Figure 4-1585 por_mpu_m0_prlar28 (low)

The following table shows the por_mpu_m0_prlar28 lower register bit assignments.

Table 4-1602 por_mpu_m0_prlar28 (low)

Bits	Field name	Description	Type	Reset
31:12	region28_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region28_en	Region 28 enable.	RW	1'b0

por_mpu_m0_prbar29

MPU master 0 programmable base address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h11E0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

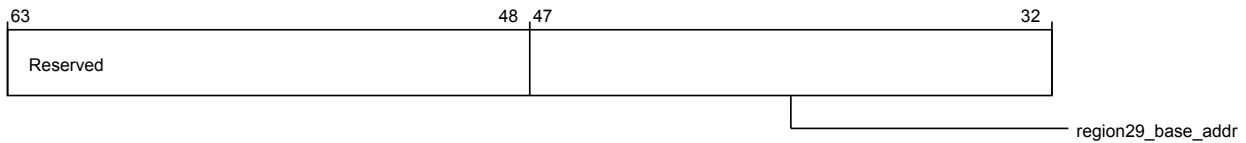


Figure 4-1586 `por_mpu_por_mpu_m0_prbar29` (high)

The following table shows the `por_mpu_m0_prbar29` higher register bit assignments.

Table 4-1603 `por_mpu_por_mpu_m0_prbar29` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region29_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

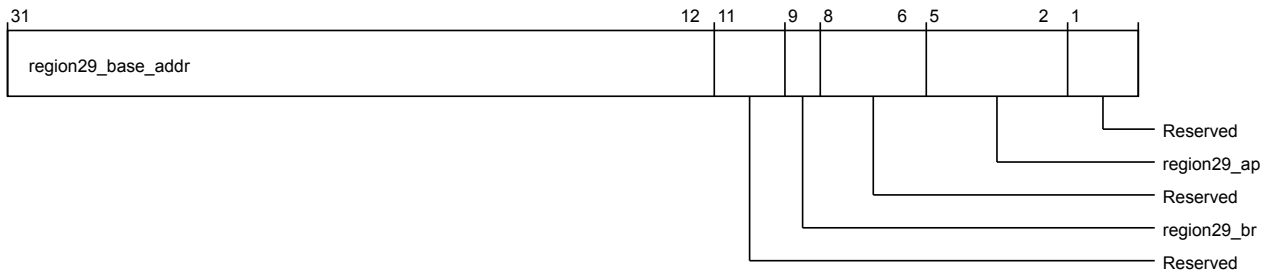


Figure 4-1587 `por_mpu_por_mpu_m0_prbar29` (low)

The following table shows the `por_mpu_m0_prbar29` lower register bit assignments.

Table 4-1604 `por_mpu_por_mpu_m0_prbar29` (low)

Bits	Field name	Description	Type	Reset
31:12	region29_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region29_br	Region 29 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region29_ap	Region 29 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar29

MPU master 0 programmable limit address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h11E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

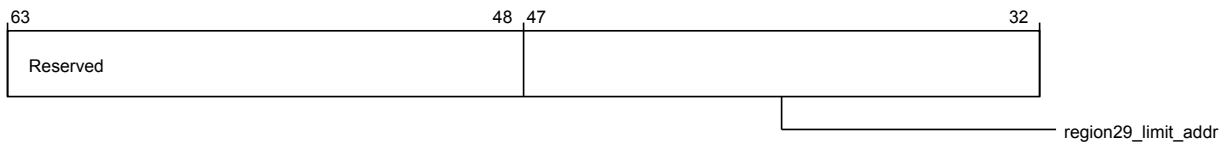


Figure 4-1588 por_mpu_por_mpu_m0_prlar29 (high)

The following table shows the `por_mpu_m0_prlar29` higher register bit assignments.

Table 4-1605 por_mpu_por_mpu_m0_prlar29 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region29_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

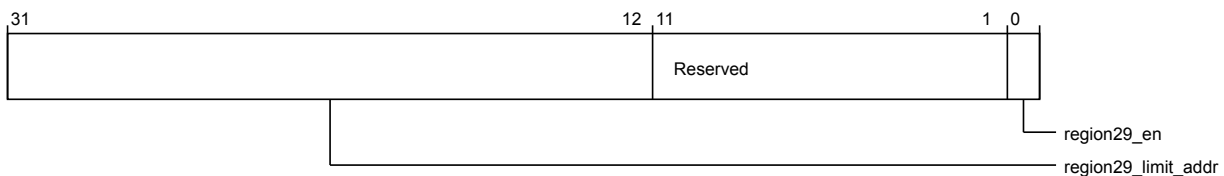


Figure 4-1589 por_mpu_por_mpu_m0_prlar29 (low)

The following table shows the `por_mpu_m0_prlar29` lower register bit assignments.

Table 4-1606 por_mpu_por_mpu_m0_prlar29 (low)

Bits	Field name	Description	Type	Reset
31:12	region29_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region29_en	Region 29 enable.	RW	1'b0

por_mpu_m0_prbar30

MPU master 0 programmable base address register 30.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h11F0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

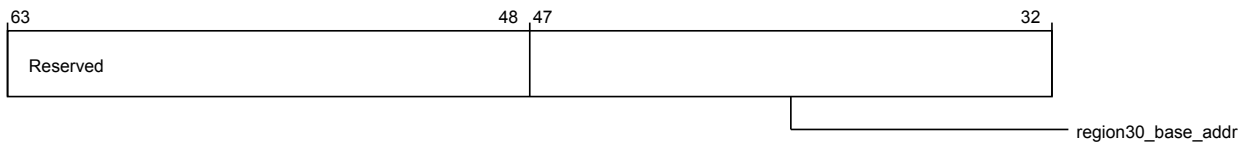


Figure 4-1590 por_mpu_m0_prbar30 (high)

The following table shows the por_mpu_m0_prbar30 higher register bit assignments.

Table 4-1607 por_mpu_m0_prbar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

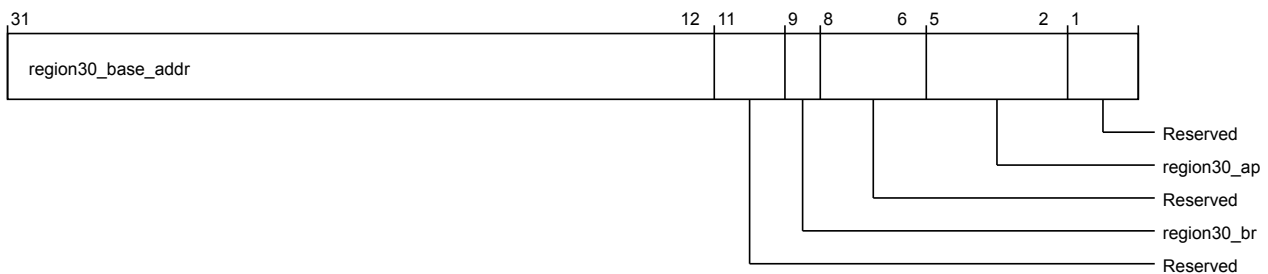


Figure 4-1591 por_mpu_m0_prbar30 (low)

The following table shows the por_mpu_m0_prbar30 lower register bit assignments.

Table 4-1608 por_mpu_m0_prbar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1608 por_mpu_por_mpu_m0_prbar30 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region30_br	Region 30 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region30_ap	Region 30 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m0_prlar30

MPU master 0 programmable limit address register 30.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h11F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

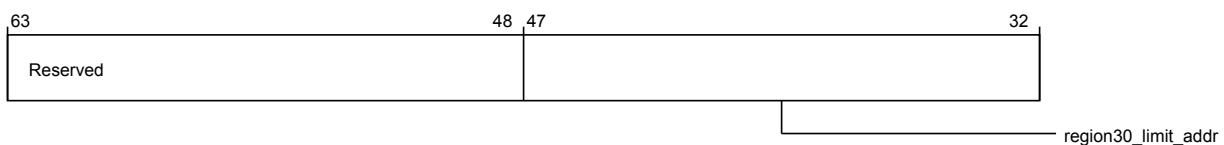


Figure 4-1592 por_mpu_por_mpu_m0_prlar30 (high)

The following table shows the por_mpu_m0_prlar30 higher register bit assignments.

Table 4-1609 por_mpu_por_mpu_m0_prlar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

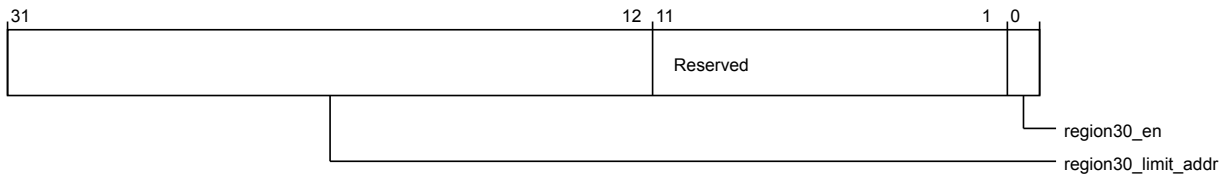


Figure 4-1593 `por_mpu_por_mpu_m0_prlar30` (low)

The following table shows the `por_mpu_m0_prlar30` lower register bit assignments.

Table 4-1610 `por_mpu_por_mpu_m0_prlar30` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region30_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region30_en</code>	Region 30 enable.	RW	1'b0

`por_mpu_m0_prbar31`

MPU master 0 programmable base address register 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1200

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

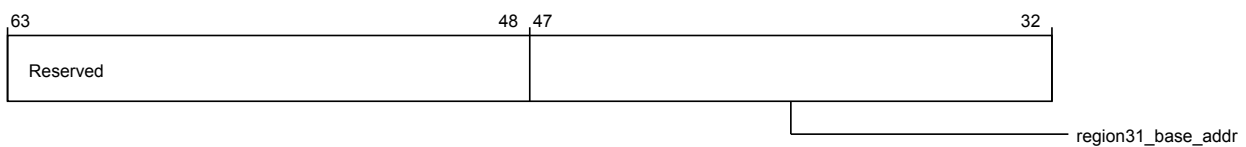


Figure 4-1594 `por_mpu_por_mpu_m0_prbar31` (high)

The following table shows the `por_mpu_m0_prbar31` higher register bit assignments.

Table 4-1611 `por_mpu_por_mpu_m0_prbar31` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region31_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

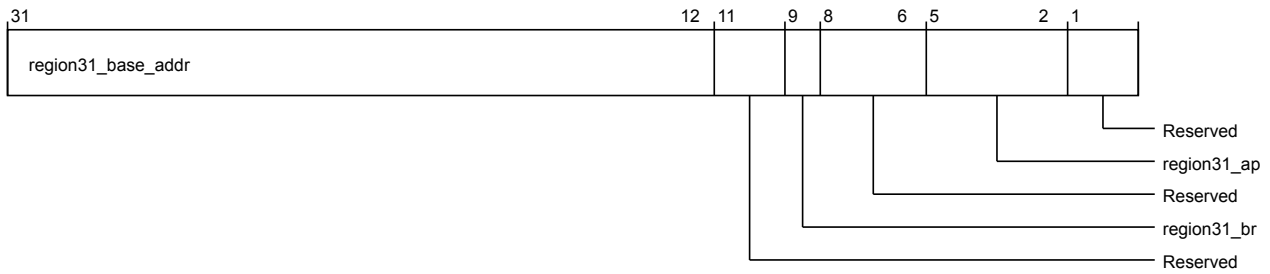


Figure 4-1595 `por_mpu_m0_prbar31` (low)

The following table shows the `por_mpu_m0_prbar31` lower register bit assignments.

Table 4-1612 `por_mpu_m0_prbar31` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region31_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region31_br</code>	Region 31 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region31_ap</code>	Region 31 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m0_prlar31`

MPU master 0 programmable limit address register 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1208

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

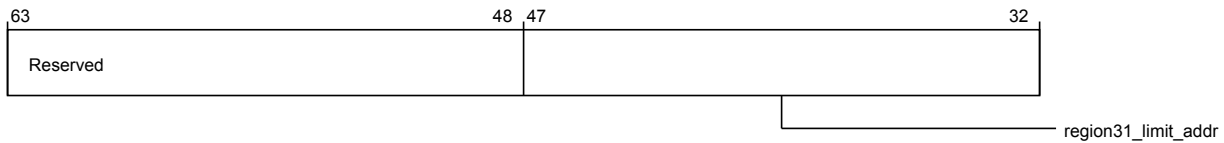


Figure 4-1596 por_mpu_m0_prlar31 (high)

The following table shows the por_mpu_m0_prlar31 higher register bit assignments.

Table 4-1613 por_mpu_m0_prlar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

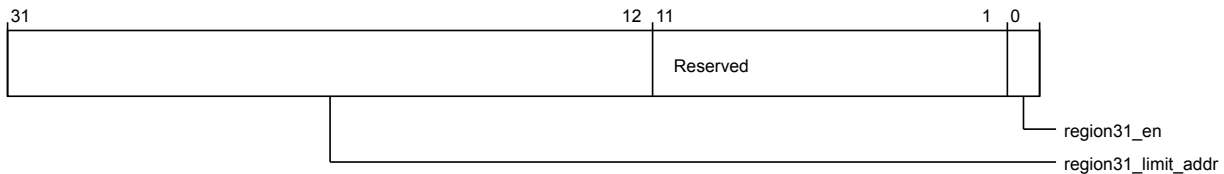


Figure 4-1597 por_mpu_m0_prlar31 (low)

The following table shows the por_mpu_m0_prlar31 lower register bit assignments.

Table 4-1614 por_mpu_m0_prlar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region31_en	Region 31 enable.	RW	1'b0

por_mpu_m1_ctl

Functions as the MPU Master 1 control register.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1400

Register reset 64'b010

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

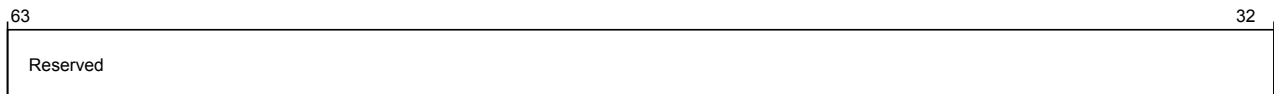


Figure 4-1598 por_mpu_por_mpu_m1_ctl (high)

The following table shows the por_mpu_m1_ctl higher register bit assignments.

Table 4-1615 por_mpu_por_mpu_m1_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

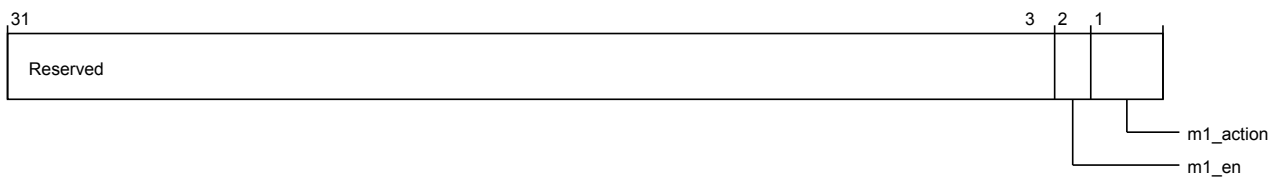


Figure 4-1599 por_mpu_por_mpu_m1_ctl (low)

The following table shows the por_mpu_m1_ctl lower register bit assignments.

Table 4-1616 por_mpu_por_mpu_m1_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	m1_en	MPU master 1 enable.	RW	1'b0
1:0	m1_action	Indicates action HN* should take if no access permission is granted 2'b00: FUSA interrupt 2'b01: Bus error to the originating bus master 2'b10: Both FUSA interrupt and bus error.	RW	2'b10

por_mpu_m1_prbar0

MPU master 0 programmable base address register 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1410

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

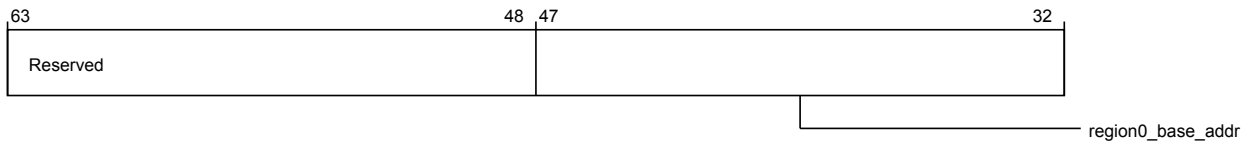


Figure 4-1600 por_mpu_por_mpu_m1_prbar0 (high)

The following table shows the por_mpu_m1_prbar0 higher register bit assignments.

Table 4-1617 por_mpu_por_mpu_m1_prbar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

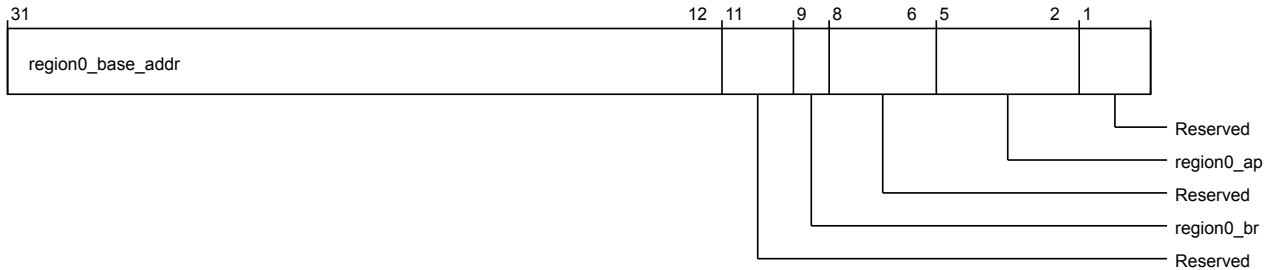


Figure 4-1601 por_mpu_por_mpu_m1_prbar0 (low)

The following table shows the por_mpu_m1_prbar0 lower register bit assignments.

Table 4-1618 por_mpu_por_mpu_m1_prbar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region0_br	Region 0 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region0_ap	Region 0 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar0

MPU master 0 programmable limit address register 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1418

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

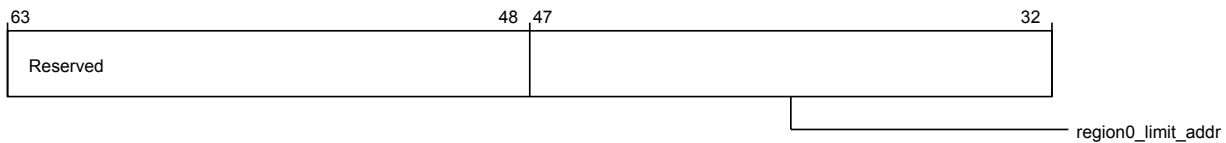


Figure 4-1602 por_mpu_por_mpu_m1_prlar0 (high)

The following table shows the por_mpu_m1_prlar0 higher register bit assignments.

Table 4-1619 por_mpu_por_mpu_m1_prlar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

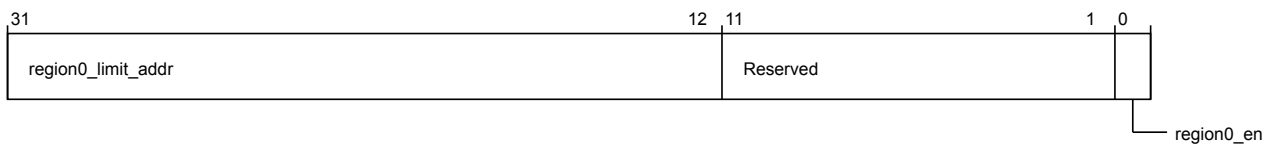


Figure 4-1603 por_mpu_por_mpu_m1_prlar0 (low)

The following table shows the por_mpu_m1_prlar0 lower register bit assignments.

Table 4-1620 por_mpu_por_mpu_m1_prlar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region0_en	Region 0 enable.	RW	1'b0

por_mpu_m1_prbar1

MPU master 0 programmable base address register 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1420

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

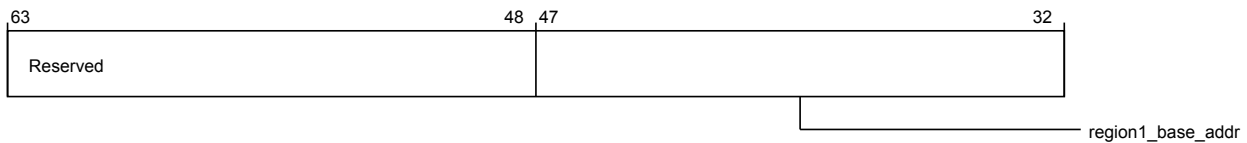


Figure 4-1604 por_mpu_por_mpu_m1_prbar1 (high)

The following table shows the por_mpu_m1_prbar1 higher register bit assignments.

Table 4-1621 por_mpu_por_mpu_m1_prbar1 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region1_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

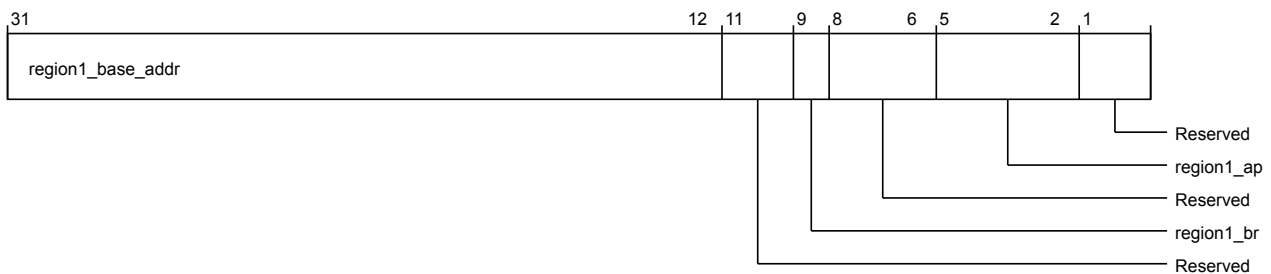


Figure 4-1605 por_mpu_por_mpu_m1_prbar1 (low)

The following table shows the por_mpu_m1_prbar1 lower register bit assignments.

Table 4-1622 por_mpu_por_mpu_m1_prbar1 (low)

Bits	Field name	Description	Type	Reset
31:12	region1_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1622 por_mpu_por_mpu_m1_prbar1 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region1_br	Region 1 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region1_ap	Region 1 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar1

MPU master 0 programmable limit address register 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1428

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

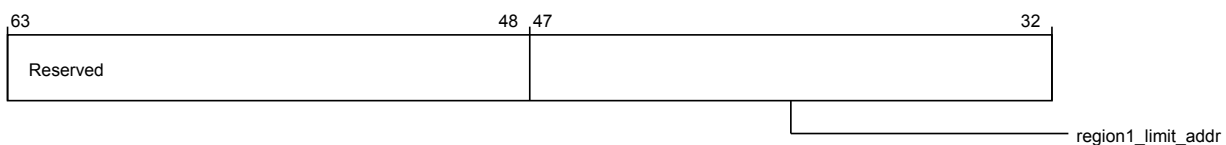


Figure 4-1606 por_mpu_por_mpu_m1_prlar1 (high)

The following table shows the por_mpu_m1_prlar1 higher register bit assignments.

Table 4-1623 por_mpu_por_mpu_m1_prlar1 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region1_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

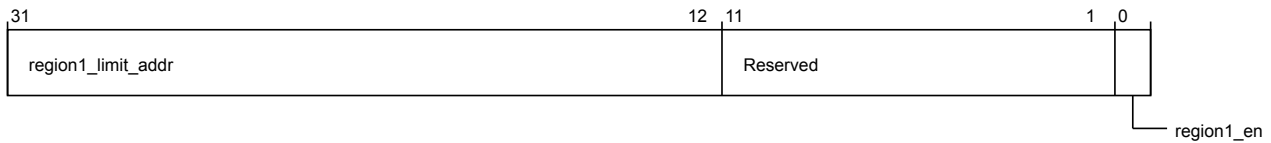


Figure 4-1607 `por_mpu_por_mpu_m1_prlar1` (low)

The following table shows the `por_mpu_m1_prlar1` lower register bit assignments.

Table 4-1624 `por_mpu_por_mpu_m1_prlar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region1_en</code>	Region 1 enable.	RW	1'b0

`por_mpu_m1_prbar2`

MPU master 0 programmable base address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1430

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

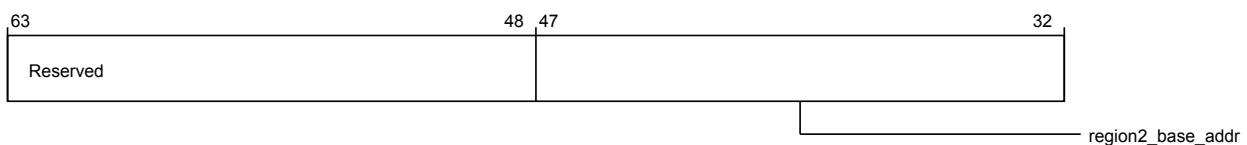


Figure 4-1608 `por_mpu_por_mpu_m1_prbar2` (high)

The following table shows the `por_mpu_m1_prbar2` higher register bit assignments.

Table 4-1625 `por_mpu_por_mpu_m1_prbar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

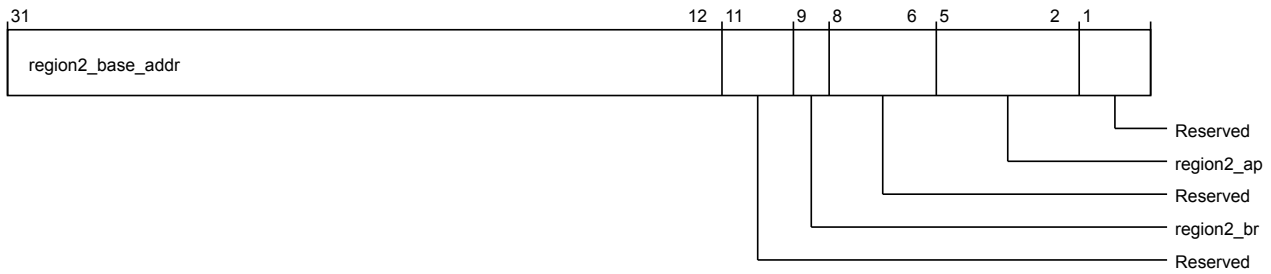


Figure 4-1609 por_mpu_m1_prbar2 (low)

The following table shows the por_mpu_m1_prbar2 lower register bit assignments.

Table 4-1626 por_mpu_m1_prbar2 (low)

Bits	Field name	Description	Type	Reset
31:12	region2_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region2_br	Region 2 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region2_ap	Region 2 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar2

MPU master 0 programmable limit address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1438

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

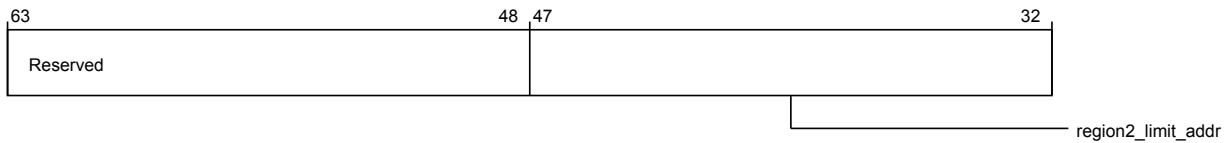


Figure 4-1610 `por_mpu_m1_prlar2` (high)

The following table shows the `por_mpu_m1_prlar2` higher register bit assignments.

Table 4-1627 `por_mpu_m1_prlar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

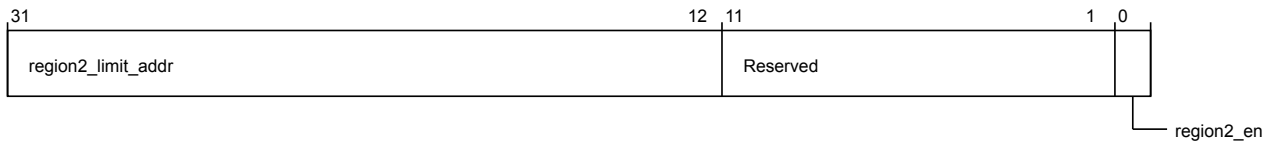


Figure 4-1611 `por_mpu_m1_prlar2` (low)

The following table shows the `por_mpu_m1_prlar2` lower register bit assignments.

Table 4-1628 `por_mpu_m1_prlar2` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region2_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region2_en</code>	Region 2 enable.	RW	1'b0

`por_mpu_m1_prbar3`

MPU master 0 programmable base address register 3.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1440
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

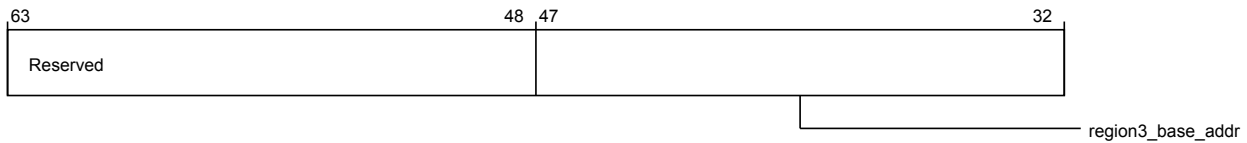


Figure 4-1612 `por_mpu_por_mpu_m1_prbar3` (high)

The following table shows the `por_mpu_m1_prbar3` higher register bit assignments.

Table 4-1629 `por_mpu_por_mpu_m1_prbar3` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

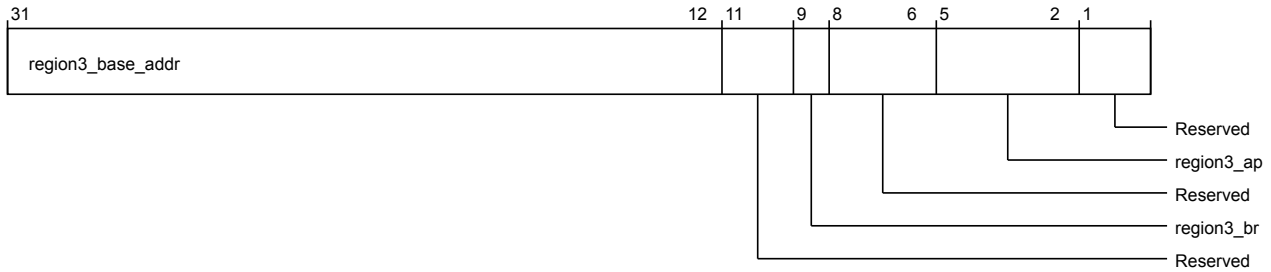


Figure 4-1613 `por_mpu_por_mpu_m1_prbar3` (low)

The following table shows the `por_mpu_m1_prbar3` lower register bit assignments.

Table 4-1630 `por_mpu_por_mpu_m1_prbar3` (low)

Bits	Field name	Description	Type	Reset
31:12	region3_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region3_br	Region 3 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region3_ap	Region 3 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar3

MPU master 0 programmable limit address register 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1448

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

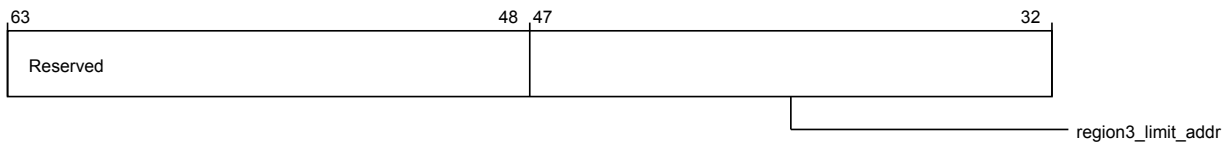


Figure 4-1614 por_mpu_por_mpu_m1_prlar3 (high)

The following table shows the por_mpu_m1_prlar3 higher register bit assignments.

Table 4-1631 por_mpu_por_mpu_m1_prlar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

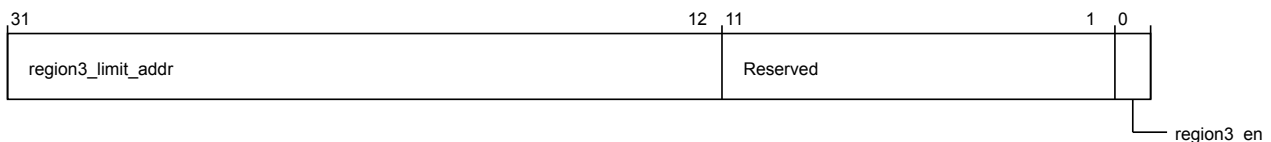


Figure 4-1615 por_mpu_por_mpu_m1_prlar3 (low)

The following table shows the por_mpu_m1_prlar3 lower register bit assignments.

Table 4-1632 por_mpu_por_mpu_m1_prlar3 (low)

Bits	Field name	Description	Type	Reset
31:12	region3_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region3_en	Region 3 enable.	RW	1'b0

por_mpu_m1_prbar4

MPU master 0 programmable base address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1450

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

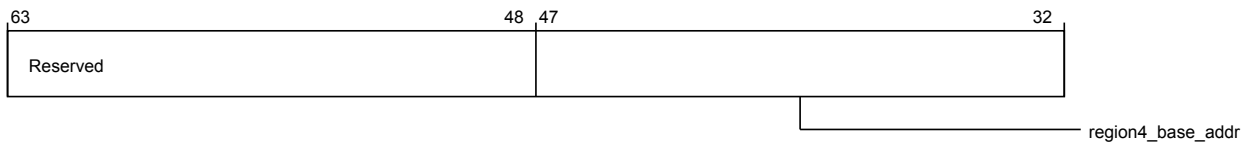


Figure 4-1616 por_mpu_por_mpu_m1_prbar4 (high)

The following table shows the por_mpu_m1_prbar4 higher register bit assignments.

Table 4-1633 por_mpu_por_mpu_m1_prbar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

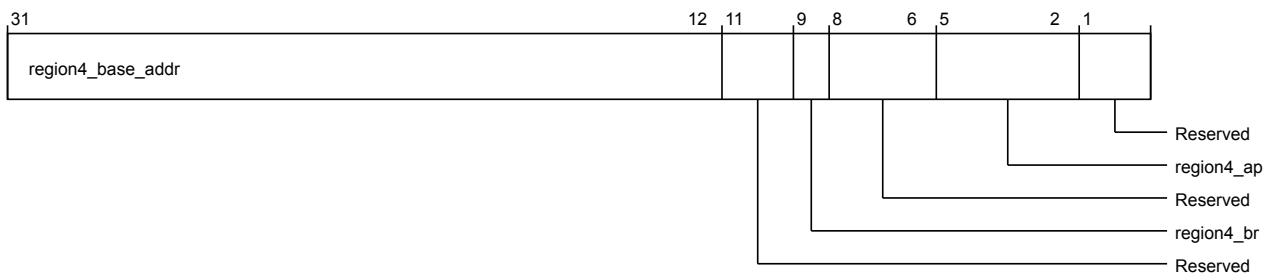


Figure 4-1617 por_mpu_por_mpu_m1_prbar4 (low)

The following table shows the por_mpu_m1_prbar4 lower register bit assignments.

Table 4-1634 por_mpu_por_mpu_m1_prbar4 (low)

Bits	Field name	Description	Type	Reset
31:12	region4_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1634 por_mpu_por_mpu_m1_prbar4 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region4_br	Region 4 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region4_ap	Region 4 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar4

MPU master 0 programmable limit address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1458

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

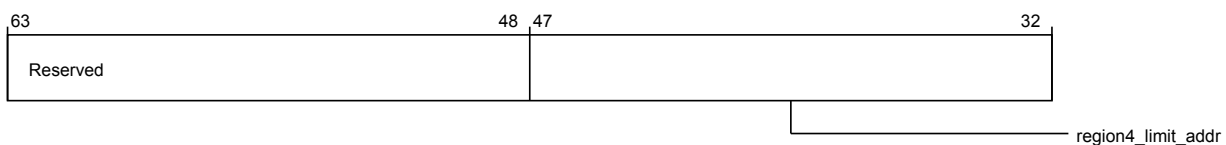


Figure 4-1618 por_mpu_por_mpu_m1_prlar4 (high)

The following table shows the por_mpu_m1_prlar4 higher register bit assignments.

Table 4-1635 por_mpu_por_mpu_m1_prlar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

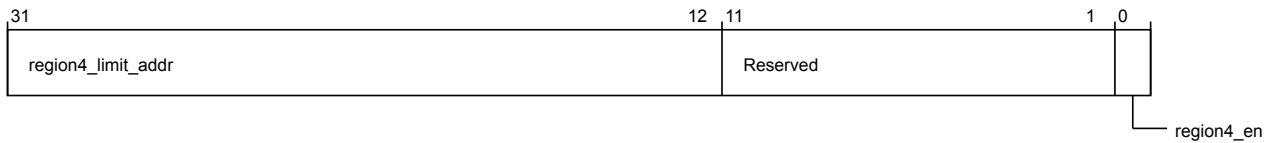


Figure 4-1619 `por_mpu_por_mpu_m1_prlar4` (low)

The following table shows the `por_mpu_m1_prlar4` lower register bit assignments.

Table 4-1636 `por_mpu_por_mpu_m1_prlar4` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region4_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region4_en</code>	Region 4 enable.	RW	1'b0

`por_mpu_m1_prbar5`

MPU master 0 programmable base address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1460

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

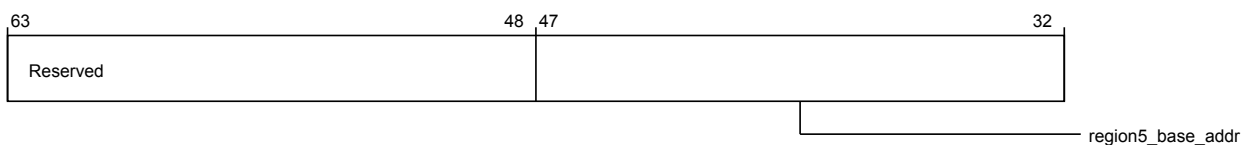


Figure 4-1620 `por_mpu_por_mpu_m1_prbar5` (high)

The following table shows the `por_mpu_m1_prbar5` higher register bit assignments.

Table 4-1637 `por_mpu_por_mpu_m1_prbar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

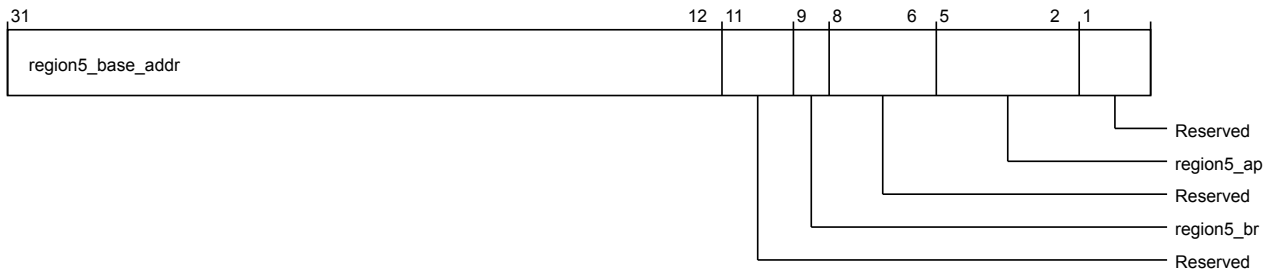


Figure 4-1621 por_mpu_por_mpu_m1_prbar5 (low)

The following table shows the por_mpu_m1_prbar5 lower register bit assignments.

Table 4-1638 por_mpu_por_mpu_m1_prbar5 (low)

Bits	Field name	Description	Type	Reset
31:12	region5_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region5_br	Region 5 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region5_ap	Region 5 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar5

MPU master 0 programmable limit address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1468

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

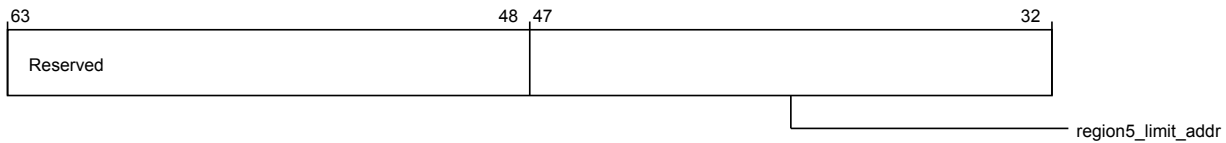


Figure 4-1622 `por_mpu_m1_prlar5` (high)

The following table shows the `por_mpu_m1_prlar5` higher register bit assignments.

Table 4-1639 `por_mpu_m1_prlar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

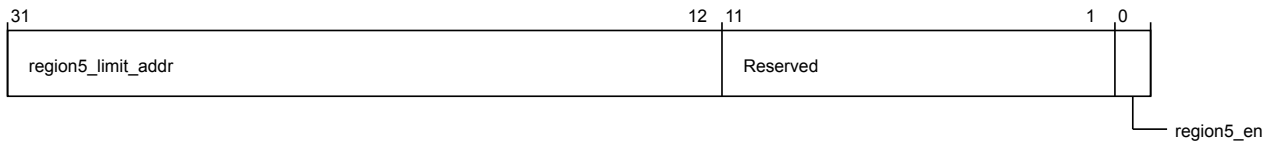


Figure 4-1623 `por_mpu_m1_prlar5` (low)

The following table shows the `por_mpu_m1_prlar5` lower register bit assignments.

Table 4-1640 `por_mpu_m1_prlar5` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region5_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region5_en</code>	Region 5 enable.	RW	1'b0

`por_mpu_m1_prbar6`

MPU master 0 programmable base address register 6.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1470
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

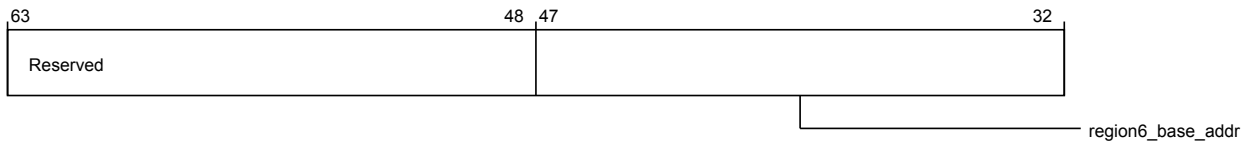


Figure 4-1624 por_mpu_por_mpu_m1_prbar6 (high)

The following table shows the por_mpu_m1_prbar6 higher register bit assignments.

Table 4-1641 por_mpu_por_mpu_m1_prbar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

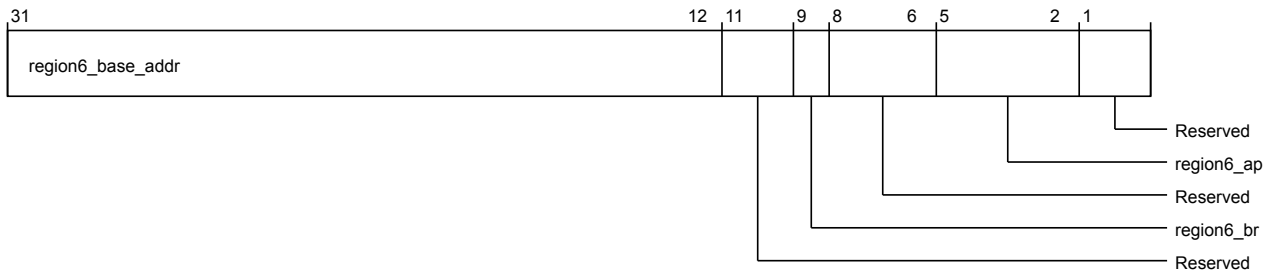


Figure 4-1625 por_mpu_por_mpu_m1_prbar6 (low)

The following table shows the por_mpu_m1_prbar6 lower register bit assignments.

Table 4-1642 por_mpu_por_mpu_m1_prbar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region6_br	Region 6 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region6_ap	Region 6 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar6

MPU master 0 programmable limit address register 6.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1478

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

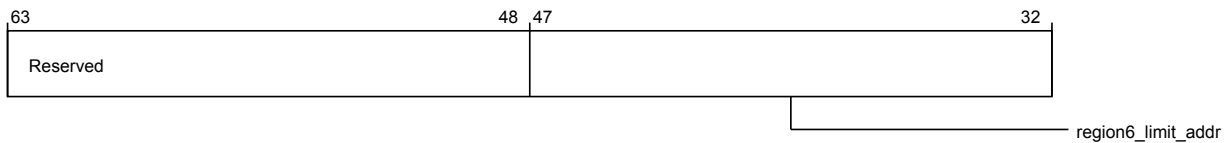


Figure 4-1626 por_mpu_por_mpu_m1_prlar6 (high)

The following table shows the por_mpu_m1_prlar6 higher register bit assignments.

Table 4-1643 por_mpu_por_mpu_m1_prlar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

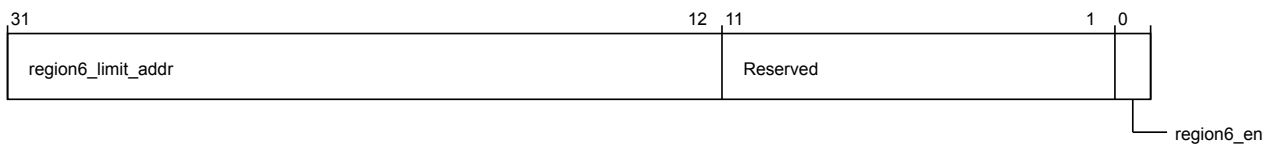


Figure 4-1627 por_mpu_por_mpu_m1_prlar6 (low)

The following table shows the por_mpu_m1_prlar6 lower register bit assignments.

Table 4-1644 por_mpu_por_mpu_m1_prlar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region6_en	Region 6 enable.	RW	1'b0

por_mpu_m1_prbar7

MPU master 0 programmable base address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1480

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

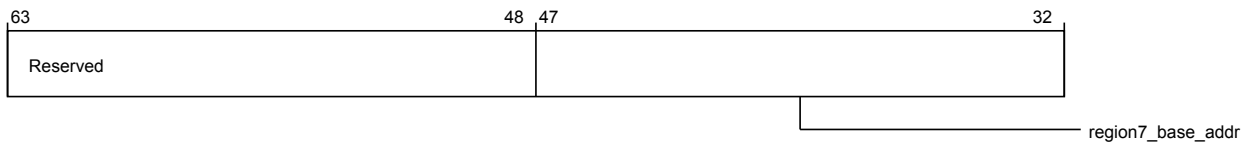


Figure 4-1628 `por_mpu_m1_prbar7` (high)

The following table shows the `por_mpu_m1_prbar7` higher register bit assignments.

Table 4-1645 `por_mpu_m1_prbar7` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

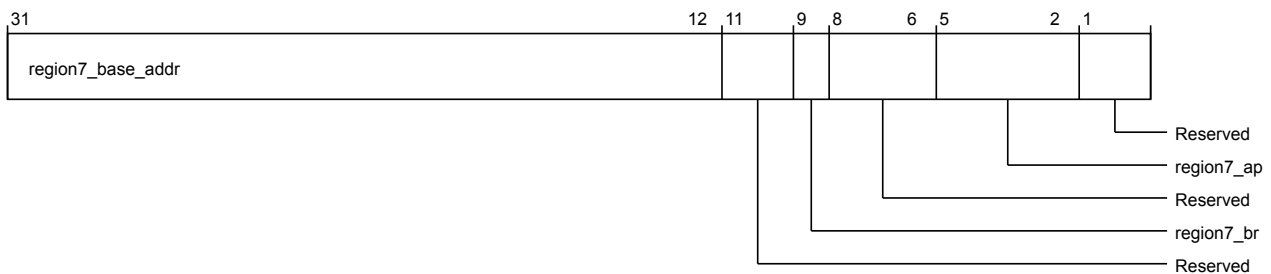


Figure 4-1629 `por_mpu_m1_prbar7` (low)

The following table shows the `por_mpu_m1_prbar7` lower register bit assignments.

Table 4-1646 `por_mpu_m1_prbar7` (low)

Bits	Field name	Description	Type	Reset
31:12	region7_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1646 por_mpu_por_mpu_m1_prbar7 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region7_br	Region 7 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region7_ap	Region 7 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar7

MPU master 0 programmable limit address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1488

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

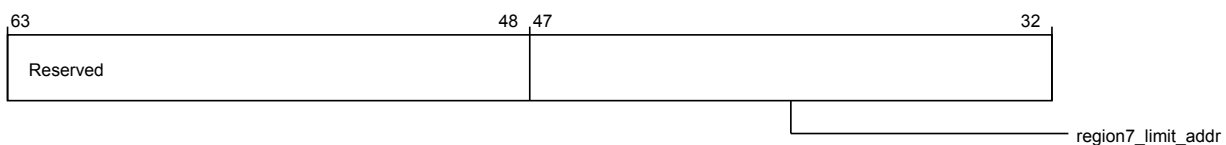


Figure 4-1630 por_mpu_por_mpu_m1_prlar7 (high)

The following table shows the por_mpu_m1_prlar7 higher register bit assignments.

Table 4-1647 por_mpu_por_mpu_m1_prlar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

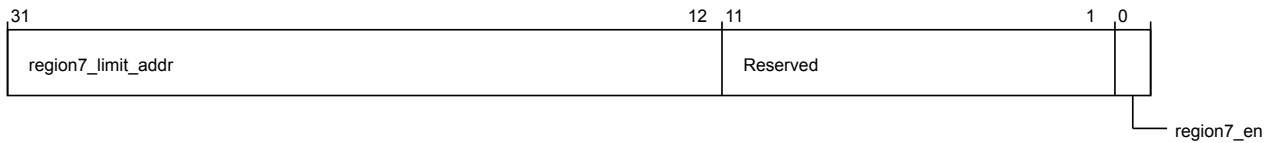


Figure 4-1631 `por_mpu_por_mpu_m1_prlar7` (low)

The following table shows the `por_mpu_m1_prlar7` lower register bit assignments.

Table 4-1648 `por_mpu_por_mpu_m1_prlar7` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region7_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region7_en</code>	Region 7 enable.	RW	1'b0

`por_mpu_m1_prbar8`

MPU master 0 programmable base address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1490

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

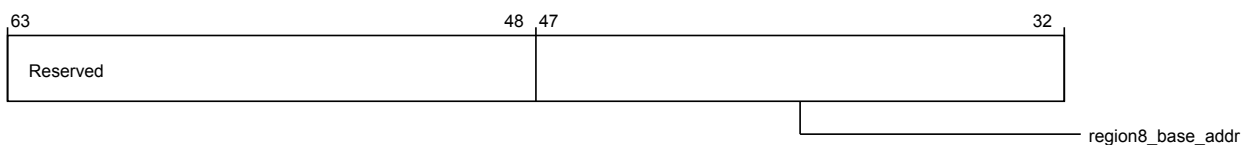


Figure 4-1632 `por_mpu_por_mpu_m1_prbar8` (high)

The following table shows the `por_mpu_m1_prbar8` higher register bit assignments.

Table 4-1649 `por_mpu_por_mpu_m1_prbar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

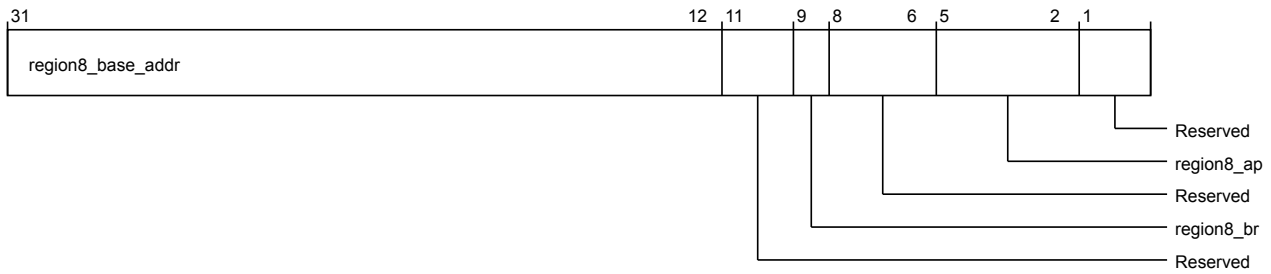


Figure 4-1633 por_mpu_por_mpu_m1_prbar8 (low)

The following table shows the por_mpu_m1_prbar8 lower register bit assignments.

Table 4-1650 por_mpu_por_mpu_m1_prbar8 (low)

Bits	Field name	Description	Type	Reset
31:12	region8_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region8_br	Region 8 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region8_ap	Region 8 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar8

MPU master 0 programmable limit address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1498

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

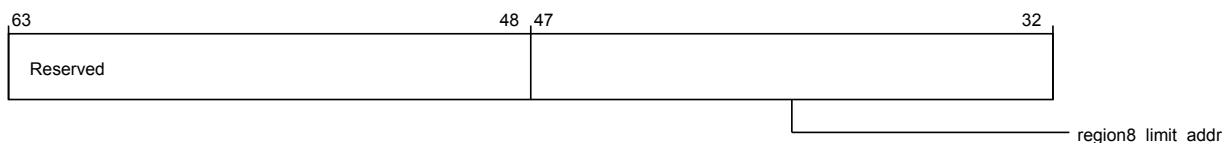


Figure 4-1634 `por_mpu_m1_prlar8` (high)

The following table shows the `por_mpu_m1_prlar8` higher register bit assignments.

Table 4-1651 `por_mpu_m1_prlar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

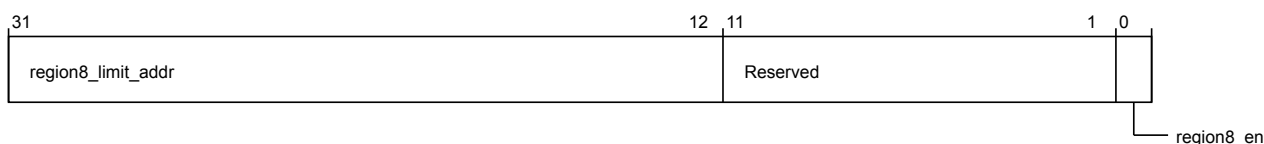


Figure 4-1635 `por_mpu_m1_prlar8` (low)

The following table shows the `por_mpu_m1_prlar8` lower register bit assignments.

Table 4-1652 `por_mpu_m1_prlar8` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region8_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region8_en</code>	Region 8 enable.	RW	1'b0

`por_mpu_m1_prbar9`

MPU master 0 programmable base address register 9.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h14A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

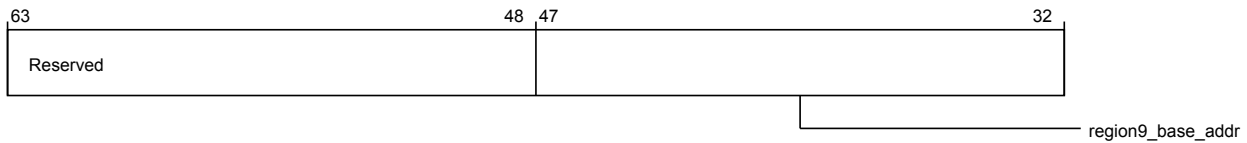


Figure 4-1636 por_mpu_por_mpu_m1_prbar9 (high)

The following table shows the por_mpu_m1_prbar9 higher register bit assignments.

Table 4-1653 por_mpu_por_mpu_m1_prbar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

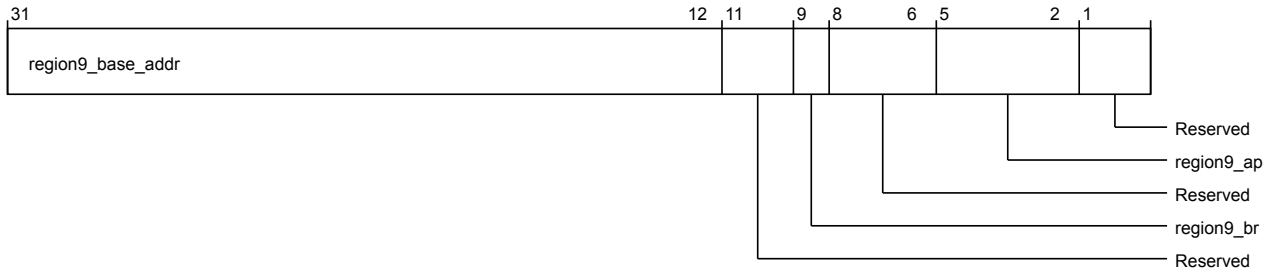


Figure 4-1637 por_mpu_por_mpu_m1_prbar9 (low)

The following table shows the por_mpu_m1_prbar9 lower register bit assignments.

Table 4-1654 por_mpu_por_mpu_m1_prbar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region9_br	Region 9 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region9_ap	Region 9 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar9

MPU master 0 programmable limit address register 9.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h14A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

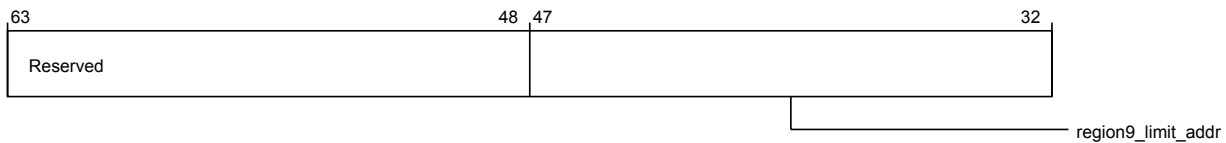


Figure 4-1638 por_mpu_por_mpu_m1_prlar9 (high)

The following table shows the por_mpu_m1_prlar9 higher register bit assignments.

Table 4-1655 por_mpu_por_mpu_m1_prlar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

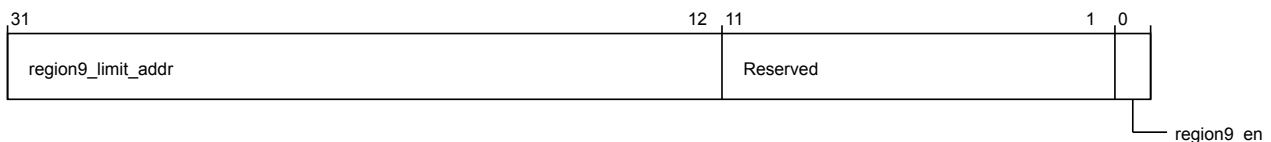


Figure 4-1639 por_mpu_por_mpu_m1_prlar9 (low)

The following table shows the por_mpu_m1_prlar9 lower register bit assignments.

Table 4-1656 por_mpu_por_mpu_m1_prlar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region9_en	Region 9 enable.	RW	1'b0

por_mpu_m1_prbar10

MPU master 0 programmable base address register 10.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h14B0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

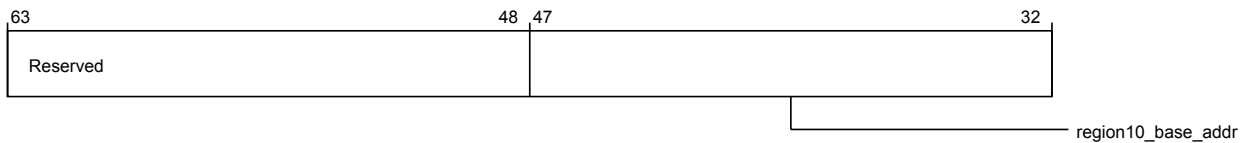


Figure 4-1640 por_mpu_por_mpu_m1_prbar10 (high)

The following table shows the por_mpu_m1_prbar10 higher register bit assignments.

Table 4-1657 por_mpu_por_mpu_m1_prbar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_base_addr	Bits [47:2] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

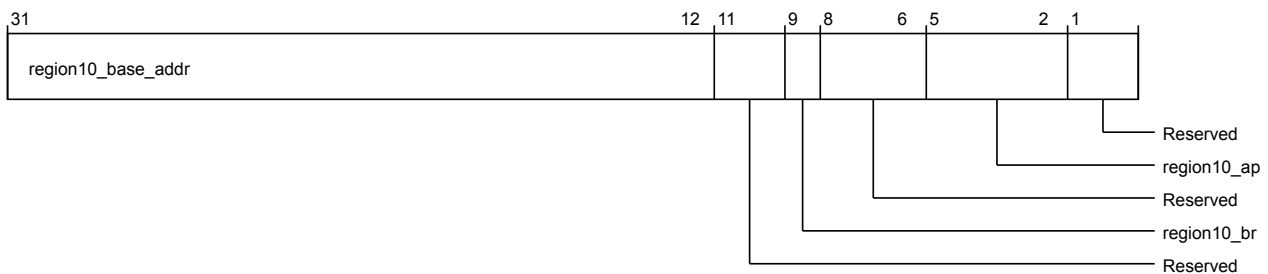


Figure 4-1641 por_mpu_por_mpu_m1_prbar10 (low)

The following table shows the por_mpu_m1_prbar10 lower register bit assignments.

Table 4-1658 por_mpu_por_mpu_m1_prbar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1658 por_mpu_por_mpu_m1_prbar10 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region10_br	Region 10 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region10_ap	Region 10 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar10

MPU master 0 programmable limit address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h14B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

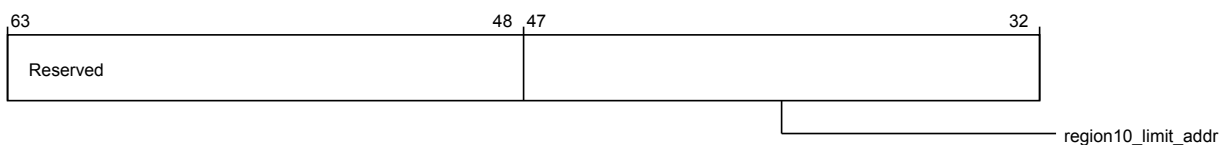


Figure 4-1642 por_mpu_por_mpu_m1_prlar10 (high)

The following table shows the por_mpu_m1_prlar10 higher register bit assignments.

Table 4-1659 por_mpu_por_mpu_m1_prlar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

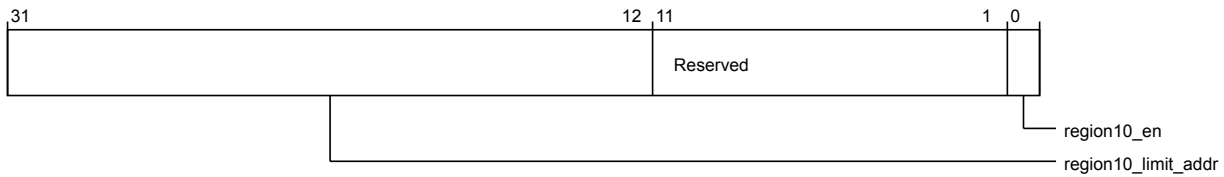


Figure 4-1643 por_mpu_por_mpu_m1_prlar10 (low)

The following table shows the por_mpu_m1_prlar10 lower register bit assignments.

Table 4-1660 por_mpu_por_mpu_m1_prlar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region10_en	Region 10 enable.	RW	1'b0

por_mpu_m1_prbar11

MPU master 0 programmable base address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h14C0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

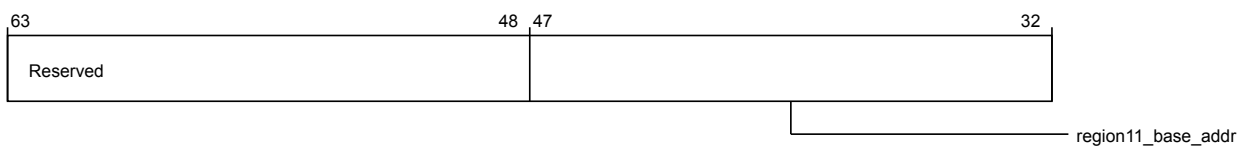


Figure 4-1644 por_mpu_por_mpu_m1_prbar11 (high)

The following table shows the por_mpu_m1_prbar11 higher register bit assignments.

Table 4-1661 por_mpu_por_mpu_m1_prbar11 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

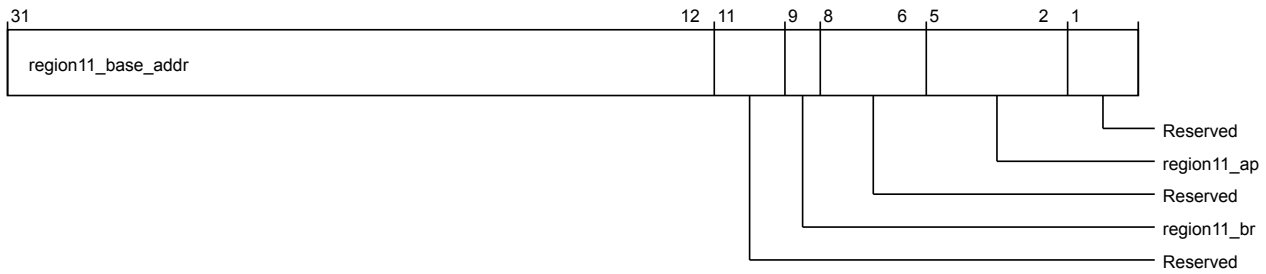


Figure 4-1645 `por_mpu_por_mpu_m1_prbar11` (low)

The following table shows the `por_mpu_m1_prbar11` lower register bit assignments.

Table 4-1662 `por_mpu_por_mpu_m1_prbar11` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region11_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region11_br</code>	Region 11 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region11_ap</code>	Region 11 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m1_prlar11`

MPU master 0 programmable limit address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h14C8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

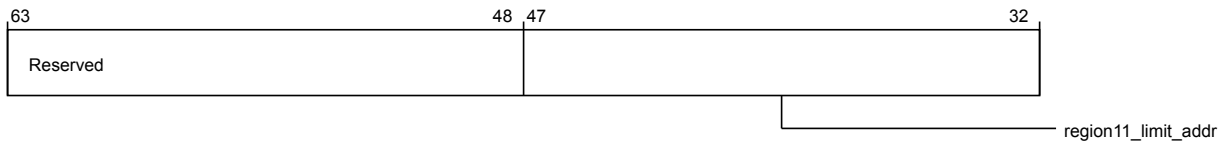


Figure 4-1646 por_mpu_por_mpu_m1_prlar11 (high)

The following table shows the por_mpu_m1_prlar11 higher register bit assignments.

Table 4-1663 por_mpu_por_mpu_m1_prlar11 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

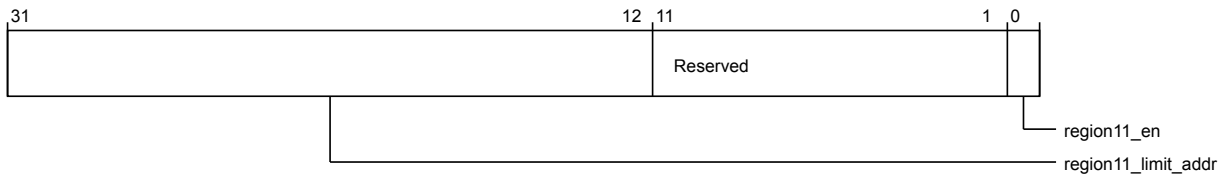


Figure 4-1647 por_mpu_por_mpu_m1_prlar11 (low)

The following table shows the por_mpu_m1_prlar11 lower register bit assignments.

Table 4-1664 por_mpu_por_mpu_m1_prlar11 (low)

Bits	Field name	Description	Type	Reset
31:12	region11_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region11_en	Region 11 enable.	RW	1'b0

por_mpu_m1_prbar12

MPU master 0 programmable base address register 12.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h14D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

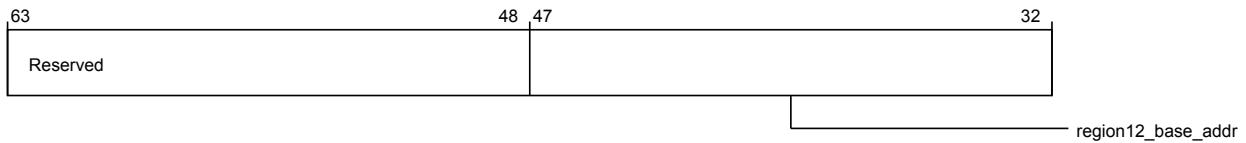


Figure 4-1648 por_mpu_por_mpu_m1_prbar12 (high)

The following table shows the por_mpu_m1_prbar12 higher register bit assignments.

Table 4-1665 por_mpu_por_mpu_m1_prbar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

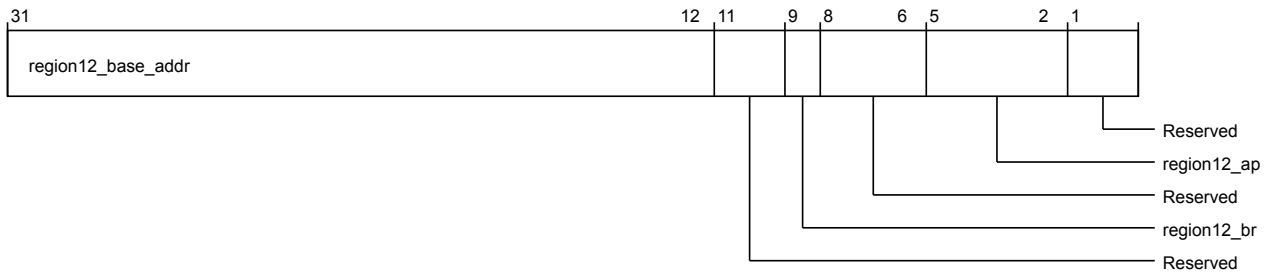


Figure 4-1649 por_mpu_por_mpu_m1_prbar12 (low)

The following table shows the por_mpu_m1_prbar12 lower register bit assignments.

Table 4-1666 por_mpu_por_mpu_m1_prbar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region12_br	Region 12 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region12_ap	Region 12 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar12

MPU master 0 programmable limit address register 12.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h14D8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

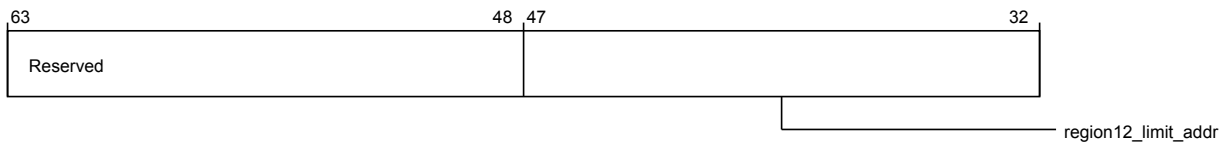


Figure 4-1650 por_mpu_por_mpu_m1_prlar12 (high)

The following table shows the por_mpu_m1_prlar12 higher register bit assignments.

Table 4-1667 por_mpu_por_mpu_m1_prlar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

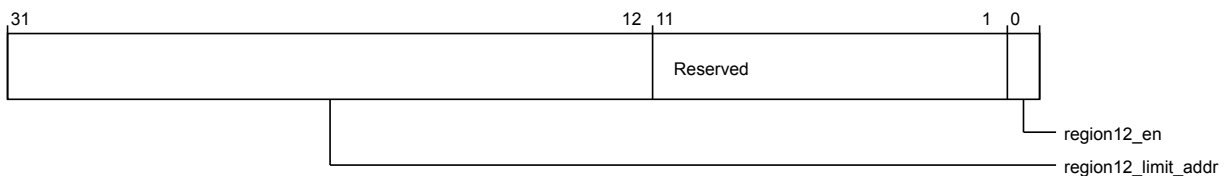


Figure 4-1651 por_mpu_por_mpu_m1_prlar12 (low)

The following table shows the por_mpu_m1_prlar12 lower register bit assignments.

Table 4-1668 por_mpu_por_mpu_m1_prlar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region12_en	Region 12 enable.	RW	1'b0

por_mpu_m1_prbar13

MPU master 0 programmable base address register 13.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h14E0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

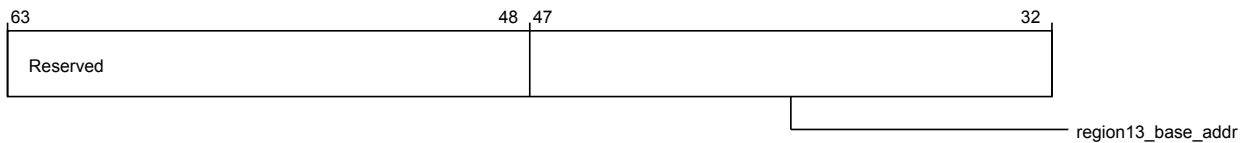


Figure 4-1652 por_mpu_por_mpu_m1_prbar13 (high)

The following table shows the por_mpu_m1_prbar13 higher register bit assignments.

Table 4-1669 por_mpu_por_mpu_m1_prbar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

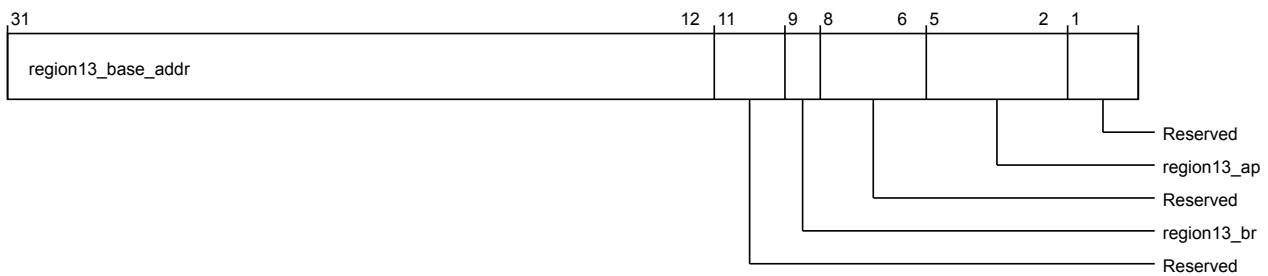


Figure 4-1653 por_mpu_por_mpu_m1_prbar13 (low)

The following table shows the por_mpu_m1_prbar13 lower register bit assignments.

Table 4-1670 por_mpu_por_mpu_m1_prbar13 (low)

Bits	Field name	Description	Type	Reset
31:12	region13_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1670 por_mpu_por_mpu_m1_prbar13 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region13_br	Region 13 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region13_ap	Region 13 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar13

MPU master 0 programmable limit address register 13.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h14E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

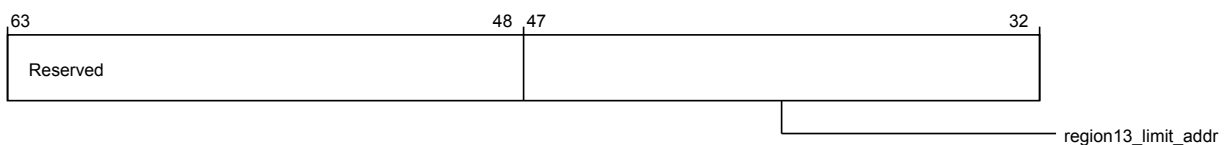


Figure 4-1654 por_mpu_por_mpu_m1_prlar13 (high)

The following table shows the por_mpu_m1_prlar13 higher register bit assignments.

Table 4-1671 por_mpu_por_mpu_m1_prlar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

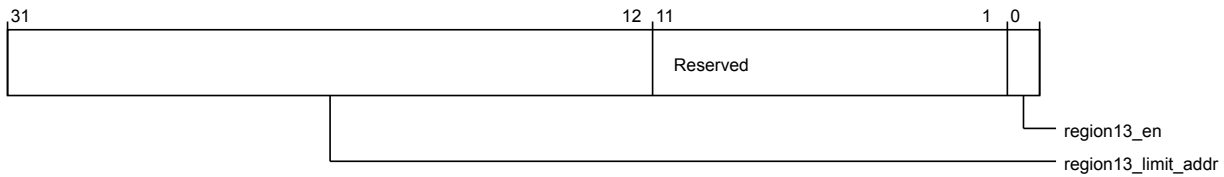


Figure 4-1655 `por_mpu_por_mpu_m1_prlar13` (low)

The following table shows the `por_mpu_m1_prlar13` lower register bit assignments.

Table 4-1672 `por_mpu_por_mpu_m1_prlar13` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region13_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region13_en</code>	Region 13 enable.	RW	1'b0

`por_mpu_m1_prbar14`

MPU master 0 programmable base address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h14F0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

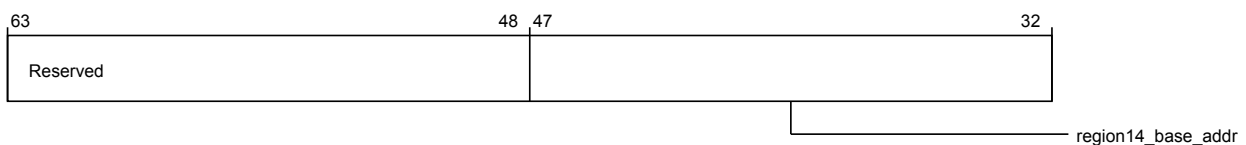


Figure 4-1656 `por_mpu_por_mpu_m1_prbar14` (high)

The following table shows the `por_mpu_m1_prbar14` higher register bit assignments.

Table 4-1673 `por_mpu_por_mpu_m1_prbar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region14_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

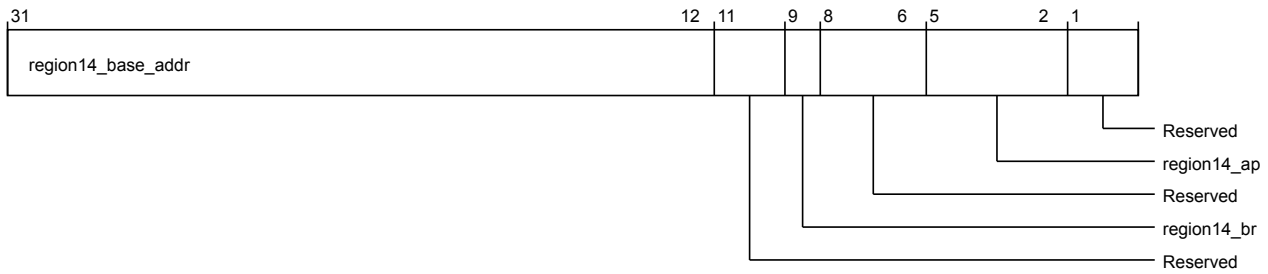


Figure 4-1657 por_mpu_m1_prbar14 (low)

The following table shows the por_mpu_m1_prbar14 lower register bit assignments.

Table 4-1674 por_mpu_m1_prbar14 (low)

Bits	Field name	Description	Type	Reset
31:12	region14_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region14_br	Region 14 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region14_ap	Region 14 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar14

MPU master 0 programmable limit address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h14F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

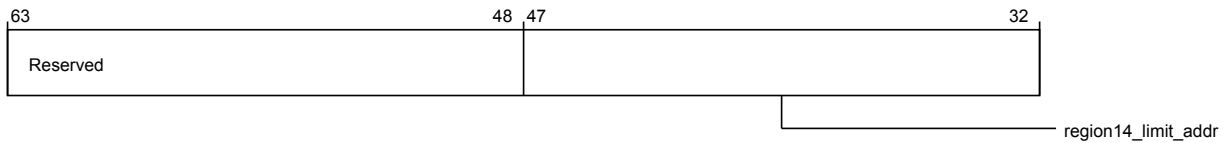


Figure 4-1658 por_mpu_m1_prlar14 (high)

The following table shows the por_mpu_m1_prlar14 higher register bit assignments.

Table 4-1675 por_mpu_m1_prlar14 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region14_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

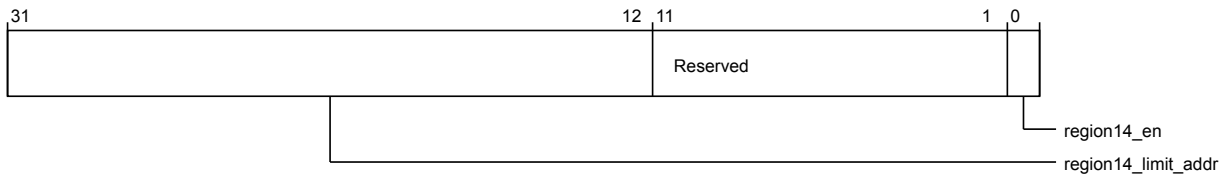


Figure 4-1659 por_mpu_m1_prlar14 (low)

The following table shows the por_mpu_m1_prlar14 lower register bit assignments.

Table 4-1676 por_mpu_m1_prlar14 (low)

Bits	Field name	Description	Type	Reset
31:12	region14_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region14_en	Region 14 enable.	RW	1'b0

por_mpu_m1_prbar15

MPU master 0 programmable base address register 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1500
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

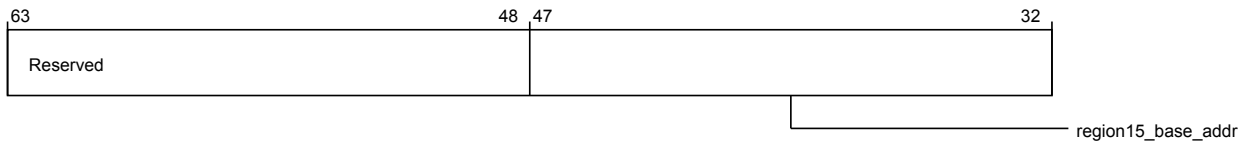


Figure 4-1660 `por_mpu_por_mpu_m1_prbar15` (high)

The following table shows the `por_mpu_m1_prbar15` higher register bit assignments.

Table 4-1677 `por_mpu_por_mpu_m1_prbar15` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

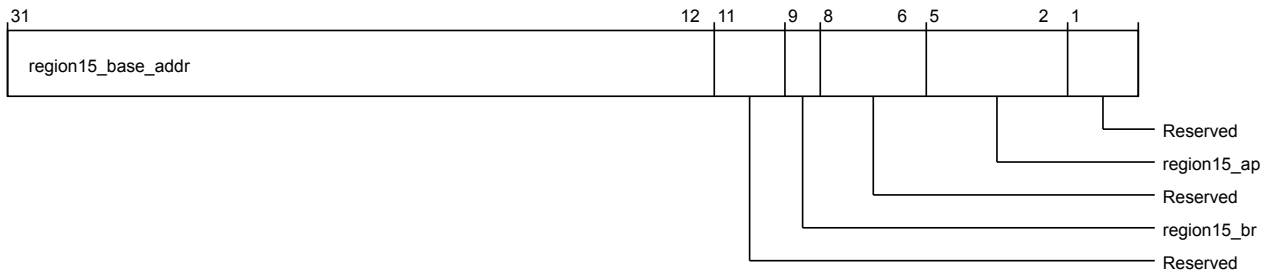


Figure 4-1661 `por_mpu_por_mpu_m1_prbar15` (low)

The following table shows the `por_mpu_m1_prbar15` lower register bit assignments.

Table 4-1678 `por_mpu_por_mpu_m1_prbar15` (low)

Bits	Field name	Description	Type	Reset
31:12	region15_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region15_br	Region 15 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region15_ap	Region 15 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar15

MPU master 0 programmable limit address register 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1508

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

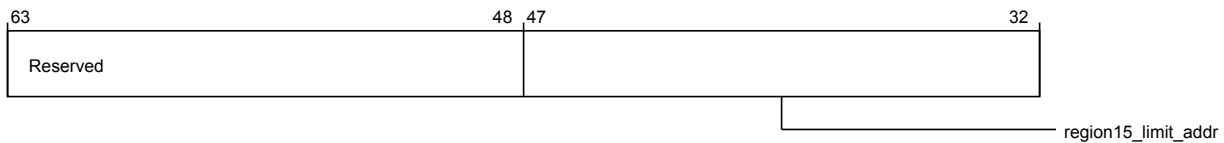


Figure 4-1662 por_mpu_por_mpu_m1_prlar15 (high)

The following table shows the por_mpu_m1_prlar15 higher register bit assignments.

Table 4-1679 por_mpu_por_mpu_m1_prlar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

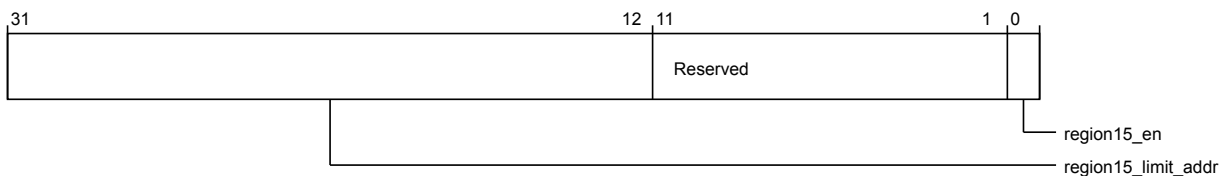


Figure 4-1663 por_mpu_por_mpu_m1_prlar15 (low)

The following table shows the por_mpu_m1_prlar15 lower register bit assignments.

Table 4-1680 por_mpu_por_mpu_m1_prlar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region15_en	Region 15 enable.	RW	1'b0

por_mpu_m1_prbar16

MPU master 0 programmable base address register 16.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1510
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

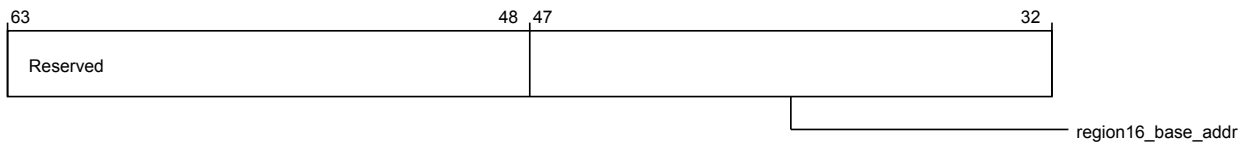


Figure 4-1664 por_mpu_por_mpu_m1_prbar16 (high)

The following table shows the por_mpu_m1_prbar16 higher register bit assignments.

Table 4-1681 por_mpu_por_mpu_m1_prbar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

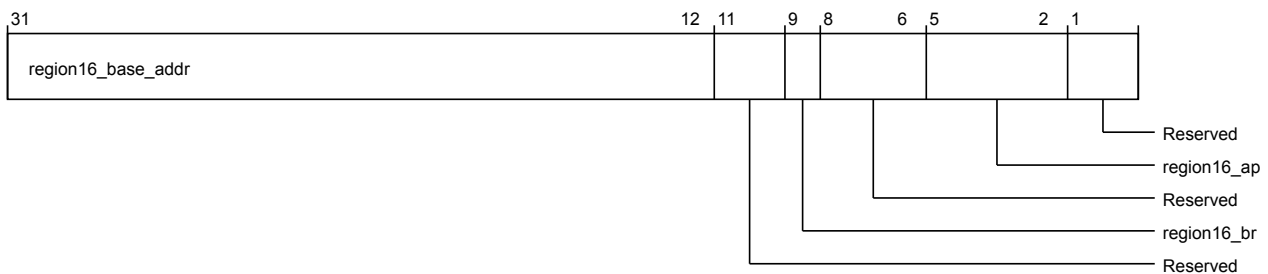


Figure 4-1665 por_mpu_por_mpu_m1_prbar16 (low)

The following table shows the por_mpu_m1_prbar16 lower register bit assignments.

Table 4-1682 por_mpu_por_mpu_m1_prbar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1682 por_mpu_por_mpu_m1_prbar16 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region16_br	Region 16 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region16_ap	Region 16 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar16

MPU master 0 programmable limit address register 16.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1518

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

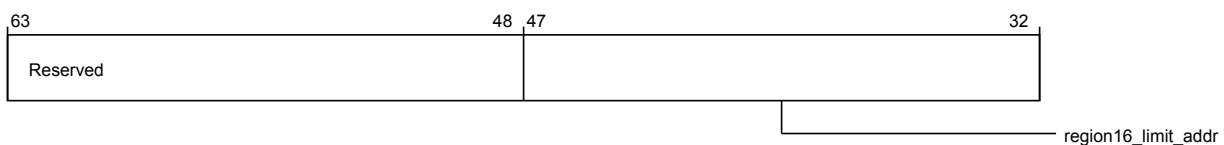


Figure 4-1666 por_mpu_por_mpu_m1_prlar16 (high)

The following table shows the por_mpu_m1_prlar16 higher register bit assignments.

Table 4-1683 por_mpu_por_mpu_m1_prlar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

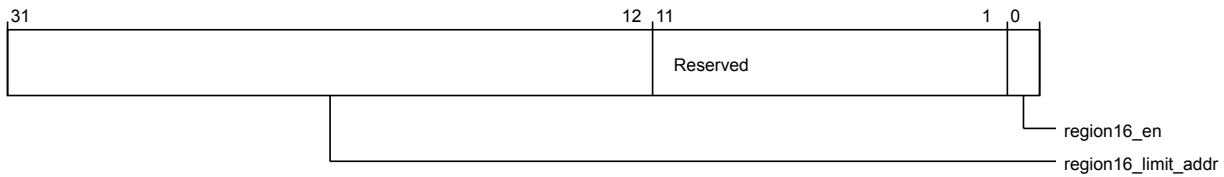


Figure 4-1667 por_mpu_por_mpu_m1_prlar16 (low)

The following table shows the por_mpu_m1_prlar16 lower register bit assignments.

Table 4-1684 por_mpu_por_mpu_m1_prlar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region16_en	Region 16 enable.	RW	1'b0

por_mpu_m1_prbar17

MPU master 0 programmable base address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1520

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

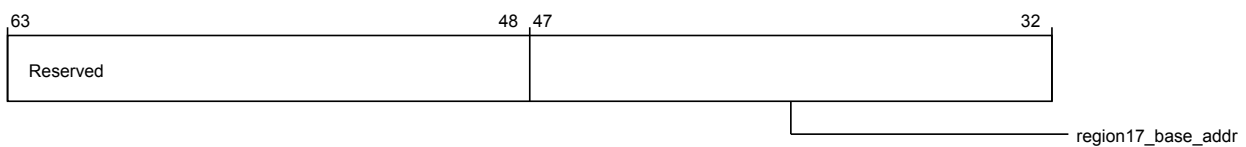


Figure 4-1668 por_mpu_por_mpu_m1_prbar17 (high)

The following table shows the por_mpu_m1_prbar17 higher register bit assignments.

Table 4-1685 por_mpu_por_mpu_m1_prbar17 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

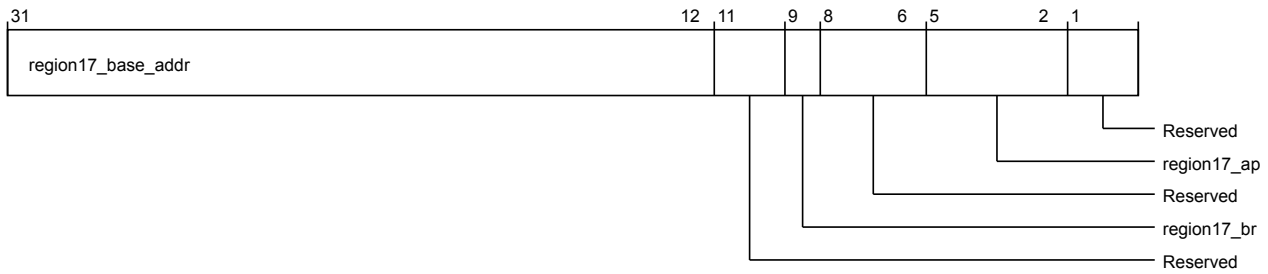


Figure 4-1669 por_mpu_por_mpu_m1_prbar17 (low)

The following table shows the por_mpu_m1_prbar17 lower register bit assignments.

Table 4-1686 por_mpu_por_mpu_m1_prbar17 (low)

Bits	Field name	Description	Type	Reset
31:12	region17_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region17_br	Region 17 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region17_ap	Region 17 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar17

MPU master 0 programmable limit address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1528

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

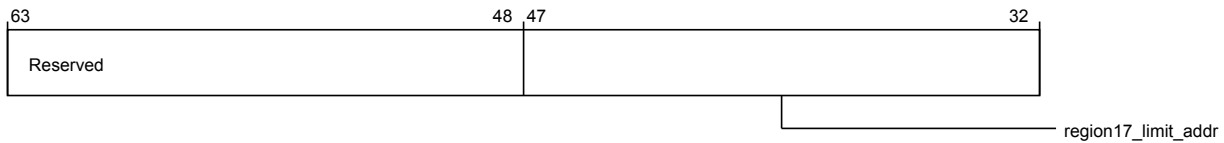


Figure 4-1670 `por_mpu_m1_prlar17` (high)

The following table shows the `por_mpu_m1_prlar17` higher register bit assignments.

Table 4-1687 `por_mpu_m1_prlar17` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

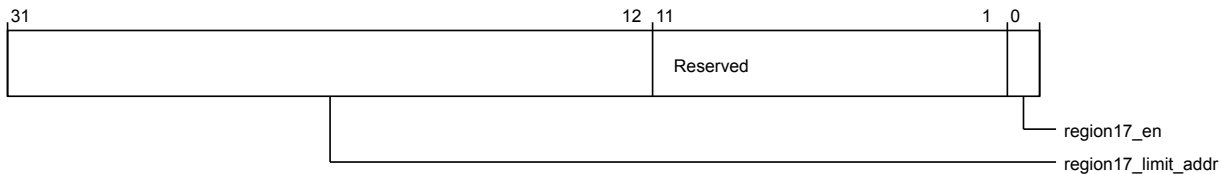


Figure 4-1671 `por_mpu_m1_prlar17` (low)

The following table shows the `por_mpu_m1_prlar17` lower register bit assignments.

Table 4-1688 `por_mpu_m1_prlar17` (low)

Bits	Field name	Description	Type	Reset
31:12	region17_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region17_en	Region 17 enable.	RW	1'b0

`por_mpu_m1_prbar18`

MPU master 0 programmable base address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1530
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

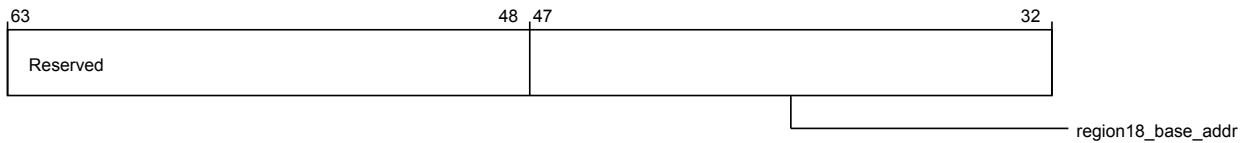


Figure 4-1672 por_mpu_por_mpu_m1_prbar18 (high)

The following table shows the por_mpu_m1_prbar18 higher register bit assignments.

Table 4-1689 por_mpu_por_mpu_m1_prbar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

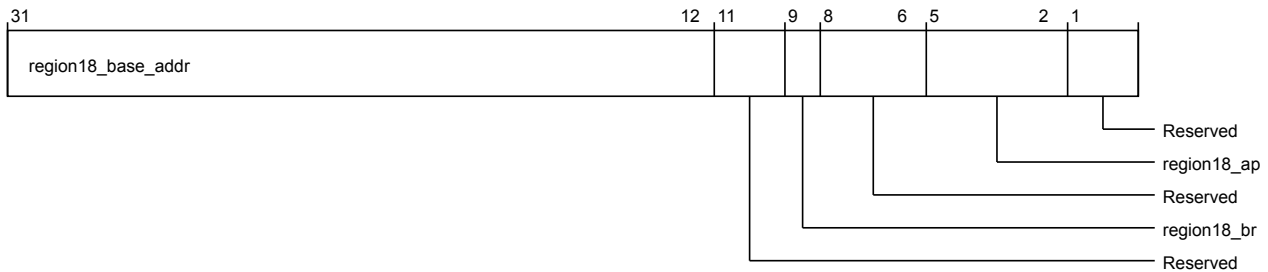


Figure 4-1673 por_mpu_por_mpu_m1_prbar18 (low)

The following table shows the por_mpu_m1_prbar18 lower register bit assignments.

Table 4-1690 por_mpu_por_mpu_m1_prbar18 (low)

Bits	Field name	Description	Type	Reset
31:12	region18_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region18_br	Region 18 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region18_ap	Region 18 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar18

MPU master 0 programmable limit address register 18.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1538

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

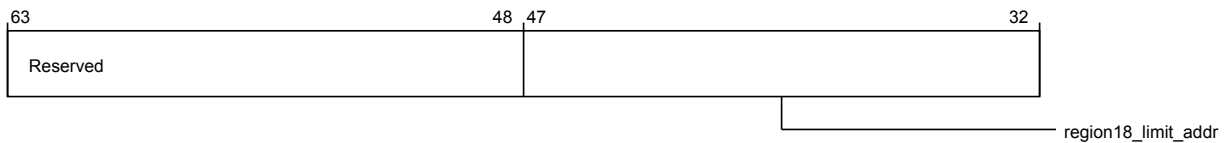


Figure 4-1674 por_mpu_por_mpu_m1_prlar18 (high)

The following table shows the por_mpu_m1_prlar18 higher register bit assignments.

Table 4-1691 por_mpu_por_mpu_m1_prlar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

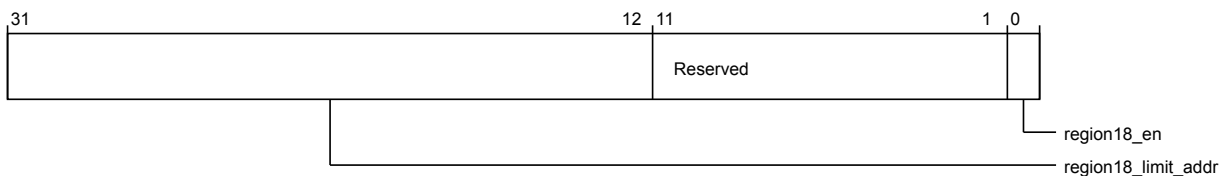


Figure 4-1675 por_mpu_por_mpu_m1_prlar18 (low)

The following table shows the por_mpu_m1_prlar18 lower register bit assignments.

Table 4-1692 por_mpu_por_mpu_m1_prlar18 (low)

Bits	Field name	Description	Type	Reset
31:12	region18_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region18_en	Region 18 enable.	RW	1'b0

por_mpu_m1_prbar19

MPU master 0 programmable base address register 19.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1540
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

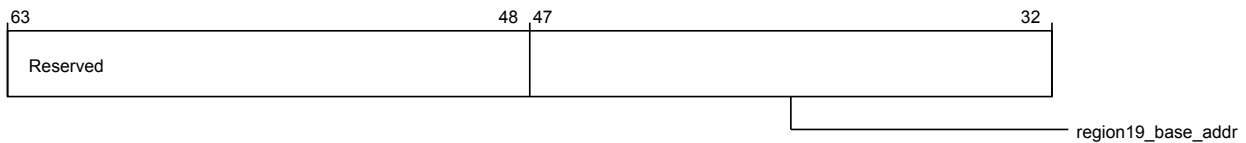


Figure 4-1676 por_mpu_por_mpu_m1_prbar19 (high)

The following table shows the por_mpu_m1_prbar19 higher register bit assignments.

Table 4-1693 por_mpu_por_mpu_m1_prbar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

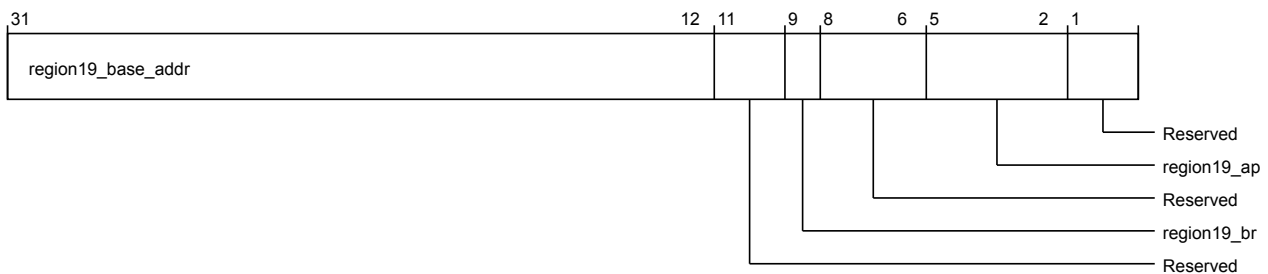


Figure 4-1677 por_mpu_por_mpu_m1_prbar19 (low)

The following table shows the por_mpu_m1_prbar19 lower register bit assignments.

Table 4-1694 por_mpu_por_mpu_m1_prbar19 (low)

Bits	Field name	Description	Type	Reset
31:12	region19_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1694 por_mpu_por_mpu_m1_prbar19 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region19_br	Region 19 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region19_ap	Region 19 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar19

MPU master 0 programmable limit address register 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1548

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

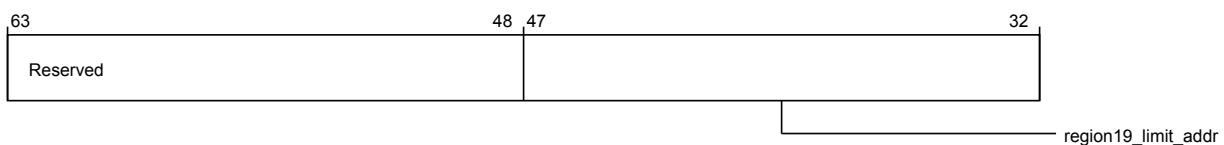


Figure 4-1678 por_mpu_por_mpu_m1_prlar19 (high)

The following table shows the por_mpu_m1_prlar19 higher register bit assignments.

Table 4-1695 por_mpu_por_mpu_m1_prlar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

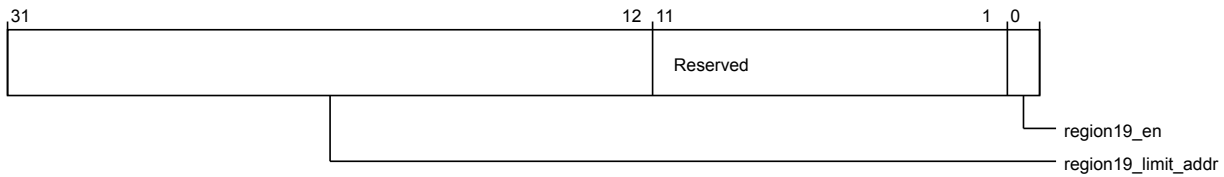


Figure 4-1679 `por_mpu_por_mpu_m1_prlar19` (low)

The following table shows the `por_mpu_m1_prlar19` lower register bit assignments.

Table 4-1696 `por_mpu_por_mpu_m1_prlar19` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region19_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region19_en</code>	Region 19 enable.	RW	1'b0

`por_mpu_m1_prbar20`

MPU master 0 programmable base address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1550

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

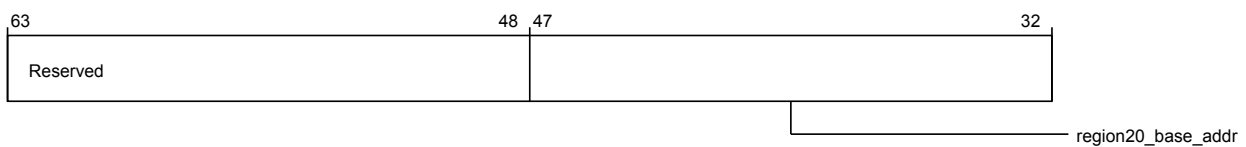


Figure 4-1680 `por_mpu_por_mpu_m1_prbar20` (high)

The following table shows the `por_mpu_m1_prbar20` higher register bit assignments.

Table 4-1697 `por_mpu_por_mpu_m1_prbar20` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region20_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

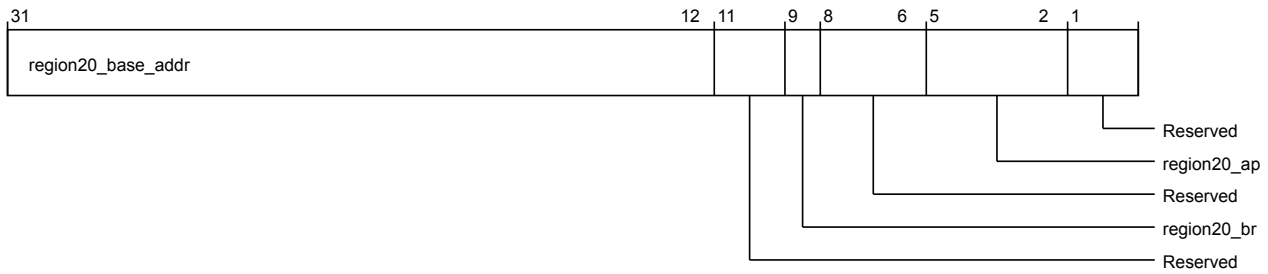


Figure 4-1681 por_mpu_por_mpu_m1_prbar20 (low)

The following table shows the por_mpu_m1_prbar20 lower register bit assignments.

Table 4-1698 por_mpu_por_mpu_m1_prbar20 (low)

Bits	Field name	Description	Type	Reset
31:12	region20_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region20_br	Region 20 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region20_ap	Region 20 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar20

MPU master 0 programmable limit address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1558

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

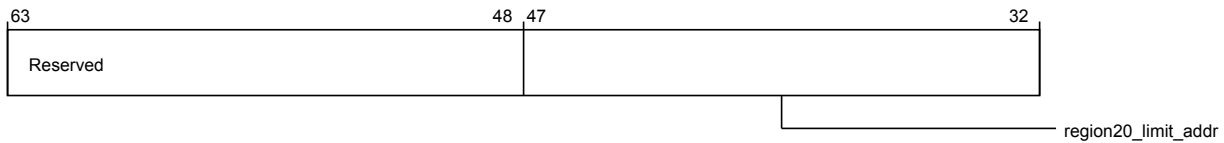


Figure 4-1682 por_mpu_m1_prlar20 (high)

The following table shows the por_mpu_m1_prlar20 higher register bit assignments.

Table 4-1699 por_mpu_m1_prlar20 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region20_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

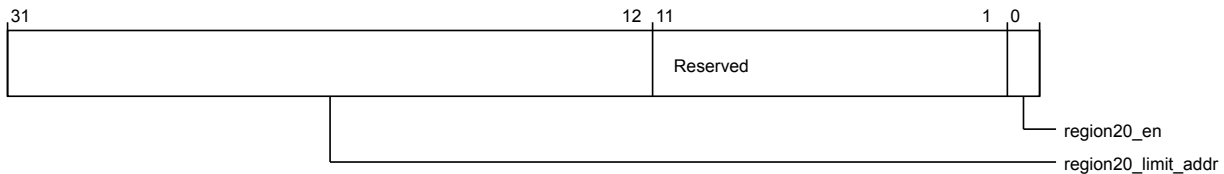


Figure 4-1683 por_mpu_m1_prlar20 (low)

The following table shows the por_mpu_m1_prlar20 lower register bit assignments.

Table 4-1700 por_mpu_m1_prlar20 (low)

Bits	Field name	Description	Type	Reset
31:12	region20_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region20_en	Region 20 enable.	RW	1'b0

por_mpu_m1_prbar21

MPU master 0 programmable base address register 21.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1560

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

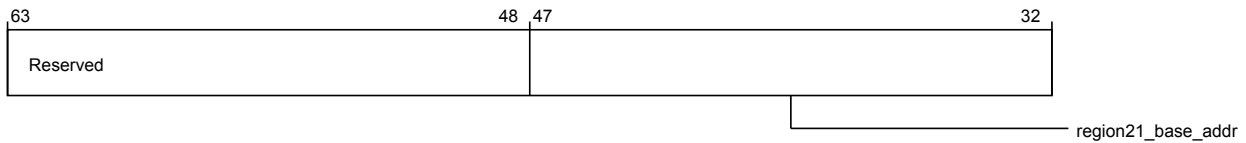


Figure 4-1684 por_mpu_por_mpu_m1_prbar21 (high)

The following table shows the por_mpu_m1_prbar21 higher register bit assignments.

Table 4-1701 por_mpu_por_mpu_m1_prbar21 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

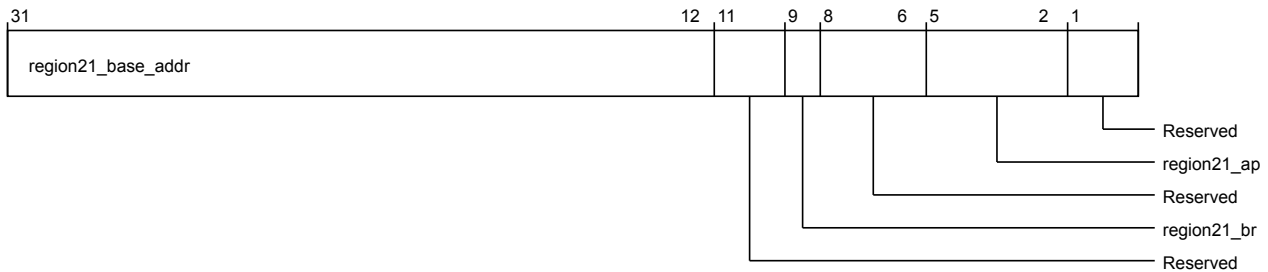


Figure 4-1685 por_mpu_por_mpu_m1_prbar21 (low)

The following table shows the por_mpu_m1_prbar21 lower register bit assignments.

Table 4-1702 por_mpu_por_mpu_m1_prbar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region21_br	Region 21 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region21_ap	Region 21 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar21

MPU master 0 programmable limit address register 21.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1568
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

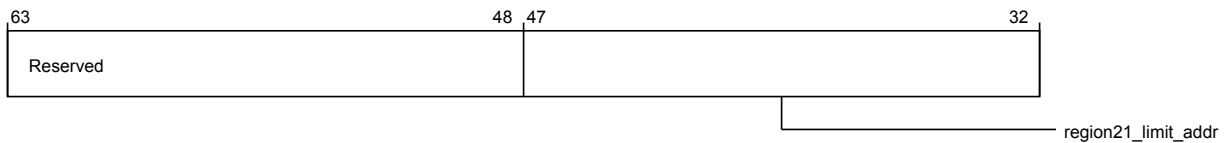


Figure 4-1686 por_mpu_por_mpu_m1_prlar21 (high)

The following table shows the por_mpu_m1_prlar21 higher register bit assignments.

Table 4-1703 por_mpu_por_mpu_m1_prlar21 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

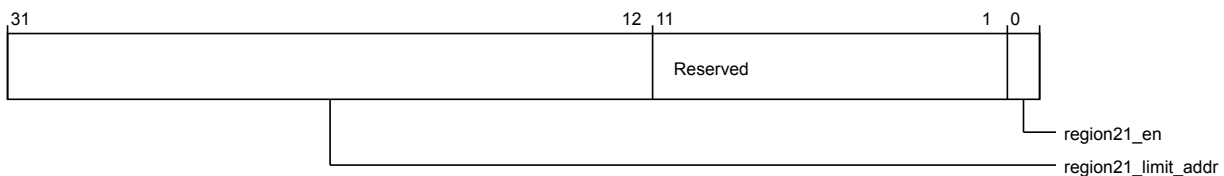


Figure 4-1687 por_mpu_por_mpu_m1_prlar21 (low)

The following table shows the por_mpu_m1_prlar21 lower register bit assignments.

Table 4-1704 por_mpu_por_mpu_m1_prlar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region21_en	Region 21 enable.	RW	1'b0

por_mpu_m1_prbar22

MPU master 0 programmable base address register 22.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1570
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

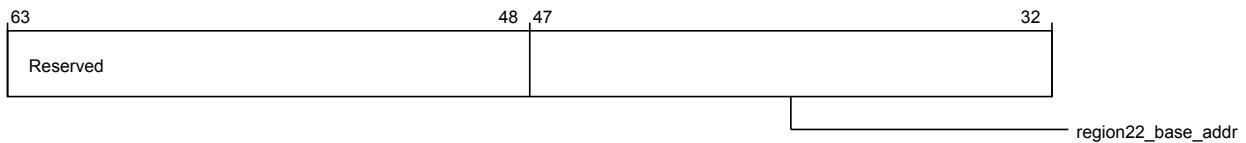


Figure 4-1688 por_mpu_por_mpu_m1_prbar22 (high)

The following table shows the por_mpu_m1_prbar22 higher register bit assignments.

Table 4-1705 por_mpu_por_mpu_m1_prbar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

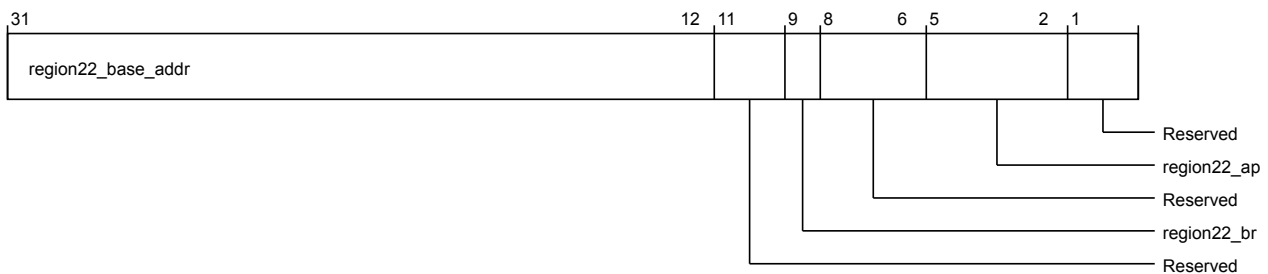


Figure 4-1689 por_mpu_por_mpu_m1_prbar22 (low)

The following table shows the por_mpu_m1_prbar22 lower register bit assignments.

Table 4-1706 por_mpu_por_mpu_m1_prbar22 (low)

Bits	Field name	Description	Type	Reset
31:12	region22_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1706 por_mpu_por_mpu_m1_prbar22 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region22_br	Region 22 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region22_ap	Region 22 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar22

MPU master 0 programmable limit address register 22.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1578

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

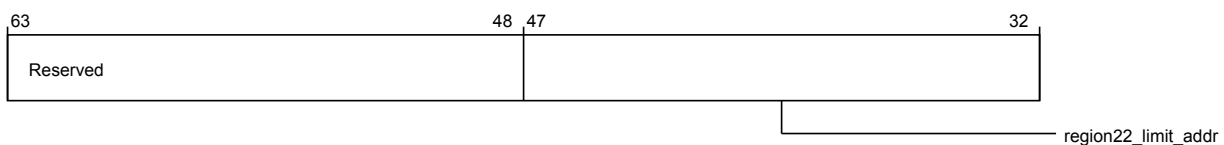


Figure 4-1690 por_mpu_por_mpu_m1_prlar22 (high)

The following table shows the por_mpu_m1_prlar22 higher register bit assignments.

Table 4-1707 por_mpu_por_mpu_m1_prlar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

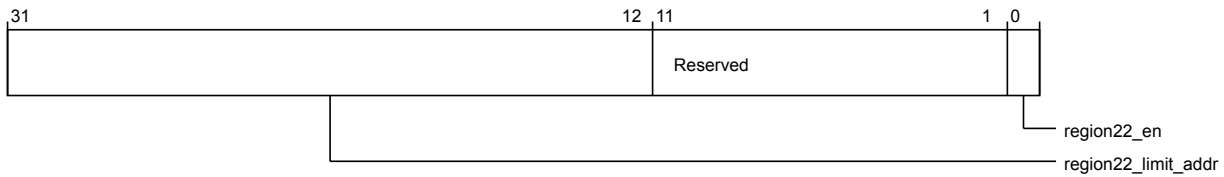


Figure 4-1691 `por_mpu_por_mpu_m1_prlar22` (low)

The following table shows the `por_mpu_m1_prlar22` lower register bit assignments.

Table 4-1708 `por_mpu_por_mpu_m1_prlar22` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region22_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region22_en</code>	Region 22 enable.	RW	1'b0

`por_mpu_m1_prbar23`

MPU master 0 programmable base address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1580

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

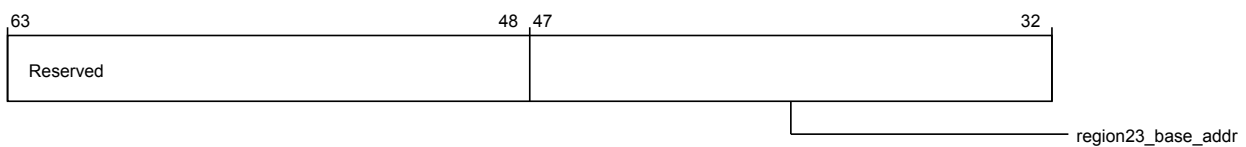


Figure 4-1692 `por_mpu_por_mpu_m1_prbar23` (high)

The following table shows the `por_mpu_m1_prbar23` higher register bit assignments.

Table 4-1709 `por_mpu_por_mpu_m1_prbar23` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region23_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

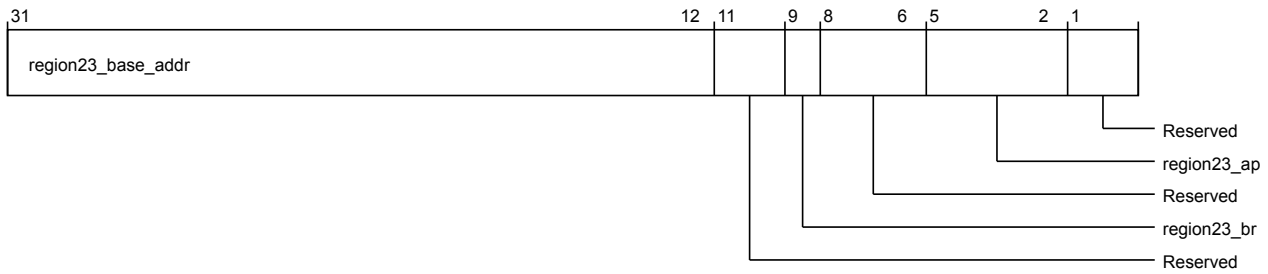


Figure 4-1693 `por_mpu_por_mpu_m1_prbar23 (low)`

The following table shows the `por_mpu_m1_prbar23` lower register bit assignments.

Table 4-1710 `por_mpu_por_mpu_m1_prbar23 (low)`

Bits	Field name	Description	Type	Reset
31:12	<code>region23_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region23_br</code>	Region 23 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region23_ap</code>	Region 23 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m1_prlar23`

MPU master 0 programmable limit address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1588

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

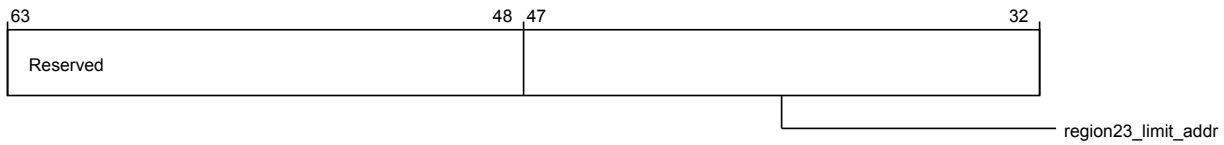


Figure 4-1694 por_mpu_m1_prlar23 (high)

The following table shows the por_mpu_m1_prlar23 higher register bit assignments.

Table 4-1711 por_mpu_m1_prlar23 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region23_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

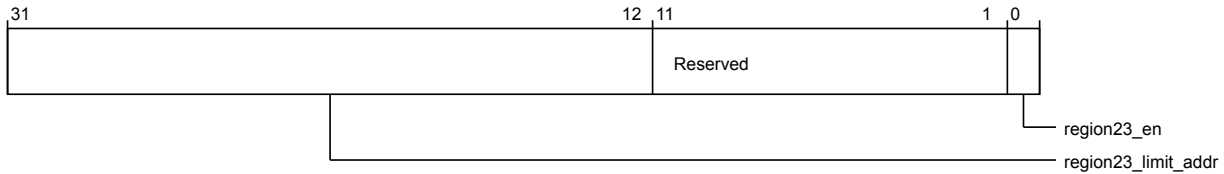


Figure 4-1695 por_mpu_m1_prlar23 (low)

The following table shows the por_mpu_m1_prlar23 lower register bit assignments.

Table 4-1712 por_mpu_m1_prlar23 (low)

Bits	Field name	Description	Type	Reset
31:12	region23_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region23_en	Region 23 enable.	RW	1'b0

por_mpu_m1_prbar24

MPU master 0 programmable base address register 24.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1590

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

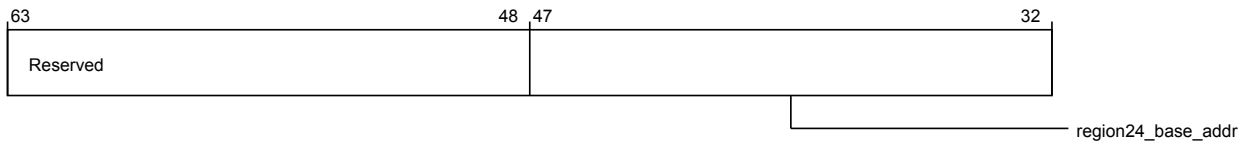


Figure 4-1696 `por_mpu_por_mpu_m1_prbar24` (high)

The following table shows the `por_mpu_m1_prbar24` higher register bit assignments.

Table 4-1713 `por_mpu_por_mpu_m1_prbar24` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

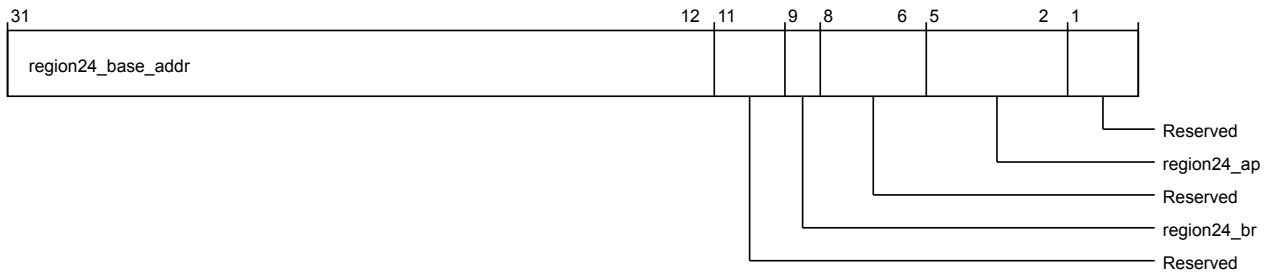


Figure 4-1697 `por_mpu_por_mpu_m1_prbar24` (low)

The following table shows the `por_mpu_m1_prbar24` lower register bit assignments.

Table 4-1714 `por_mpu_por_mpu_m1_prbar24` (low)

Bits	Field name	Description	Type	Reset
31:12	region24_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region24_br	Region 24 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region24_ap	Region 24 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar24

MPU master 0 programmable limit address register 24.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1598

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

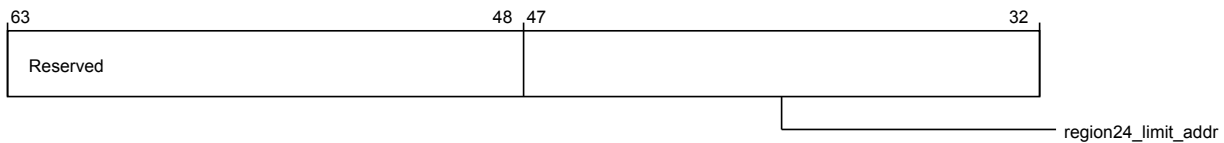


Figure 4-1698 por_mpu_por_mpu_m1_prlar24 (high)

The following table shows the por_mpu_m1_prlar24 higher register bit assignments.

Table 4-1715 por_mpu_por_mpu_m1_prlar24 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

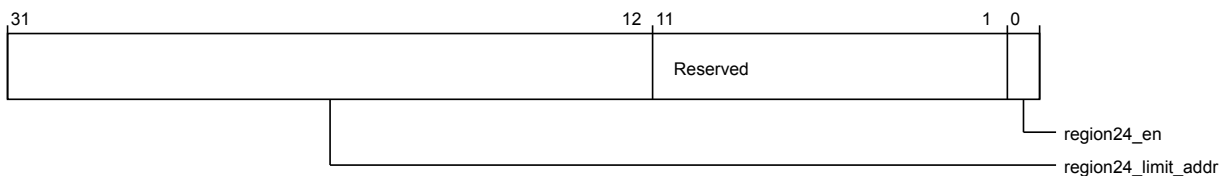


Figure 4-1699 por_mpu_por_mpu_m1_prlar24 (low)

The following table shows the por_mpu_m1_prlar24 lower register bit assignments.

Table 4-1716 por_mpu_por_mpu_m1_prlar24 (low)

Bits	Field name	Description	Type	Reset
31:12	region24_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region24_en	Region 24 enable.	RW	1'b0

por_mpu_m1_prbar25

MPU master 0 programmable base address register 25.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h15A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

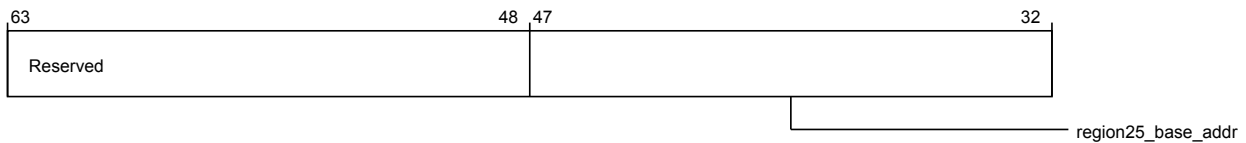


Figure 4-1700 por_mpu_por_mpu_m1_prbar25 (high)

The following table shows the por_mpu_m1_prbar25 higher register bit assignments.

Table 4-1717 por_mpu_por_mpu_m1_prbar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

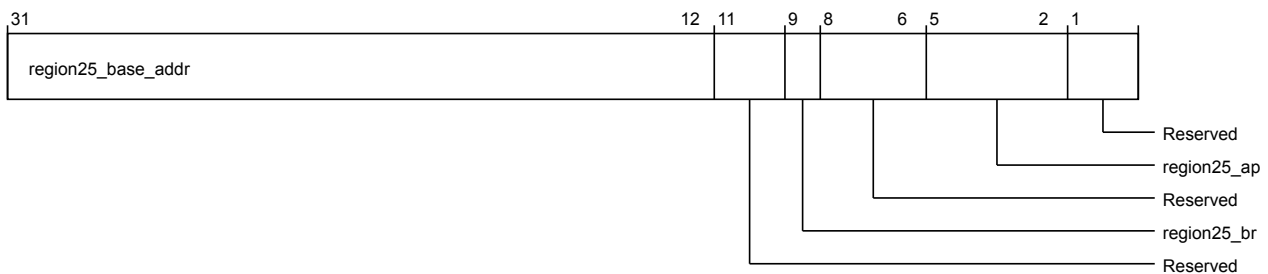


Figure 4-1701 por_mpu_por_mpu_m1_prbar25 (low)

The following table shows the por_mpu_m1_prbar25 lower register bit assignments.

Table 4-1718 por_mpu_por_mpu_m1_prbar25 (low)

Bits	Field name	Description	Type	Reset
31:12	region25_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1718 por_mpu_por_mpu_m1_prbar25 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region25_br	Region 25 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region25_ap	Region 25 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar25

MPU master 0 programmable limit address register 25.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h15A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

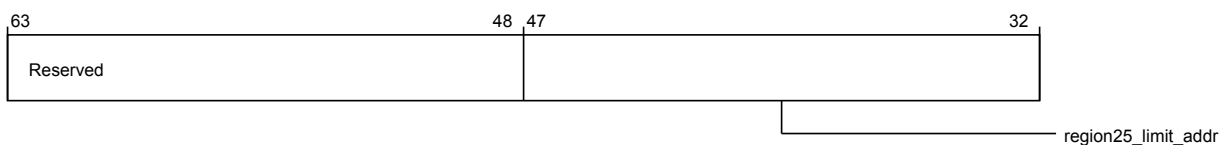


Figure 4-1702 por_mpu_por_mpu_m1_prlar25 (high)

The following table shows the por_mpu_m1_prlar25 higher register bit assignments.

Table 4-1719 por_mpu_por_mpu_m1_prlar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

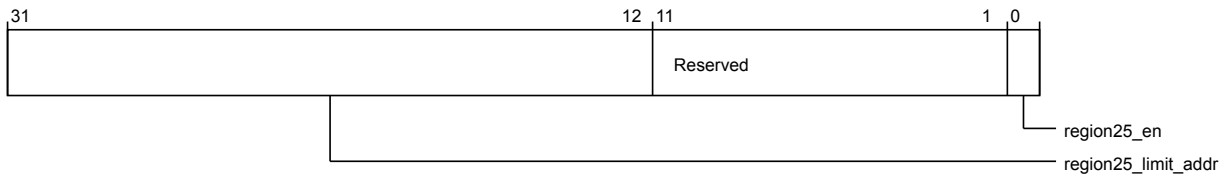


Figure 4-1703 `por_mpu_por_mpu_m1_prlar25` (low)

The following table shows the `por_mpu_m1_prlar25` lower register bit assignments.

Table 4-1720 `por_mpu_por_mpu_m1_prlar25` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region25_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region25_en</code>	Region 25 enable.	RW	1'b0

`por_mpu_m1_prbar26`

MPU master 0 programmable base address register 26.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h15B0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

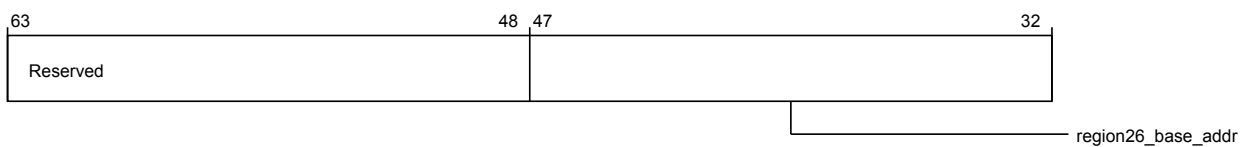


Figure 4-1704 `por_mpu_por_mpu_m1_prbar26` (high)

The following table shows the `por_mpu_m1_prbar26` higher register bit assignments.

Table 4-1721 `por_mpu_por_mpu_m1_prbar26` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region26_base_addr</code>	Bits [47:62] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

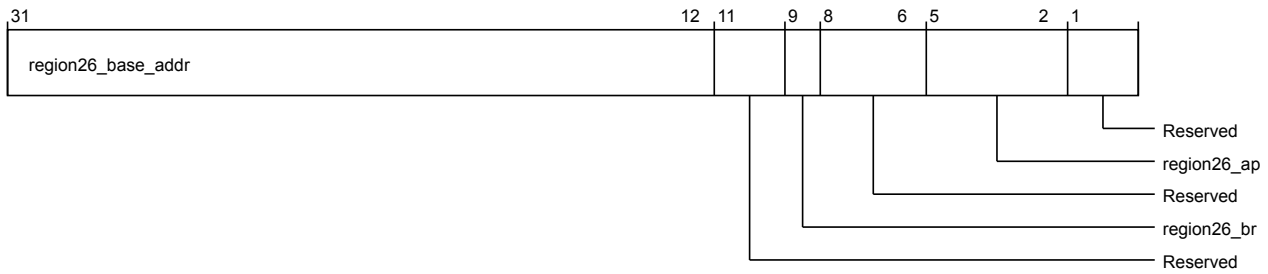


Figure 4-1705 `por_mpu_m1_prbar26` (low)

The following table shows the `por_mpu_m1_prbar26` lower register bit assignments.

Table 4-1722 `por_mpu_m1_prbar26` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region26_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region26_br</code>	Region 26 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region26_ap</code>	Region 26 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m1_prlar26`

MPU master 0 programmable limit address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h15B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

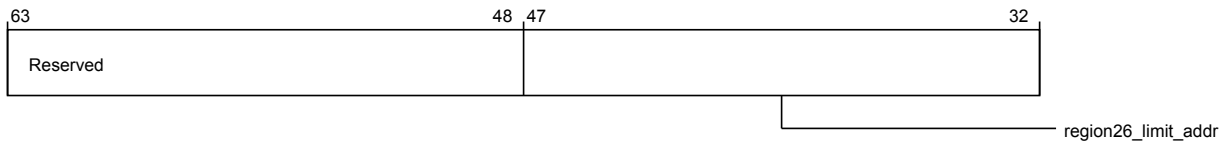


Figure 4-1706 `por_mpu_m1_prlar26` (high)

The following table shows the `por_mpu_m1_prlar26` higher register bit assignments.

Table 4-1723 `por_mpu_m1_prlar26` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region26_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

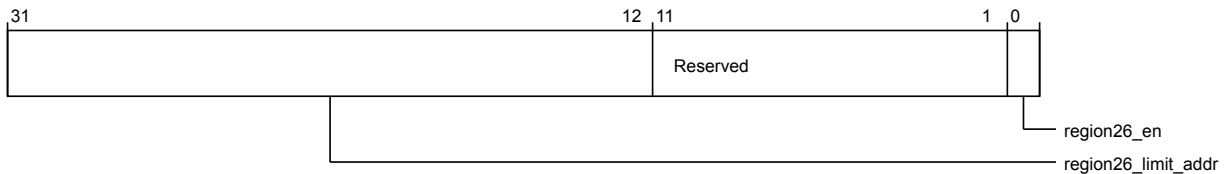


Figure 4-1707 `por_mpu_m1_prlar26` (low)

The following table shows the `por_mpu_m1_prlar26` lower register bit assignments.

Table 4-1724 `por_mpu_m1_prlar26` (low)

Bits	Field name	Description	Type	Reset
31:12	region26_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region26_en	Region 26 enable.	RW	1'b0

`por_mpu_m1_prbar27`

MPU master 0 programmable base address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h15C0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

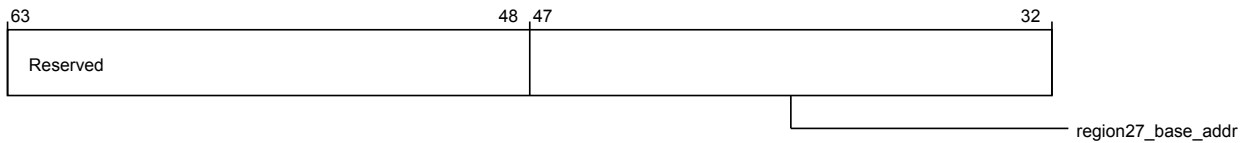


Figure 4-1708 `por_mpu_por_mpu_m1_prbar27` (high)

The following table shows the `por_mpu_m1_prbar27` higher register bit assignments.

Table 4-1725 `por_mpu_por_mpu_m1_prbar27` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

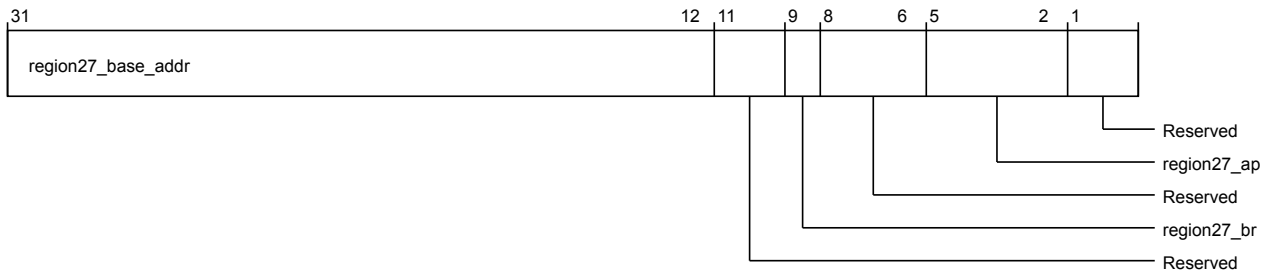


Figure 4-1709 `por_mpu_por_mpu_m1_prbar27` (low)

The following table shows the `por_mpu_m1_prbar27` lower register bit assignments.

Table 4-1726 `por_mpu_por_mpu_m1_prbar27` (low)

Bits	Field name	Description	Type	Reset
31:12	region27_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region27_br	Region 27 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region27_ap	Region 27 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar27

MPU master 0 programmable limit address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h15C8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

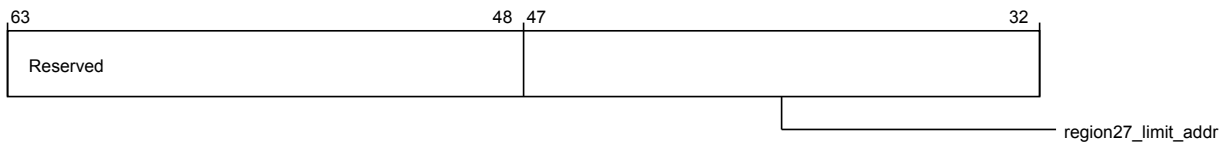


Figure 4-1710 por_mpu_por_mpu_m1_prlar27 (high)

The following table shows the por_mpu_m1_prlar27 higher register bit assignments.

Table 4-1727 por_mpu_por_mpu_m1_prlar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

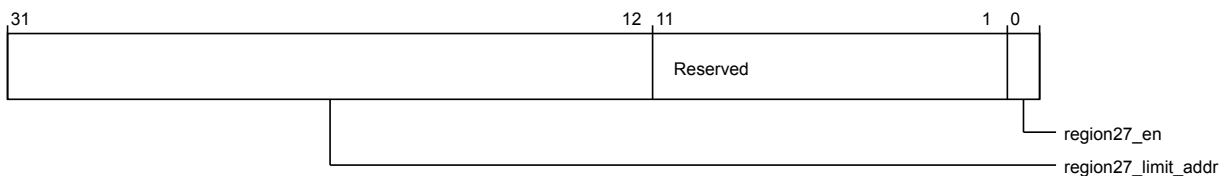


Figure 4-1711 por_mpu_por_mpu_m1_prlar27 (low)

The following table shows the por_mpu_m1_prlar27 lower register bit assignments.

Table 4-1728 por_mpu_por_mpu_m1_prlar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region27_en	Region 27 enable.	RW	1'b0

por_mpu_m1_prbar28

MPU master 0 programmable base address register 28.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h15D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

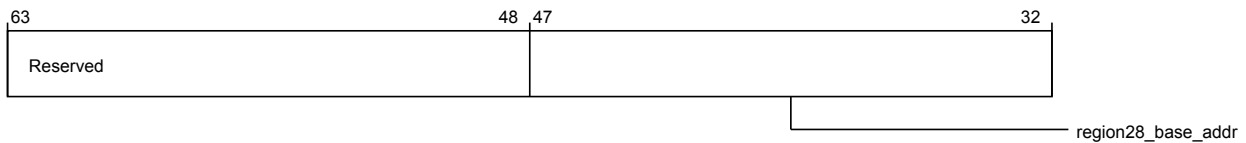


Figure 4-1712 por_mpu_por_mpu_m1_prbar28 (high)

The following table shows the por_mpu_m1_prbar28 higher register bit assignments.

Table 4-1729 por_mpu_por_mpu_m1_prbar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

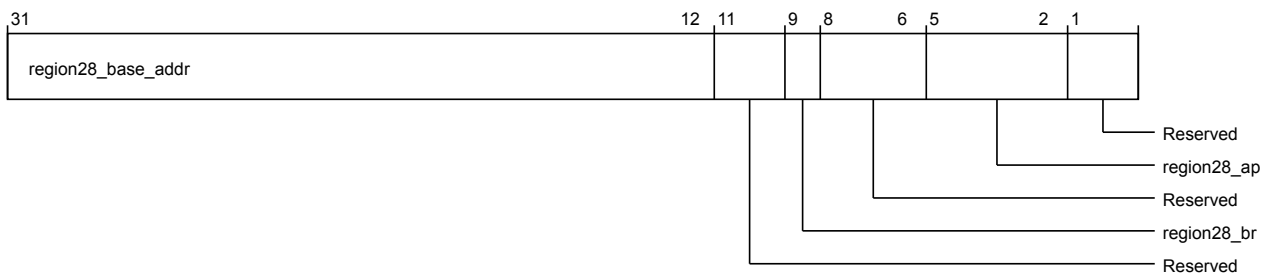


Figure 4-1713 por_mpu_por_mpu_m1_prbar28 (low)

The following table shows the por_mpu_m1_prbar28 lower register bit assignments.

Table 4-1730 por_mpu_por_mpu_m1_prbar28 (low)

Bits	Field name	Description	Type	Reset
31:12	region28_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1730 por_mpu_por_mpu_m1_prbar28 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region28_br	Region 28 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region28_ap	Region 28 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar28

MPU master 0 programmable limit address register 28.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h15D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

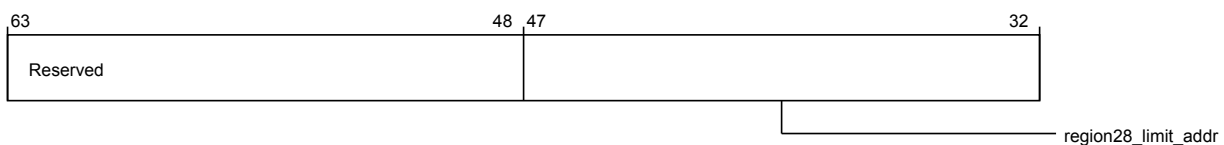


Figure 4-1714 por_mpu_por_mpu_m1_prlar28 (high)

The following table shows the por_mpu_m1_prlar28 higher register bit assignments.

Table 4-1731 por_mpu_por_mpu_m1_prlar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

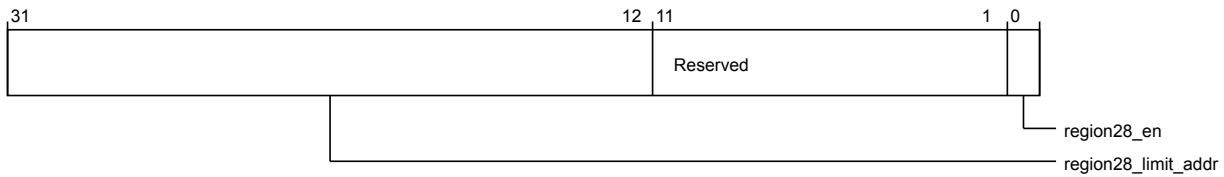


Figure 4-1715 `por_mpu_por_mpu_m1_prlar28` (low)

The following table shows the `por_mpu_m1_prlar28` lower register bit assignments.

Table 4-1732 `por_mpu_por_mpu_m1_prlar28` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region28_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region28_en</code>	Region 28 enable.	RW	1'b0

`por_mpu_m1_prbar29`

MPU master 0 programmable base address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h15E0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

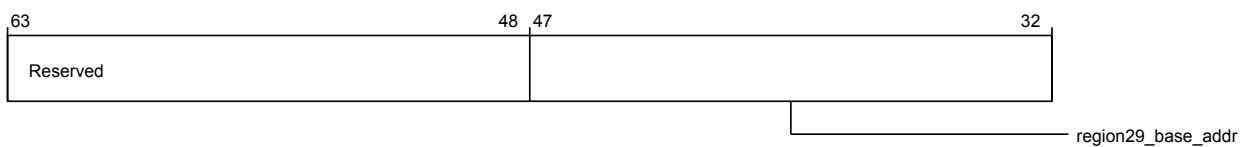


Figure 4-1716 `por_mpu_por_mpu_m1_prbar29` (high)

The following table shows the `por_mpu_m1_prbar29` higher register bit assignments.

Table 4-1733 `por_mpu_por_mpu_m1_prbar29` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region29_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

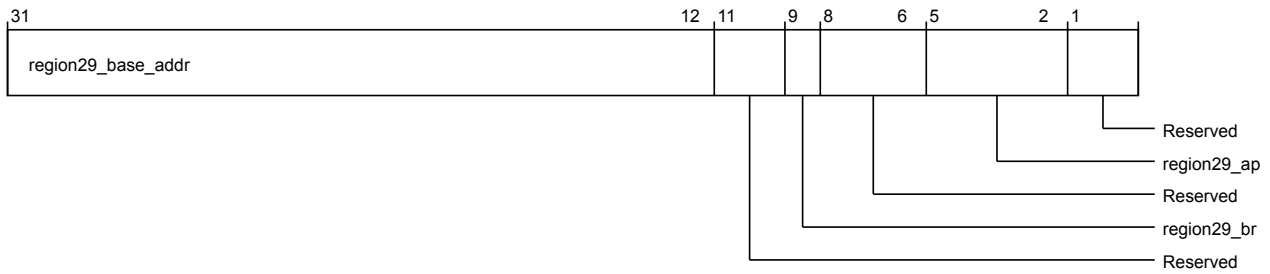


Figure 4-1717 `por_mpu_por_mpu_m1_prbar29` (low)

The following table shows the `por_mpu_m1_prbar29` lower register bit assignments.

Table 4-1734 `por_mpu_por_mpu_m1_prbar29` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region29_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region29_br</code>	Region 29 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region29_ap</code>	Region 29 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m1_prlar29`

MPU master 0 programmable limit address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h15E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

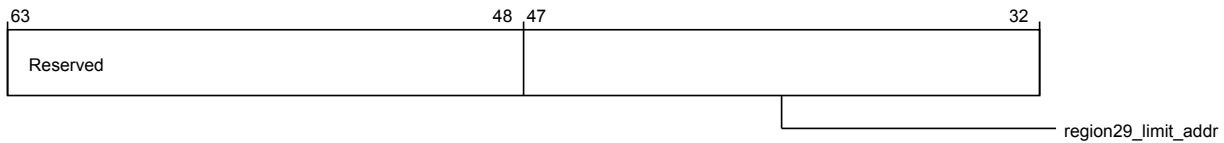


Figure 4-1718 por_mpu_m1_prlar29 (high)

The following table shows the por_mpu_m1_prlar29 higher register bit assignments.

Table 4-1735 por_mpu_m1_prlar29 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region29_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

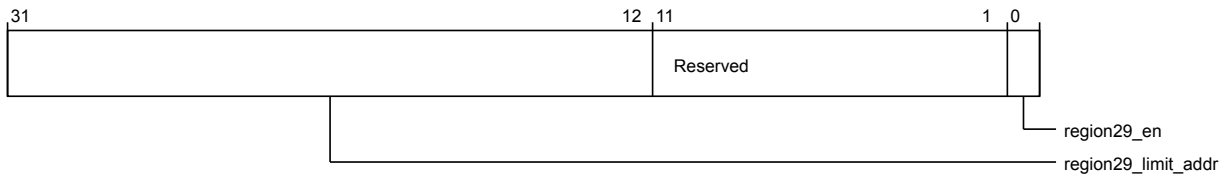


Figure 4-1719 por_mpu_m1_prlar29 (low)

The following table shows the por_mpu_m1_prlar29 lower register bit assignments.

Table 4-1736 por_mpu_m1_prlar29 (low)

Bits	Field name	Description	Type	Reset
31:12	region29_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region29_en	Region 29 enable.	RW	1'b0

por_mpu_m1_prbar30

MPU master 0 programmable base address register 30.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h15F0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

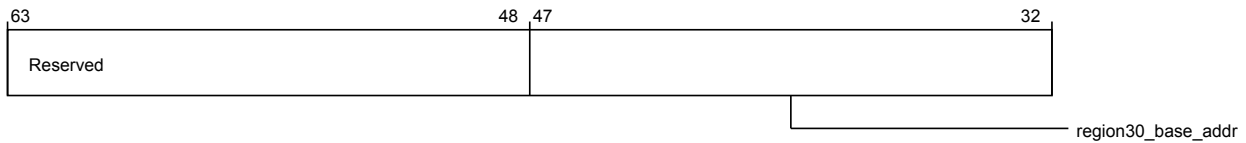


Figure 4-1720 por_mpu_por_mpu_m1_prbar30 (high)

The following table shows the por_mpu_m1_prbar30 higher register bit assignments.

Table 4-1737 por_mpu_por_mpu_m1_prbar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

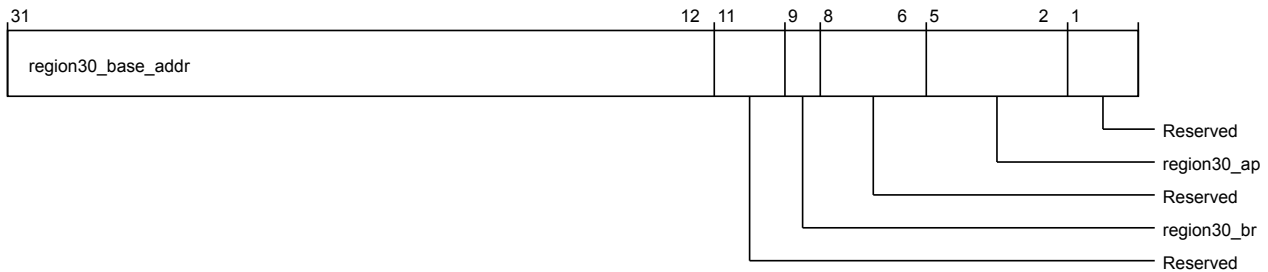


Figure 4-1721 por_mpu_por_mpu_m1_prbar30 (low)

The following table shows the por_mpu_m1_prbar30 lower register bit assignments.

Table 4-1738 por_mpu_por_mpu_m1_prbar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region30_br	Region 30 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region30_ap	Region 30 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m1_prlar30

MPU master 0 programmable limit address register 30.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h15F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

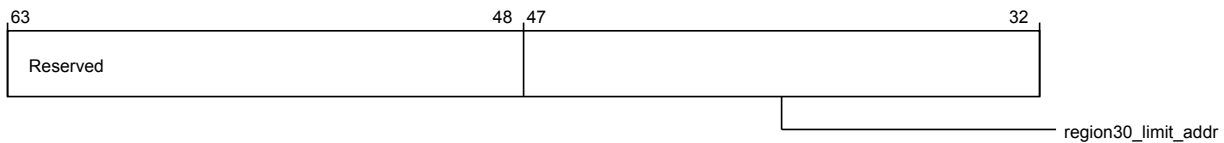


Figure 4-1722 por_mpu_por_mpu_m1_prlar30 (high)

The following table shows the `por_mpu_m1_prlar30` higher register bit assignments.

Table 4-1739 por_mpu_por_mpu_m1_prlar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

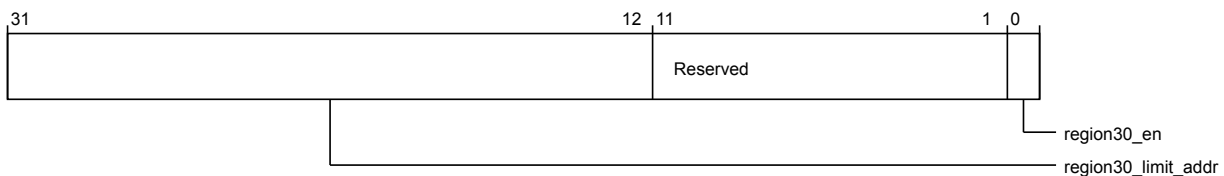


Figure 4-1723 por_mpu_por_mpu_m1_prlar30 (low)

The following table shows the `por_mpu_m1_prlar30` lower register bit assignments.

Table 4-1740 por_mpu_por_mpu_m1_prlar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region30_en	Region 30 enable.	RW	1'b0

por_mpu_m1_prbar31

MPU master 0 programmable base address register 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1600
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

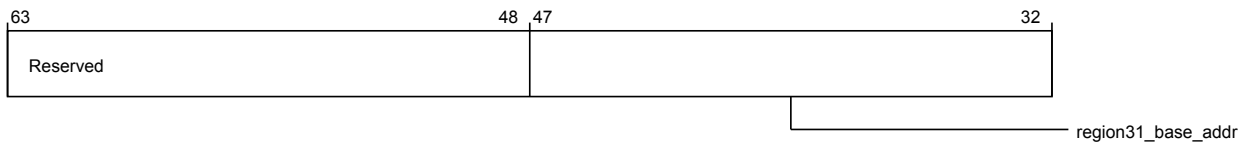


Figure 4-1724 por_mpu_por_mpu_m1_prbar31 (high)

The following table shows the por_mpu_m1_prbar31 higher register bit assignments.

Table 4-1741 por_mpu_por_mpu_m1_prbar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

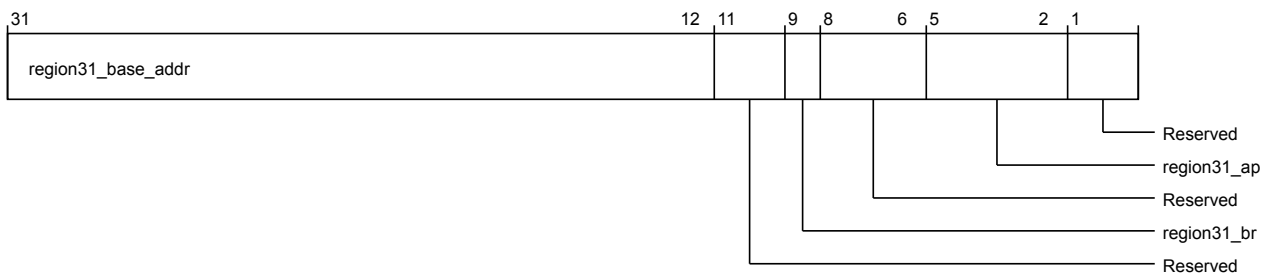


Figure 4-1725 por_mpu_por_mpu_m1_prbar31 (low)

The following table shows the por_mpu_m1_prbar31 lower register bit assignments.

Table 4-1742 por_mpu_por_mpu_m1_prbar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1742 `por_mpu_por_mpu_m1_prbar31` (low) (continued)

Bits	Field name	Description	Type	Reset
9	region31_br	Region 31 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region31_ap	Region 31 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m1_prlar31`

MPU master 0 programmable limit address register 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1608

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

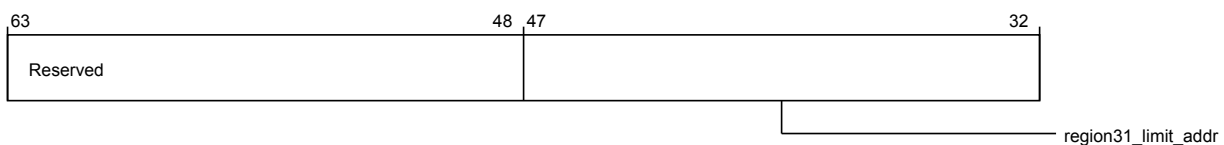


Figure 4-1726 `por_mpu_por_mpu_m1_prlar31` (high)

The following table shows the `por_mpu_m1_prlar31` higher register bit assignments.

Table 4-1743 `por_mpu_por_mpu_m1_prlar31` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

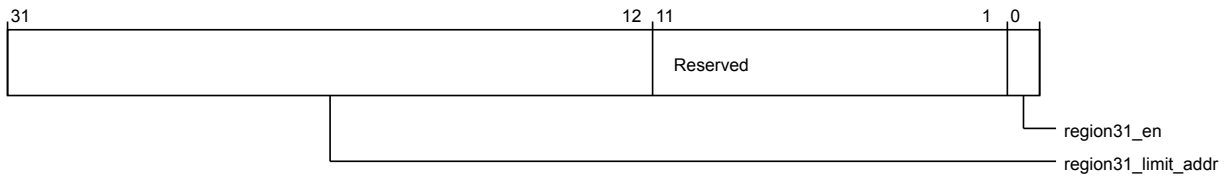


Figure 4-1727 `por_mpu_por_mpu_m1_prlar31` (low)

The following table shows the `por_mpu_m1_prlar31` lower register bit assignments.

Table 4-1744 `por_mpu_por_mpu_m1_prlar31` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region31_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region31_en</code>	Region 31 enable.	RW	1'b0

`por_mpu_m2_ctl`

Functions as the MPU Master 2 control register.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1800

Register reset 64'b010

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

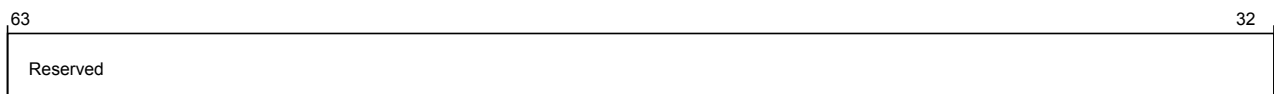


Figure 4-1728 `por_mpu_por_mpu_m2_ctl` (high)

The following table shows the `por_mpu_m2_ctl` higher register bit assignments.

Table 4-1745 `por_mpu_por_mpu_m2_ctl` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

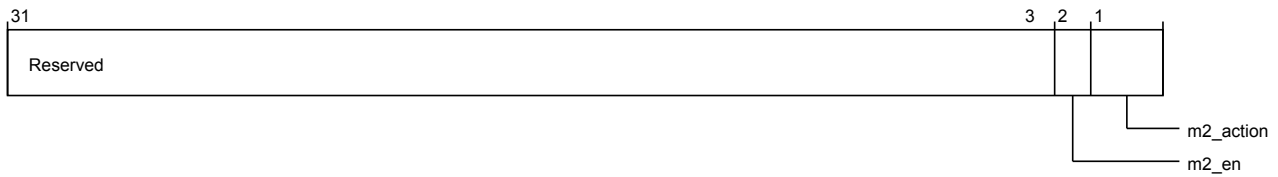


Figure 4-1729 por_mpu_m2_ctl (low)

The following table shows the por_mpu_m2_ctl lower register bit assignments.

Table 4-1746 por_mpu_m2_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	m2_en	MPU master 2 enable.	RW	1'b0
1:0	m2_action	Indicates action HN* should take if no access permission is granted 2'b00: FUSA interrupt 2'b01: Bus error to the originating bus master 2'b10: Both FUSA interrupt and bus error.	RW	2'b10

por_mpu_m2_prbar0

MPU master 0 programmable base address register 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1810

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

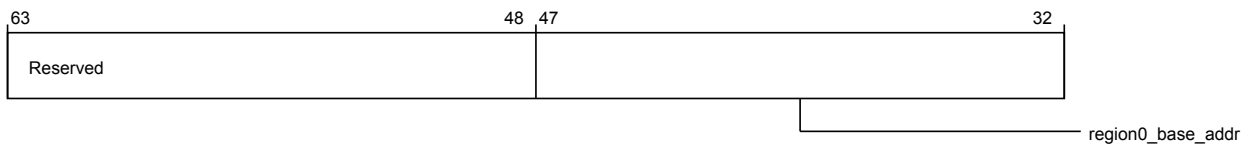


Figure 4-1730 por_mpu_m2_prbar0 (high)

The following table shows the por_mpu_m2_prbar0 higher register bit assignments.

Table 4-1747 por_mpu_por_mpu_m2_prbar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

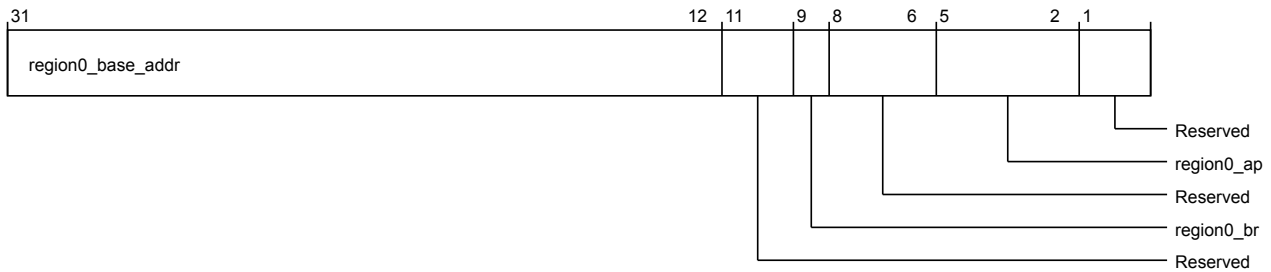


Figure 4-1731 por_mpu_por_mpu_m2_prbar0 (low)

The following table shows the por_mpu_m2_prbar0 lower register bit assignments.

Table 4-1748 por_mpu_por_mpu_m2_prbar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region0_br	Region 0 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region0_ap	Region 0 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar0

MPU master 0 programmable limit address register 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1818
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

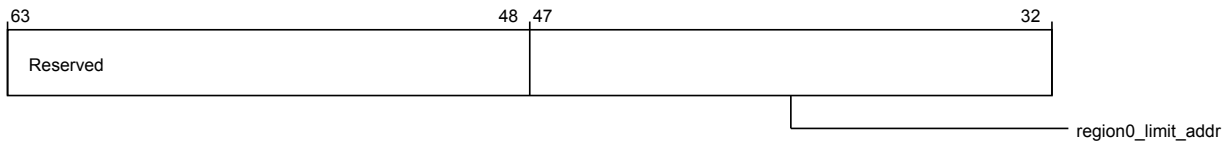


Figure 4-1732 por_mpu_m2_prlar0 (high)

The following table shows the por_mpu_m2_prlar0 higher register bit assignments.

Table 4-1749 por_mpu_m2_prlar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

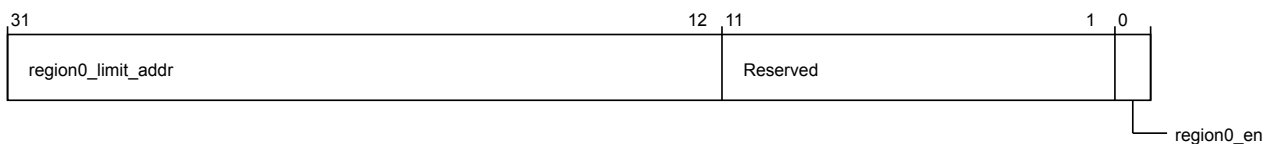


Figure 4-1733 por_mpu_m2_prlar0 (low)

The following table shows the por_mpu_m2_prlar0 lower register bit assignments.

Table 4-1750 por_mpu_m2_prlar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region0_en	Region 0 enable.	RW	1'b0

por_mpu_m2_prbar1

MPU master 0 programmable base address register 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1820
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

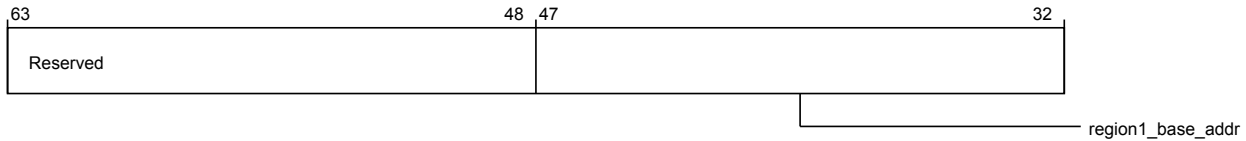


Figure 4-1734 `por_mpu_por_mpu_m2_prbar1` (high)

The following table shows the `por_mpu_m2_prbar1` higher register bit assignments.

Table 4-1751 `por_mpu_por_mpu_m2_prbar1` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region1_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

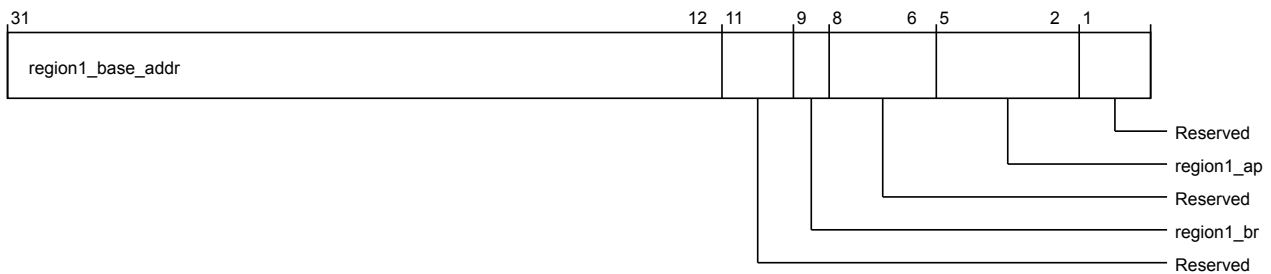


Figure 4-1735 `por_mpu_por_mpu_m2_prbar1` (low)

The following table shows the `por_mpu_m2_prbar1` lower register bit assignments.

Table 4-1752 `por_mpu_por_mpu_m2_prbar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region1_br</code>	Region 1 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-

Table 4-1752 por_mpu_por_mpu_m2_prbar1 (low) (continued)

Bits	Field name	Description	Type	Reset
5:2	region1_ap	Region 1 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar1

MPU master 0 programmable limit address register 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1828

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

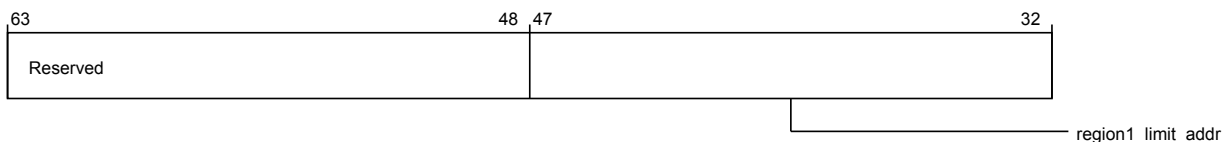


Figure 4-1736 por_mpu_por_mpu_m2_prlar1 (high)

The following table shows the por_mpu_m2_prlar1 higher register bit assignments.

Table 4-1753 por_mpu_por_mpu_m2_prlar1 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region1_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

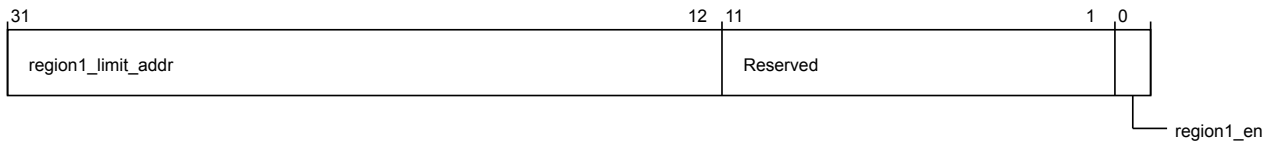


Figure 4-1737 `por_mpu_por_mpu_m2_prlar1` (low)

The following table shows the `por_mpu_m2_prlar1` lower register bit assignments.

Table 4-1754 `por_mpu_por_mpu_m2_prlar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region1_en</code>	Region 1 enable.	RW	1'b0

`por_mpu_m2_prbar2`

MPU master 0 programmable base address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1830

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

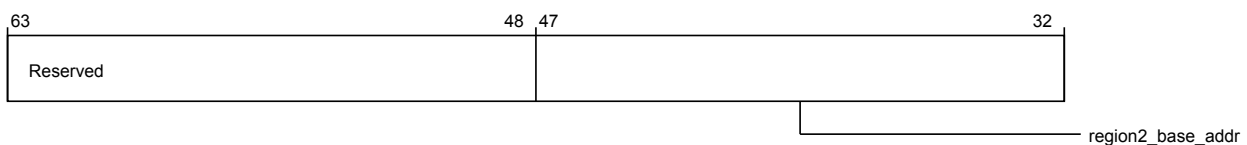


Figure 4-1738 `por_mpu_por_mpu_m2_prbar2` (high)

The following table shows the `por_mpu_m2_prbar2` higher register bit assignments.

Table 4-1755 `por_mpu_por_mpu_m2_prbar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

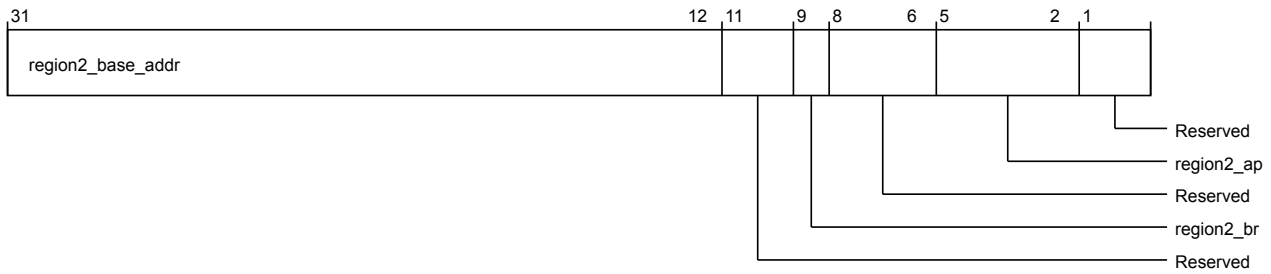


Figure 4-1739 por_mpu_por_mpu_m2_prbar2 (low)

The following table shows the por_mpu_m2_prbar2 lower register bit assignments.

Table 4-1756 por_mpu_por_mpu_m2_prbar2 (low)

Bits	Field name	Description	Type	Reset
31:12	region2_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region2_br	Region 2 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region2_ap	Region 2 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar2

MPU master 0 programmable limit address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1838

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

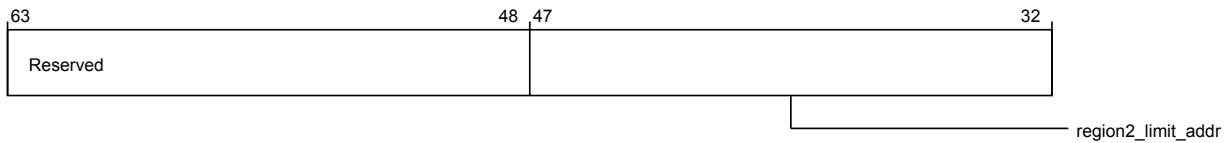


Figure 4-1740 `por_mpu_m2_prlar2` (high)

The following table shows the `por_mpu_m2_prlar2` higher register bit assignments.

Table 4-1757 `por_mpu_m2_prlar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

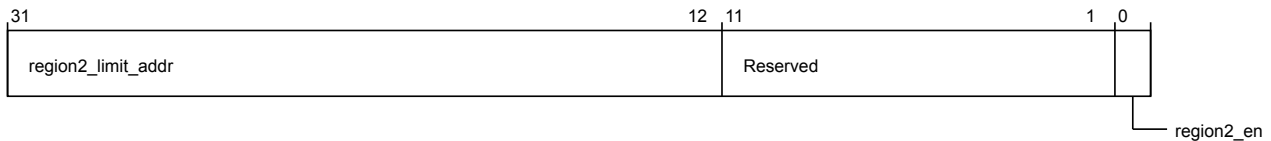


Figure 4-1741 `por_mpu_m2_prlar2` (low)

The following table shows the `por_mpu_m2_prlar2` lower register bit assignments.

Table 4-1758 `por_mpu_m2_prlar2` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region2_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region2_en</code>	Region 2 enable.	RW	1'b0

`por_mpu_m2_prbar3`

MPU master 0 programmable base address register 3.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1840
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

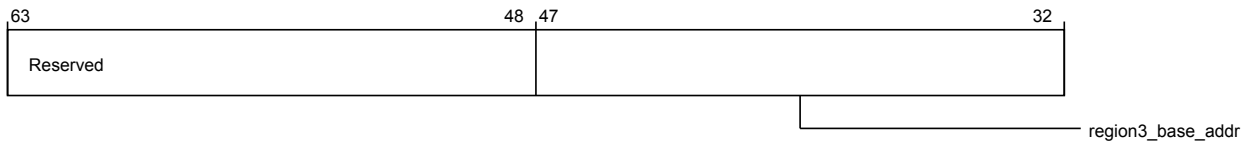


Figure 4-1742 `por_mpu_m2_prbar3` (high)

The following table shows the `por_mpu_m2_prbar3` higher register bit assignments.

Table 4-1759 `por_mpu_m2_prbar3` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

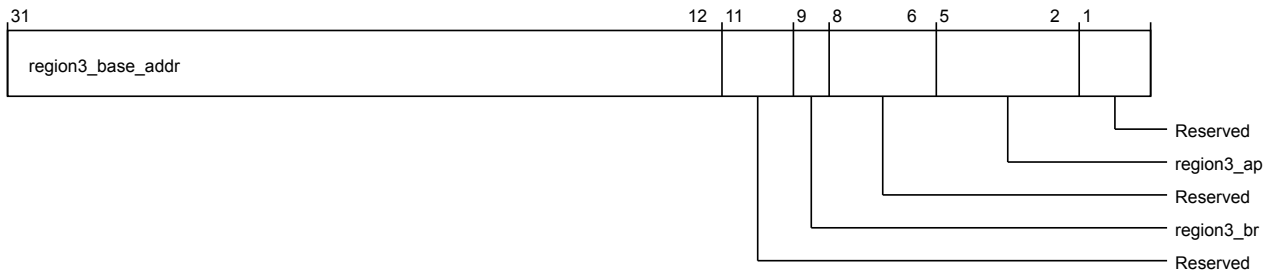


Figure 4-1743 `por_mpu_m2_prbar3` (low)

The following table shows the `por_mpu_m2_prbar3` lower register bit assignments.

Table 4-1760 `por_mpu_m2_prbar3` (low)

Bits	Field name	Description	Type	Reset
31:12	region3_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region3_br	Region 3 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region3_ap	Region 3 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar3

MPU master 0 programmable limit address register 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1848

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

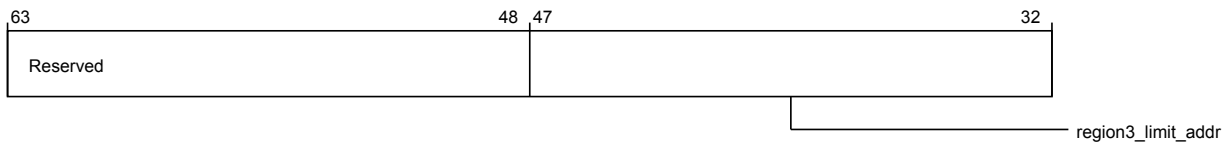


Figure 4-1744 por_mpu_por_mpu_m2_prlar3 (high)

The following table shows the por_mpu_m2_prlar3 higher register bit assignments.

Table 4-1761 por_mpu_por_mpu_m2_prlar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

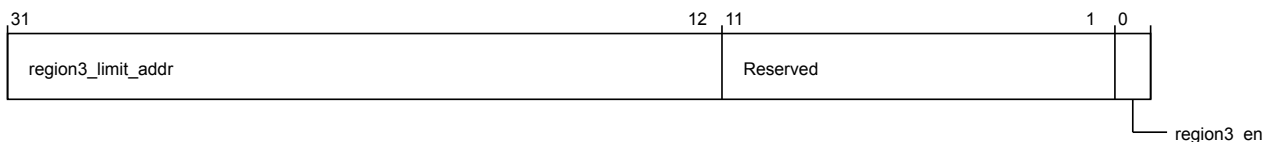


Figure 4-1745 por_mpu_por_mpu_m2_prlar3 (low)

The following table shows the por_mpu_m2_prlar3 lower register bit assignments.

Table 4-1762 por_mpu_por_mpu_m2_prlar3 (low)

Bits	Field name	Description	Type	Reset
31:12	region3_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region3_en	Region 3 enable.	RW	1'b0

por_mpu_m2_prbar4

MPU master 0 programmable base address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1850

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

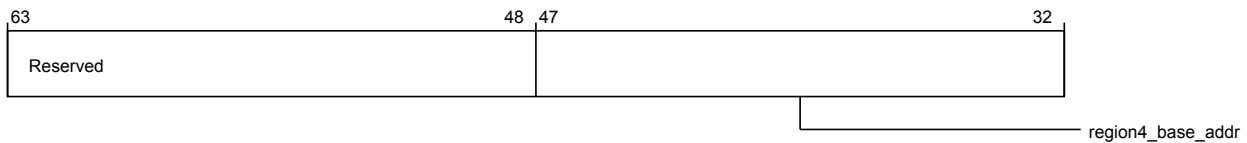


Figure 4-1746 por_mpu_por_mpu_m2_prbar4 (high)

The following table shows the por_mpu_m2_prbar4 higher register bit assignments.

Table 4-1763 por_mpu_por_mpu_m2_prbar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

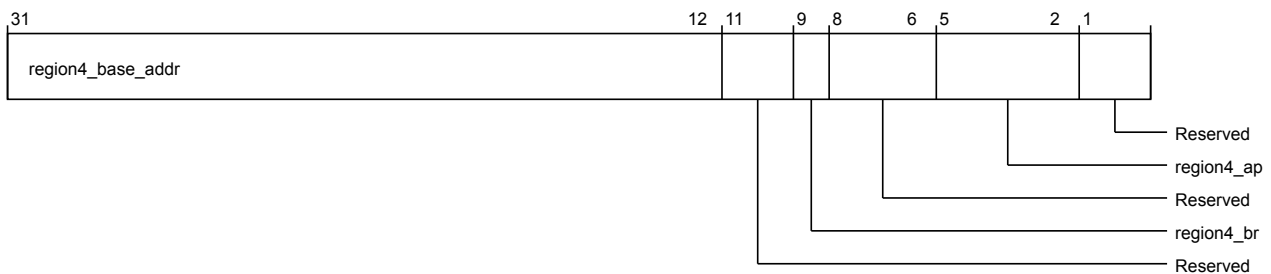


Figure 4-1747 por_mpu_por_mpu_m2_prbar4 (low)

The following table shows the por_mpu_m2_prbar4 lower register bit assignments.

Table 4-1764 por_mpu_por_mpu_m2_prbar4 (low)

Bits	Field name	Description	Type	Reset
31:12	region4_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1764 por_mpu_por_mpu_m2_prbar4 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region4_br	Region 4 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region4_ap	Region 4 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar4

MPU master 0 programmable limit address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1858

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

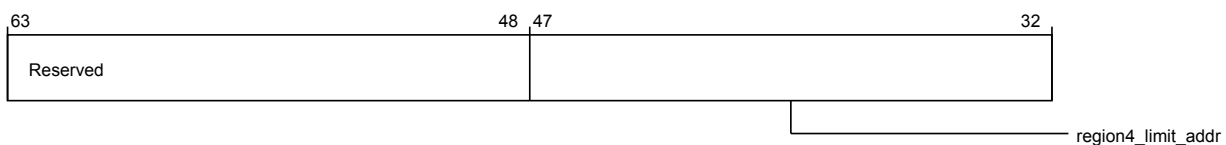


Figure 4-1748 por_mpu_por_mpu_m2_prlar4 (high)

The following table shows the por_mpu_m2_prlar4 higher register bit assignments.

Table 4-1765 por_mpu_por_mpu_m2_prlar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

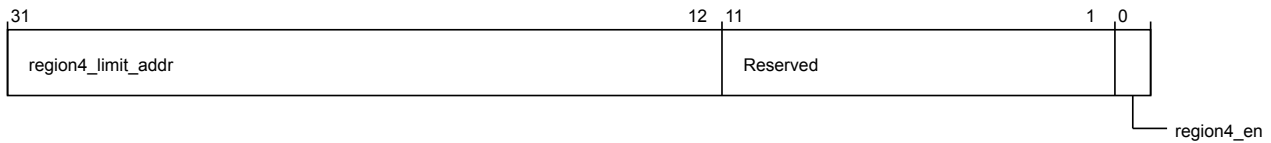


Figure 4-1749 `por_mpu_por_mpu_m2_prlar4` (low)

The following table shows the `por_mpu_m2_prlar4` lower register bit assignments.

Table 4-1766 `por_mpu_por_mpu_m2_prlar4` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region4_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region4_en</code>	Region 4 enable.	RW	1'b0

`por_mpu_m2_prbar5`

MPU master 0 programmable base address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1860

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

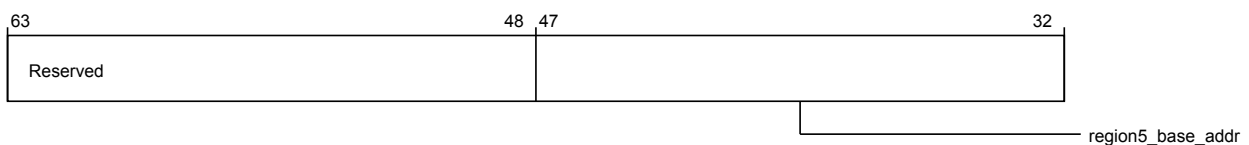


Figure 4-1750 `por_mpu_por_mpu_m2_prbar5` (high)

The following table shows the `por_mpu_m2_prbar5` higher register bit assignments.

Table 4-1767 `por_mpu_por_mpu_m2_prbar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

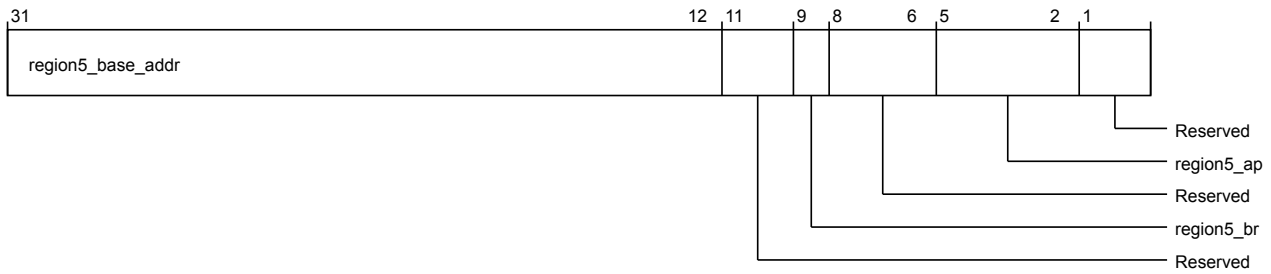


Figure 4-1751 por_mpu_por_mpu_m2_prbar5 (low)

The following table shows the por_mpu_m2_prbar5 lower register bit assignments.

Table 4-1768 por_mpu_por_mpu_m2_prbar5 (low)

Bits	Field name	Description	Type	Reset
31:12	region5_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region5_br	Region 5 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region5_ap	Region 5 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar5

MPU master 0 programmable limit address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1868

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

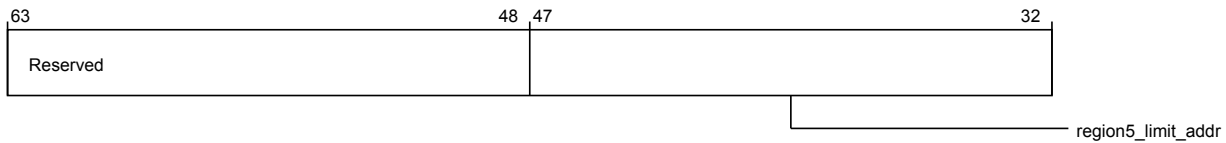


Figure 4-1752 `por_mpu_m2_prlar5` (high)

The following table shows the `por_mpu_m2_prlar5` higher register bit assignments.

Table 4-1769 `por_mpu_m2_prlar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

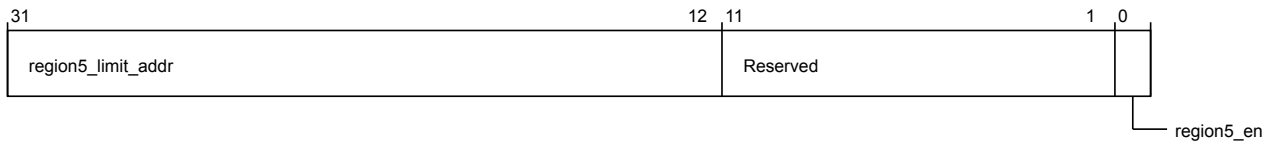


Figure 4-1753 `por_mpu_m2_prlar5` (low)

The following table shows the `por_mpu_m2_prlar5` lower register bit assignments.

Table 4-1770 `por_mpu_m2_prlar5` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region5_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region5_en</code>	Region 5 enable.	RW	1'b0

`por_mpu_m2_prbar6`

MPU master 0 programmable base address register 6.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1870
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

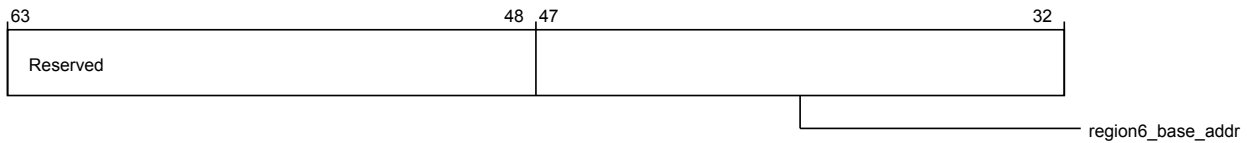


Figure 4-1754 por_mpu_por_mpu_m2_prbar6 (high)

The following table shows the por_mpu_m2_prbar6 higher register bit assignments.

Table 4-1771 por_mpu_por_mpu_m2_prbar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

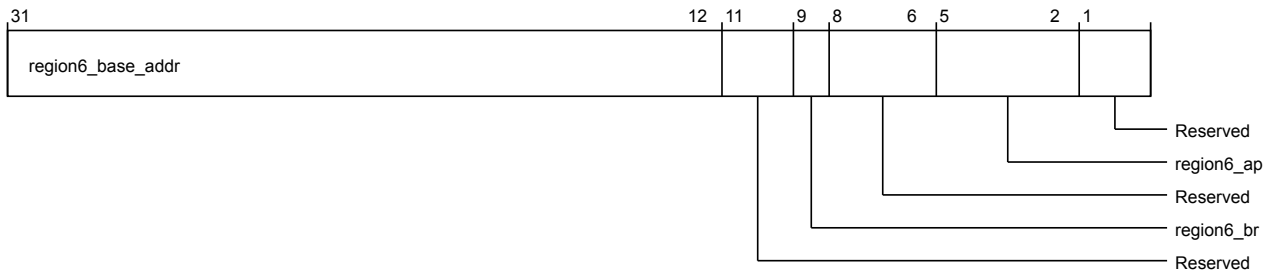


Figure 4-1755 por_mpu_por_mpu_m2_prbar6 (low)

The following table shows the por_mpu_m2_prbar6 lower register bit assignments.

Table 4-1772 por_mpu_por_mpu_m2_prbar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region6_br	Region 6 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region6_ap	Region 6 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar6

MPU master 0 programmable limit address register 6.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1878

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

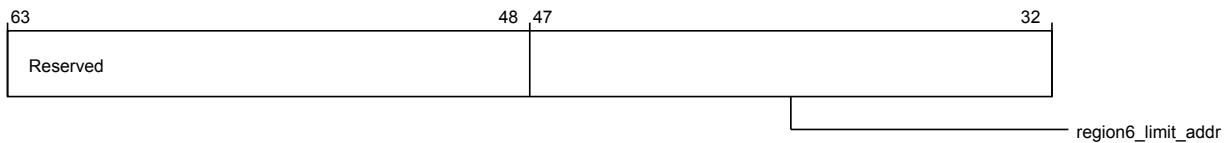


Figure 4-1756 por_mpu_por_mpu_m2_prlar6 (high)

The following table shows the por_mpu_m2_prlar6 higher register bit assignments.

Table 4-1773 por_mpu_por_mpu_m2_prlar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

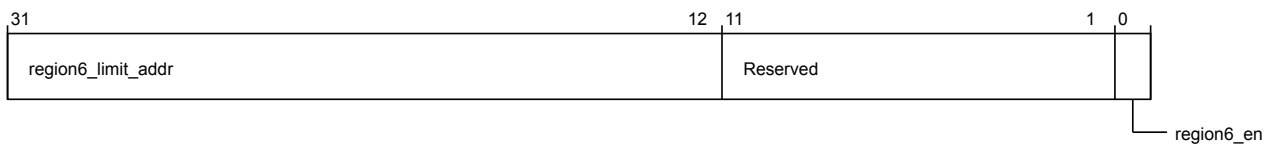


Figure 4-1757 por_mpu_por_mpu_m2_prlar6 (low)

The following table shows the por_mpu_m2_prlar6 lower register bit assignments.

Table 4-1774 por_mpu_por_mpu_m2_prlar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region6_en	Region 6 enable.	RW	1'b0

por_mpu_m2_prbar7

MPU master 0 programmable base address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1880

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

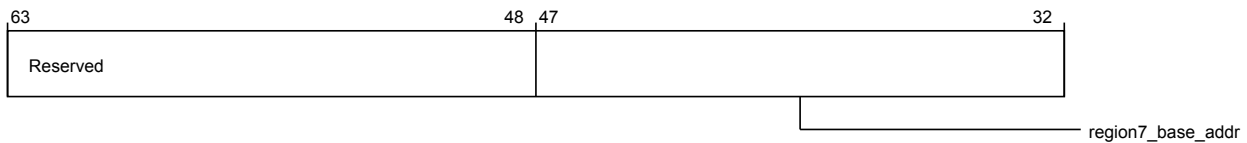


Figure 4-1758 `por_mpu_m2_prbar7` (high)

The following table shows the `por_mpu_m2_prbar7` higher register bit assignments.

Table 4-1775 `por_mpu_m2_prbar7` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

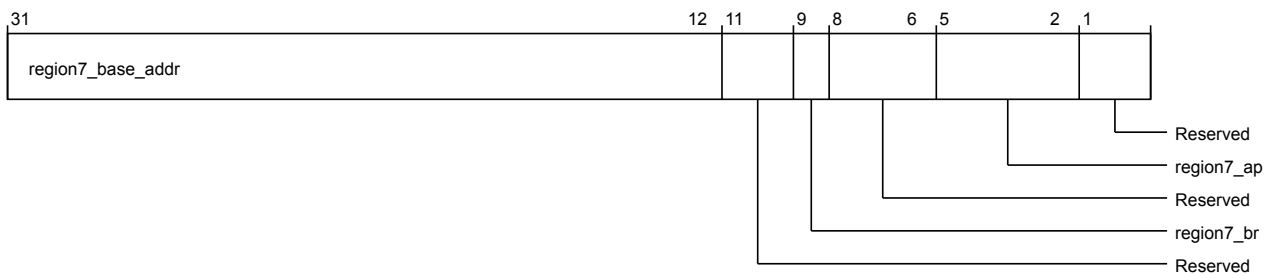


Figure 4-1759 `por_mpu_m2_prbar7` (low)

The following table shows the `por_mpu_m2_prbar7` lower register bit assignments.

Table 4-1776 `por_mpu_m2_prbar7` (low)

Bits	Field name	Description	Type	Reset
31:12	region7_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1776 por_mpu_por_mpu_m2_prbar7 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region7_br	Region 7 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region7_ap	Region 7 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar7

MPU master 0 programmable limit address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1888

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

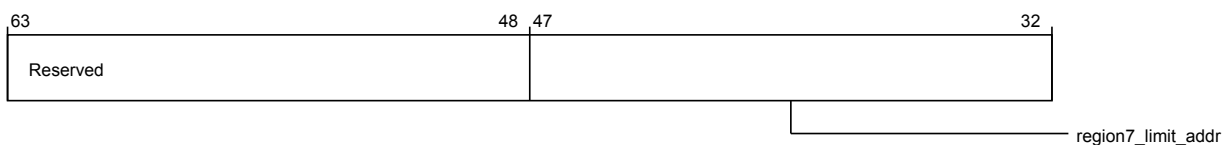


Figure 4-1760 por_mpu_por_mpu_m2_prlar7 (high)

The following table shows the por_mpu_m2_prlar7 higher register bit assignments.

Table 4-1777 por_mpu_por_mpu_m2_prlar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

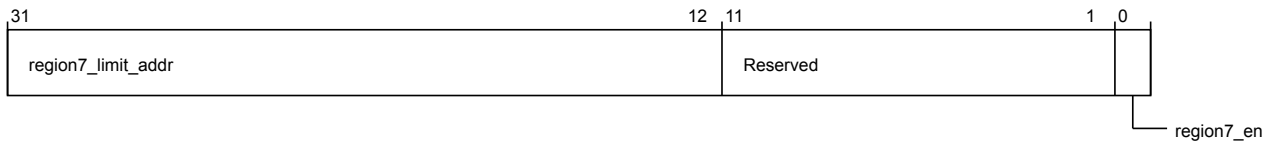


Figure 4-1761 `por_mpu_por_mpu_m2_prlar7` (low)

The following table shows the `por_mpu_m2_prlar7` lower register bit assignments.

Table 4-1778 `por_mpu_por_mpu_m2_prlar7` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region7_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region7_en</code>	Region 7 enable.	RW	1'b0

`por_mpu_m2_prbar8`

MPU master 0 programmable base address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1890

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

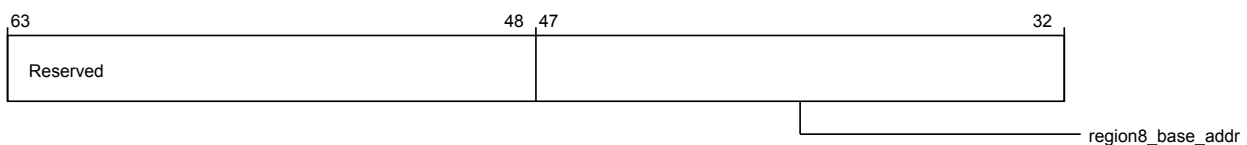


Figure 4-1762 `por_mpu_por_mpu_m2_prbar8` (high)

The following table shows the `por_mpu_m2_prbar8` higher register bit assignments.

Table 4-1779 `por_mpu_por_mpu_m2_prbar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

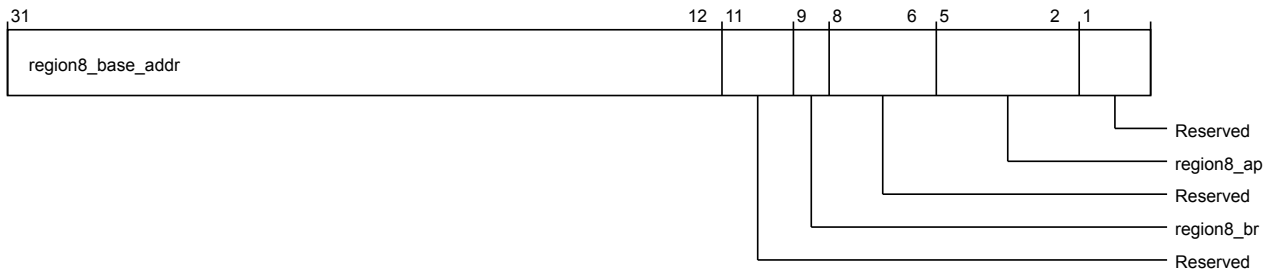


Figure 4-1763 por_mpu_por_mpu_m2_prbar8 (low)

The following table shows the por_mpu_m2_prbar8 lower register bit assignments.

Table 4-1780 por_mpu_por_mpu_m2_prbar8 (low)

Bits	Field name	Description	Type	Reset
31:12	region8_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region8_br	Region 8 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region8_ap	Region 8 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar8

MPU master 0 programmable limit address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1898

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

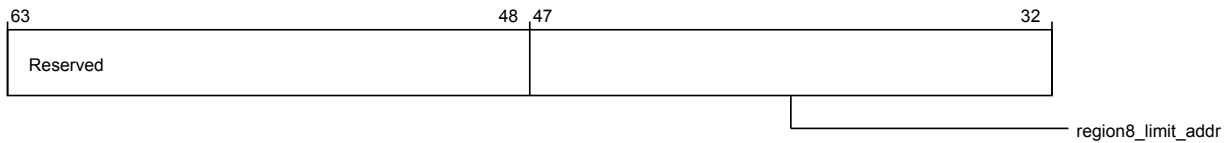


Figure 4-1764 `por_mpu_m2_prlar8` (high)

The following table shows the `por_mpu_m2_prlar8` higher register bit assignments.

Table 4-1781 `por_mpu_m2_prlar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

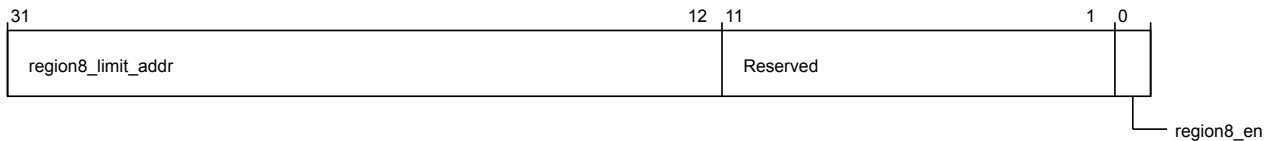


Figure 4-1765 `por_mpu_m2_prlar8` (low)

The following table shows the `por_mpu_m2_prlar8` lower register bit assignments.

Table 4-1782 `por_mpu_m2_prlar8` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region8_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region8_en</code>	Region 8 enable.	RW	1'b0

`por_mpu_m2_prbar9`

MPU master 0 programmable base address register 9.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h18A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

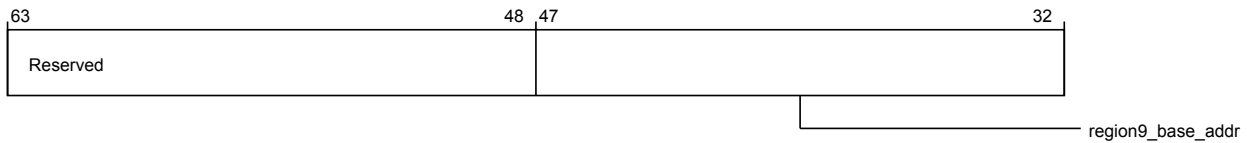


Figure 4-1766 `por_mpu_por_mpu_m2_prbar9` (high)

The following table shows the `por_mpu_m2_prbar9` higher register bit assignments.

Table 4-1783 `por_mpu_por_mpu_m2_prbar9` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

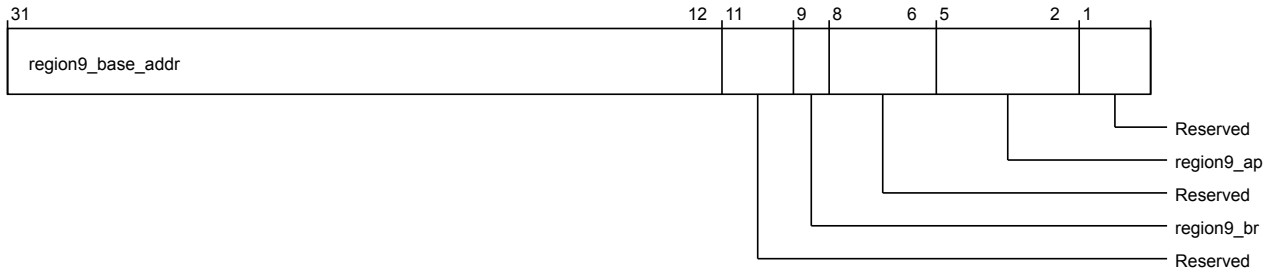


Figure 4-1767 `por_mpu_por_mpu_m2_prbar9` (low)

The following table shows the `por_mpu_m2_prbar9` lower register bit assignments.

Table 4-1784 `por_mpu_por_mpu_m2_prbar9` (low)

Bits	Field name	Description	Type	Reset
31:12	region9_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region9_br	Region 9 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region9_ap	Region 9 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar9

MPU master 0 programmable limit address register 9.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h18A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

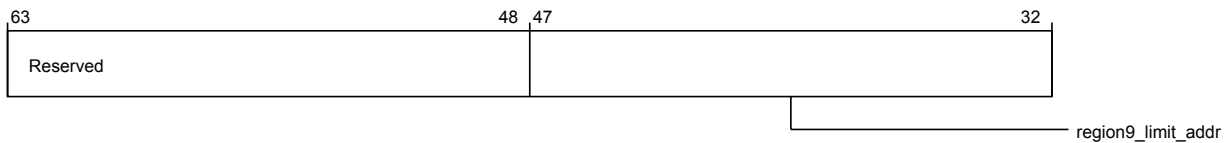


Figure 4-1768 por_mpu_por_mpu_m2_prlar9 (high)

The following table shows the por_mpu_m2_prlar9 higher register bit assignments.

Table 4-1785 por_mpu_por_mpu_m2_prlar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

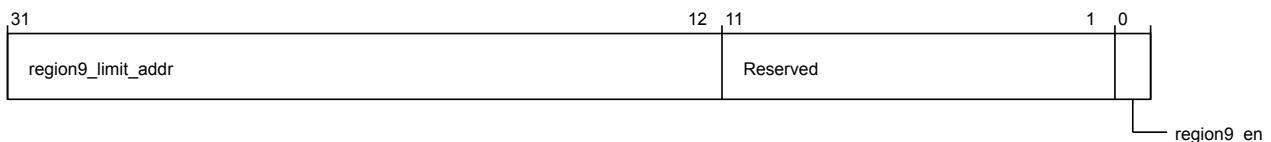


Figure 4-1769 por_mpu_por_mpu_m2_prlar9 (low)

The following table shows the por_mpu_m2_prlar9 lower register bit assignments.

Table 4-1786 por_mpu_por_mpu_m2_prlar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region9_en	Region 9 enable.	RW	1'b0

por_mpu_m2_prbar10

MPU master 0 programmable base address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h18B0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

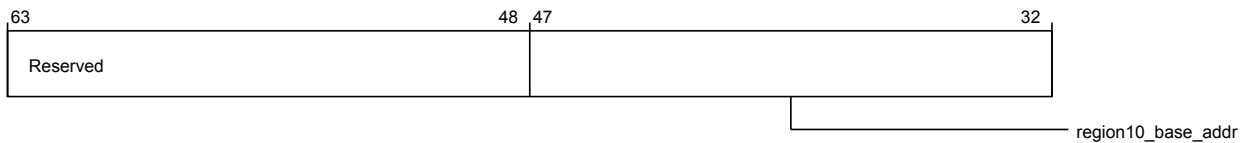


Figure 4-1770 `por_mpu_m2_prbar10` (high)

The following table shows the `por_mpu_m2_prbar10` higher register bit assignments.

Table 4-1787 `por_mpu_m2_prbar10` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

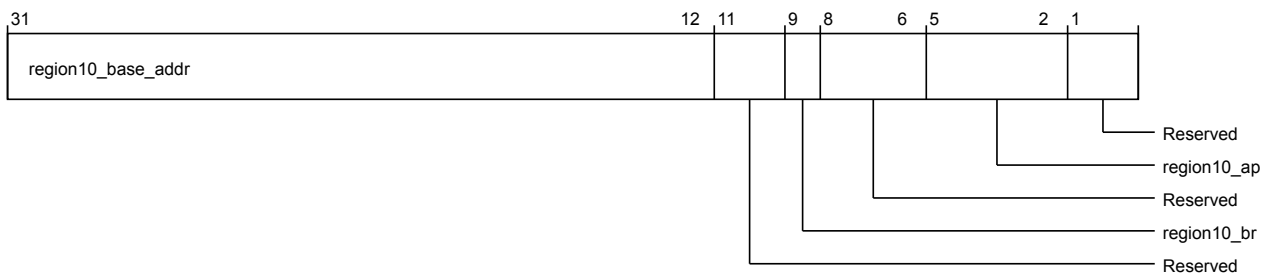


Figure 4-1771 `por_mpu_m2_prbar10` (low)

The following table shows the `por_mpu_m2_prbar10` lower register bit assignments.

Table 4-1788 `por_mpu_m2_prbar10` (low)

Bits	Field name	Description	Type	Reset
31:12	region10_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1788 por_mpu_por_mpu_m2_prbar10 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region10_br	Region 10 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region10_ap	Region 10 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar10

MPU master 0 programmable limit address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h18B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

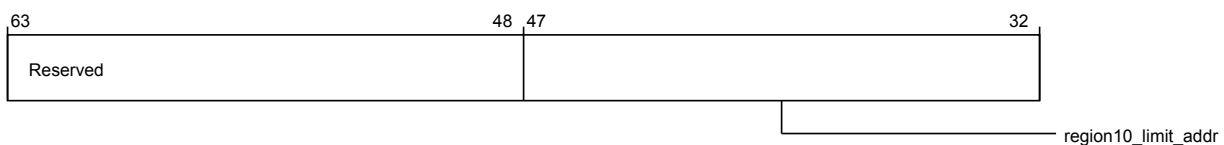


Figure 4-1772 por_mpu_por_mpu_m2_prlar10 (high)

The following table shows the por_mpu_m2_prlar10 higher register bit assignments.

Table 4-1789 por_mpu_por_mpu_m2_prlar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

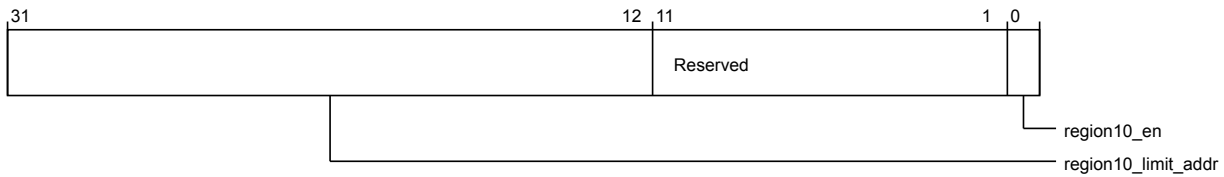


Figure 4-1773 `por_mpu_por_mpu_m2_prlar10` (low)

The following table shows the `por_mpu_m2_prlar10` lower register bit assignments.

Table 4-1790 `por_mpu_por_mpu_m2_prlar10` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region10_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region10_en</code>	Region 10 enable.	RW	1'b0

`por_mpu_m2_prbar11`

MPU master 0 programmable base address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h18C0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

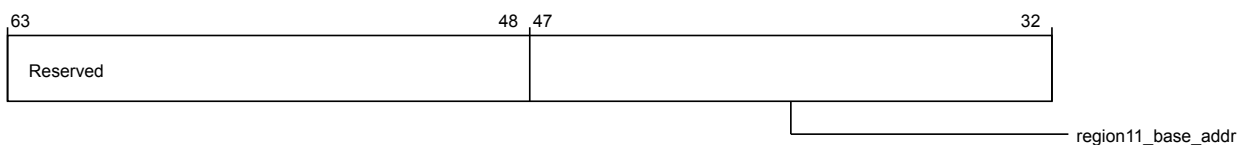


Figure 4-1774 `por_mpu_por_mpu_m2_prbar11` (high)

The following table shows the `por_mpu_m2_prbar11` higher register bit assignments.

Table 4-1791 `por_mpu_por_mpu_m2_prbar11` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region11_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

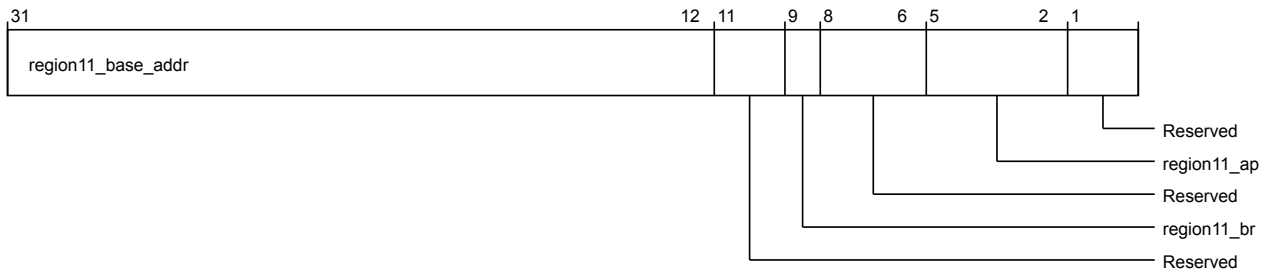


Figure 4-1775 `por_mpu_m2_prbar11` (low)

The following table shows the `por_mpu_m2_prbar11` lower register bit assignments.

Table 4-1792 `por_mpu_m2_prbar11` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region11_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region11_br</code>	Region 11 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region11_ap</code>	Region 11 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m2_prlar11`

MPU master 0 programmable limit address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h18C8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

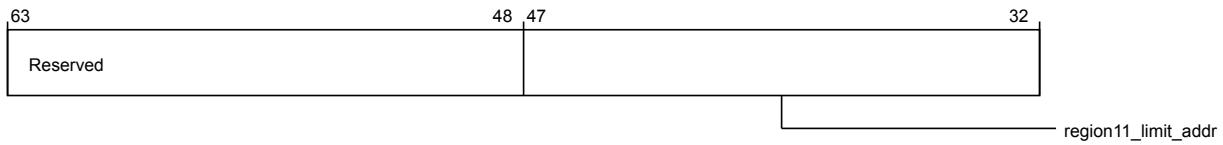


Figure 4-1776 por_mpu_m2_prlar11 (high)

The following table shows the por_mpu_m2_prlar11 higher register bit assignments.

Table 4-1793 por_mpu_m2_prlar11 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

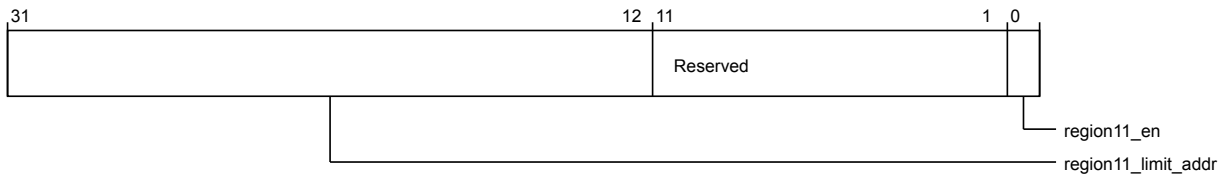


Figure 4-1777 por_mpu_m2_prlar11 (low)

The following table shows the por_mpu_m2_prlar11 lower register bit assignments.

Table 4-1794 por_mpu_m2_prlar11 (low)

Bits	Field name	Description	Type	Reset
31:12	region11_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region11_en	Region 11 enable.	RW	1'b0

por_mpu_m2_prbar12

MPU master 0 programmable base address register 12.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h18D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

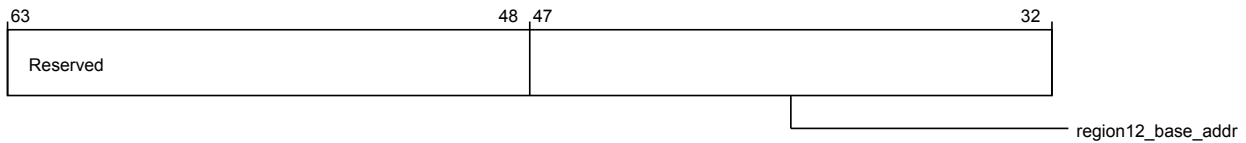


Figure 4-1778 `por_mpu_por_mpu_m2_prbar12` (high)

The following table shows the `por_mpu_m2_prbar12` higher register bit assignments.

Table 4-1795 `por_mpu_por_mpu_m2_prbar12` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region12_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

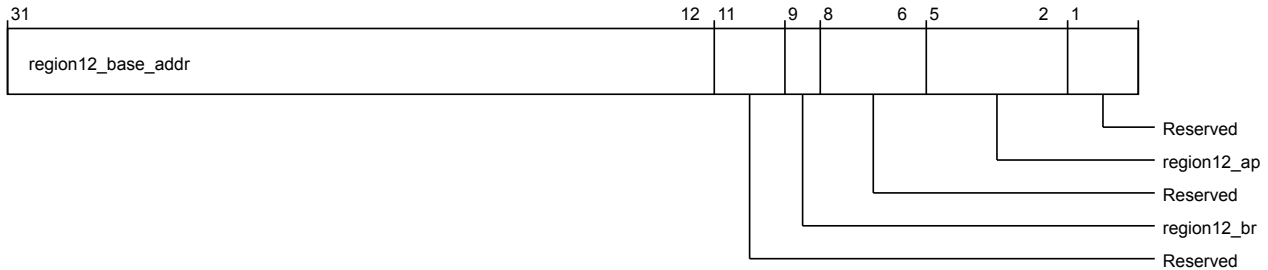


Figure 4-1779 `por_mpu_por_mpu_m2_prbar12` (low)

The following table shows the `por_mpu_m2_prbar12` lower register bit assignments.

Table 4-1796 `por_mpu_por_mpu_m2_prbar12` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region12_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region12_br</code>	Region 12 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region12_ap</code>	Region 12 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar12

MPU master 0 programmable limit address register 12.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h18D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

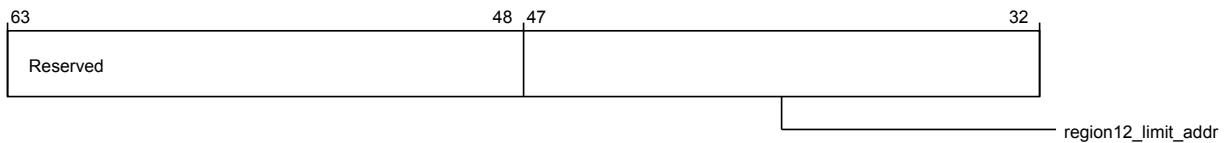


Figure 4-1780 por_mpu_por_mpu_m2_prlar12 (high)

The following table shows the por_mpu_m2_prlar12 higher register bit assignments.

Table 4-1797 por_mpu_por_mpu_m2_prlar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

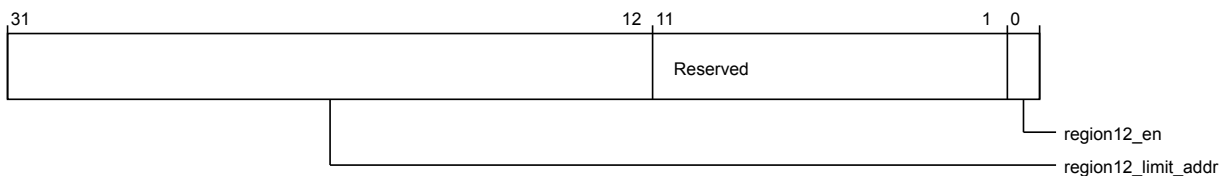


Figure 4-1781 por_mpu_por_mpu_m2_prlar12 (low)

The following table shows the por_mpu_m2_prlar12 lower register bit assignments.

Table 4-1798 por_mpu_por_mpu_m2_prlar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region12_en	Region 12 enable.	RW	1'b0

por_mpu_m2_prbar13

MPU master 0 programmable base address register 13.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h18E0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

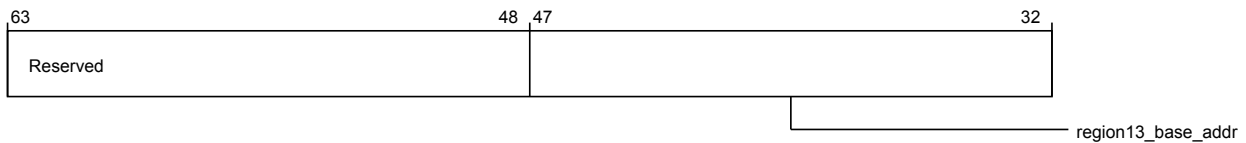


Figure 4-1782 por_mpu_por_mpu_m2_prbar13 (high)

The following table shows the por_mpu_m2_prbar13 higher register bit assignments.

Table 4-1799 por_mpu_por_mpu_m2_prbar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

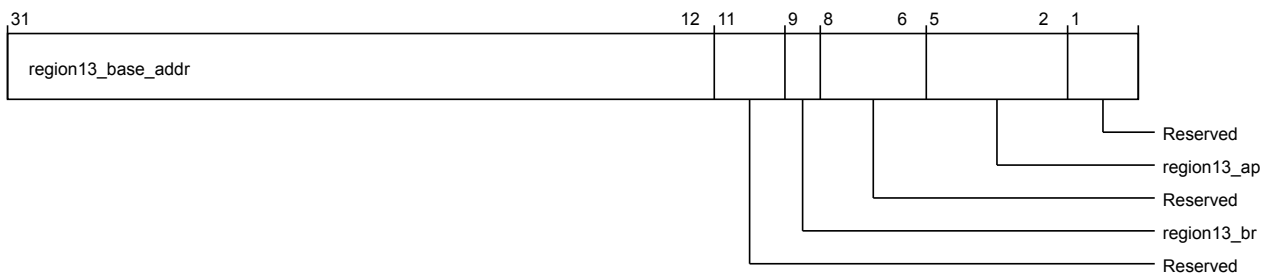


Figure 4-1783 por_mpu_por_mpu_m2_prbar13 (low)

The following table shows the por_mpu_m2_prbar13 lower register bit assignments.

Table 4-1800 por_mpu_por_mpu_m2_prbar13 (low)

Bits	Field name	Description	Type	Reset
31:12	region13_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1800 por_mpu_por_mpu_m2_prbar13 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region13_br	Region 13 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region13_ap	Region 13 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar13

MPU master 0 programmable limit address register 13.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h18E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

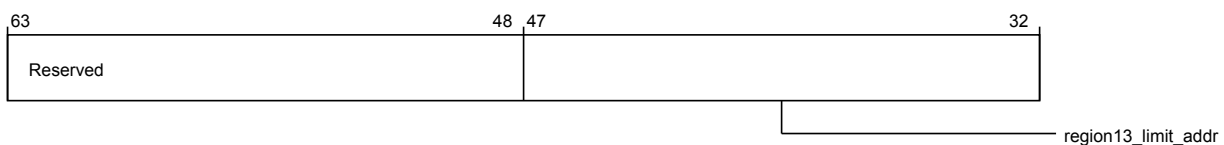


Figure 4-1784 por_mpu_por_mpu_m2_prlar13 (high)

The following table shows the por_mpu_m2_prlar13 higher register bit assignments.

Table 4-1801 por_mpu_por_mpu_m2_prlar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

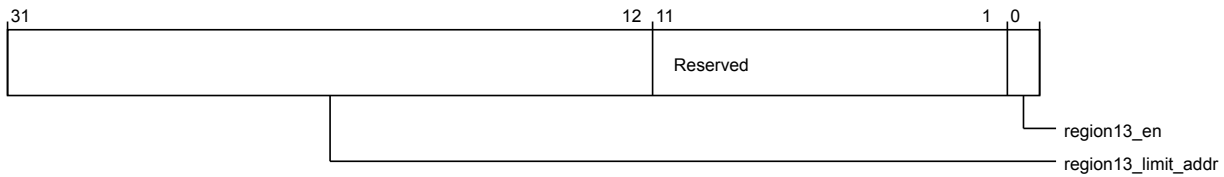


Figure 4-1785 `por_mpu_por_mpu_m2_prlar13` (low)

The following table shows the `por_mpu_m2_prlar13` lower register bit assignments.

Table 4-1802 `por_mpu_por_mpu_m2_prlar13` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region13_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region13_en</code>	Region 13 enable.	RW	1'b0

`por_mpu_m2_prbar14`

MPU master 0 programmable base address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h18F0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

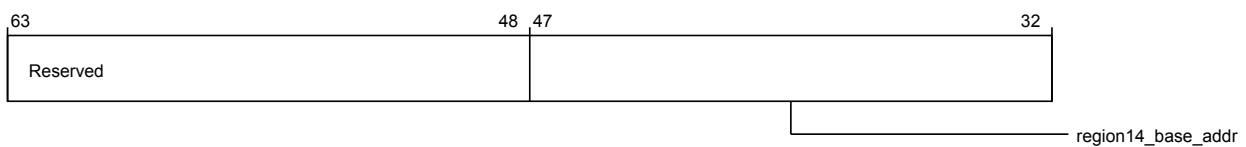


Figure 4-1786 `por_mpu_por_mpu_m2_prbar14` (high)

The following table shows the `por_mpu_m2_prbar14` higher register bit assignments.

Table 4-1803 `por_mpu_por_mpu_m2_prbar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region14_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

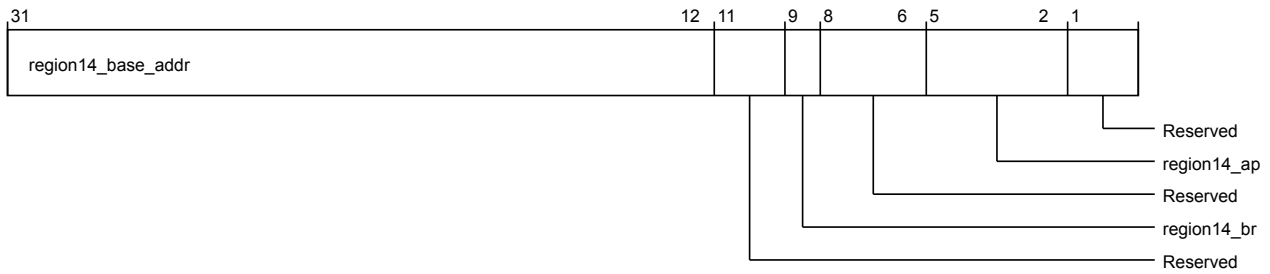


Figure 4-1787 `por_mpu_por_mpu_m2_prbar14` (low)

The following table shows the `por_mpu_m2_prbar14` lower register bit assignments.

Table 4-1804 `por_mpu_por_mpu_m2_prbar14` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region14_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region14_br</code>	Region 14 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region14_ap</code>	Region 14 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m2_prlar14`

MPU master 0 programmable limit address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h18F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

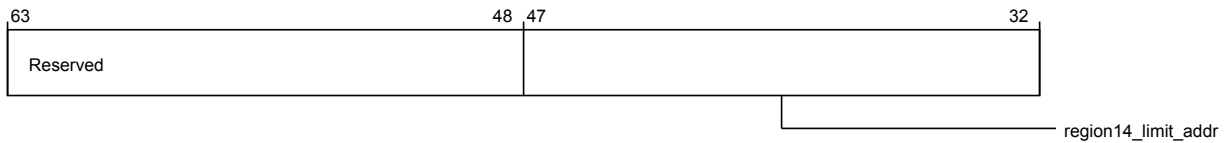


Figure 4-1788 por_mpu_m2_prlar14 (high)

The following table shows the por_mpu_m2_prlar14 higher register bit assignments.

Table 4-1805 por_mpu_m2_prlar14 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region14_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

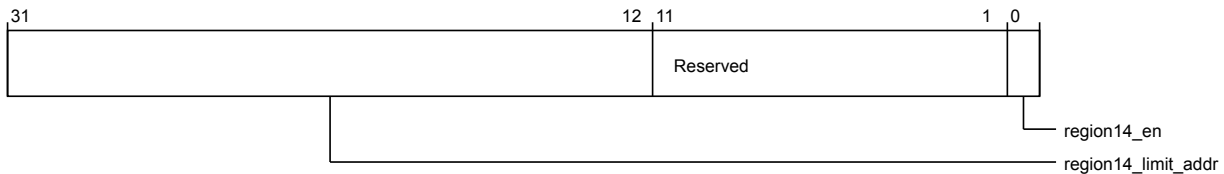


Figure 4-1789 por_mpu_m2_prlar14 (low)

The following table shows the por_mpu_m2_prlar14 lower register bit assignments.

Table 4-1806 por_mpu_m2_prlar14 (low)

Bits	Field name	Description	Type	Reset
31:12	region14_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region14_en	Region 14 enable.	RW	1'b0

por_mpu_m2_prbar15

MPU master 0 programmable base address register 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1900

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

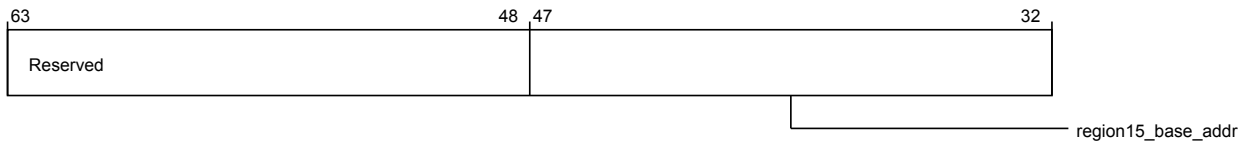


Figure 4-1790 por_mpu_por_mpu_m2_prbar15 (high)

The following table shows the por_mpu_m2_prbar15 higher register bit assignments.

Table 4-1807 por_mpu_por_mpu_m2_prbar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

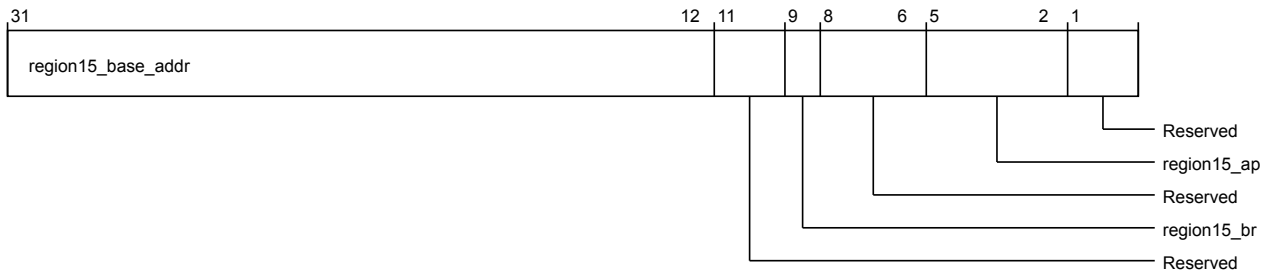


Figure 4-1791 por_mpu_por_mpu_m2_prbar15 (low)

The following table shows the por_mpu_m2_prbar15 lower register bit assignments.

Table 4-1808 por_mpu_por_mpu_m2_prbar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region15_br	Region 15 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region15_ap	Region 15 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar15

MPU master 0 programmable limit address register 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1908

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

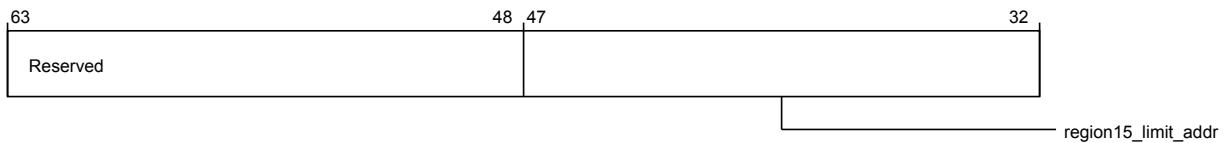


Figure 4-1792 por_mpu_por_mpu_m2_prlar15 (high)

The following table shows the por_mpu_m2_prlar15 higher register bit assignments.

Table 4-1809 por_mpu_por_mpu_m2_prlar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

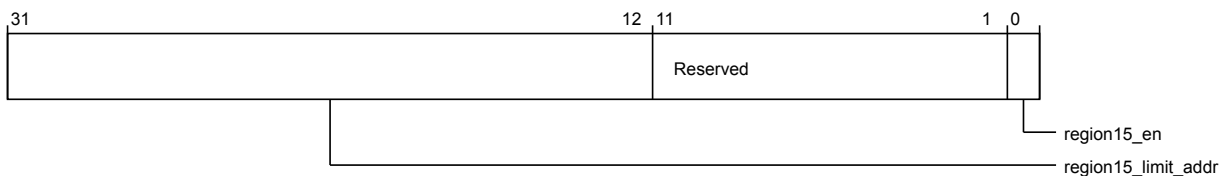


Figure 4-1793 por_mpu_por_mpu_m2_prlar15 (low)

The following table shows the por_mpu_m2_prlar15 lower register bit assignments.

Table 4-1810 por_mpu_por_mpu_m2_prlar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region15_en	Region 15 enable.	RW	1'b0

por_mpu_m2_prbar16

MPU master 0 programmable base address register 16.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1910
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

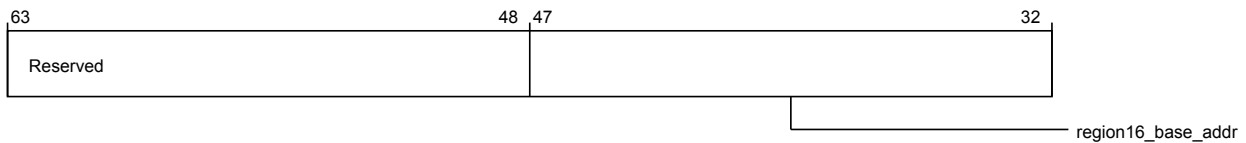


Figure 4-1794 por_mpu_por_mpu_m2_prbar16 (high)

The following table shows the por_mpu_m2_prbar16 higher register bit assignments.

Table 4-1811 por_mpu_por_mpu_m2_prbar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

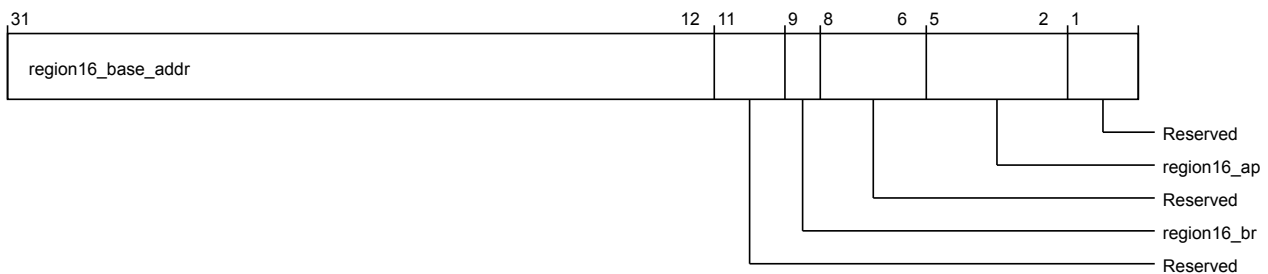


Figure 4-1795 por_mpu_por_mpu_m2_prbar16 (low)

The following table shows the por_mpu_m2_prbar16 lower register bit assignments.

Table 4-1812 por_mpu_por_mpu_m2_prbar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1812 por_mpu_por_mpu_m2_prbar16 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region16_br	Region 16 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region16_ap	Region 16 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar16

MPU master 0 programmable limit address register 16.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1918

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

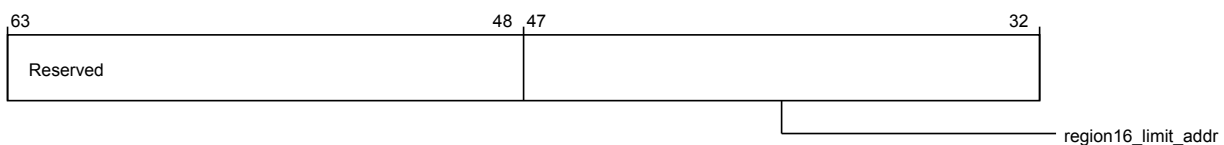


Figure 4-1796 por_mpu_por_mpu_m2_prlar16 (high)

The following table shows the por_mpu_m2_prlar16 higher register bit assignments.

Table 4-1813 por_mpu_por_mpu_m2_prlar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

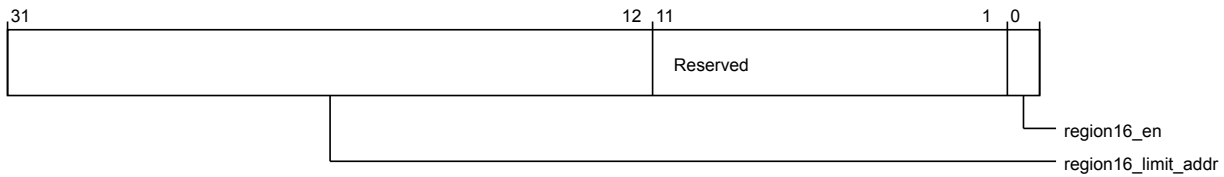


Figure 4-1797 `por_mpu_por_mpu_m2_prlar16` (low)

The following table shows the `por_mpu_m2_prlar16` lower register bit assignments.

Table 4-1814 `por_mpu_por_mpu_m2_prlar16` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region16_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region16_en</code>	Region 16 enable.	RW	1'b0

`por_mpu_m2_prbar17`

MPU master 0 programmable base address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1920

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

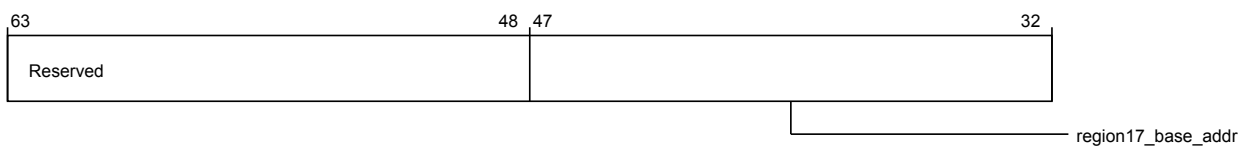


Figure 4-1798 `por_mpu_por_mpu_m2_prbar17` (high)

The following table shows the `por_mpu_m2_prbar17` higher register bit assignments.

Table 4-1815 `por_mpu_por_mpu_m2_prbar17` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region17_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

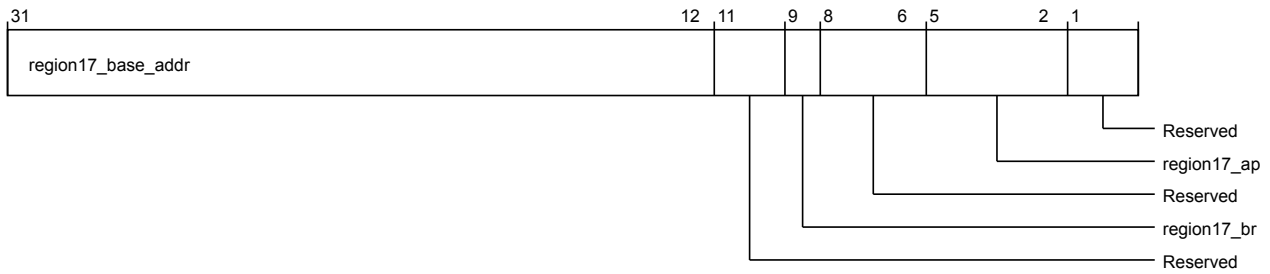


Figure 4-1799 `por_mpu_por_mpu_m2_prbar17` (low)

The following table shows the `por_mpu_m2_prbar17` lower register bit assignments.

Table 4-1816 `por_mpu_por_mpu_m2_prbar17` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region17_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region17_br</code>	Region 17 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region17_ap</code>	Region 17 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m2_prlar17`

MPU master 0 programmable limit address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1928

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

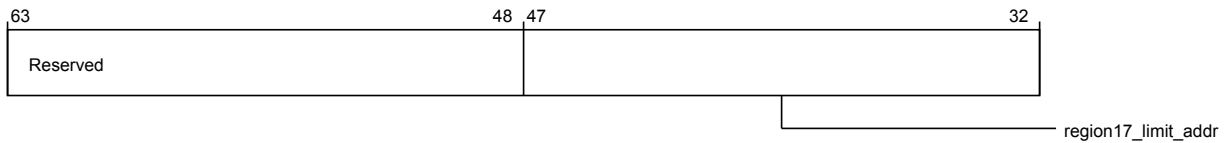


Figure 4-1800 por_mpu_m2_prlar17 (high)

The following table shows the por_mpu_m2_prlar17 higher register bit assignments.

Table 4-1817 por_mpu_m2_prlar17 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

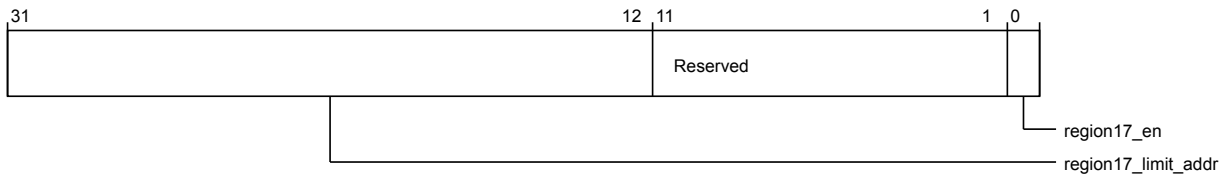


Figure 4-1801 por_mpu_m2_prlar17 (low)

The following table shows the por_mpu_m2_prlar17 lower register bit assignments.

Table 4-1818 por_mpu_m2_prlar17 (low)

Bits	Field name	Description	Type	Reset
31:12	region17_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region17_en	Region 17 enable.	RW	1'b0

por_mpu_m2_prbar18

MPU master 0 programmable base address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1930
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

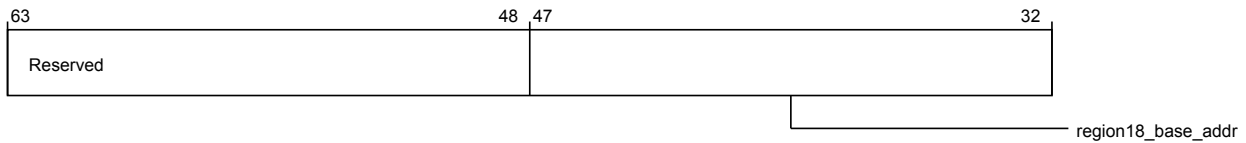


Figure 4-1802 `por_mpu_por_mpu_m2_prbar18` (high)

The following table shows the `por_mpu_m2_prbar18` higher register bit assignments.

Table 4-1819 `por_mpu_por_mpu_m2_prbar18` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

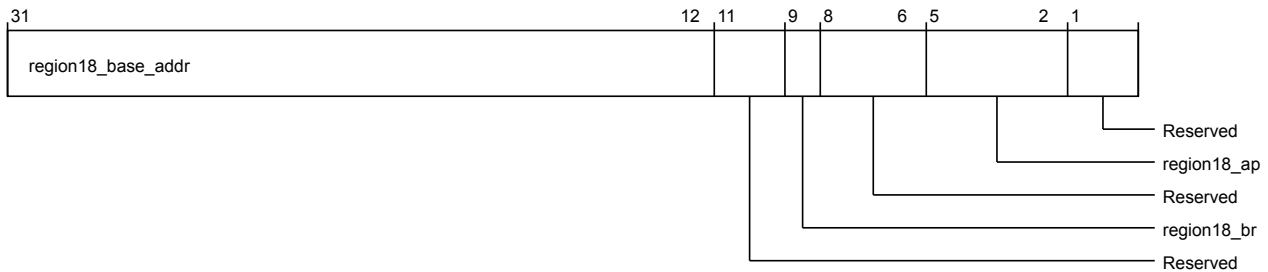


Figure 4-1803 `por_mpu_por_mpu_m2_prbar18` (low)

The following table shows the `por_mpu_m2_prbar18` lower register bit assignments.

Table 4-1820 `por_mpu_por_mpu_m2_prbar18` (low)

Bits	Field name	Description	Type	Reset
31:12	region18_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region18_br	Region 18 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region18_ap	Region 18 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar18

MPU master 0 programmable limit address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1938
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

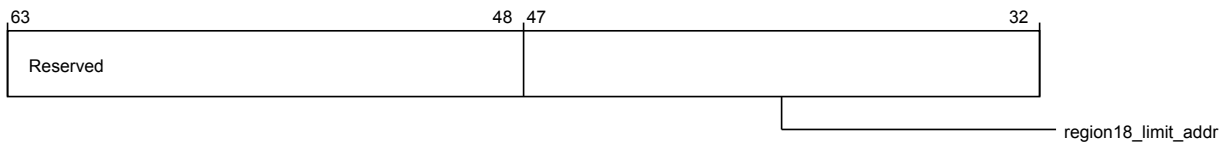


Figure 4-1804 por_mpu_por_mpu_m2_prlar18 (high)

The following table shows the por_mpu_m2_prlar18 higher register bit assignments.

Table 4-1821 por_mpu_por_mpu_m2_prlar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

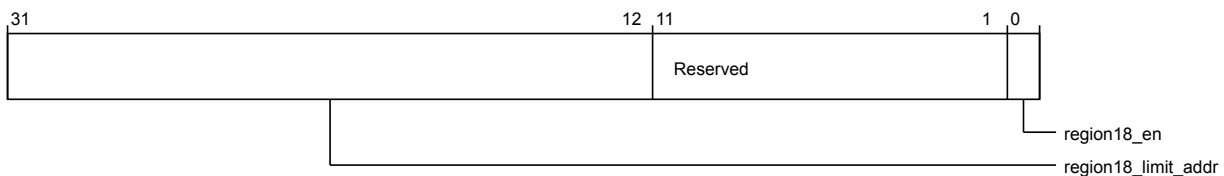


Figure 4-1805 por_mpu_por_mpu_m2_prlar18 (low)

The following table shows the por_mpu_m2_prlar18 lower register bit assignments.

Table 4-1822 por_mpu_por_mpu_m2_prlar18 (low)

Bits	Field name	Description	Type	Reset
31:12	region18_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region18_en	Region 18 enable.	RW	1'b0

por_mpu_m2_prbar19

MPU master 0 programmable base address register 19.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1940
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

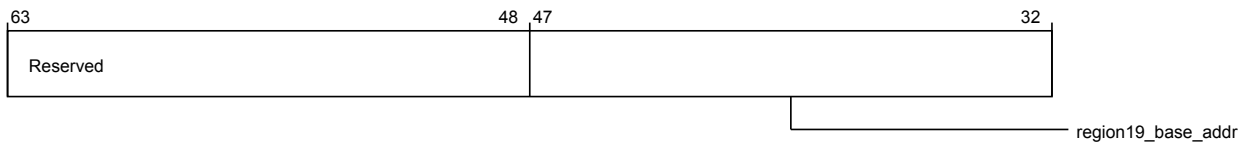


Figure 4-1806 por_mpu_por_mpu_m2_prbar19 (high)

The following table shows the por_mpu_m2_prbar19 higher register bit assignments.

Table 4-1823 por_mpu_por_mpu_m2_prbar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

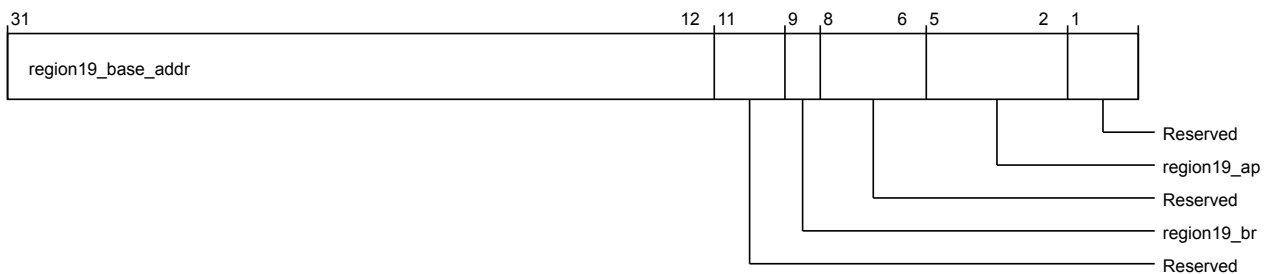


Figure 4-1807 por_mpu_por_mpu_m2_prbar19 (low)

The following table shows the por_mpu_m2_prbar19 lower register bit assignments.

Table 4-1824 por_mpu_por_mpu_m2_prbar19 (low)

Bits	Field name	Description	Type	Reset
31:12	region19_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1824 por_mpu_por_mpu_m2_prbar19 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region19_br	Region 19 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region19_ap	Region 19 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar19

MPU master 0 programmable limit address register 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1948

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

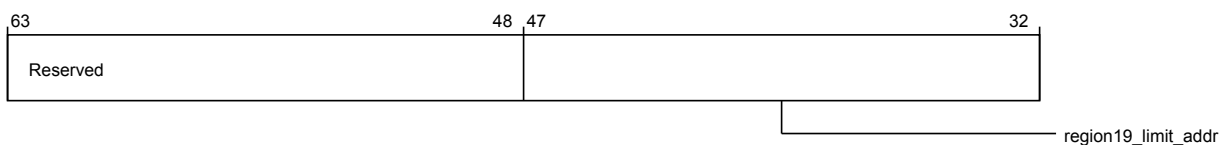


Figure 4-1808 por_mpu_por_mpu_m2_prlar19 (high)

The following table shows the por_mpu_m2_prlar19 higher register bit assignments.

Table 4-1825 por_mpu_por_mpu_m2_prlar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

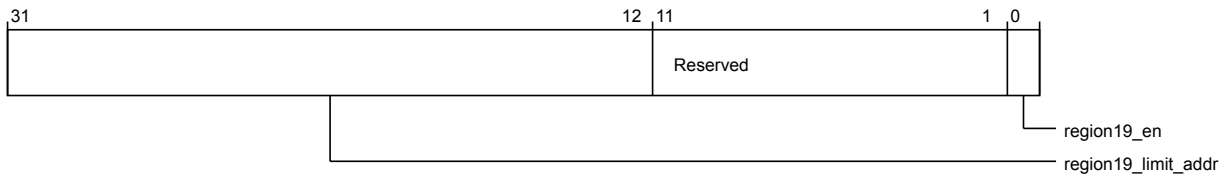


Figure 4-1809 `por_mpu_por_mpu_m2_prlar19` (low)

The following table shows the `por_mpu_m2_prlar19` lower register bit assignments.

Table 4-1826 `por_mpu_por_mpu_m2_prlar19` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region19_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region19_en</code>	Region 19 enable.	RW	1'b0

`por_mpu_m2_prbar20`

MPU master 0 programmable base address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1950

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

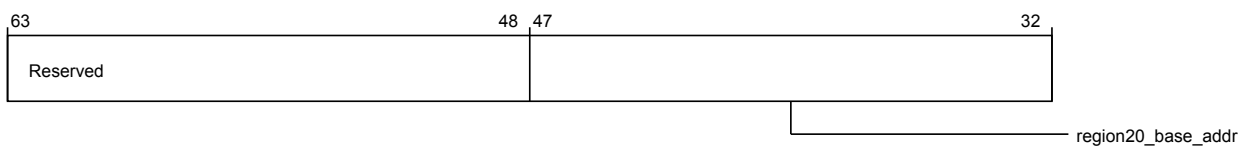


Figure 4-1810 `por_mpu_por_mpu_m2_prbar20` (high)

The following table shows the `por_mpu_m2_prbar20` higher register bit assignments.

Table 4-1827 `por_mpu_por_mpu_m2_prbar20` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region20_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

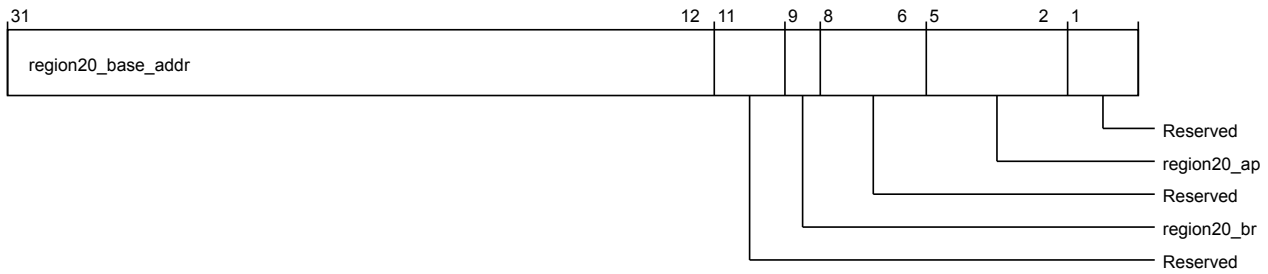


Figure 4-1811 `por_mpu_por_mpu_m2_prbar20` (low)

The following table shows the `por_mpu_m2_prbar20` lower register bit assignments.

Table 4-1828 `por_mpu_por_mpu_m2_prbar20` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region20_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region20_br</code>	Region 20 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region20_ap</code>	Region 20 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m2_prlar20`

MPU master 0 programmable limit address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1958

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

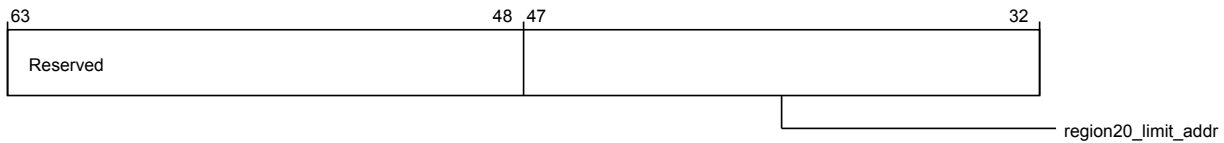


Figure 4-1812 `por_mpu_m2_prlar20` (high)

The following table shows the `por_mpu_m2_prlar20` higher register bit assignments.

Table 4-1829 `por_mpu_m2_prlar20` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region20_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

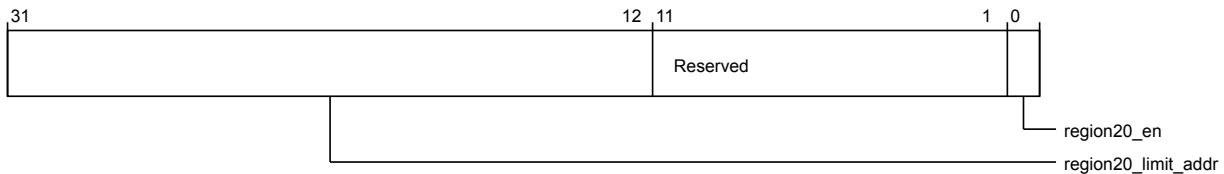


Figure 4-1813 `por_mpu_m2_prlar20` (low)

The following table shows the `por_mpu_m2_prlar20` lower register bit assignments.

Table 4-1830 `por_mpu_m2_prlar20` (low)

Bits	Field name	Description	Type	Reset
31:12	region20_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region20_en	Region 20 enable.	RW	1'b0

`por_mpu_m2_prbar21`

MPU master 0 programmable base address register 21.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1960
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

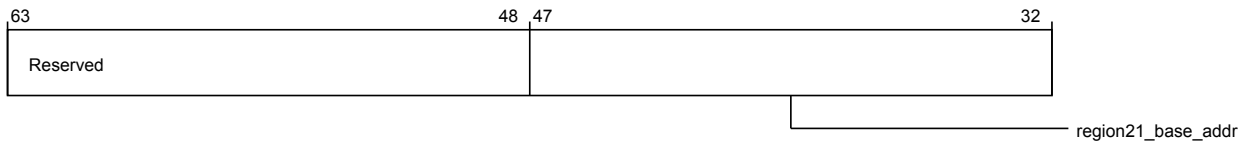


Figure 4-1814 `por_mpu_por_mpu_m2_prbar21` (high)

The following table shows the `por_mpu_m2_prbar21` higher register bit assignments.

Table 4-1831 `por_mpu_por_mpu_m2_prbar21` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

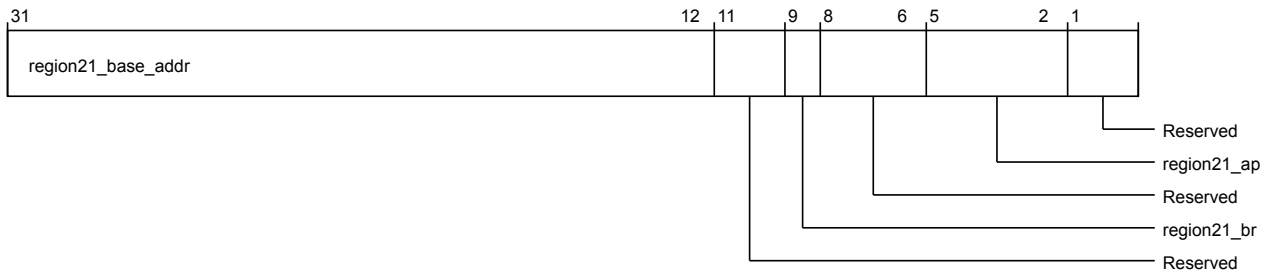


Figure 4-1815 `por_mpu_por_mpu_m2_prbar21` (low)

The following table shows the `por_mpu_m2_prbar21` lower register bit assignments.

Table 4-1832 `por_mpu_por_mpu_m2_prbar21` (low)

Bits	Field name	Description	Type	Reset
31:12	region21_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region21_br	Region 21 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region21_ap	Region 21 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar21

MPU master 0 programmable limit address register 21.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1968

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

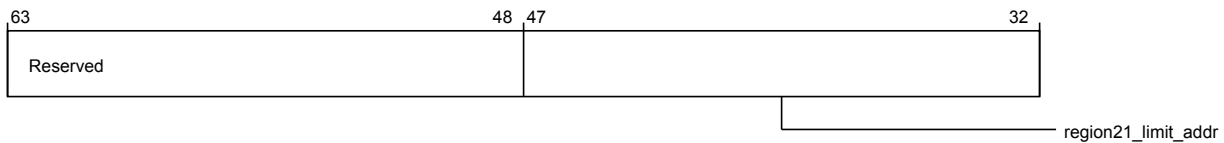


Figure 4-1816 por_mpu_por_mpu_m2_prlar21 (high)

The following table shows the por_mpu_m2_prlar21 higher register bit assignments.

Table 4-1833 por_mpu_por_mpu_m2_prlar21 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

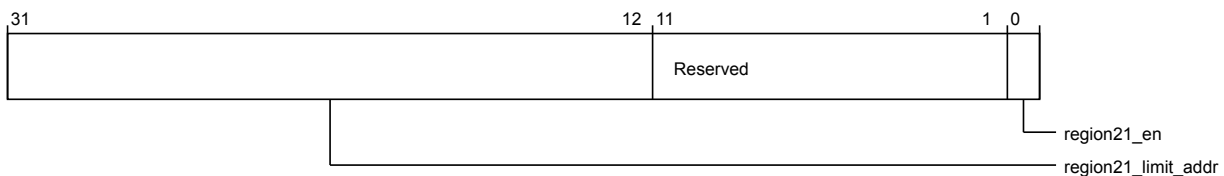


Figure 4-1817 por_mpu_por_mpu_m2_prlar21 (low)

The following table shows the por_mpu_m2_prlar21 lower register bit assignments.

Table 4-1834 por_mpu_por_mpu_m2_prlar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region21_en	Region 21 enable.	RW	1'b0

por_mpu_m2_prbar22

MPU master 0 programmable base address register 22.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1970
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

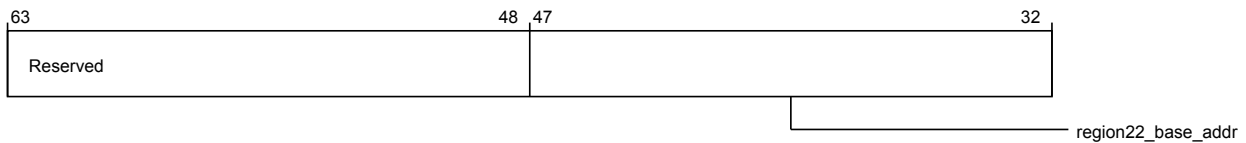


Figure 4-1818 por_mpu_por_mpu_m2_prbar22 (high)

The following table shows the `por_mpu_m2_prbar22` higher register bit assignments.

Table 4-1835 por_mpu_por_mpu_m2_prbar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

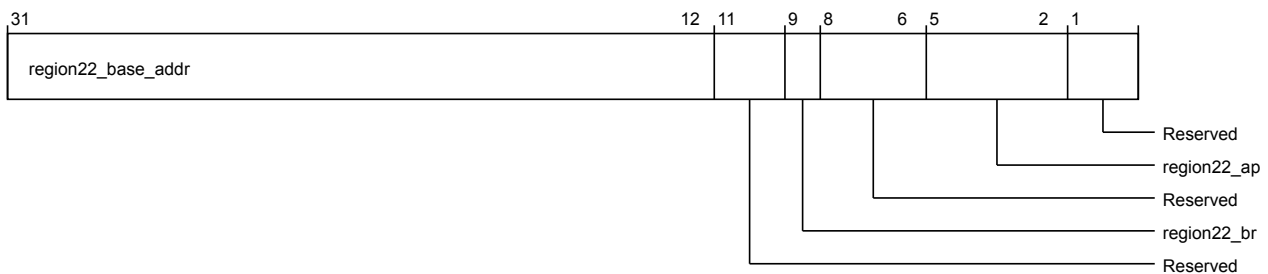


Figure 4-1819 por_mpu_por_mpu_m2_prbar22 (low)

The following table shows the `por_mpu_m2_prbar22` lower register bit assignments.

Table 4-1836 por_mpu_por_mpu_m2_prbar22 (low)

Bits	Field name	Description	Type	Reset
31:12	region22_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1836 por_mpu_por_mpu_m2_prbar22 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region22_br	Region 22 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region22_ap	Region 22 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar22

MPU master 0 programmable limit address register 22.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1978

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

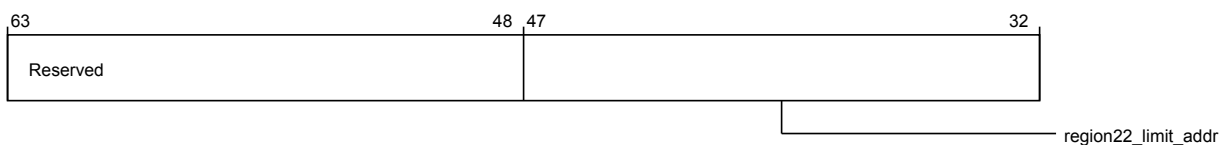


Figure 4-1820 por_mpu_por_mpu_m2_prlar22 (high)

The following table shows the por_mpu_m2_prlar22 higher register bit assignments.

Table 4-1837 por_mpu_por_mpu_m2_prlar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

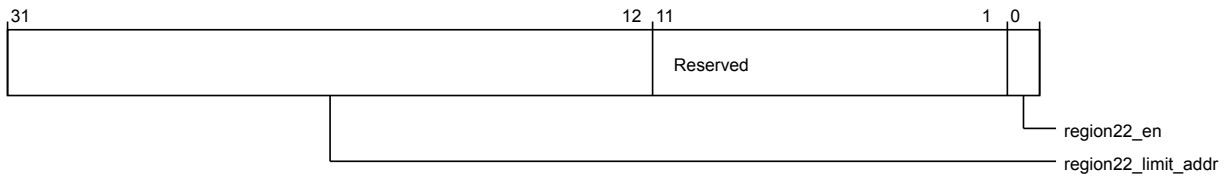


Figure 4-1821 `por_mpu_por_mpu_m2_prlar22` (low)

The following table shows the `por_mpu_m2_prlar22` lower register bit assignments.

Table 4-1838 `por_mpu_por_mpu_m2_prlar22` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region22_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region22_en</code>	Region 22 enable.	RW	1'b0

`por_mpu_m2_prbar23`

MPU master 0 programmable base address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

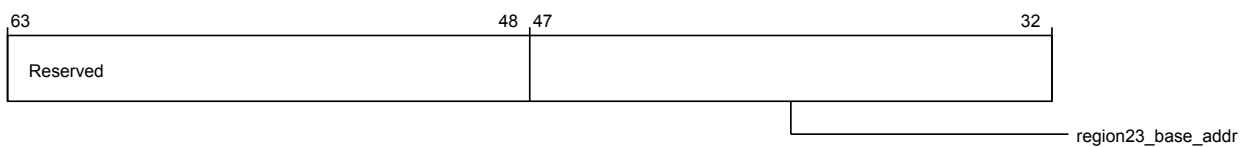


Figure 4-1822 `por_mpu_por_mpu_m2_prbar23` (high)

The following table shows the `por_mpu_m2_prbar23` higher register bit assignments.

Table 4-1839 `por_mpu_por_mpu_m2_prbar23` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region23_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

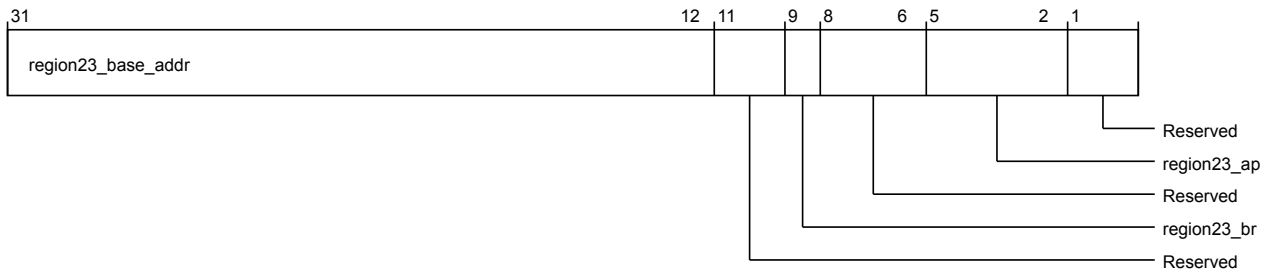


Figure 4-1823 por_mpu_m2_prbar23 (low)

The following table shows the por_mpu_m2_prbar23 lower register bit assignments.

Table 4-1840 por_mpu_m2_prbar23 (low)

Bits	Field name	Description	Type	Reset
31:12	region23_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region23_br	Region 23 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region23_ap	Region 23 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar23

MPU master 0 programmable limit address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1988

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

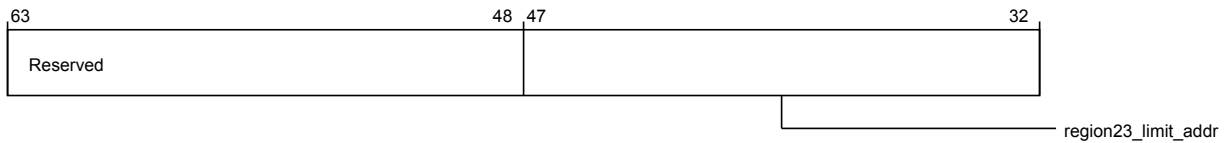


Figure 4-1824 por_mpu_m2_prlar23 (high)

The following table shows the por_mpu_m2_prlar23 higher register bit assignments.

Table 4-1841 por_mpu_m2_prlar23 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region23_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

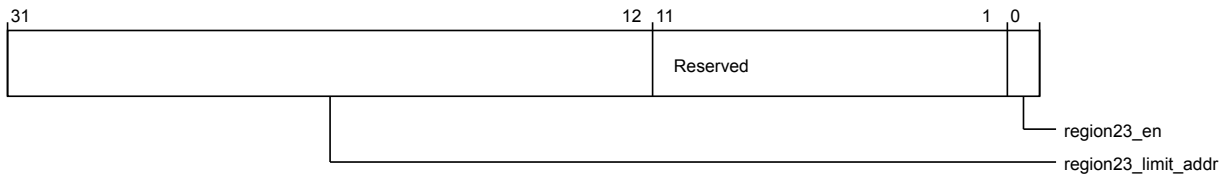


Figure 4-1825 por_mpu_m2_prlar23 (low)

The following table shows the por_mpu_m2_prlar23 lower register bit assignments.

Table 4-1842 por_mpu_m2_prlar23 (low)

Bits	Field name	Description	Type	Reset
31:12	region23_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region23_en	Region 23 enable.	RW	1'b0

por_mpu_m2_prbar24

MPU master 0 programmable base address register 24.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1990
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

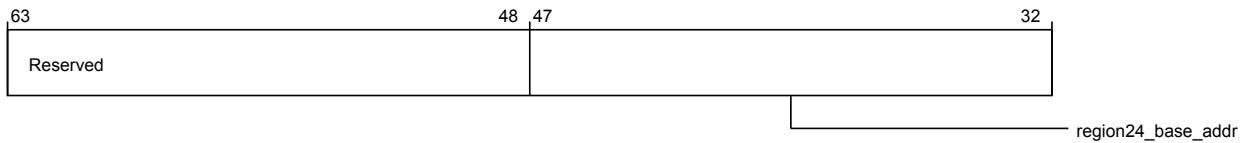


Figure 4-1826 `por_mpu_por_mpu_m2_prbar24` (high)

The following table shows the `por_mpu_m2_prbar24` higher register bit assignments.

Table 4-1843 `por_mpu_por_mpu_m2_prbar24` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

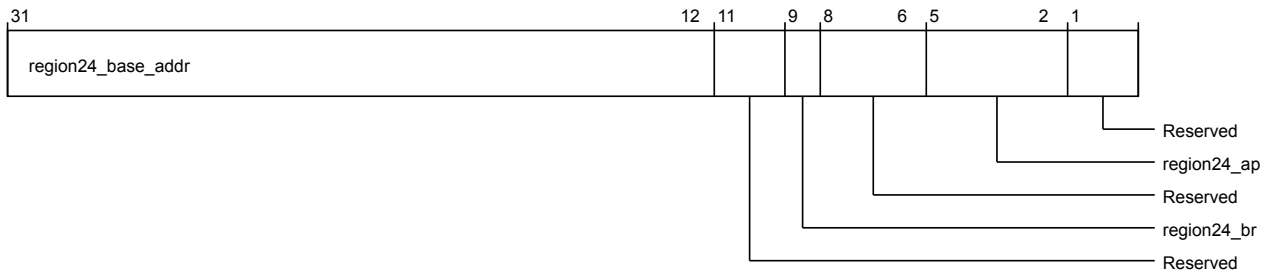


Figure 4-1827 `por_mpu_por_mpu_m2_prbar24` (low)

The following table shows the `por_mpu_m2_prbar24` lower register bit assignments.

Table 4-1844 `por_mpu_por_mpu_m2_prbar24` (low)

Bits	Field name	Description	Type	Reset
31:12	region24_base_addr	Bits [31:12] of base address of the range.	RW	20
11:10	Reserved	Reserved	RO	-
9	region24_br	Region 24 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region24_ap	Region 24 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar24

MPU master 0 programmable limit address register 24.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1998

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

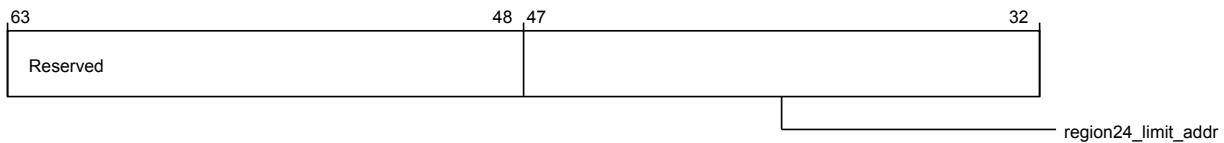


Figure 4-1828 por_mpu_por_mpu_m2_prlar24 (high)

The following table shows the por_mpu_m2_prlar24 higher register bit assignments.

Table 4-1845 por_mpu_por_mpu_m2_prlar24 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

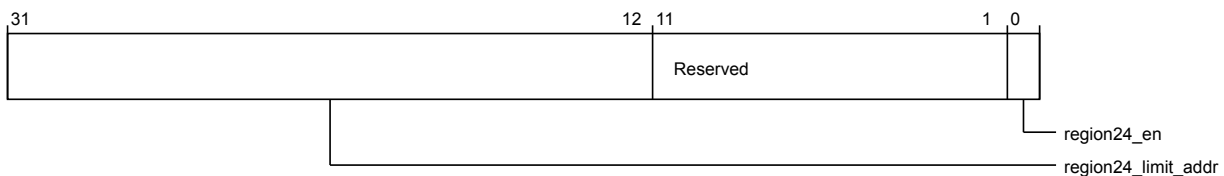


Figure 4-1829 por_mpu_por_mpu_m2_prlar24 (low)

The following table shows the por_mpu_m2_prlar24 lower register bit assignments.

Table 4-1846 por_mpu_por_mpu_m2_prlar24 (low)

Bits	Field name	Description	Type	Reset
31:12	region24_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region24_en	Region 24 enable.	RW	1'b0

por_mpu_m2_prbar25

MPU master 0 programmable base address register 25.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h19A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

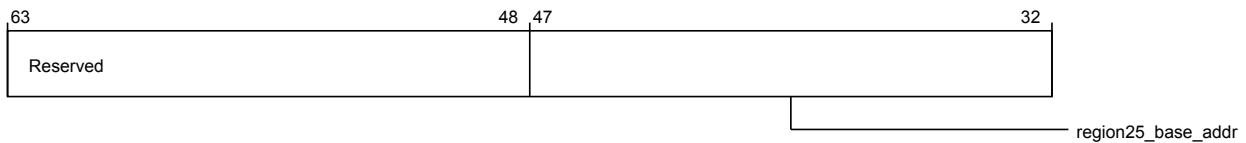


Figure 4-1830 por_mpu_por_mpu_m2_prbar25 (high)

The following table shows the por_mpu_m2_prbar25 higher register bit assignments.

Table 4-1847 por_mpu_por_mpu_m2_prbar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

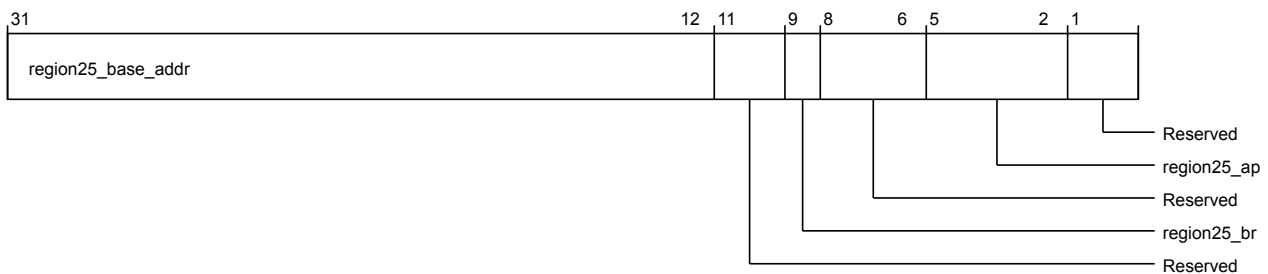


Figure 4-1831 por_mpu_por_mpu_m2_prbar25 (low)

The following table shows the por_mpu_m2_prbar25 lower register bit assignments.

Table 4-1848 por_mpu_por_mpu_m2_prbar25 (low)

Bits	Field name	Description	Type	Reset
31:12	region25_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1848 por_mpu_por_mpu_m2_prbar25 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region25_br	Region 25 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region25_ap	Region 25 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar25

MPU master 0 programmable limit address register 25.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h19A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

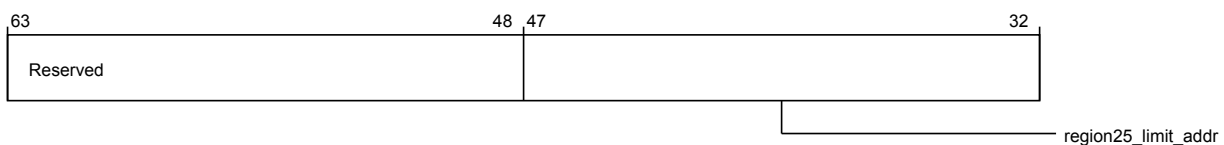


Figure 4-1832 por_mpu_por_mpu_m2_prlar25 (high)

The following table shows the por_mpu_m2_prlar25 higher register bit assignments.

Table 4-1849 por_mpu_por_mpu_m2_prlar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

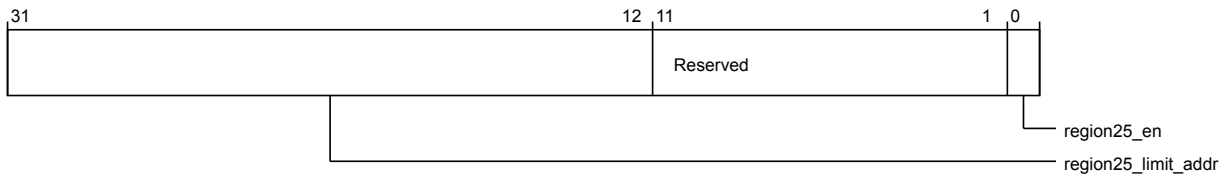


Figure 4-1833 `por_mpu_por_mpu_m2_prlar25` (low)

The following table shows the `por_mpu_m2_prlar25` lower register bit assignments.

Table 4-1850 `por_mpu_por_mpu_m2_prlar25` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region25_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region25_en</code>	Region 25 enable.	RW	1'b0

`por_mpu_m2_prbar26`

MPU master 0 programmable base address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h19B0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

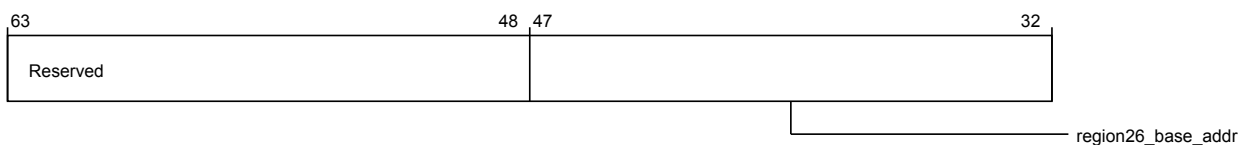


Figure 4-1834 `por_mpu_por_mpu_m2_prbar26` (high)

The following table shows the `por_mpu_m2_prbar26` higher register bit assignments.

Table 4-1851 `por_mpu_por_mpu_m2_prbar26` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region26_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

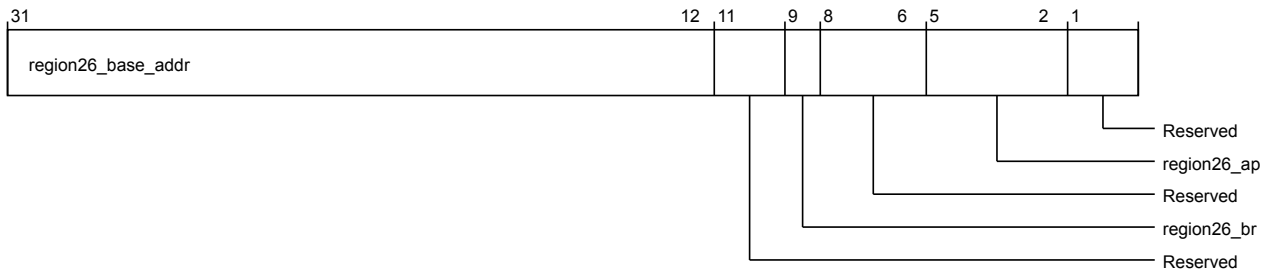


Figure 4-1835 por_mpu_m2_prbar26 (low)

The following table shows the por_mpu_m2_prbar26 lower register bit assignments.

Table 4-1852 por_mpu_m2_prbar26 (low)

Bits	Field name	Description	Type	Reset
31:12	region26_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region26_br	Region 26 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region26_ap	Region 26 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar26

MPU master 0 programmable limit address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h19B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

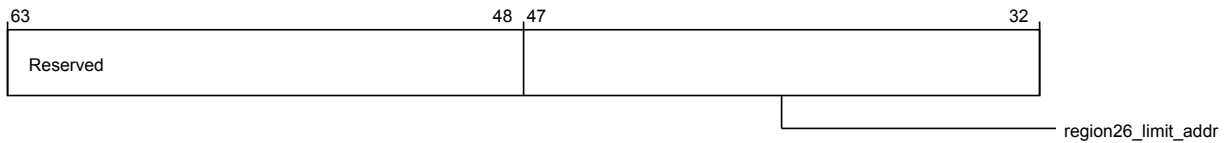


Figure 4-1836 `por_mpu_m2_prlar26` (high)

The following table shows the `por_mpu_m2_prlar26` higher register bit assignments.

Table 4-1853 `por_mpu_m2_prlar26` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region26_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

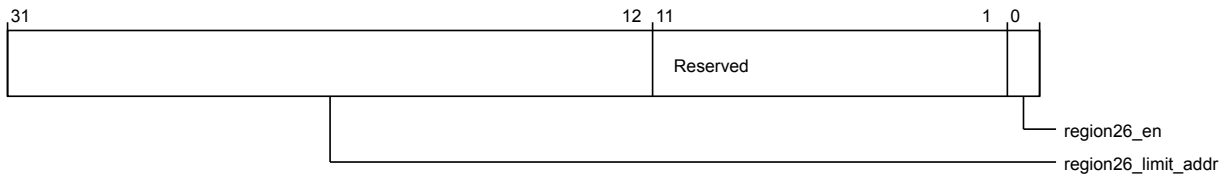


Figure 4-1837 `por_mpu_m2_prlar26` (low)

The following table shows the `por_mpu_m2_prlar26` lower register bit assignments.

Table 4-1854 `por_mpu_m2_prlar26` (low)

Bits	Field name	Description	Type	Reset
31:12	region26_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region26_en	Region 26 enable.	RW	1'b0

`por_mpu_m2_prbar27`

MPU master 0 programmable base address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h19C0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

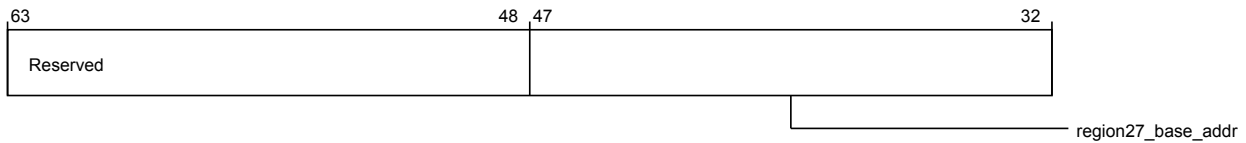


Figure 4-1838 por_mpu_por_mpu_m2_prbar27 (high)

The following table shows the por_mpu_m2_prbar27 higher register bit assignments.

Table 4-1855 por_mpu_por_mpu_m2_prbar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

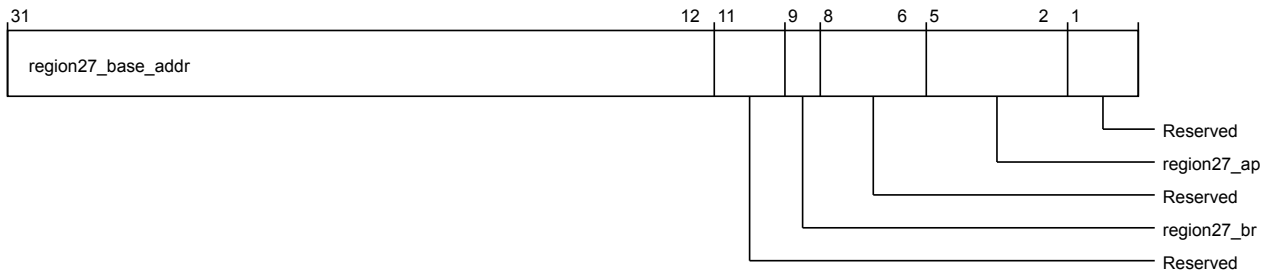


Figure 4-1839 por_mpu_por_mpu_m2_prbar27 (low)

The following table shows the por_mpu_m2_prbar27 lower register bit assignments.

Table 4-1856 por_mpu_por_mpu_m2_prbar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region27_br	Region 27 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region27_ap	Region 27 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar27

MPU master 0 programmable limit address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h19C8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

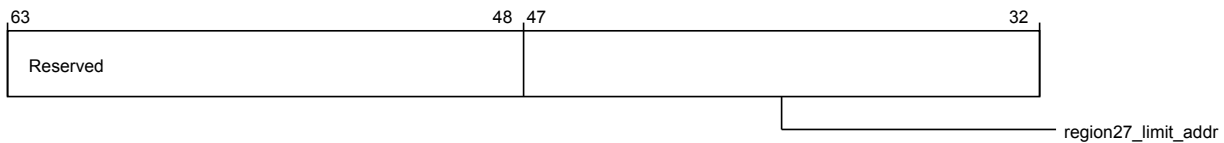


Figure 4-1840 por_mpu_por_mpu_m2_prlar27 (high)

The following table shows the por_mpu_m2_prlar27 higher register bit assignments.

Table 4-1857 por_mpu_por_mpu_m2_prlar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

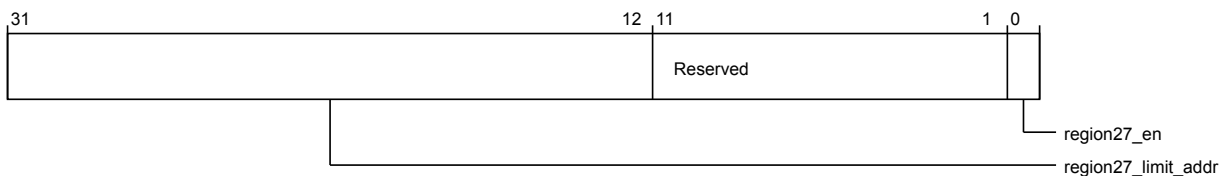


Figure 4-1841 por_mpu_por_mpu_m2_prlar27 (low)

The following table shows the por_mpu_m2_prlar27 lower register bit assignments.

Table 4-1858 por_mpu_por_mpu_m2_prlar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region27_en	Region 27 enable.	RW	1'b0

por_mpu_m2_prbar28

MPU master 0 programmable base address register 28.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h19D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

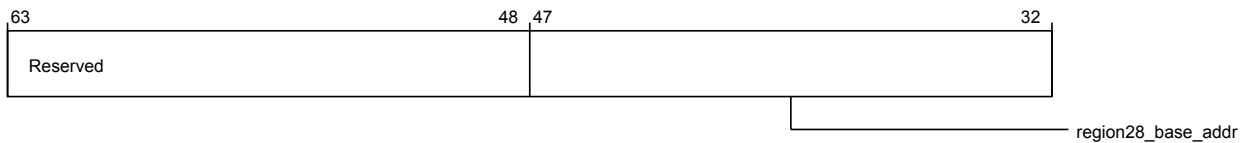


Figure 4-1842 por_mpu_por_mpu_m2_prbar28 (high)

The following table shows the por_mpu_m2_prbar28 higher register bit assignments.

Table 4-1859 por_mpu_por_mpu_m2_prbar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

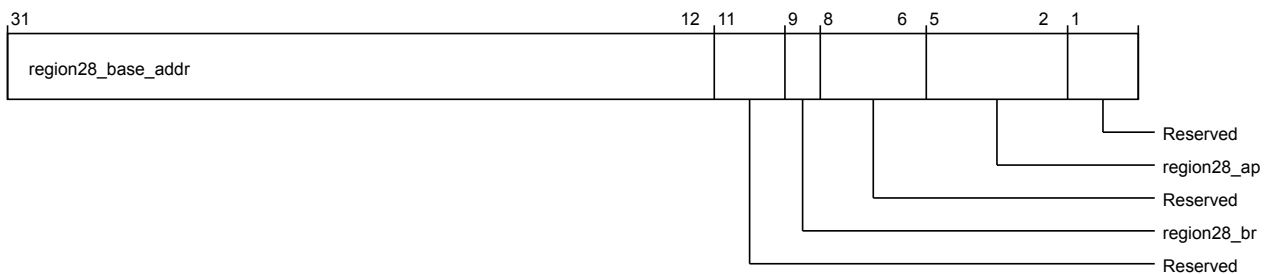


Figure 4-1843 por_mpu_por_mpu_m2_prbar28 (low)

The following table shows the por_mpu_m2_prbar28 lower register bit assignments.

Table 4-1860 por_mpu_por_mpu_m2_prbar28 (low)

Bits	Field name	Description	Type	Reset
31:12	region28_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1860 por_mpu_por_mpu_m2_prbar28 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region28_br	Region 28 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region28_ap	Region 28 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar28

MPU master 0 programmable limit address register 28.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h19D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

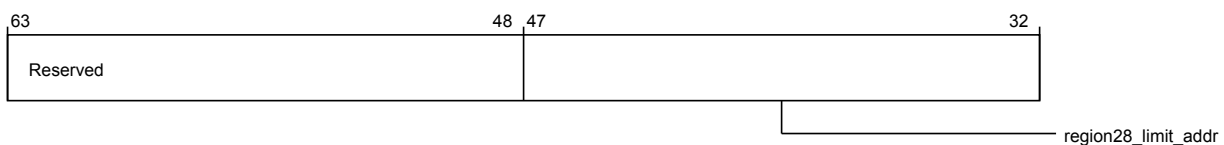


Figure 4-1844 por_mpu_por_mpu_m2_prlar28 (high)

The following table shows the por_mpu_m2_prlar28 higher register bit assignments.

Table 4-1861 por_mpu_por_mpu_m2_prlar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

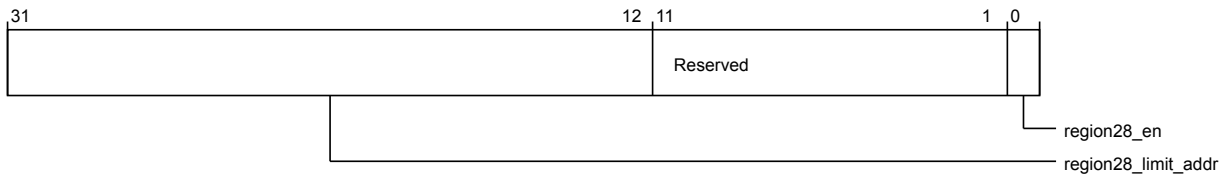


Figure 4-1845 `por_mpu_por_mpu_m2_prlar28` (low)

The following table shows the `por_mpu_m2_prlar28` lower register bit assignments.

Table 4-1862 `por_mpu_por_mpu_m2_prlar28` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region28_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region28_en</code>	Region 28 enable.	RW	1'b0

`por_mpu_m2_prbar29`

MPU master 0 programmable base address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h19E0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

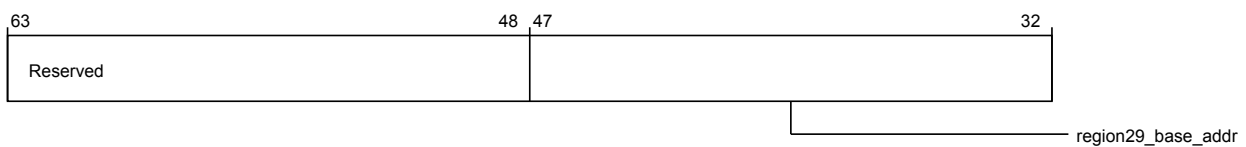


Figure 4-1846 `por_mpu_por_mpu_m2_prbar29` (high)

The following table shows the `por_mpu_m2_prbar29` higher register bit assignments.

Table 4-1863 `por_mpu_por_mpu_m2_prbar29` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region29_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

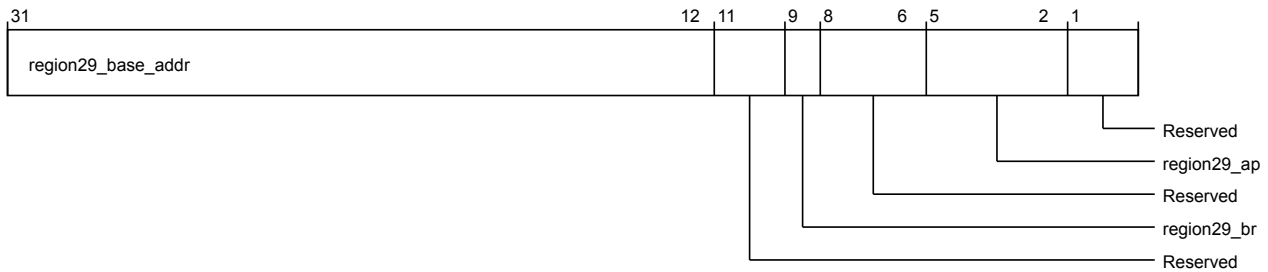


Figure 4-1847 por_mpu_m2_prbar29 (low)

The following table shows the por_mpu_m2_prbar29 lower register bit assignments.

Table 4-1864 por_mpu_m2_prbar29 (low)

Bits	Field name	Description	Type	Reset
31:12	region29_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region29_br	Region 29 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region29_ap	Region 29 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar29

MPU master 0 programmable limit address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h19E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

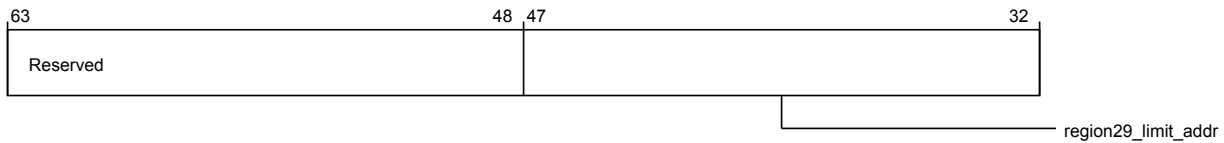


Figure 4-1848 por_mpu_m2_prlar29 (high)

The following table shows the por_mpu_m2_prlar29 higher register bit assignments.

Table 4-1865 por_mpu_m2_prlar29 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region29_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

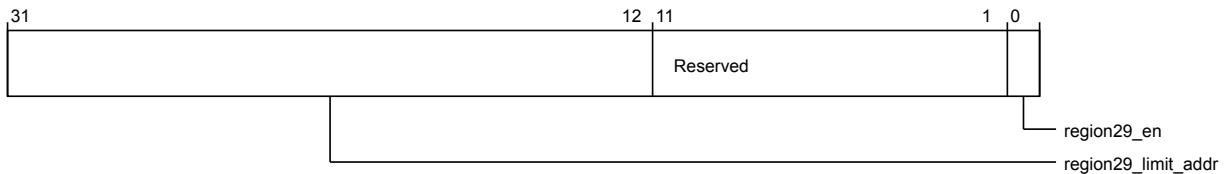


Figure 4-1849 por_mpu_m2_prlar29 (low)

The following table shows the por_mpu_m2_prlar29 lower register bit assignments.

Table 4-1866 por_mpu_m2_prlar29 (low)

Bits	Field name	Description	Type	Reset
31:12	region29_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region29_en	Region 29 enable.	RW	1'b0

por_mpu_m2_prbar30

MPU master 0 programmable base address register 30.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h19F0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

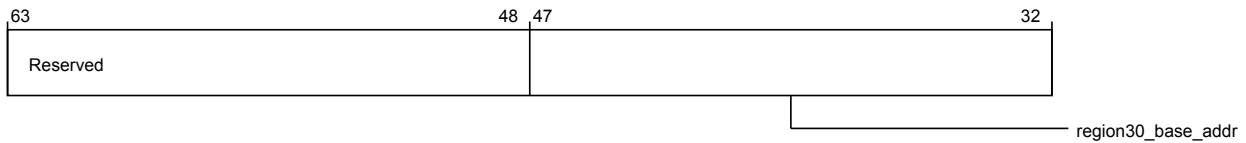


Figure 4-1850 por_mpu_por_mpu_m2_prbar30 (high)

The following table shows the por_mpu_m2_prbar30 higher register bit assignments.

Table 4-1867 por_mpu_por_mpu_m2_prbar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

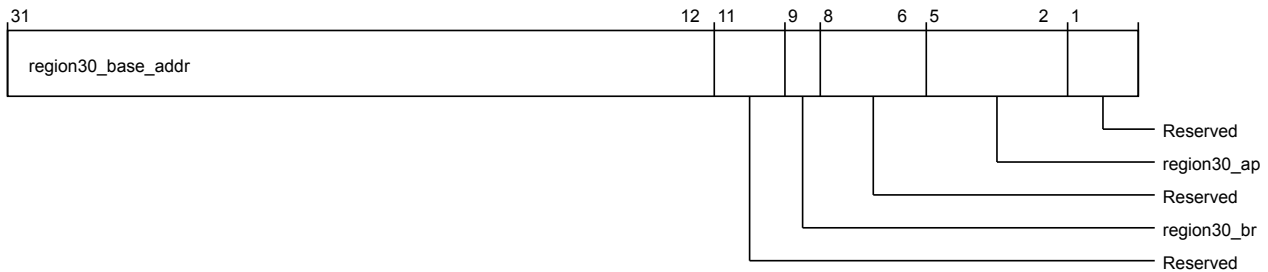


Figure 4-1851 por_mpu_por_mpu_m2_prbar30 (low)

The following table shows the por_mpu_m2_prbar30 lower register bit assignments.

Table 4-1868 por_mpu_por_mpu_m2_prbar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region30_br	Region 30 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region30_ap	Region 30 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar30

MPU master 0 programmable limit address register 30.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h19F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

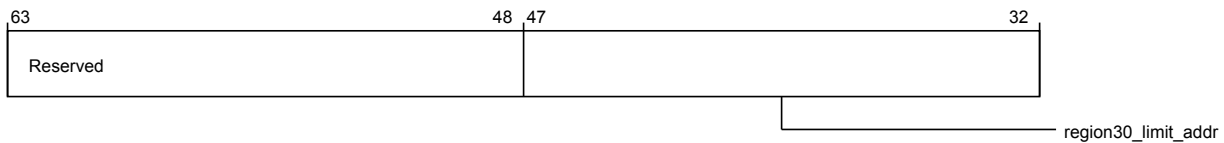


Figure 4-1852 por_mpu_por_mpu_m2_prlar30 (high)

The following table shows the por_mpu_m2_prlar30 higher register bit assignments.

Table 4-1869 por_mpu_por_mpu_m2_prlar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

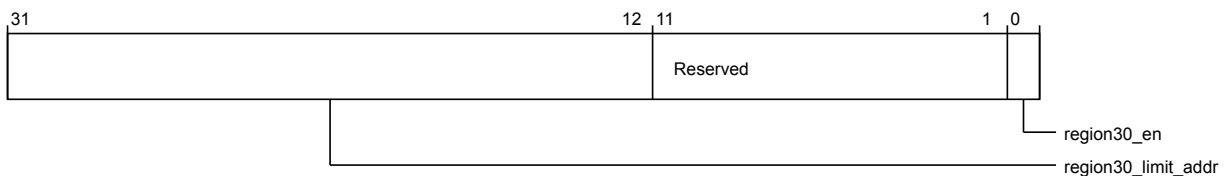


Figure 4-1853 por_mpu_por_mpu_m2_prlar30 (low)

The following table shows the por_mpu_m2_prlar30 lower register bit assignments.

Table 4-1870 por_mpu_por_mpu_m2_prlar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region30_en	Region 30 enable.	RW	1'b0

por_mpu_m2_prbar31

MPU master 0 programmable base address register 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1A00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

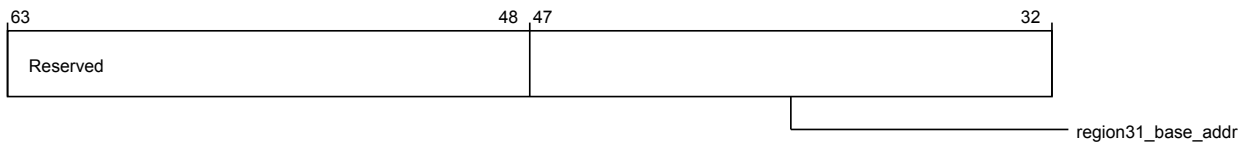


Figure 4-1854 por_mpu_por_mpu_m2_prbar31 (high)

The following table shows the por_mpu_m2_prbar31 higher register bit assignments.

Table 4-1871 por_mpu_por_mpu_m2_prbar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

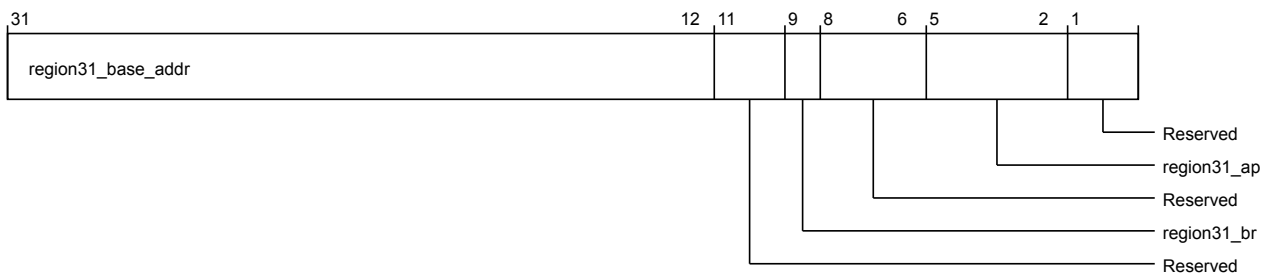


Figure 4-1855 por_mpu_por_mpu_m2_prbar31 (low)

The following table shows the por_mpu_m2_prbar31 lower register bit assignments.

Table 4-1872 por_mpu_por_mpu_m2_prbar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1872 por_mpu_por_mpu_m2_prbar31 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region31_br	Region 31 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region31_ap	Region 31 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m2_prlar31

MPU master 0 programmable limit address register 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1A08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

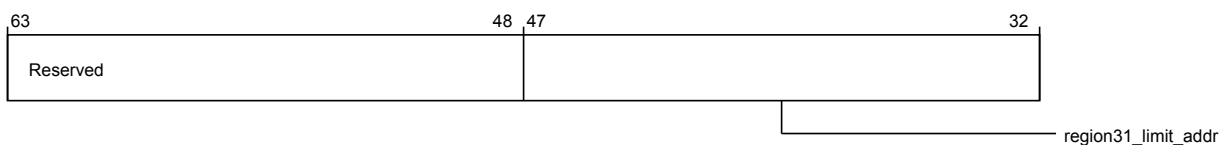


Figure 4-1856 por_mpu_por_mpu_m2_prlar31 (high)

The following table shows the por_mpu_m2_prlar31 higher register bit assignments.

Table 4-1873 por_mpu_por_mpu_m2_prlar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

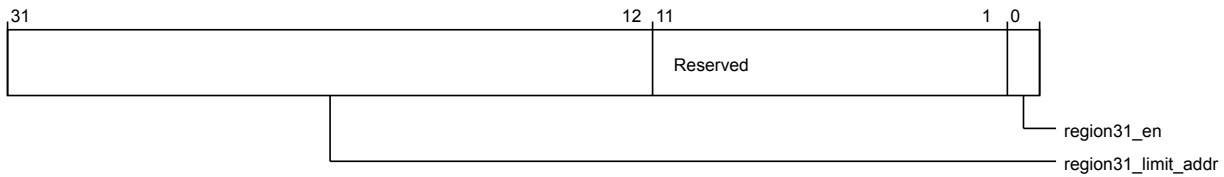


Figure 4-1857 por_mpu_por_mpu_m2_prlar31 (low)

The following table shows the por_mpu_m2_prlar31 lower register bit assignments.

Table 4-1874 por_mpu_por_mpu_m2_prlar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region31_en	Region 31 enable.	RW	1'b0

por_mpu_m3_ctl

Functions as the MPU Master 3 control register.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C00

Register reset 64'b010

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

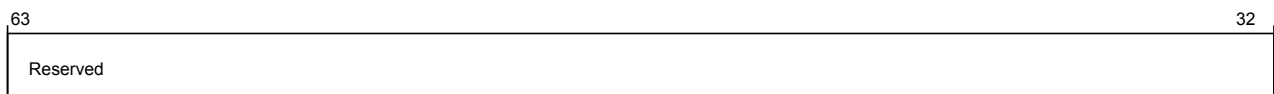


Figure 4-1858 por_mpu_por_mpu_m3_ctl (high)

The following table shows the por_mpu_m3_ctl higher register bit assignments.

Table 4-1875 por_mpu_por_mpu_m3_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

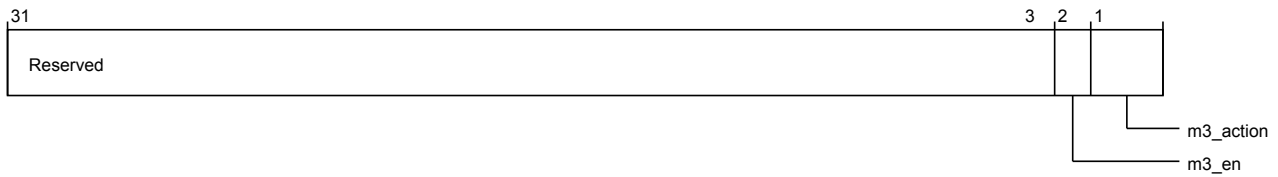


Figure 4-1859 por_mpu_m3_ctl (low)

The following table shows the por_mpu_m3_ctl lower register bit assignments.

Table 4-1876 por_mpu_m3_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	m3_en	MPU master 3 enable.	RW	1'b0
1:0	m3_action	Indicates action HN* should take if no access permission is granted 2'b00: FUSA interrupt 2'b01: Bus error to the originating bus master 2'b10: Both FUSA interrupt and bus error.	RW	2'b10

por_mpu_m3_prbar0

MPU master 0 programmable base address register 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

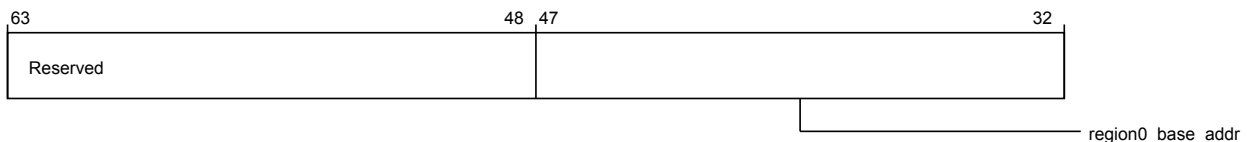


Figure 4-1860 por_mpu_m3_prbar0 (high)

The following table shows the por_mpu_m3_prbar0 higher register bit assignments.

Table 4-1877 por_mpu_por_mpu_m3_prbar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

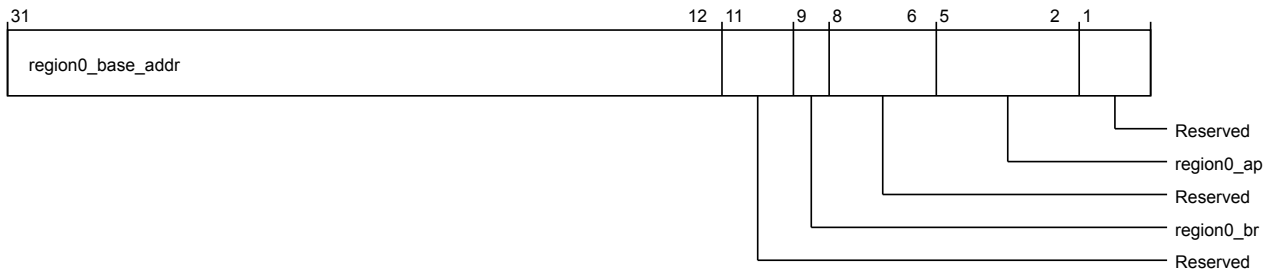


Figure 4-1861 por_mpu_por_mpu_m3_prbar0 (low)

The following table shows the por_mpu_m3_prbar0 lower register bit assignments.

Table 4-1878 por_mpu_por_mpu_m3_prbar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region0_br	Region 0 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region0_ap	Region 0 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar0

MPU master 0 programmable limit address register 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1C18
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

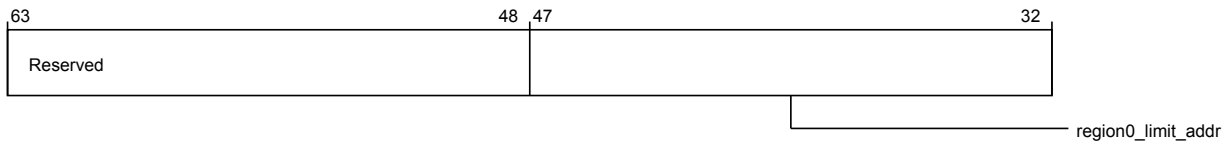


Figure 4-1862 por_mpu_m3_prlar0 (high)

The following table shows the por_mpu_m3_prlar0 higher register bit assignments.

Table 4-1879 por_mpu_m3_prlar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

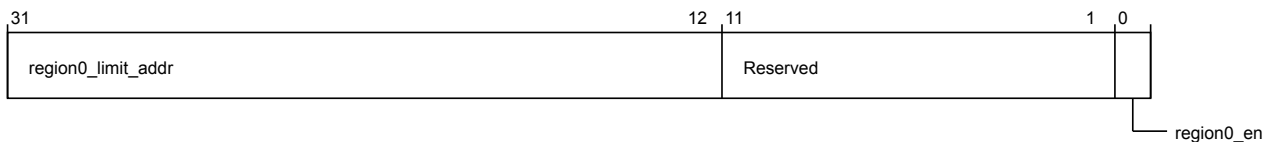


Figure 4-1863 por_mpu_m3_prlar0 (low)

The following table shows the por_mpu_m3_prlar0 lower register bit assignments.

Table 4-1880 por_mpu_m3_prlar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region0_en	Region 0 enable.	RW	1'b0

por_mpu_m3_prbar1

MPU master 0 programmable base address register 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1C20
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

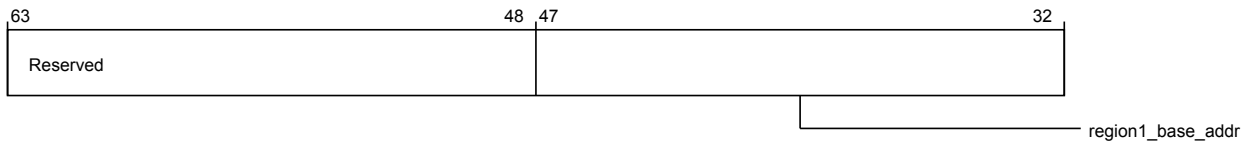


Figure 4-1864 `por_mpu_por_mpu_m3_prbar1` (high)

The following table shows the `por_mpu_m3_prbar1` higher register bit assignments.

Table 4-1881 `por_mpu_por_mpu_m3_prbar1` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region1_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

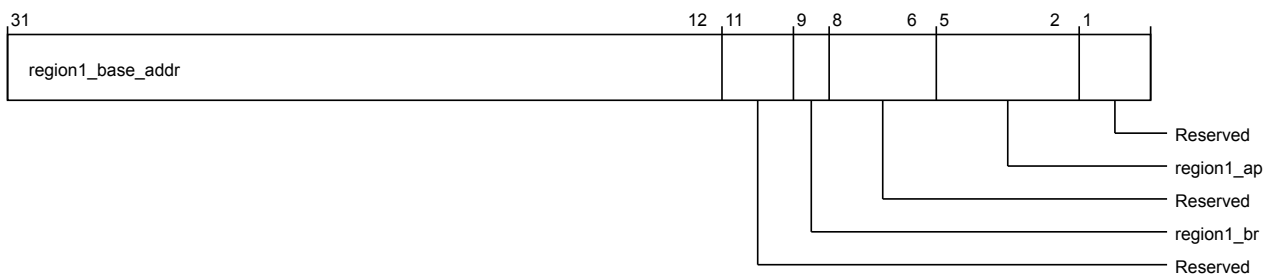


Figure 4-1865 `por_mpu_por_mpu_m3_prbar1` (low)

The following table shows the `por_mpu_m3_prbar1` lower register bit assignments.

Table 4-1882 `por_mpu_por_mpu_m3_prbar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region1_br</code>	Region 1 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-

Table 4-1882 por_mpu_por_mpu_m3_prbar1 (low) (continued)

Bits	Field name	Description	Type	Reset
5:2	region1_ap	Region 1 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar1

MPU master 0 programmable limit address register 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C28

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

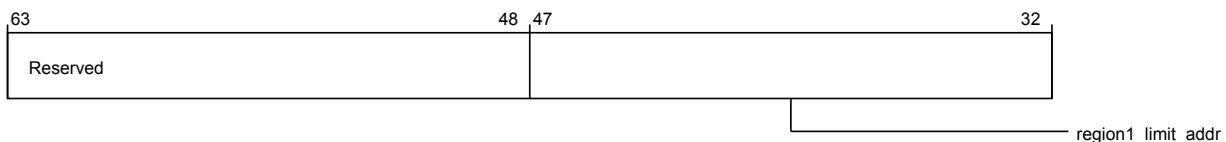


Figure 4-1866 por_mpu_por_mpu_m3_prlar1 (high)

The following table shows the por_mpu_m3_prlar1 higher register bit assignments.

Table 4-1883 por_mpu_por_mpu_m3_prlar1 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region1_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

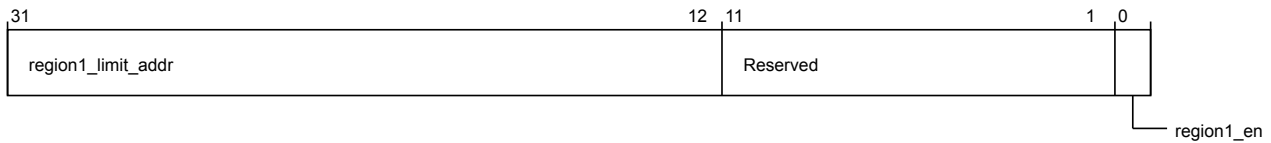


Figure 4-1867 `por_mpu_por_mpu_m3_prlar1` (low)

The following table shows the `por_mpu_m3_prlar1` lower register bit assignments.

Table 4-1884 `por_mpu_por_mpu_m3_prlar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region1_en</code>	Region 1 enable.	RW	1'b0

`por_mpu_m3_prbar2`

MPU master 0 programmable base address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C30

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

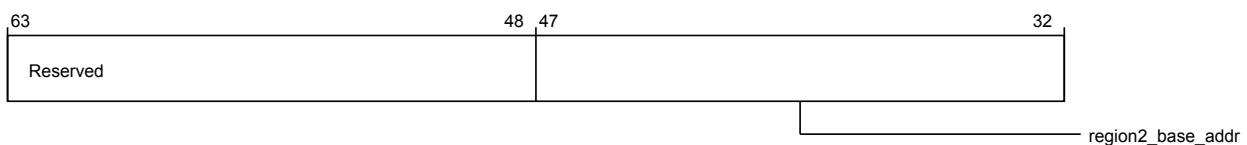


Figure 4-1868 `por_mpu_por_mpu_m3_prbar2` (high)

The following table shows the `por_mpu_m3_prbar2` higher register bit assignments.

Table 4-1885 `por_mpu_por_mpu_m3_prbar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

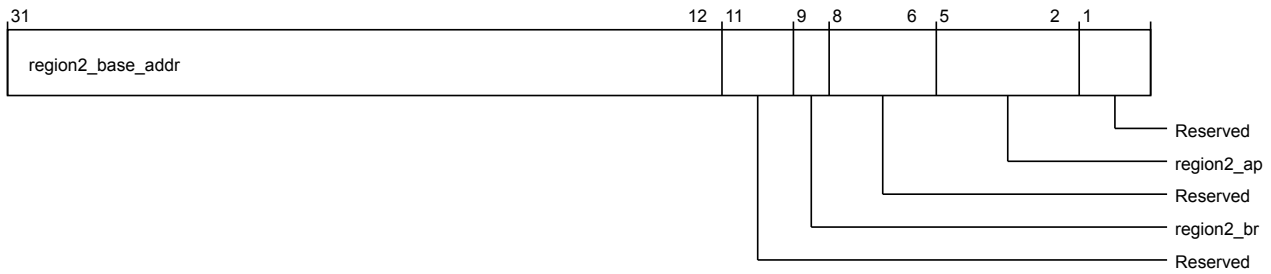


Figure 4-1869 por_mpu_por_mpu_m3_prbar2 (low)

The following table shows the por_mpu_m3_prbar2 lower register bit assignments.

Table 4-1886 por_mpu_por_mpu_m3_prbar2 (low)

Bits	Field name	Description	Type	Reset
31:12	region2_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region2_br	Region 2 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region2_ap	Region 2 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar2

MPU master 0 programmable limit address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C38

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

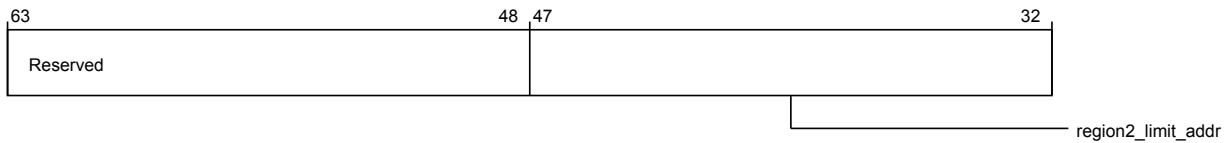


Figure 4-1870 `por_mpu_m3_prlar2` (high)

The following table shows the `por_mpu_m3_prlar2` higher register bit assignments.

Table 4-1887 `por_mpu_m3_prlar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

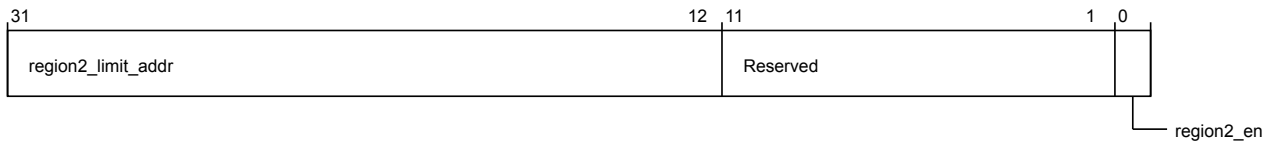


Figure 4-1871 `por_mpu_m3_prlar2` (low)

The following table shows the `por_mpu_m3_prlar2` lower register bit assignments.

Table 4-1888 `por_mpu_m3_prlar2` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region2_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region2_en</code>	Region 2 enable.	RW	1'b0

`por_mpu_m3_prbar3`

MPU master 0 programmable base address register 3.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1C40
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

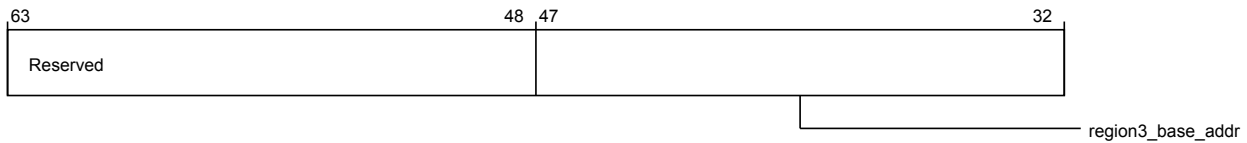


Figure 4-1872 `por_mpu_por_mpu_m3_prbar3` (high)

The following table shows the `por_mpu_m3_prbar3` higher register bit assignments.

Table 4-1889 `por_mpu_por_mpu_m3_prbar3` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

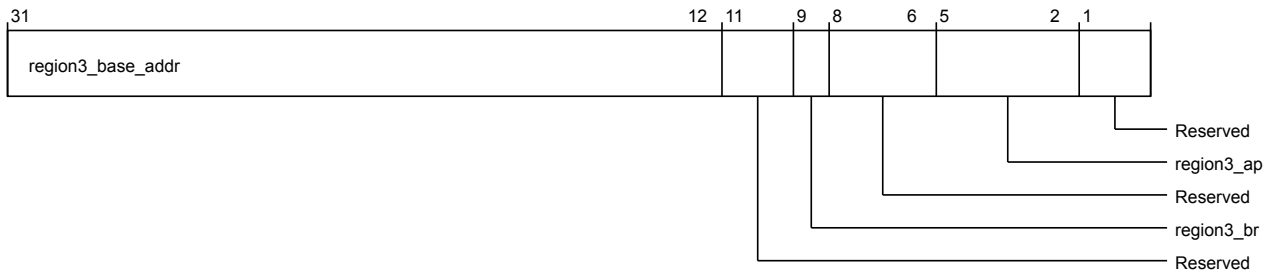


Figure 4-1873 `por_mpu_por_mpu_m3_prbar3` (low)

The following table shows the `por_mpu_m3_prbar3` lower register bit assignments.

Table 4-1890 `por_mpu_por_mpu_m3_prbar3` (low)

Bits	Field name	Description	Type	Reset
31:12	region3_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region3_br	Region 3 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region3_ap	Region 3 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar3

MPU master 0 programmable limit address register 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C48

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

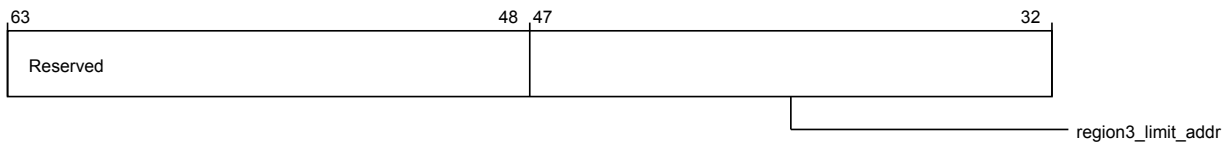


Figure 4-1874 por_mpu_por_mpu_m3_prlar3 (high)

The following table shows the por_mpu_m3_prlar3 higher register bit assignments.

Table 4-1891 por_mpu_por_mpu_m3_prlar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

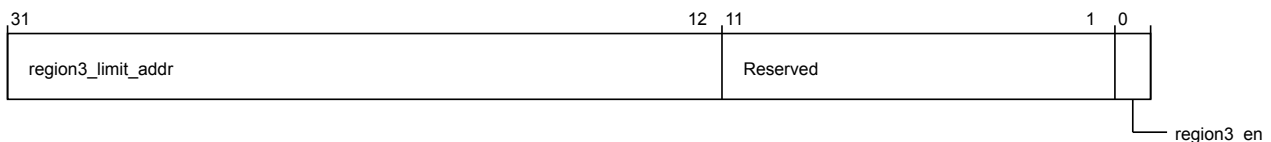


Figure 4-1875 por_mpu_por_mpu_m3_prlar3 (low)

The following table shows the por_mpu_m3_prlar3 lower register bit assignments.

Table 4-1892 por_mpu_por_mpu_m3_prlar3 (low)

Bits	Field name	Description	Type	Reset
31:12	region3_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region3_en	Region 3 enable.	RW	1'b0

por_mpu_m3_prbar4

MPU master 0 programmable base address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C50

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

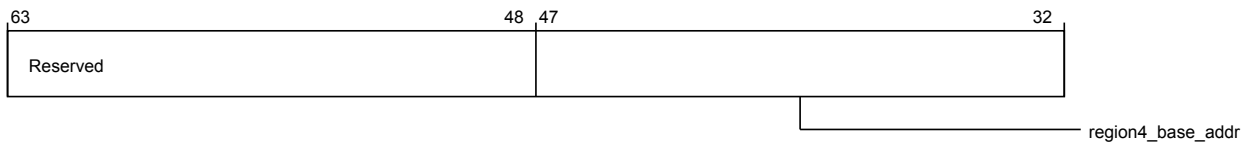


Figure 4-1876 por_mpu_por_mpu_m3_prbar4 (high)

The following table shows the `por_mpu_m3_prbar4` higher register bit assignments.

Table 4-1893 por_mpu_por_mpu_m3_prbar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

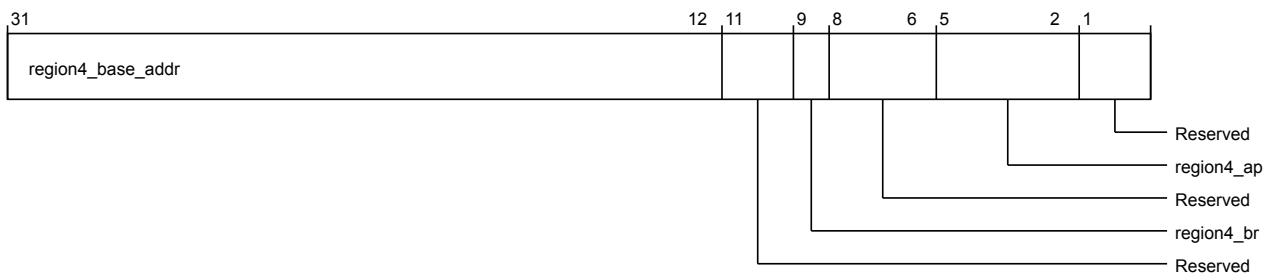


Figure 4-1877 por_mpu_por_mpu_m3_prbar4 (low)

The following table shows the `por_mpu_m3_prbar4` lower register bit assignments.

Table 4-1894 por_mpu_por_mpu_m3_prbar4 (low)

Bits	Field name	Description	Type	Reset
31:12	region4_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1894 por_mpu_por_mpu_m3_prbar4 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region4_br	Region 4 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region4_ap	Region 4 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar4

MPU master 0 programmable limit address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C58

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

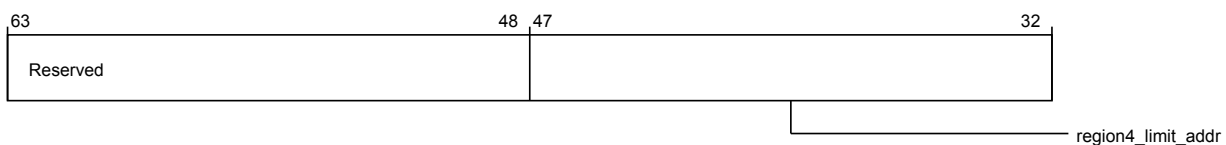


Figure 4-1878 por_mpu_por_mpu_m3_prlar4 (high)

The following table shows the por_mpu_m3_prlar4 higher register bit assignments.

Table 4-1895 por_mpu_por_mpu_m3_prlar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

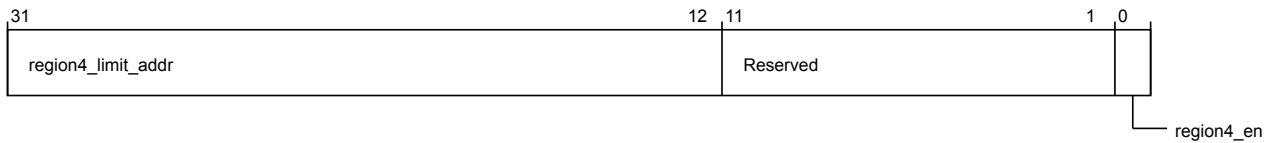


Figure 4-1879 `por_mpu_por_mpu_m3_prlar4` (low)

The following table shows the `por_mpu_m3_prlar4` lower register bit assignments.

Table 4-1896 `por_mpu_por_mpu_m3_prlar4` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region4_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region4_en</code>	Region 4 enable.	RW	1'b0

`por_mpu_m3_prbar5`

MPU master 0 programmable base address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C60

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

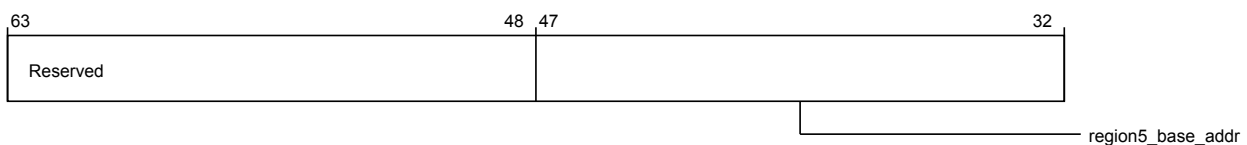


Figure 4-1880 `por_mpu_por_mpu_m3_prbar5` (high)

The following table shows the `por_mpu_m3_prbar5` higher register bit assignments.

Table 4-1897 `por_mpu_por_mpu_m3_prbar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

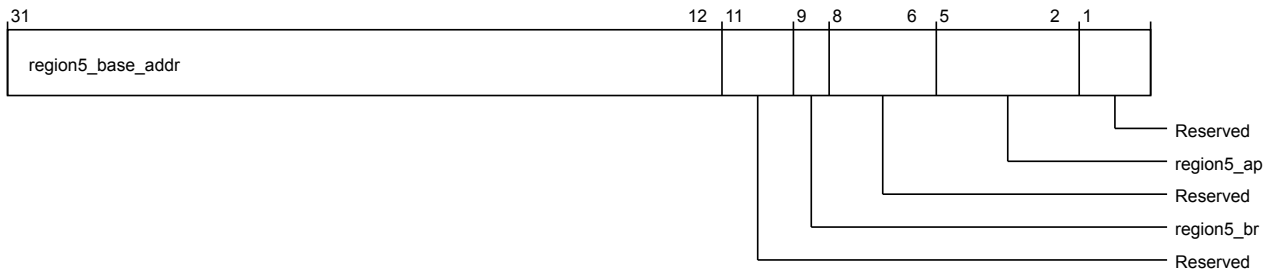


Figure 4-1881 por_mpu_por_mpu_m3_prbar5 (low)

The following table shows the por_mpu_m3_prbar5 lower register bit assignments.

Table 4-1898 por_mpu_por_mpu_m3_prbar5 (low)

Bits	Field name	Description	Type	Reset
31:12	region5_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region5_br	Region 5 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region5_ap	Region 5 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar5

MPU master 0 programmable limit address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C68

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

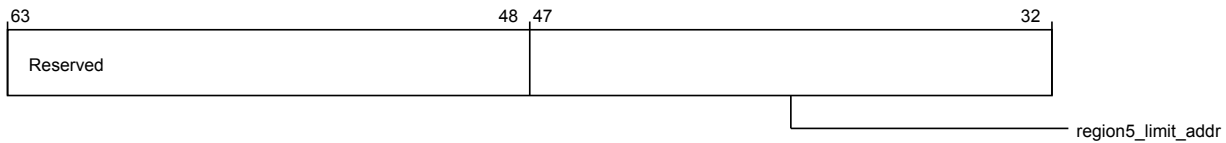


Figure 4-1882 `por_mpu_m3_prlar5` (high)

The following table shows the `por_mpu_m3_prlar5` higher register bit assignments.

Table 4-1899 `por_mpu_m3_prlar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

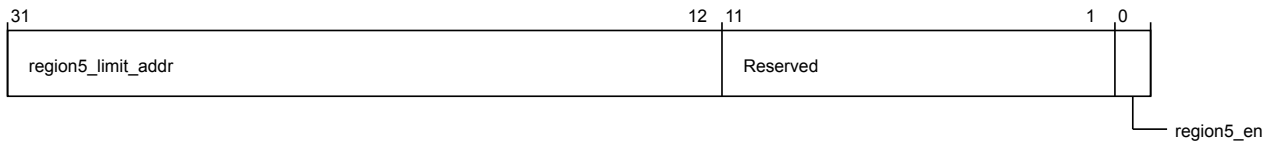


Figure 4-1883 `por_mpu_m3_prlar5` (low)

The following table shows the `por_mpu_m3_prlar5` lower register bit assignments.

Table 4-1900 `por_mpu_m3_prlar5` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region5_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region5_en</code>	Region 5 enable.	RW	1'b0

`por_mpu_m3_prbar6`

MPU master 0 programmable base address register 6.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1C70
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

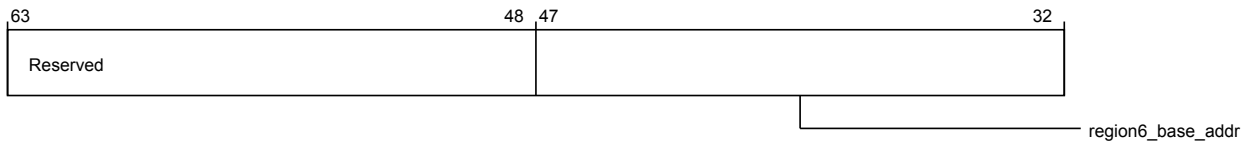


Figure 4-1884 `por_mpu_por_mpu_m3_prbar6` (high)

The following table shows the `por_mpu_m3_prbar6` higher register bit assignments.

Table 4-1901 `por_mpu_por_mpu_m3_prbar6` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region6_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

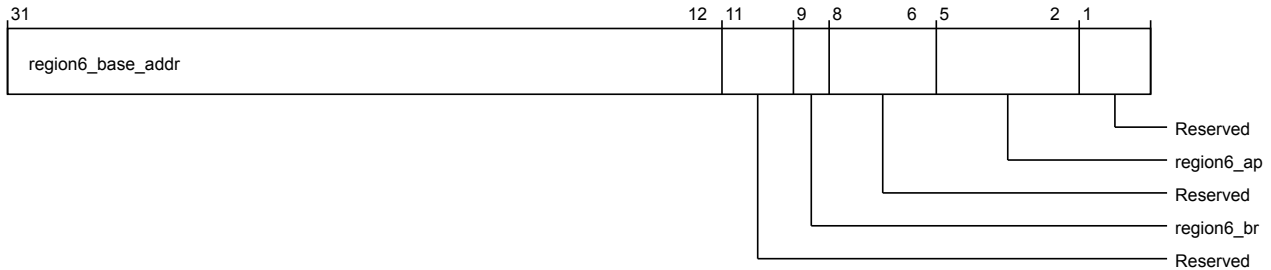


Figure 4-1885 `por_mpu_por_mpu_m3_prbar6` (low)

The following table shows the `por_mpu_m3_prbar6` lower register bit assignments.

Table 4-1902 `por_mpu_por_mpu_m3_prbar6` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region6_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region6_br</code>	Region 6 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region6_ap</code>	Region 6 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar6

MPU master 0 programmable limit address register 6.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C78

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

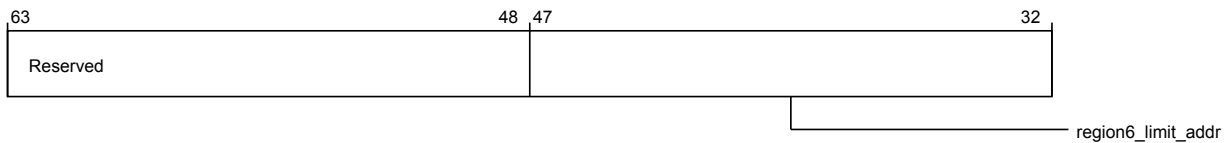


Figure 4-1886 por_mpu_por_mpu_m3_prlar6 (high)

The following table shows the por_mpu_m3_prlar6 higher register bit assignments.

Table 4-1903 por_mpu_por_mpu_m3_prlar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

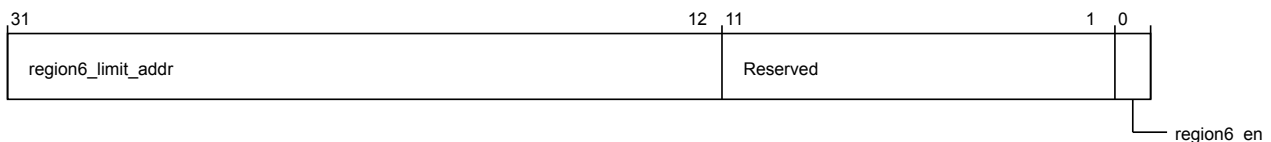


Figure 4-1887 por_mpu_por_mpu_m3_prlar6 (low)

The following table shows the por_mpu_m3_prlar6 lower register bit assignments.

Table 4-1904 por_mpu_por_mpu_m3_prlar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region6_en	Region 6 enable.	RW	1'b0

por_mpu_m3_prbar7

MPU master 0 programmable base address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

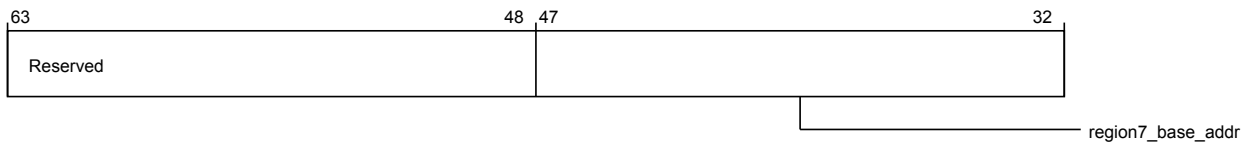


Figure 4-1888 por_mpu_por_mpu_m3_prbar7 (high)

The following table shows the `por_mpu_m3_prbar7` higher register bit assignments.

Table 4-1905 por_mpu_por_mpu_m3_prbar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

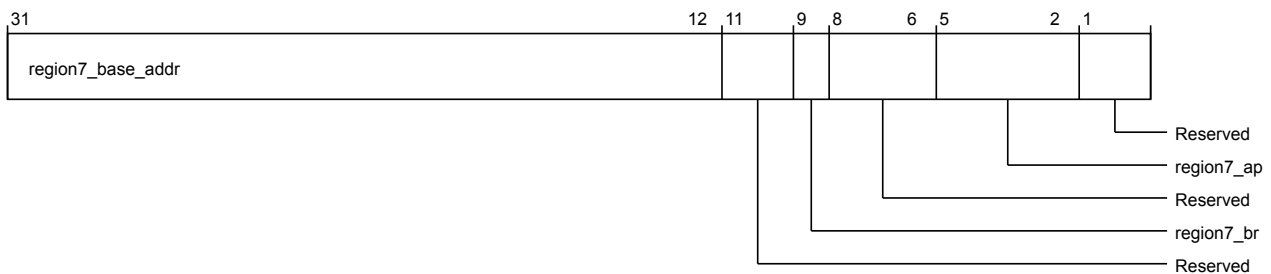


Figure 4-1889 por_mpu_por_mpu_m3_prbar7 (low)

The following table shows the `por_mpu_m3_prbar7` lower register bit assignments.

Table 4-1906 por_mpu_por_mpu_m3_prbar7 (low)

Bits	Field name	Description	Type	Reset
31:12	region7_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1906 por_mpu_por_mpu_m3_prbar7 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region7_br	Region 7 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region7_ap	Region 7 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar7

MPU master 0 programmable limit address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C88

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

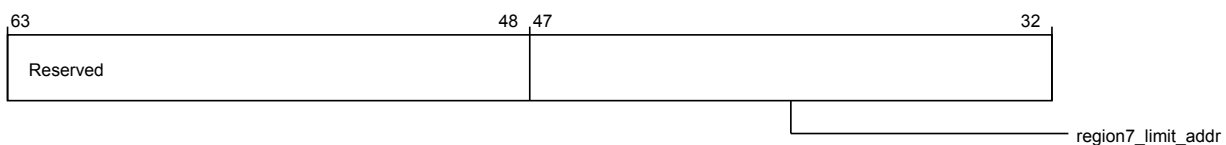


Figure 4-1890 por_mpu_por_mpu_m3_prlar7 (high)

The following table shows the por_mpu_m3_prlar7 higher register bit assignments.

Table 4-1907 por_mpu_por_mpu_m3_prlar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

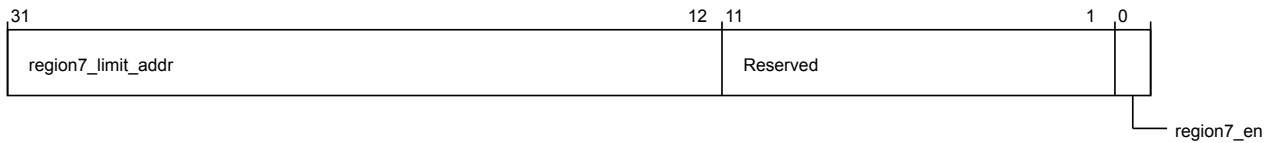


Figure 4-1891 `por_mpu_por_mpu_m3_prlar7` (low)

The following table shows the `por_mpu_m3_prlar7` lower register bit assignments.

Table 4-1908 `por_mpu_por_mpu_m3_prlar7` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region7_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region7_en</code>	Region 7 enable.	RW	1'b0

`por_mpu_m3_prbar8`

MPU master 0 programmable base address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C90

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

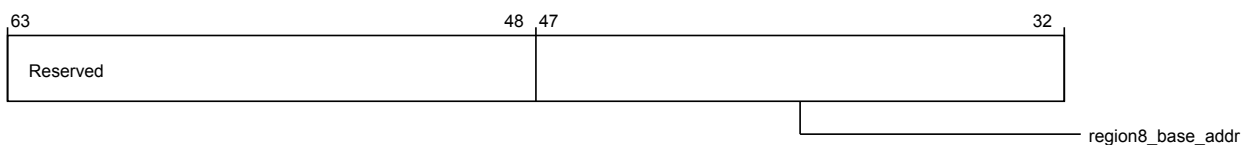


Figure 4-1892 `por_mpu_por_mpu_m3_prbar8` (high)

The following table shows the `por_mpu_m3_prbar8` higher register bit assignments.

Table 4-1909 `por_mpu_por_mpu_m3_prbar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

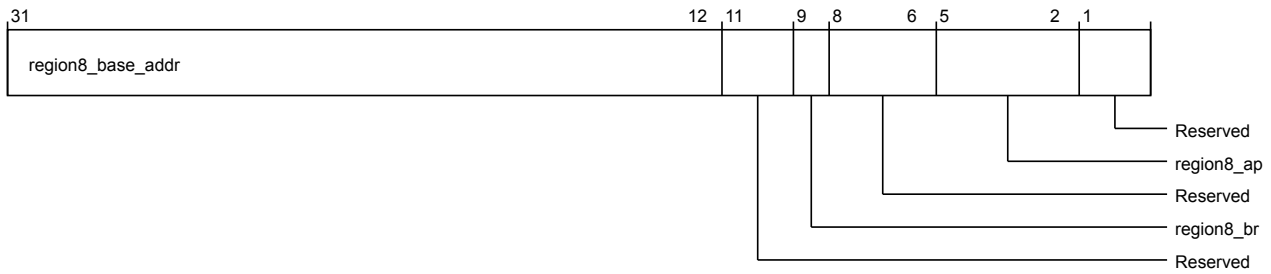


Figure 4-1893 por_mpu_por_mpu_m3_prbar8 (low)

The following table shows the por_mpu_m3_prbar8 lower register bit assignments.

Table 4-1910 por_mpu_por_mpu_m3_prbar8 (low)

Bits	Field name	Description	Type	Reset
31:12	region8_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region8_br	Region 8 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region8_ap	Region 8 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar8

MPU master 0 programmable limit address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1C98

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

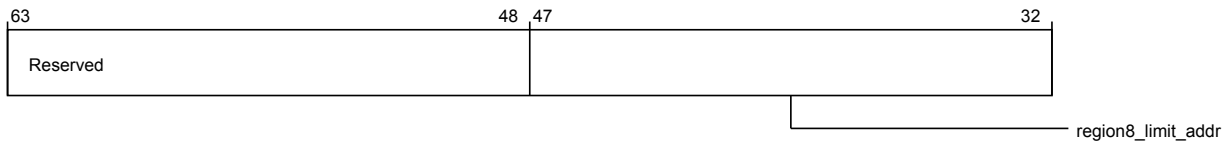


Figure 4-1894 `por_mpu_m3_prlar8` (high)

The following table shows the `por_mpu_m3_prlar8` higher register bit assignments.

Table 4-1911 `por_mpu_m3_prlar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

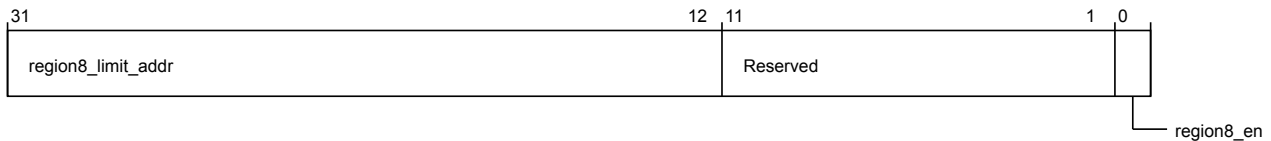


Figure 4-1895 `por_mpu_m3_prlar8` (low)

The following table shows the `por_mpu_m3_prlar8` lower register bit assignments.

Table 4-1912 `por_mpu_m3_prlar8` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region8_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region8_en</code>	Region 8 enable.	RW	1'b0

`por_mpu_m3_prbar9`

MPU master 0 programmable base address register 9.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1CA0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

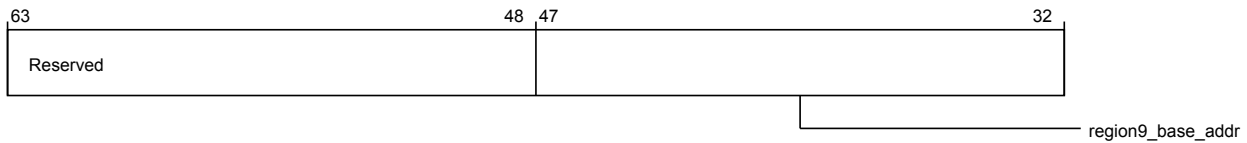


Figure 4-1896 por_mpu_por_mpu_m3_prbar9 (high)

The following table shows the por_mpu_m3_prbar9 higher register bit assignments.

Table 4-1913 por_mpu_por_mpu_m3_prbar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

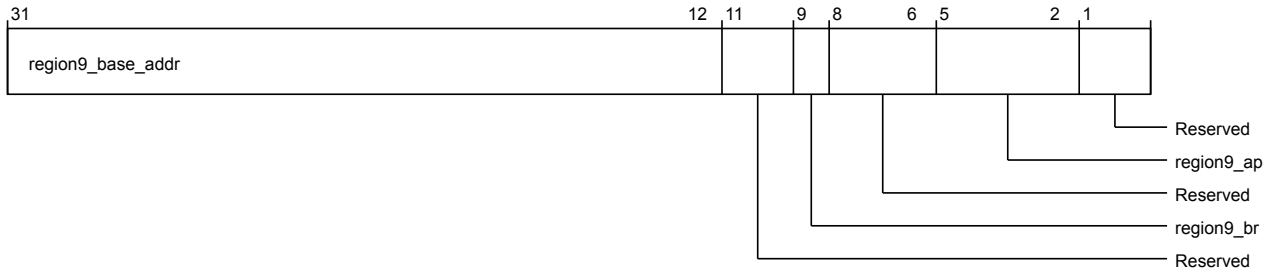


Figure 4-1897 por_mpu_por_mpu_m3_prbar9 (low)

The following table shows the por_mpu_m3_prbar9 lower register bit assignments.

Table 4-1914 por_mpu_por_mpu_m3_prbar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region9_br	Region 9 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region9_ap	Region 9 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar9

MPU master 0 programmable limit address register 9.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1CA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

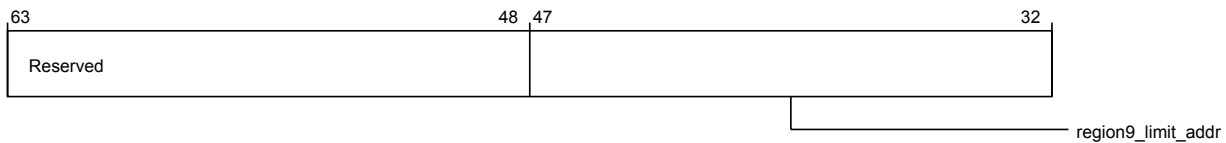


Figure 4-1898 por_mpu_por_mpu_m3_prlar9 (high)

The following table shows the por_mpu_m3_prlar9 higher register bit assignments.

Table 4-1915 por_mpu_por_mpu_m3_prlar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

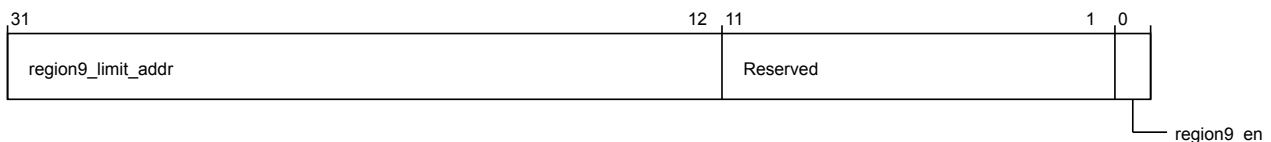


Figure 4-1899 por_mpu_por_mpu_m3_prlar9 (low)

The following table shows the por_mpu_m3_prlar9 lower register bit assignments.

Table 4-1916 por_mpu_por_mpu_m3_prlar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region9_en	Region 9 enable.	RW	1'b0

por_mpu_m3_prbar10

MPU master 0 programmable base address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1CB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

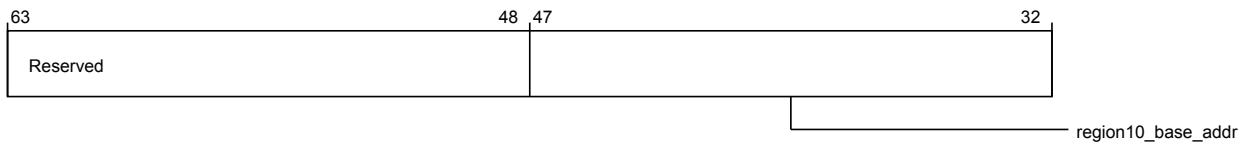


Figure 4-1900 por_mpu_por_mpu_m3_prbar10 (high)

The following table shows the por_mpu_m3_prbar10 higher register bit assignments.

Table 4-1917 por_mpu_por_mpu_m3_prbar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

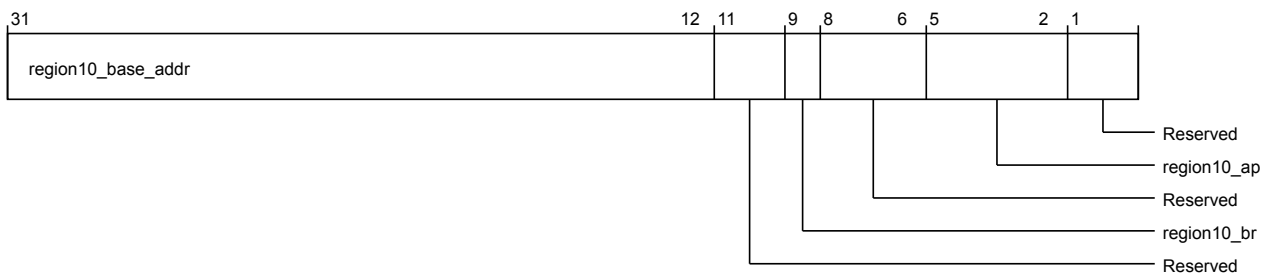


Figure 4-1901 por_mpu_por_mpu_m3_prbar10 (low)

The following table shows the por_mpu_m3_prbar10 lower register bit assignments.

Table 4-1918 por_mpu_por_mpu_m3_prbar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1918 por_mpu_por_mpu_m3_prbar10 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region10_br	Region 10 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region10_ap	Region 10 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar10

MPU master 0 programmable limit address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1CB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

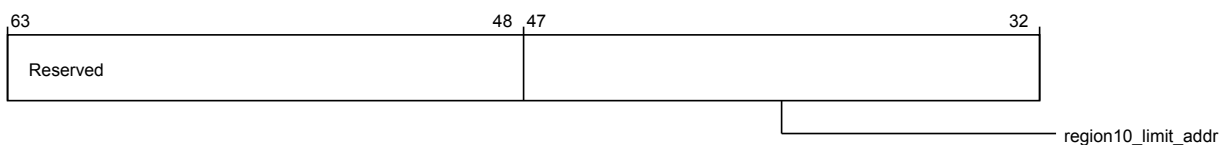


Figure 4-1902 por_mpu_por_mpu_m3_prlar10 (high)

The following table shows the por_mpu_m3_prlar10 higher register bit assignments.

Table 4-1919 por_mpu_por_mpu_m3_prlar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

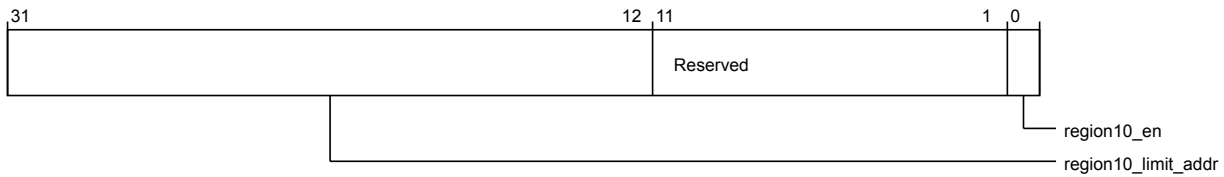


Figure 4-1903 `por_mpu_por_mpu_m3_prlar10` (low)

The following table shows the `por_mpu_m3_prlar10` lower register bit assignments.

Table 4-1920 `por_mpu_por_mpu_m3_prlar10` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region10_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region10_en</code>	Region 10 enable.	RW	1'b0

`por_mpu_m3_prbar11`

MPU master 0 programmable base address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1CC0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

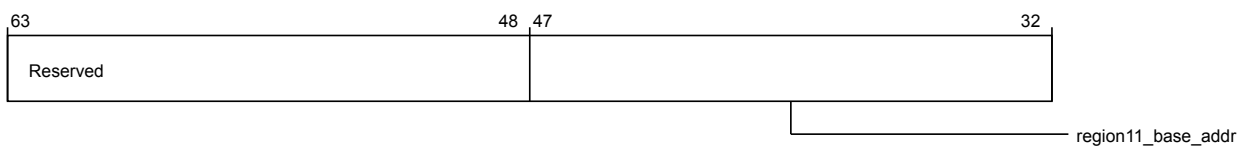


Figure 4-1904 `por_mpu_por_mpu_m3_prbar11` (high)

The following table shows the `por_mpu_m3_prbar11` higher register bit assignments.

Table 4-1921 `por_mpu_por_mpu_m3_prbar11` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region11_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

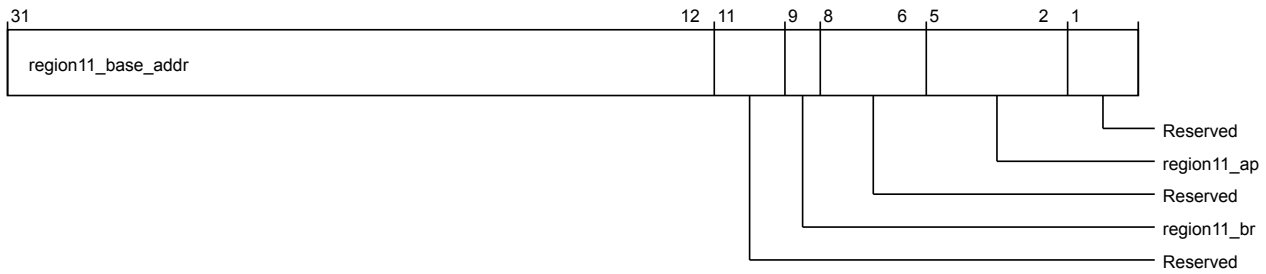


Figure 4-1905 `por_mpu_por_mpu_m3_prbar11` (low)

The following table shows the `por_mpu_m3_prbar11` lower register bit assignments.

Table 4-1922 `por_mpu_por_mpu_m3_prbar11` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region11_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region11_br</code>	Region 11 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region11_ap</code>	Region 11 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m3_prlar11`

MPU master 0 programmable limit address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1CC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

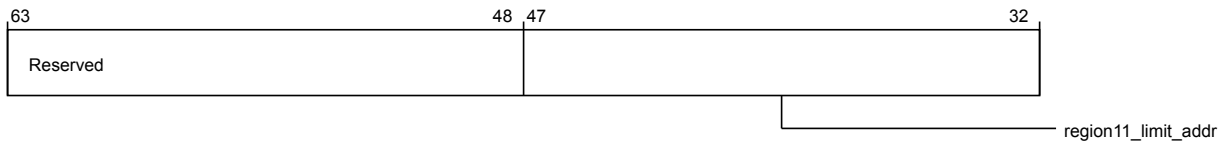


Figure 4-1906 `por_mpu_m3_prlar11` (high)

The following table shows the `por_mpu_m3_prlar11` higher register bit assignments.

Table 4-1923 `por_mpu_m3_prlar11` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

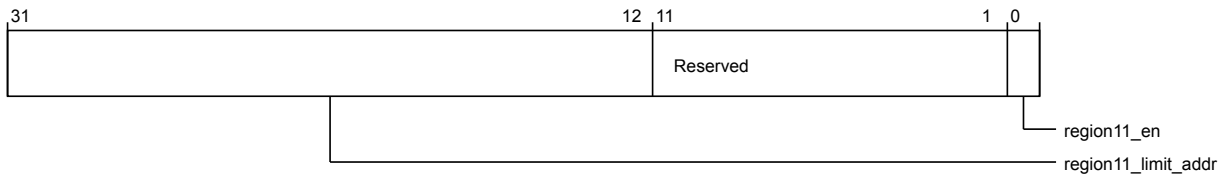


Figure 4-1907 `por_mpu_m3_prlar11` (low)

The following table shows the `por_mpu_m3_prlar11` lower register bit assignments.

Table 4-1924 `por_mpu_m3_prlar11` (low)

Bits	Field name	Description	Type	Reset
31:12	region11_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region11_en	Region 11 enable.	RW	1'b0

`por_mpu_m3_prbar12`

MPU master 0 programmable base address register 12.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1CD0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

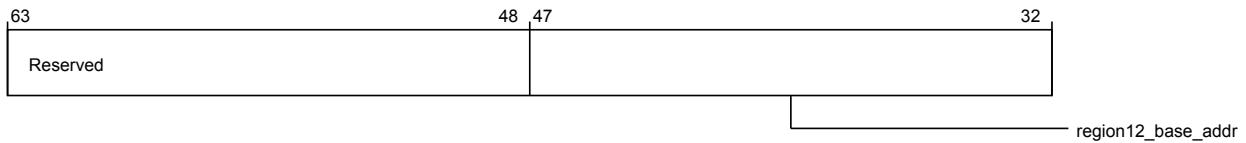


Figure 4-1908 por_mpu_por_mpu_m3_prbar12 (high)

The following table shows the por_mpu_m3_prbar12 higher register bit assignments.

Table 4-1925 por_mpu_por_mpu_m3_prbar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

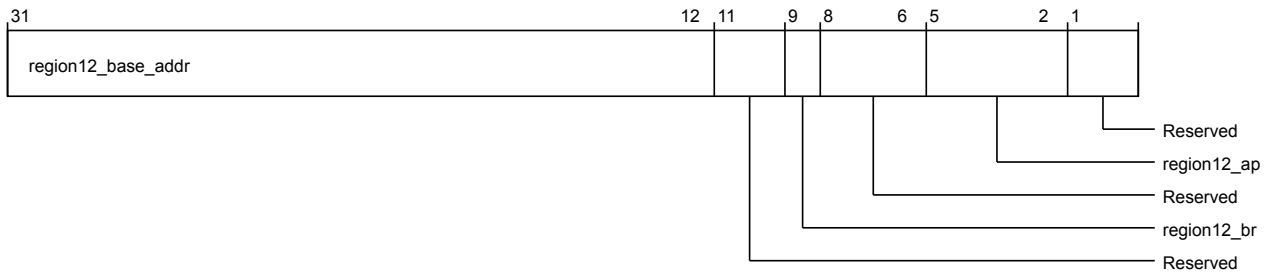


Figure 4-1909 por_mpu_por_mpu_m3_prbar12 (low)

The following table shows the por_mpu_m3_prbar12 lower register bit assignments.

Table 4-1926 por_mpu_por_mpu_m3_prbar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region12_br	Region 12 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region12_ap	Region 12 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar12

MPU master 0 programmable limit address register 12.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1CD8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

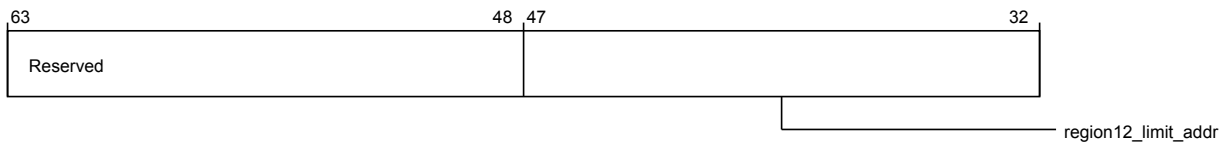


Figure 4-1910 por_mpu_por_mpu_m3_prlar12 (high)

The following table shows the por_mpu_m3_prlar12 higher register bit assignments.

Table 4-1927 por_mpu_por_mpu_m3_prlar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

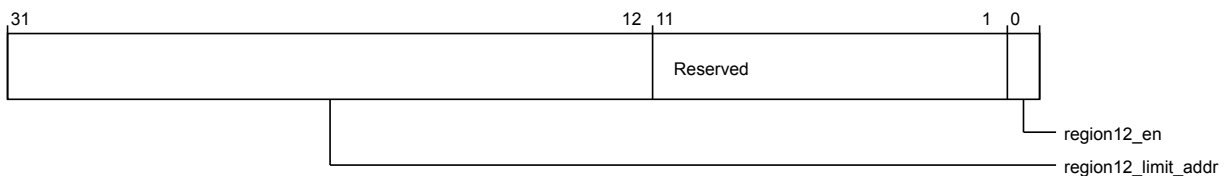


Figure 4-1911 por_mpu_por_mpu_m3_prlar12 (low)

The following table shows the por_mpu_m3_prlar12 lower register bit assignments.

Table 4-1928 por_mpu_por_mpu_m3_prlar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region12_en	Region 12 enable.	RW	1'b0

por_mpu_m3_prbar13

MPU master 0 programmable base address register 13.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1CE0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

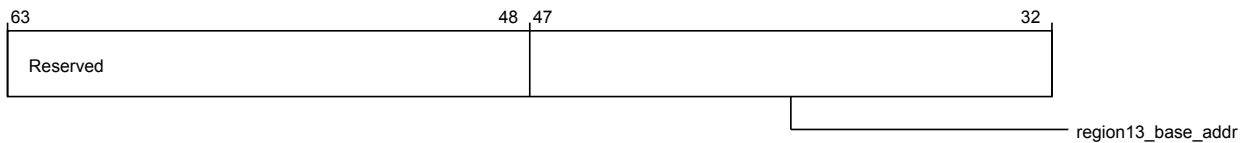


Figure 4-1912 por_mpu_por_mpu_m3_prbar13 (high)

The following table shows the por_mpu_m3_prbar13 higher register bit assignments.

Table 4-1929 por_mpu_por_mpu_m3_prbar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

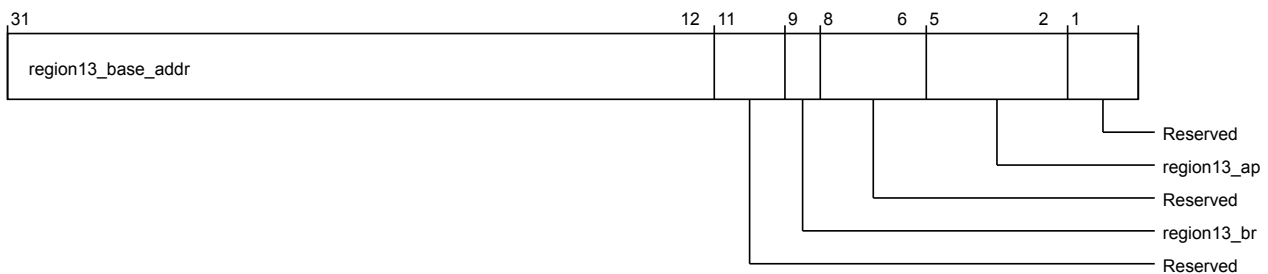


Figure 4-1913 por_mpu_por_mpu_m3_prbar13 (low)

The following table shows the por_mpu_m3_prbar13 lower register bit assignments.

Table 4-1930 por_mpu_por_mpu_m3_prbar13 (low)

Bits	Field name	Description	Type	Reset
31:12	region13_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1930 por_mpu_por_mpu_m3_prbar13 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region13_br	Region 13 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region13_ap	Region 13 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar13

MPU master 0 programmable limit address register 13.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1CE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

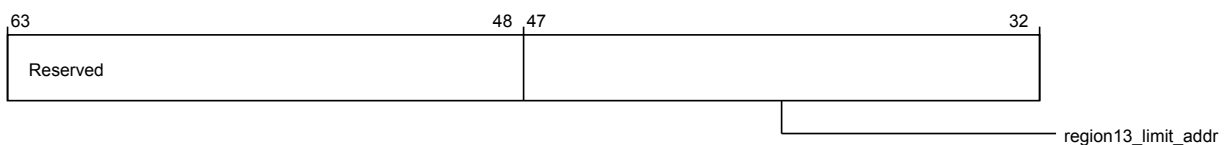


Figure 4-1914 por_mpu_por_mpu_m3_prlar13 (high)

The following table shows the por_mpu_m3_prlar13 higher register bit assignments.

Table 4-1931 por_mpu_por_mpu_m3_prlar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

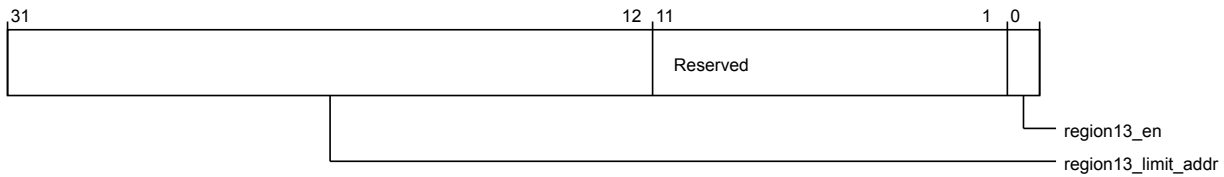


Figure 4-1915 `por_mpu_por_mpu_m3_prlar13` (low)

The following table shows the `por_mpu_m3_prlar13` lower register bit assignments.

Table 4-1932 `por_mpu_por_mpu_m3_prlar13` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region13_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region13_en</code>	Region 13 enable.	RW	1'b0

`por_mpu_m3_prbar14`

MPU master 0 programmable base address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1CF0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

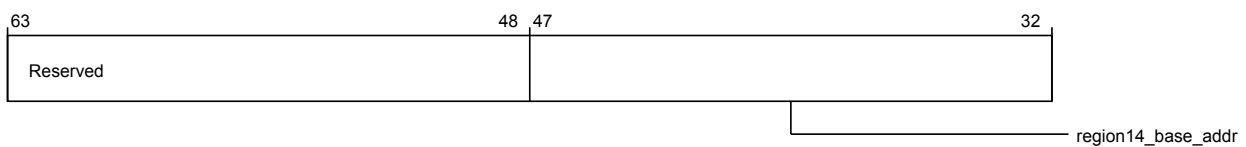


Figure 4-1916 `por_mpu_por_mpu_m3_prbar14` (high)

The following table shows the `por_mpu_m3_prbar14` higher register bit assignments.

Table 4-1933 `por_mpu_por_mpu_m3_prbar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region14_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

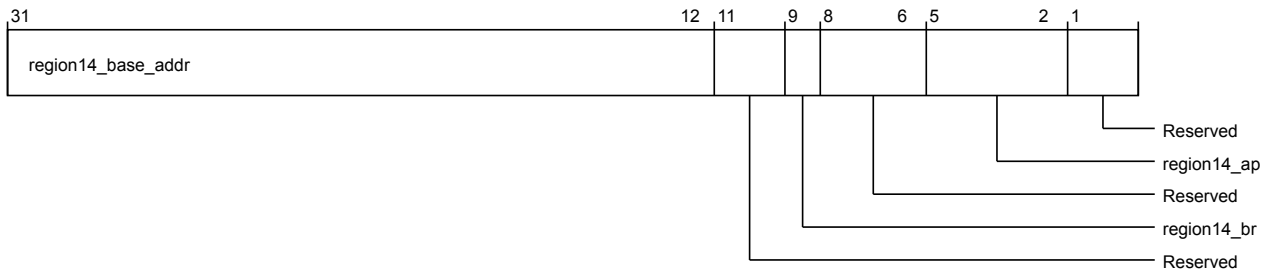


Figure 4-1917 por_mpu_por_mpu_m3_prbar14 (low)

The following table shows the por_mpu_m3_prbar14 lower register bit assignments.

Table 4-1934 por_mpu_por_mpu_m3_prbar14 (low)

Bits	Field name	Description	Type	Reset
31:12	region14_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region14_br	Region 14 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region14_ap	Region 14 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar14

MPU master 0 programmable limit address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1CF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

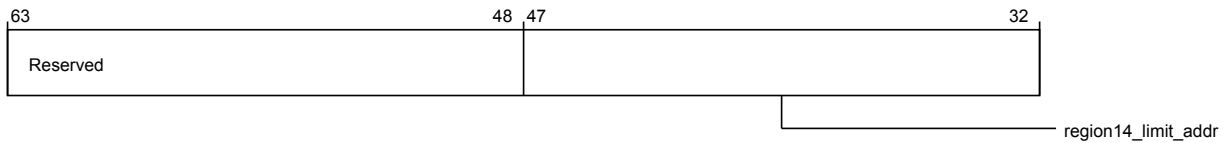


Figure 4-1918 `por_mpu_m3_prlar14` (high)

The following table shows the `por_mpu_m3_prlar14` higher register bit assignments.

Table 4-1935 `por_mpu_m3_prlar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region14_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

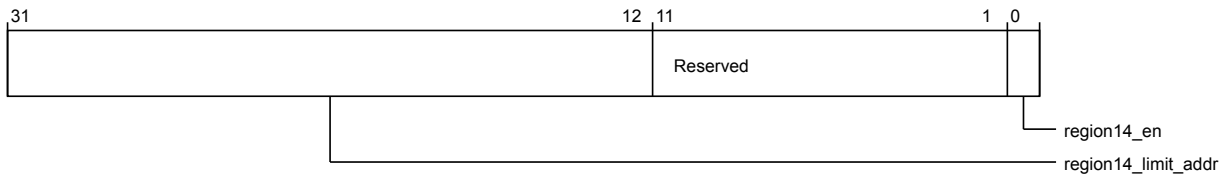


Figure 4-1919 `por_mpu_m3_prlar14` (low)

The following table shows the `por_mpu_m3_prlar14` lower register bit assignments.

Table 4-1936 `por_mpu_m3_prlar14` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region14_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region14_en</code>	Region 14 enable.	RW	1'b0

`por_mpu_m3_prbar15`

MPU master 0 programmable base address register 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1D00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

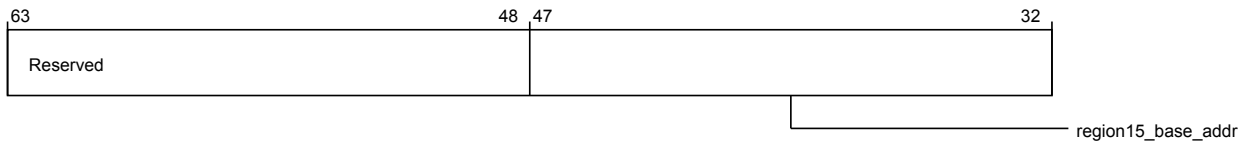


Figure 4-1920 `por_mpu_por_mpu_m3_prbar15` (high)

The following table shows the `por_mpu_m3_prbar15` higher register bit assignments.

Table 4-1937 `por_mpu_por_mpu_m3_prbar15` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

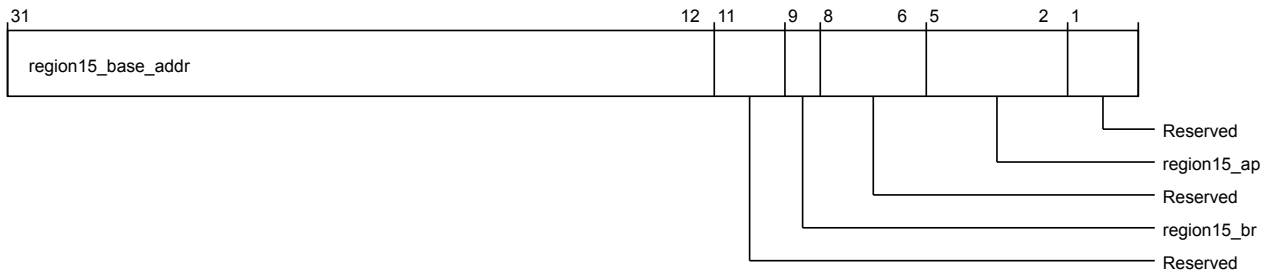


Figure 4-1921 `por_mpu_por_mpu_m3_prbar15` (low)

The following table shows the `por_mpu_m3_prbar15` lower register bit assignments.

Table 4-1938 `por_mpu_por_mpu_m3_prbar15` (low)

Bits	Field name	Description	Type	Reset
31:12	region15_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region15_br	Region 15 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region15_ap	Region 15 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar15

MPU master 0 programmable limit address register 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

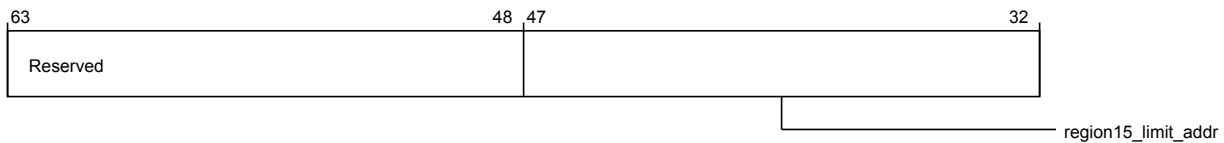


Figure 4-1922 por_mpu_por_mpu_m3_prlar15 (high)

The following table shows the por_mpu_m3_prlar15 higher register bit assignments.

Table 4-1939 por_mpu_por_mpu_m3_prlar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

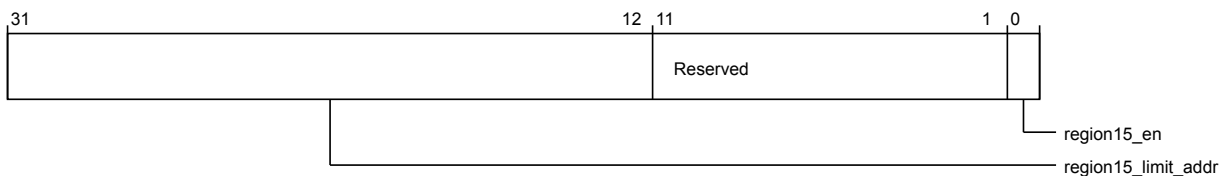


Figure 4-1923 por_mpu_por_mpu_m3_prlar15 (low)

The following table shows the por_mpu_m3_prlar15 lower register bit assignments.

Table 4-1940 por_mpu_por_mpu_m3_prlar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region15_en	Region 15 enable.	RW	1'b0

por_mpu_m3_prbar16

MPU master 0 programmable base address register 16.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1D10
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

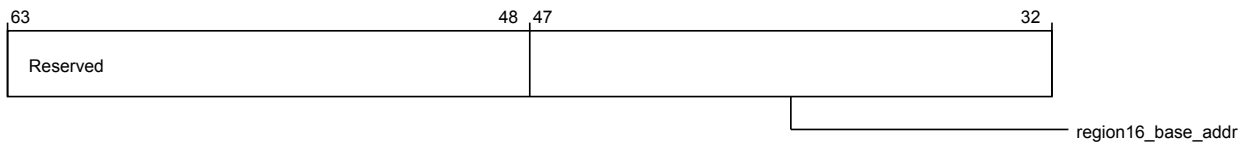


Figure 4-1924 por_mpu_por_mpu_m3_prbar16 (high)

The following table shows the por_mpu_m3_prbar16 higher register bit assignments.

Table 4-1941 por_mpu_por_mpu_m3_prbar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

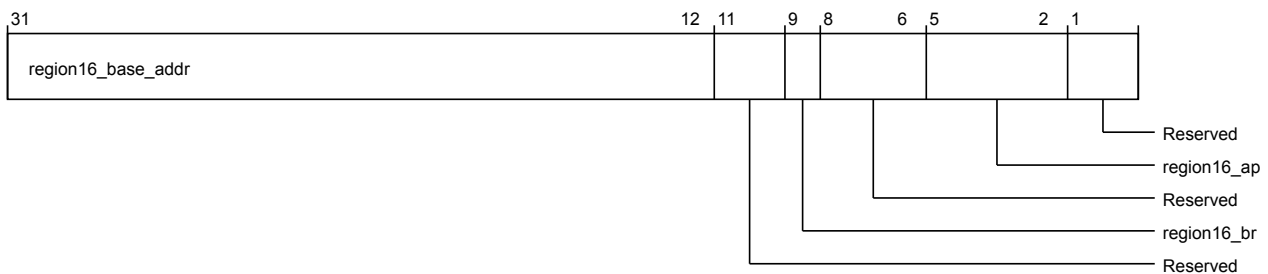


Figure 4-1925 por_mpu_por_mpu_m3_prbar16 (low)

The following table shows the por_mpu_m3_prbar16 lower register bit assignments.

Table 4-1942 por_mpu_por_mpu_m3_prbar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1942 por_mpu_por_mpu_m3_prbar16 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region16_br	Region 16 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region16_ap	Region 16 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar16

MPU master 0 programmable limit address register 16.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D18

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

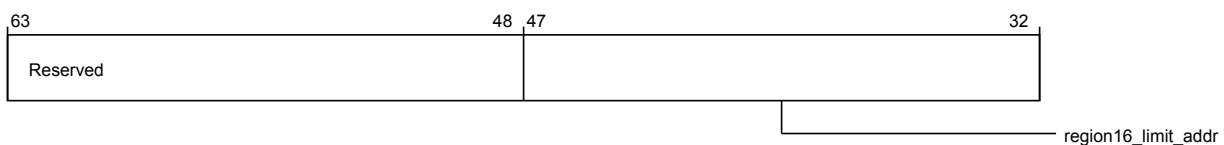


Figure 4-1926 por_mpu_por_mpu_m3_prlar16 (high)

The following table shows the por_mpu_m3_prlar16 higher register bit assignments.

Table 4-1943 por_mpu_por_mpu_m3_prlar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

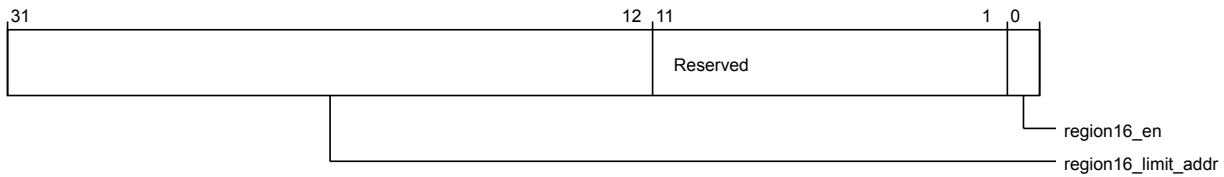


Figure 4-1927 por_mpu_por_mpu_m3_prlar16 (low)

The following table shows the por_mpu_m3_prlar16 lower register bit assignments.

Table 4-1944 por_mpu_por_mpu_m3_prlar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region16_en	Region 16 enable.	RW	1'b0

por_mpu_m3_prbar17

MPU master 0 programmable base address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D20

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

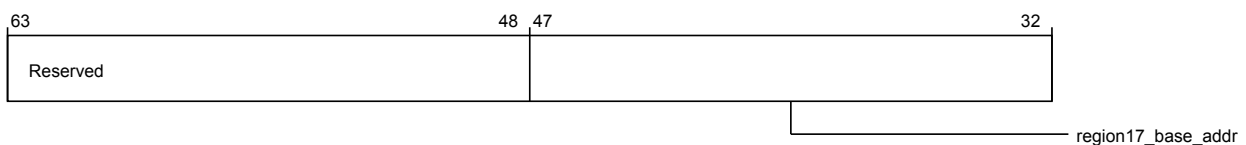


Figure 4-1928 por_mpu_por_mpu_m3_prbar17 (high)

The following table shows the por_mpu_m3_prbar17 higher register bit assignments.

Table 4-1945 por_mpu_por_mpu_m3_prbar17 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

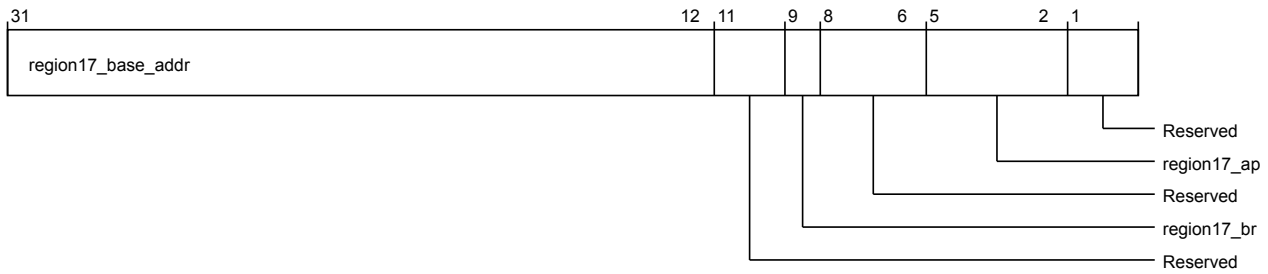


Figure 4-1929 por_mpu_por_mpu_m3_prbar17 (low)

The following table shows the por_mpu_m3_prbar17 lower register bit assignments.

Table 4-1946 por_mpu_por_mpu_m3_prbar17 (low)

Bits	Field name	Description	Type	Reset
31:12	region17_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region17_br	Region 17 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region17_ap	Region 17 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar17

MPU master 0 programmable limit address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D28

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

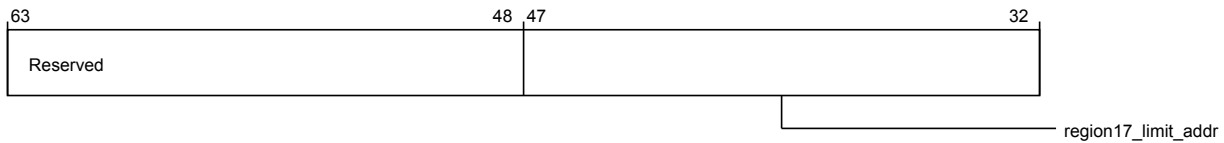


Figure 4-1930 por_mpu_m3_prlar17 (high)

The following table shows the por_mpu_m3_prlar17 higher register bit assignments.

Table 4-1947 por_mpu_m3_prlar17 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

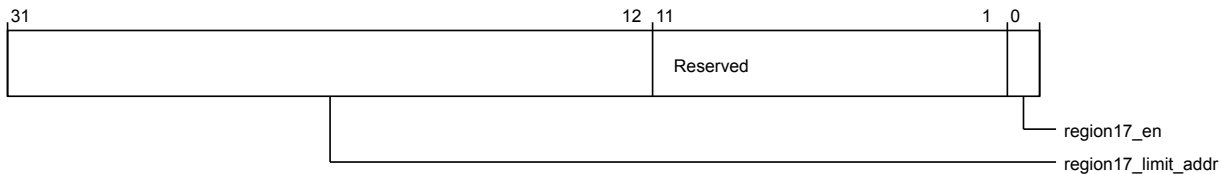


Figure 4-1931 por_mpu_m3_prlar17 (low)

The following table shows the por_mpu_m3_prlar17 lower register bit assignments.

Table 4-1948 por_mpu_m3_prlar17 (low)

Bits	Field name	Description	Type	Reset
31:12	region17_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region17_en	Region 17 enable.	RW	1'b0

por_mpu_m3_prbar18

MPU master 0 programmable base address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1D30
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

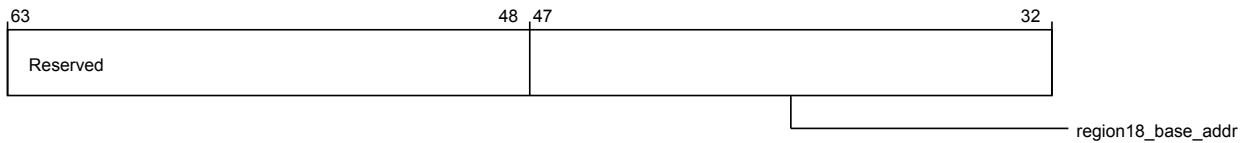


Figure 4-1932 `por_mpu_por_mpu_m3_prbar18` (high)

The following table shows the `por_mpu_m3_prbar18` higher register bit assignments.

Table 4-1949 `por_mpu_por_mpu_m3_prbar18` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region18_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

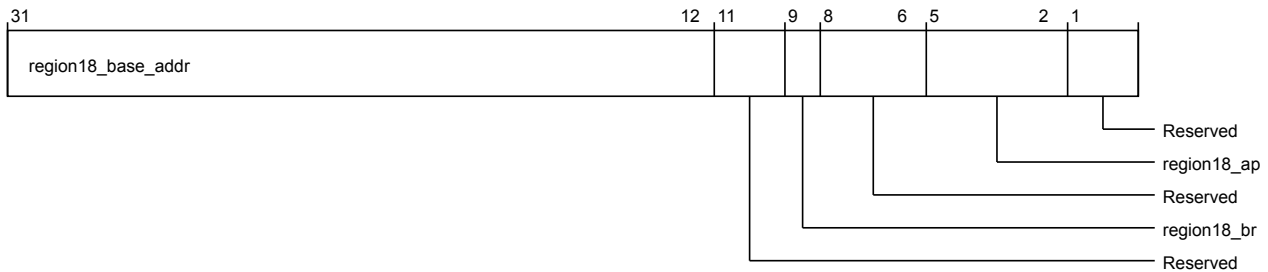


Figure 4-1933 `por_mpu_por_mpu_m3_prbar18` (low)

The following table shows the `por_mpu_m3_prbar18` lower register bit assignments.

Table 4-1950 `por_mpu_por_mpu_m3_prbar18` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region18_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region18_br</code>	Region 18 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region18_ap</code>	Region 18 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar18

MPU master 0 programmable limit address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1D38
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

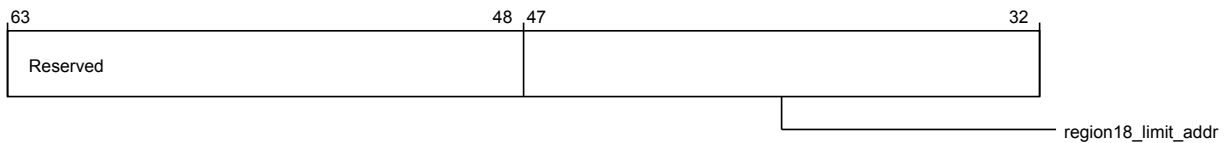


Figure 4-1934 por_mpu_por_mpu_m3_prlar18 (high)

The following table shows the por_mpu_m3_prlar18 higher register bit assignments.

Table 4-1951 por_mpu_por_mpu_m3_prlar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

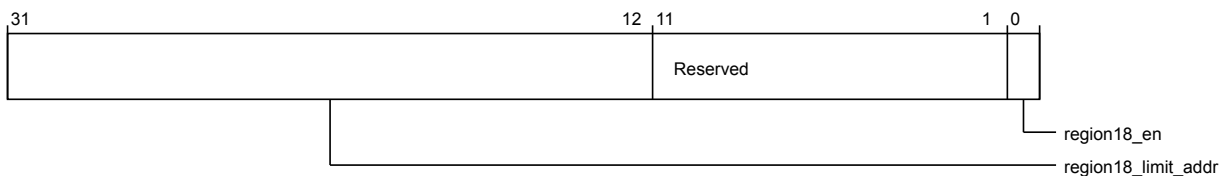


Figure 4-1935 por_mpu_por_mpu_m3_prlar18 (low)

The following table shows the por_mpu_m3_prlar18 lower register bit assignments.

Table 4-1952 por_mpu_por_mpu_m3_prlar18 (low)

Bits	Field name	Description	Type	Reset
31:12	region18_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region18_en	Region 18 enable.	RW	1'b0

por_mpu_m3_prbar19

MPU master 0 programmable base address register 19.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1D40
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

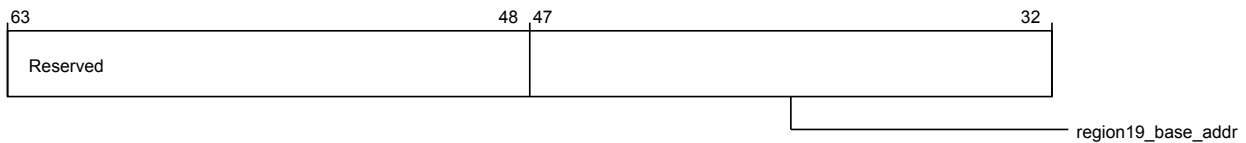


Figure 4-1936 por_mpu_por_mpu_m3_prbar19 (high)

The following table shows the por_mpu_m3_prbar19 higher register bit assignments.

Table 4-1953 por_mpu_por_mpu_m3_prbar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

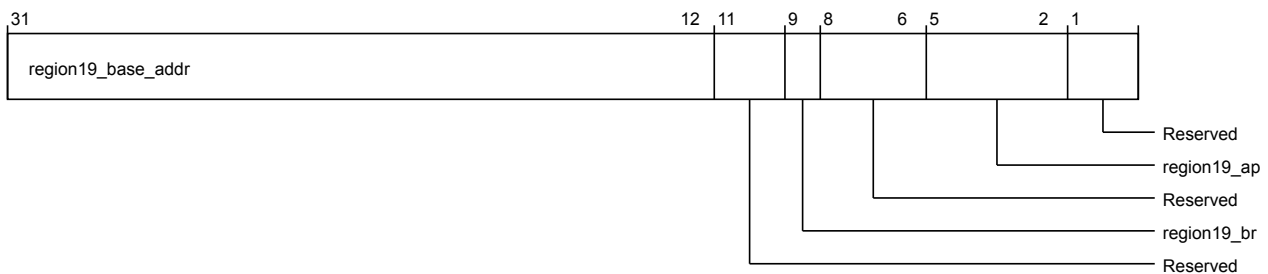


Figure 4-1937 por_mpu_por_mpu_m3_prbar19 (low)

The following table shows the por_mpu_m3_prbar19 lower register bit assignments.

Table 4-1954 por_mpu_por_mpu_m3_prbar19 (low)

Bits	Field name	Description	Type	Reset
31:12	region19_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1954 por_mpu_por_mpu_m3_prbar19 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region19_br	Region 19 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region19_ap	Region 19 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar19

MPU master 0 programmable limit address register 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D48

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

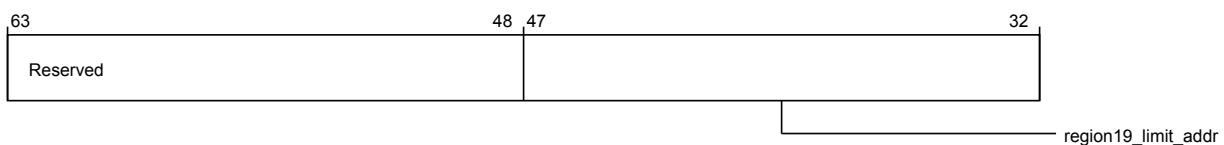


Figure 4-1938 por_mpu_por_mpu_m3_prlar19 (high)

The following table shows the por_mpu_m3_prlar19 higher register bit assignments.

Table 4-1955 por_mpu_por_mpu_m3_prlar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

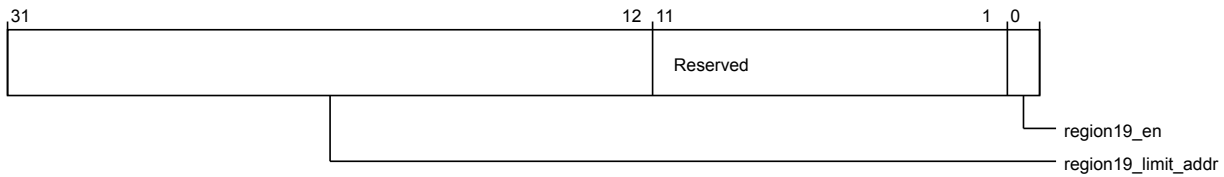


Figure 4-1939 por_mpu_por_mpu_m3_prlar19 (low)

The following table shows the por_mpu_m3_prlar19 lower register bit assignments.

Table 4-1956 por_mpu_por_mpu_m3_prlar19 (low)

Bits	Field name	Description	Type	Reset
31:12	region19_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region19_en	Region 19 enable.	RW	1'b0

por_mpu_m3_prbar20

MPU master 0 programmable base address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D50

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

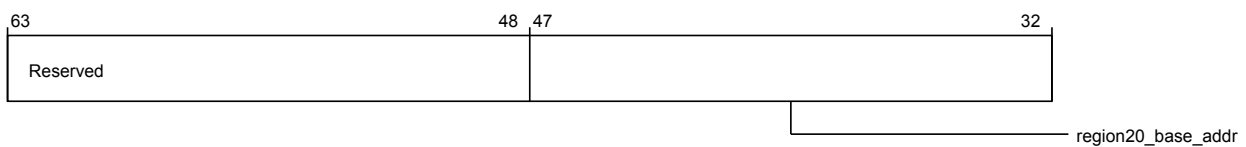


Figure 4-1940 por_mpu_por_mpu_m3_prbar20 (high)

The following table shows the por_mpu_m3_prbar20 higher register bit assignments.

Table 4-1957 por_mpu_por_mpu_m3_prbar20 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region20_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

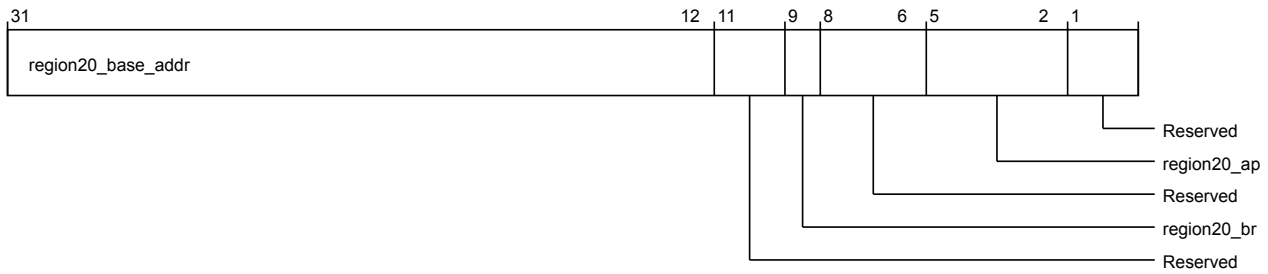


Figure 4-1941 `por_mpu_por_mpu_m3_prbar20` (low)

The following table shows the `por_mpu_m3_prbar20` lower register bit assignments.

Table 4-1958 `por_mpu_por_mpu_m3_prbar20` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region20_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region20_br</code>	Region 20 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region20_ap</code>	Region 20 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m3_prlar20`

MPU master 0 programmable limit address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D58

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

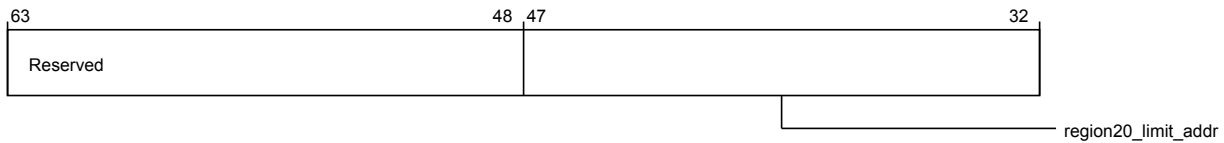


Figure 4-1942 por_mpu_m3_prlar20 (high)

The following table shows the por_mpu_m3_prlar20 higher register bit assignments.

Table 4-1959 por_mpu_m3_prlar20 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region20_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

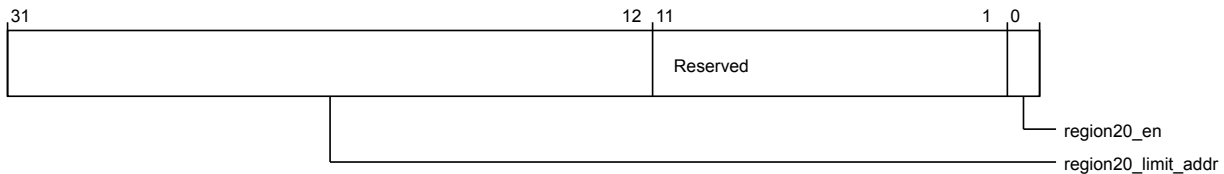


Figure 4-1943 por_mpu_m3_prlar20 (low)

The following table shows the por_mpu_m3_prlar20 lower register bit assignments.

Table 4-1960 por_mpu_m3_prlar20 (low)

Bits	Field name	Description	Type	Reset
31:12	region20_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region20_en	Region 20 enable.	RW	1'b0

por_mpu_m3_prbar21

MPU master 0 programmable base address register 21.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1D60
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

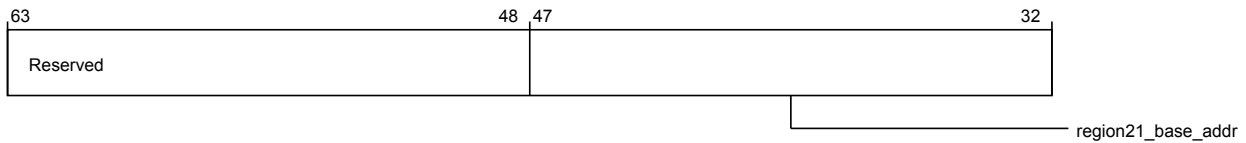


Figure 4-1944 `por_mpu_por_mpu_m3_prbar21` (high)

The following table shows the `por_mpu_m3_prbar21` higher register bit assignments.

Table 4-1961 `por_mpu_por_mpu_m3_prbar21` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

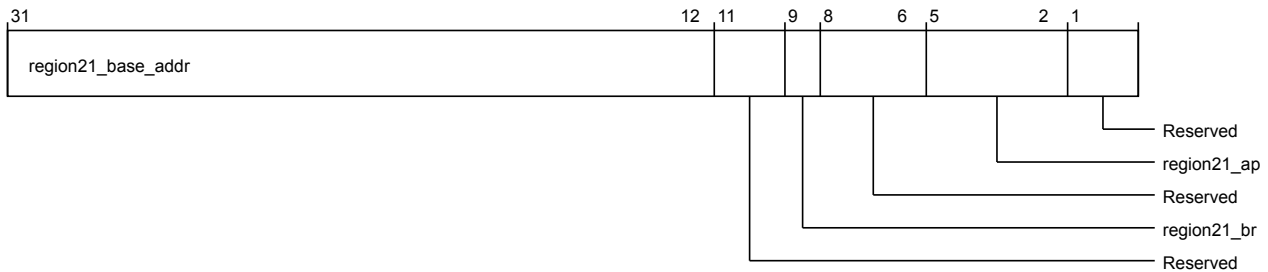


Figure 4-1945 `por_mpu_por_mpu_m3_prbar21` (low)

The following table shows the `por_mpu_m3_prbar21` lower register bit assignments.

Table 4-1962 `por_mpu_por_mpu_m3_prbar21` (low)

Bits	Field name	Description	Type	Reset
31:12	region21_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region21_br	Region 21 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region21_ap	Region 21 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar21

MPU master 0 programmable limit address register 21.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1D68
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

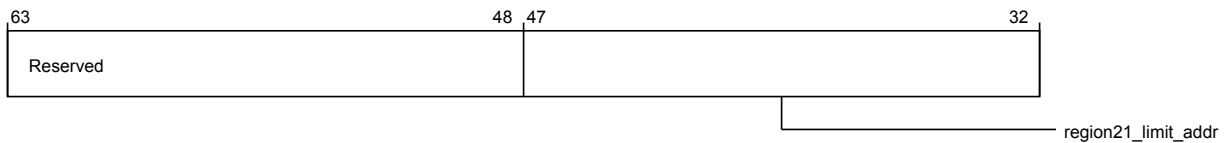


Figure 4-1946 por_mpu_por_mpu_m3_prlar21 (high)

The following table shows the por_mpu_m3_prlar21 higher register bit assignments.

Table 4-1963 por_mpu_por_mpu_m3_prlar21 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

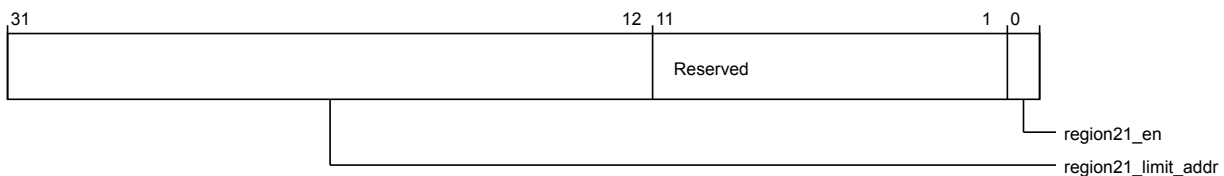


Figure 4-1947 por_mpu_por_mpu_m3_prlar21 (low)

The following table shows the por_mpu_m3_prlar21 lower register bit assignments.

Table 4-1964 por_mpu_por_mpu_m3_prlar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region21_en	Region 21 enable.	RW	1'b0

por_mpu_m3_prbar22

MPU master 0 programmable base address register 22.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1D70
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

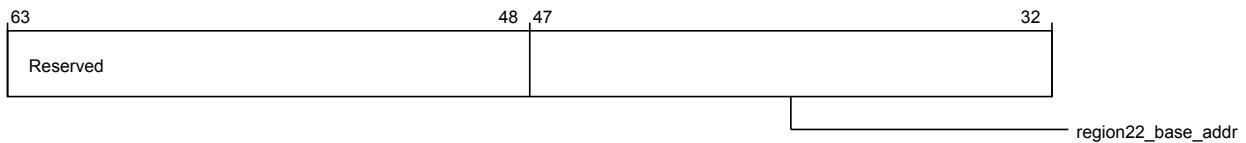


Figure 4-1948 por_mpu_por_mpu_m3_prbar22 (high)

The following table shows the por_mpu_m3_prbar22 higher register bit assignments.

Table 4-1965 por_mpu_por_mpu_m3_prbar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

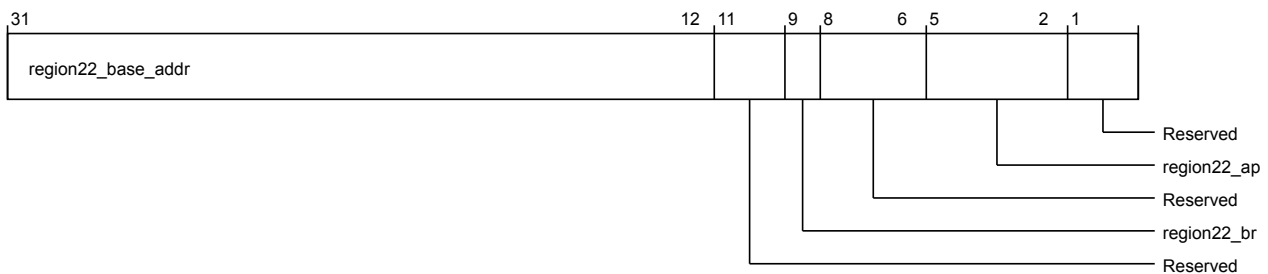


Figure 4-1949 por_mpu_por_mpu_m3_prbar22 (low)

The following table shows the por_mpu_m3_prbar22 lower register bit assignments.

Table 4-1966 por_mpu_por_mpu_m3_prbar22 (low)

Bits	Field name	Description	Type	Reset
31:12	region22_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1966 por_mpu_por_mpu_m3_prbar22 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region22_br	Region 22 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region22_ap	Region 22 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar22

MPU master 0 programmable limit address register 22.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D78

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

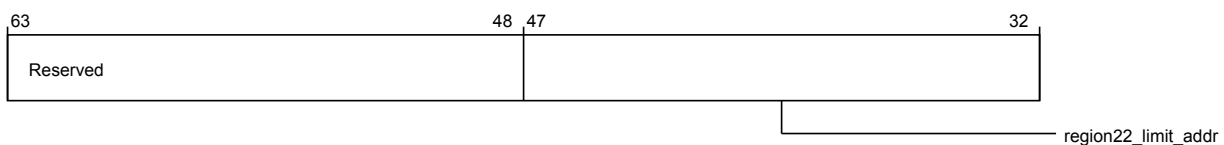


Figure 4-1950 por_mpu_por_mpu_m3_prlar22 (high)

The following table shows the por_mpu_m3_prlar22 higher register bit assignments.

Table 4-1967 por_mpu_por_mpu_m3_prlar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

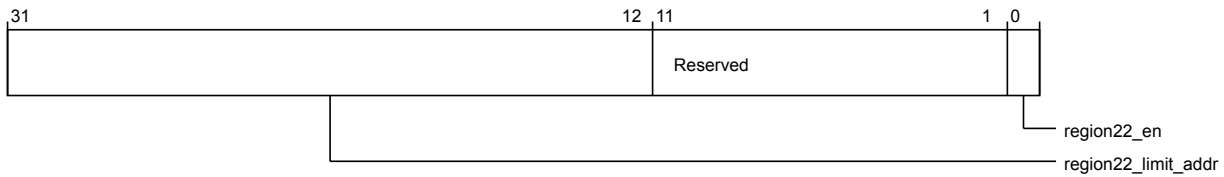


Figure 4-1951 por_mpu_por_mpu_m3_prlar22 (low)

The following table shows the por_mpu_m3_prlar22 lower register bit assignments.

Table 4-1968 por_mpu_por_mpu_m3_prlar22 (low)

Bits	Field name	Description	Type	Reset
31:12	region22_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region22_en	Region 22 enable.	RW	1'b0

por_mpu_m3_prbar23

MPU master 0 programmable base address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

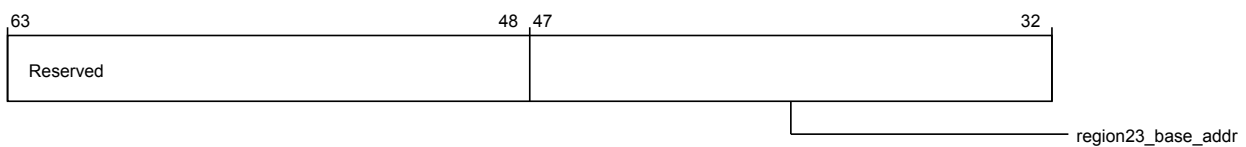


Figure 4-1952 por_mpu_por_mpu_m3_prbar23 (high)

The following table shows the por_mpu_m3_prbar23 higher register bit assignments.

Table 4-1969 por_mpu_por_mpu_m3_prbar23 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region23_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

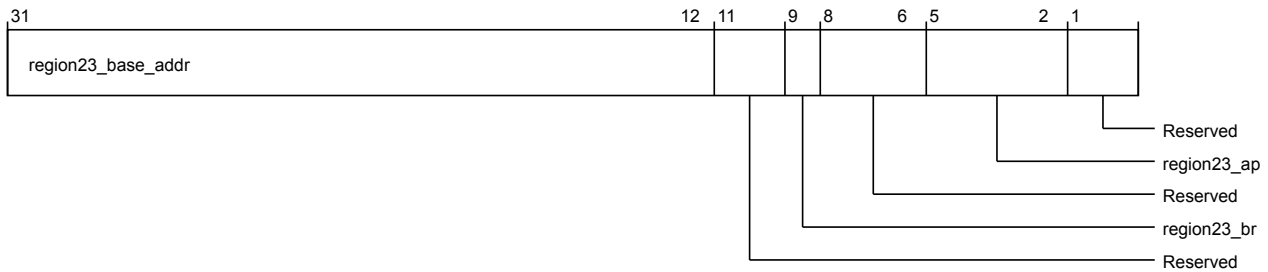


Figure 4-1953 por_mpu_por_mpu_m3_prbar23 (low)

The following table shows the por_mpu_m3_prbar23 lower register bit assignments.

Table 4-1970 por_mpu_por_mpu_m3_prbar23 (low)

Bits	Field name	Description	Type	Reset
31:12	region23_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region23_br	Region 23 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region23_ap	Region 23 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar23

MPU master 0 programmable limit address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D88

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

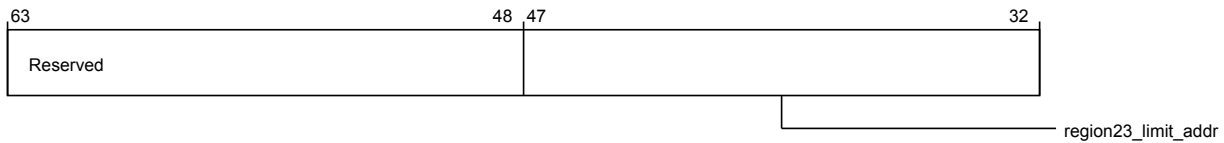


Figure 4-1954 `por_mpu_m3_prlar23` (high)

The following table shows the `por_mpu_m3_prlar23` higher register bit assignments.

Table 4-1971 `por_mpu_m3_prlar23` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region23_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

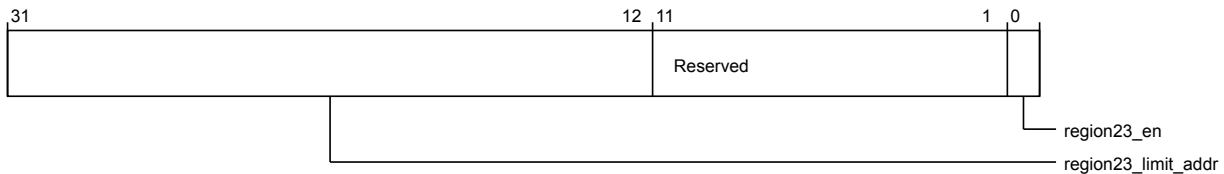


Figure 4-1955 `por_mpu_m3_prlar23` (low)

The following table shows the `por_mpu_m3_prlar23` lower register bit assignments.

Table 4-1972 `por_mpu_m3_prlar23` (low)

Bits	Field name	Description	Type	Reset
31:12	region23_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region23_en	Region 23 enable.	RW	1'b0

`por_mpu_m3_prbar24`

MPU master 0 programmable base address register 24.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1D90
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

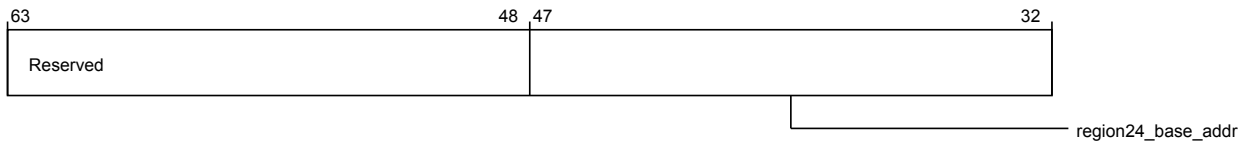


Figure 4-1956 `por_mpu_por_mpu_m3_prbar24` (high)

The following table shows the `por_mpu_m3_prbar24` higher register bit assignments.

Table 4-1973 `por_mpu_por_mpu_m3_prbar24` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

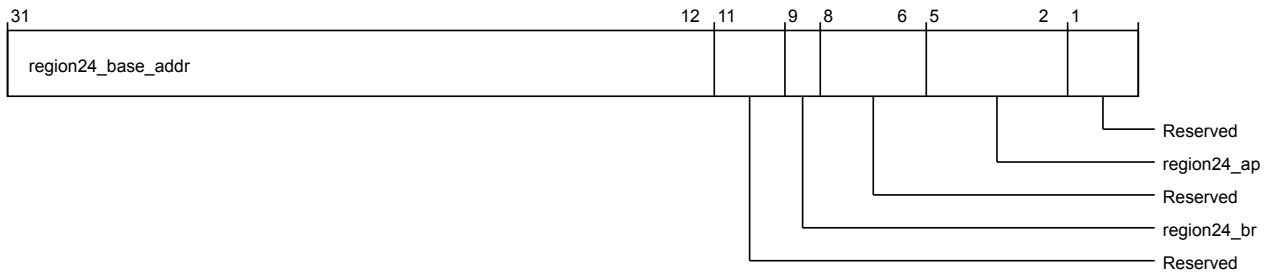


Figure 4-1957 `por_mpu_por_mpu_m3_prbar24` (low)

The following table shows the `por_mpu_m3_prbar24` lower register bit assignments.

Table 4-1974 `por_mpu_por_mpu_m3_prbar24` (low)

Bits	Field name	Description	Type	Reset
31:12	region24_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region24_br	Region 24 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region24_ap	Region 24 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar24

MPU master 0 programmable limit address register 24.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1D98

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

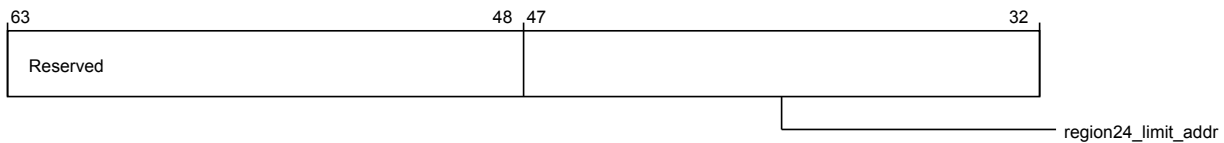


Figure 4-1958 por_mpu_por_mpu_m3_prlar24 (high)

The following table shows the `por_mpu_m3_prlar24` higher register bit assignments.

Table 4-1975 por_mpu_por_mpu_m3_prlar24 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

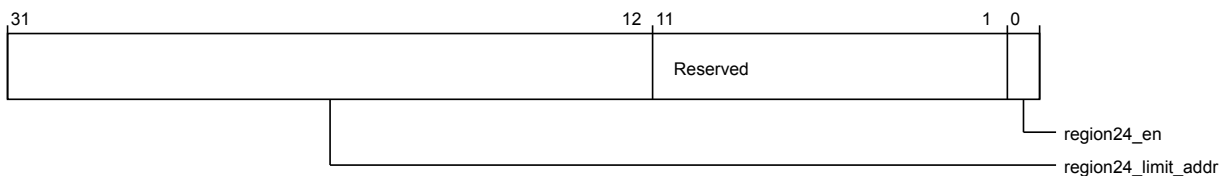


Figure 4-1959 por_mpu_por_mpu_m3_prlar24 (low)

The following table shows the `por_mpu_m3_prlar24` lower register bit assignments.

Table 4-1976 por_mpu_por_mpu_m3_prlar24 (low)

Bits	Field name	Description	Type	Reset
31:12	region24_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region24_en	Region 24 enable.	RW	1'b0

por_mpu_m3_prbar25

MPU master 0 programmable base address register 25.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1DA0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

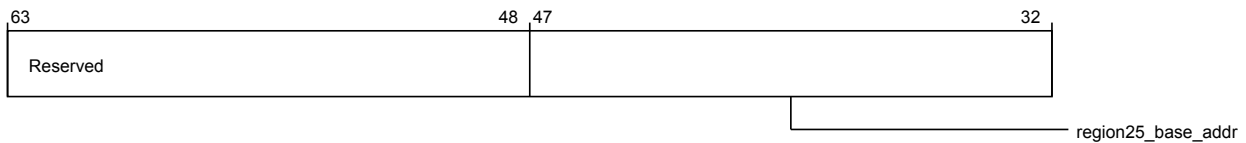


Figure 4-1960 por_mpu_por_mpu_m3_prbar25 (high)

The following table shows the por_mpu_m3_prbar25 higher register bit assignments.

Table 4-1977 por_mpu_por_mpu_m3_prbar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

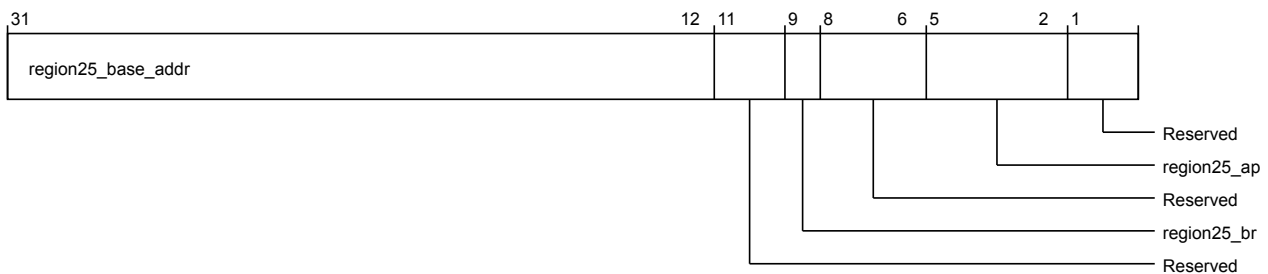


Figure 4-1961 por_mpu_por_mpu_m3_prbar25 (low)

The following table shows the por_mpu_m3_prbar25 lower register bit assignments.

Table 4-1978 por_mpu_por_mpu_m3_prbar25 (low)

Bits	Field name	Description	Type	Reset
31:12	region25_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1978 por_mpu_por_mpu_m3_prbar25 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region25_br	Region 25 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region25_ap	Region 25 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar25

MPU master 0 programmable limit address register 25.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1DA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

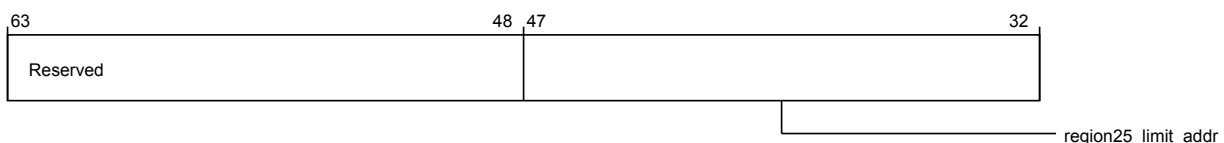


Figure 4-1962 por_mpu_por_mpu_m3_prlar25 (high)

The following table shows the por_mpu_m3_prlar25 higher register bit assignments.

Table 4-1979 por_mpu_por_mpu_m3_prlar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

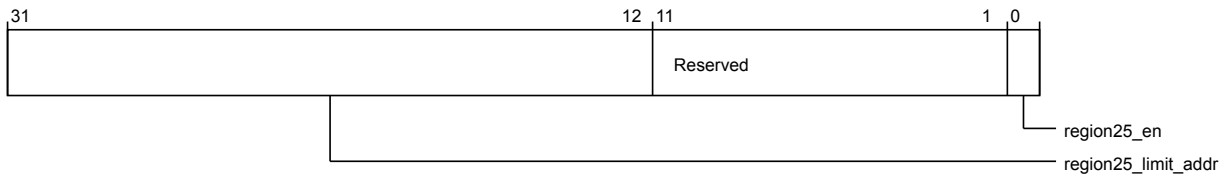


Figure 4-1963 `por_mpu_por_mpu_m3_prlar25` (low)

The following table shows the `por_mpu_m3_prlar25` lower register bit assignments.

Table 4-1980 `por_mpu_por_mpu_m3_prlar25` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region25_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region25_en</code>	Region 25 enable.	RW	1'b0

`por_mpu_m3_prbar26`

MPU master 0 programmable base address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1DB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

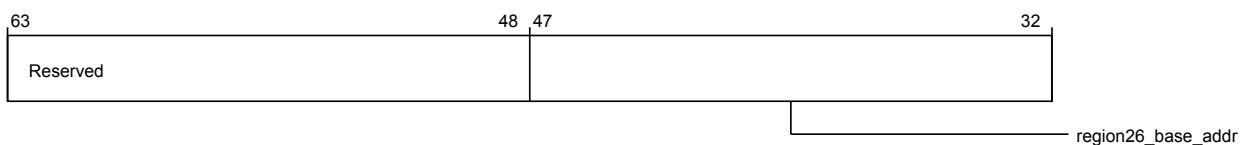


Figure 4-1964 `por_mpu_por_mpu_m3_prbar26` (high)

The following table shows the `por_mpu_m3_prbar26` higher register bit assignments.

Table 4-1981 `por_mpu_por_mpu_m3_prbar26` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region26_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

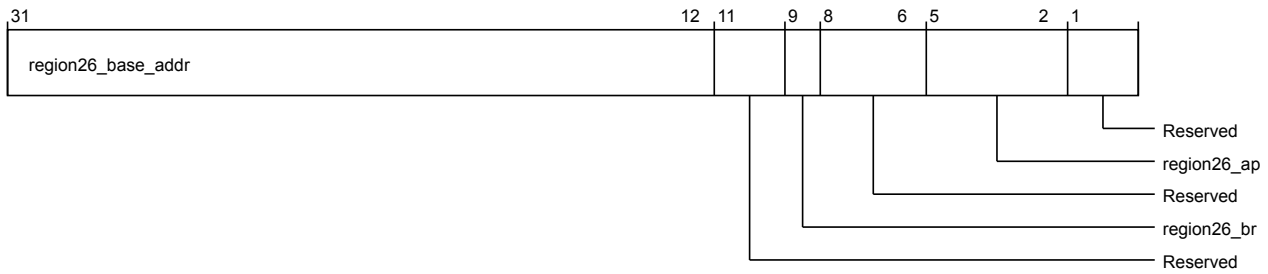


Figure 4-1965 por_mpu_por_mpu_m3_prbar26 (low)

The following table shows the por_mpu_m3_prbar26 lower register bit assignments.

Table 4-1982 por_mpu_por_mpu_m3_prbar26 (low)

Bits	Field name	Description	Type	Reset
31:12	region26_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region26_br	Region 26 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region26_ap	Region 26 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar26

MPU master 0 programmable limit address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1DB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

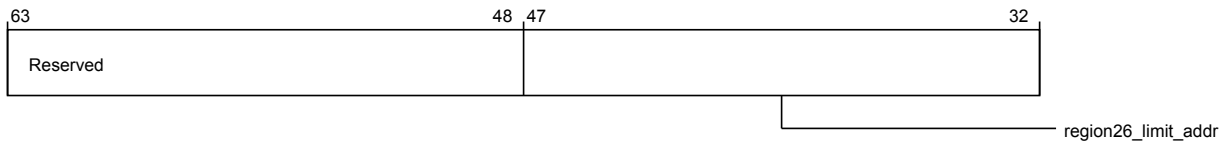


Figure 4-1966 `por_mpu_m3_prlar26` (high)

The following table shows the `por_mpu_m3_prlar26` higher register bit assignments.

Table 4-1983 `por_mpu_m3_prlar26` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region26_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

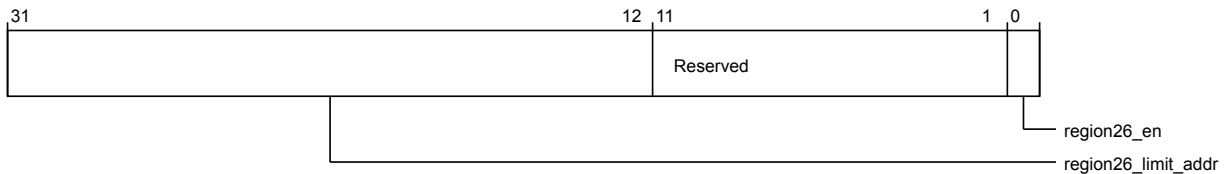


Figure 4-1967 `por_mpu_m3_prlar26` (low)

The following table shows the `por_mpu_m3_prlar26` lower register bit assignments.

Table 4-1984 `por_mpu_m3_prlar26` (low)

Bits	Field name	Description	Type	Reset
31:12	region26_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region26_en	Region 26 enable.	RW	1'b0

`por_mpu_m3_prbar27`

MPU master 0 programmable base address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1DC0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

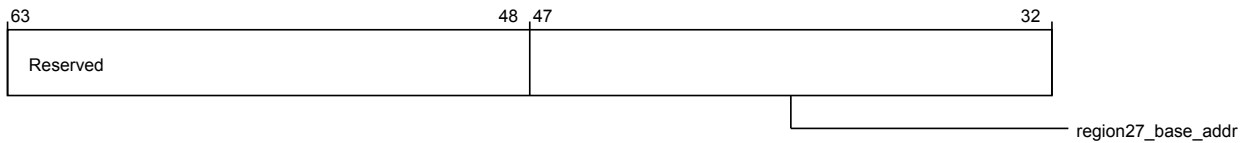


Figure 4-1968 por_mpu_por_mpu_m3_prbar27 (high)

The following table shows the por_mpu_m3_prbar27 higher register bit assignments.

Table 4-1985 por_mpu_por_mpu_m3_prbar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

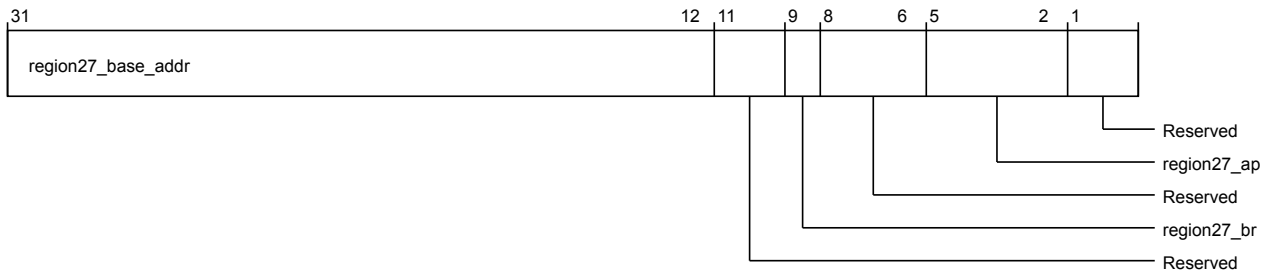


Figure 4-1969 por_mpu_por_mpu_m3_prbar27 (low)

The following table shows the por_mpu_m3_prbar27 lower register bit assignments.

Table 4-1986 por_mpu_por_mpu_m3_prbar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region27_br	Region 27 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region27_ap	Region 27 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar27

MPU master 0 programmable limit address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1DC8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

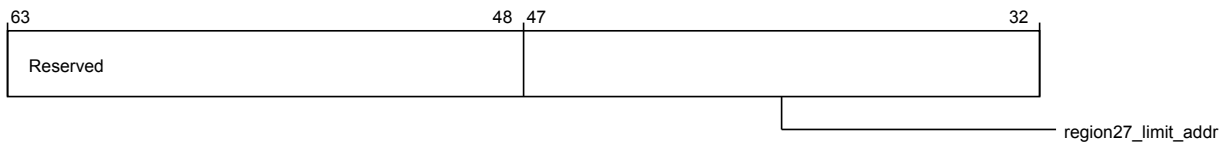


Figure 4-1970 por_mpu_por_mpu_m3_prlar27 (high)

The following table shows the por_mpu_m3_prlar27 higher register bit assignments.

Table 4-1987 por_mpu_por_mpu_m3_prlar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

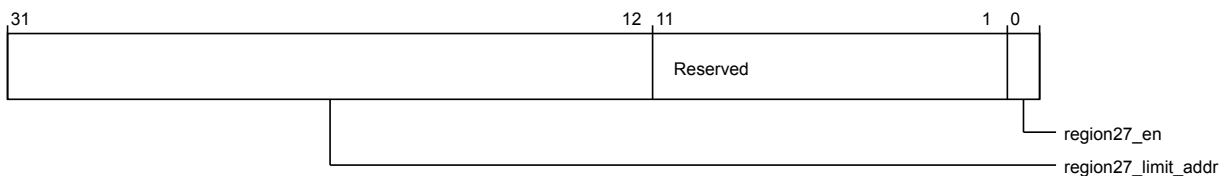


Figure 4-1971 por_mpu_por_mpu_m3_prlar27 (low)

The following table shows the por_mpu_m3_prlar27 lower register bit assignments.

Table 4-1988 por_mpu_por_mpu_m3_prlar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region27_en	Region 27 enable.	RW	1'b0

por_mpu_m3_prbar28

MPU master 0 programmable base address register 28.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1DD0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

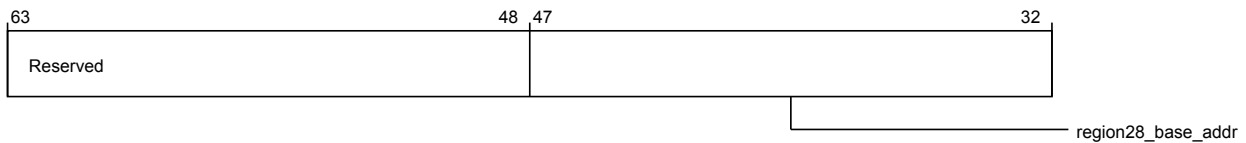


Figure 4-1972 por_mpu_por_mpu_m3_prbar28 (high)

The following table shows the por_mpu_m3_prbar28 higher register bit assignments.

Table 4-1989 por_mpu_por_mpu_m3_prbar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

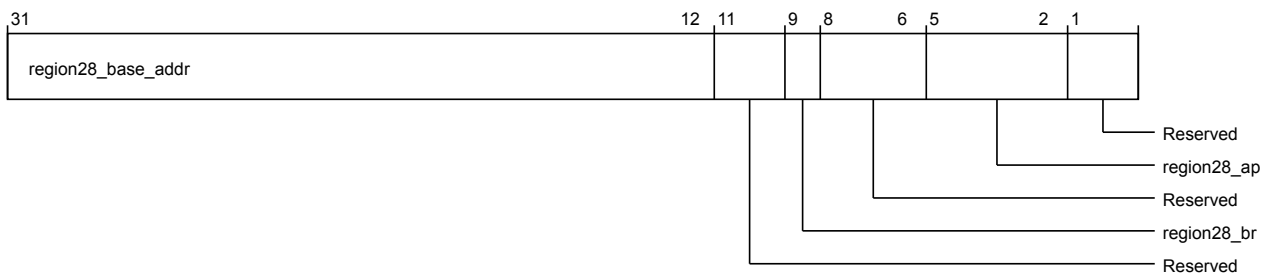


Figure 4-1973 por_mpu_por_mpu_m3_prbar28 (low)

The following table shows the por_mpu_m3_prbar28 lower register bit assignments.

Table 4-1990 por_mpu_por_mpu_m3_prbar28 (low)

Bits	Field name	Description	Type	Reset
31:12	region28_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-1990 por_mpu_por_mpu_m3_prbar28 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region28_br	Region 28 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region28_ap	Region 28 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar28

MPU master 0 programmable limit address register 28.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1DD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

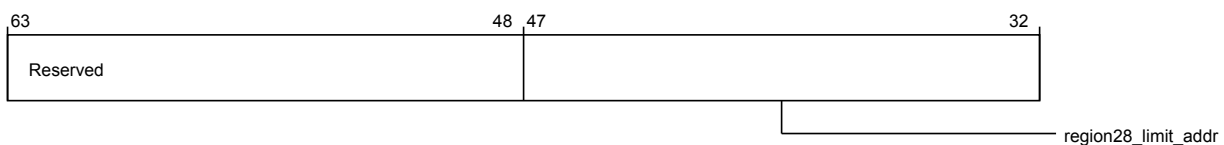


Figure 4-1974 por_mpu_por_mpu_m3_prlar28 (high)

The following table shows the por_mpu_m3_prlar28 higher register bit assignments.

Table 4-1991 por_mpu_por_mpu_m3_prlar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

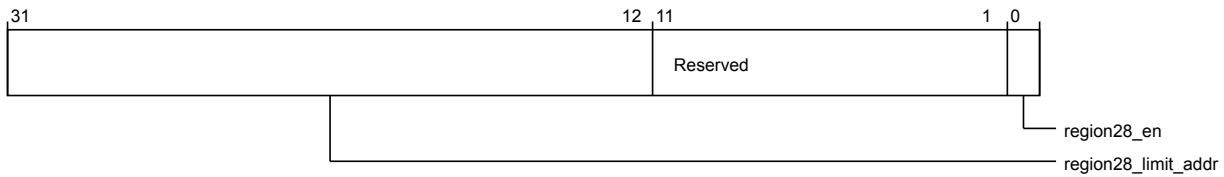


Figure 4-1975 por_mpu_por_mpu_m3_prlar28 (low)

The following table shows the por_mpu_m3_prlar28 lower register bit assignments.

Table 4-1992 por_mpu_por_mpu_m3_prlar28 (low)

Bits	Field name	Description	Type	Reset
31:12	region28_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region28_en	Region 28 enable.	RW	1'b0

por_mpu_m3_prbar29

MPU master 0 programmable base address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1DE0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

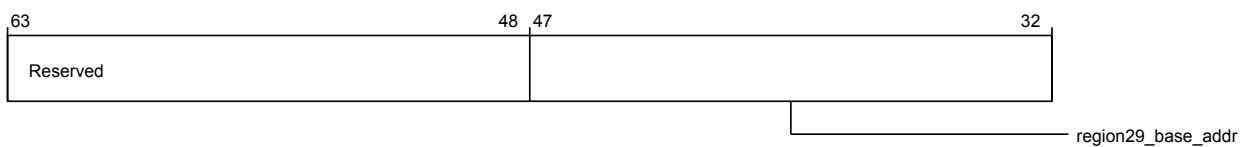


Figure 4-1976 por_mpu_por_mpu_m3_prbar29 (high)

The following table shows the por_mpu_m3_prbar29 higher register bit assignments.

Table 4-1993 por_mpu_por_mpu_m3_prbar29 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region29_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

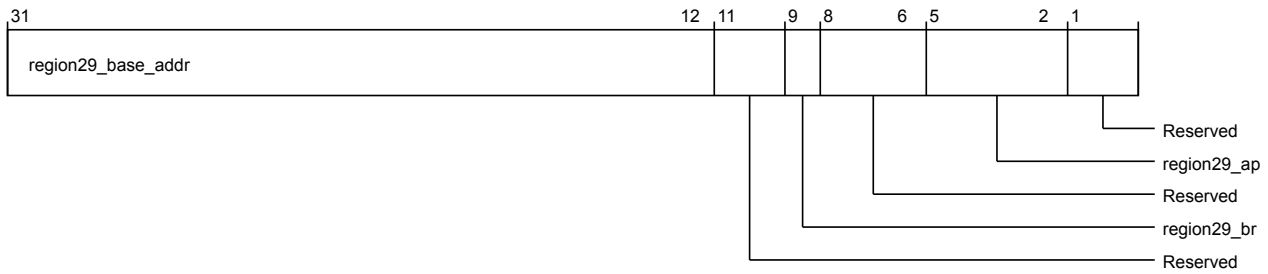


Figure 4-1977 `por_mpu_por_mpu_m3_prbar29` (low)

The following table shows the `por_mpu_m3_prbar29` lower register bit assignments.

Table 4-1994 `por_mpu_por_mpu_m3_prbar29` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region29_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region29_br</code>	Region 29 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region29_ap</code>	Region 29 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m3_prlar29`

MPU master 0 programmable limit address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1DE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

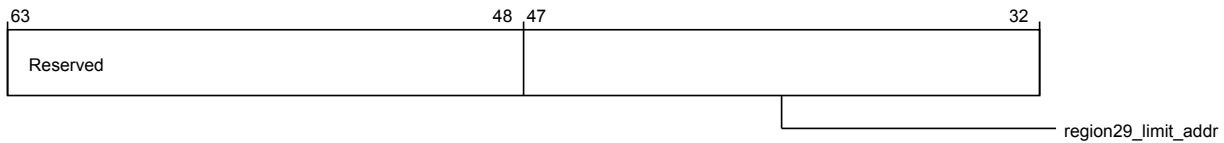


Figure 4-1978 por_mpu_m3_prlar29 (high)

The following table shows the por_mpu_m3_prlar29 higher register bit assignments.

Table 4-1995 por_mpu_m3_prlar29 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region29_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

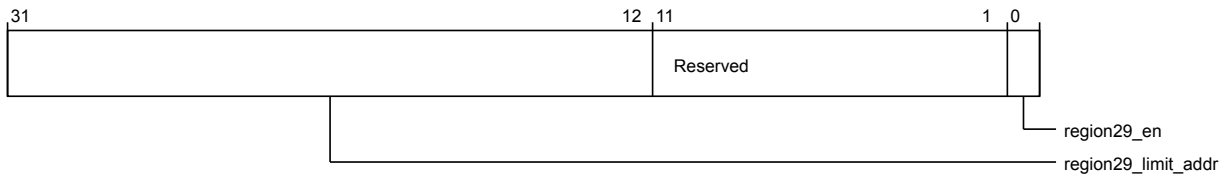


Figure 4-1979 por_mpu_m3_prlar29 (low)

The following table shows the por_mpu_m3_prlar29 lower register bit assignments.

Table 4-1996 por_mpu_m3_prlar29 (low)

Bits	Field name	Description	Type	Reset
31:12	region29_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region29_en	Region 29 enable.	RW	1'b0

por_mpu_m3_prbar30

MPU master 0 programmable base address register 30.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1DF0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

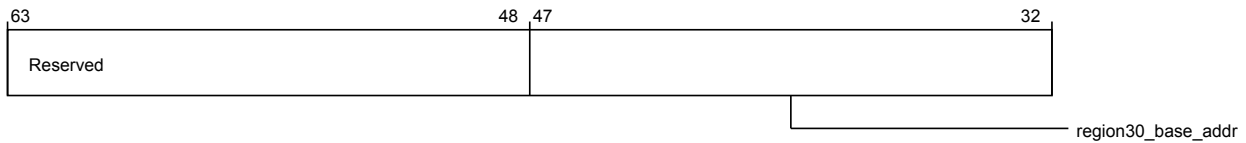


Figure 4-1980 por_mpu_por_mpu_m3_prbar30 (high)

The following table shows the por_mpu_m3_prbar30 higher register bit assignments.

Table 4-1997 por_mpu_por_mpu_m3_prbar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

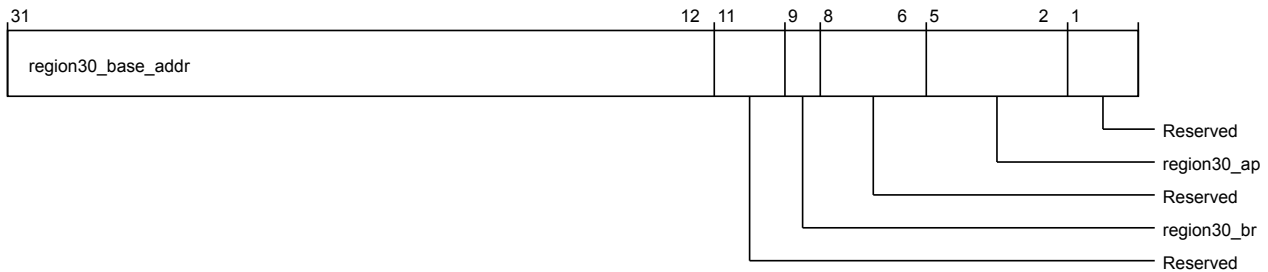


Figure 4-1981 por_mpu_por_mpu_m3_prbar30 (low)

The following table shows the por_mpu_m3_prbar30 lower register bit assignments.

Table 4-1998 por_mpu_por_mpu_m3_prbar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region30_br	Region 30 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region30_ap	Region 30 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar30

MPU master 0 programmable limit address register 30.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1DF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

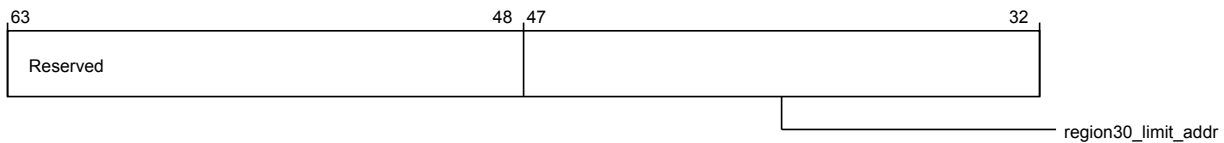


Figure 4-1982 por_mpu_por_mpu_m3_prlar30 (high)

The following table shows the por_mpu_m3_prlar30 higher register bit assignments.

Table 4-1999 por_mpu_por_mpu_m3_prlar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

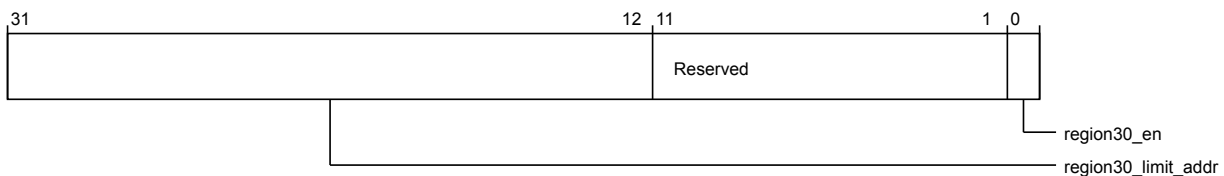


Figure 4-1983 por_mpu_por_mpu_m3_prlar30 (low)

The following table shows the por_mpu_m3_prlar30 lower register bit assignments.

Table 4-2000 por_mpu_por_mpu_m3_prlar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region30_en	Region 30 enable.	RW	1'b0

por_mpu_m3_prbar31

MPU master 0 programmable base address register 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h1E00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

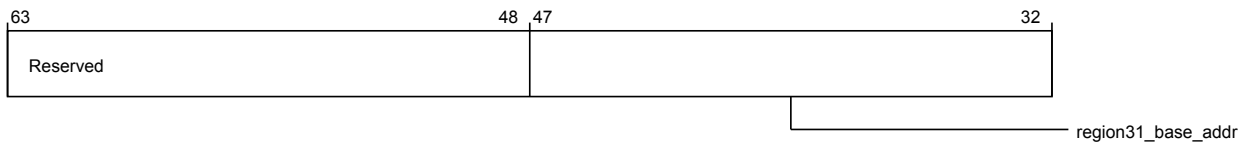


Figure 4-1984 por_mpu_por_mpu_m3_prbar31 (high)

The following table shows the por_mpu_m3_prbar31 higher register bit assignments.

Table 4-2001 por_mpu_por_mpu_m3_prbar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

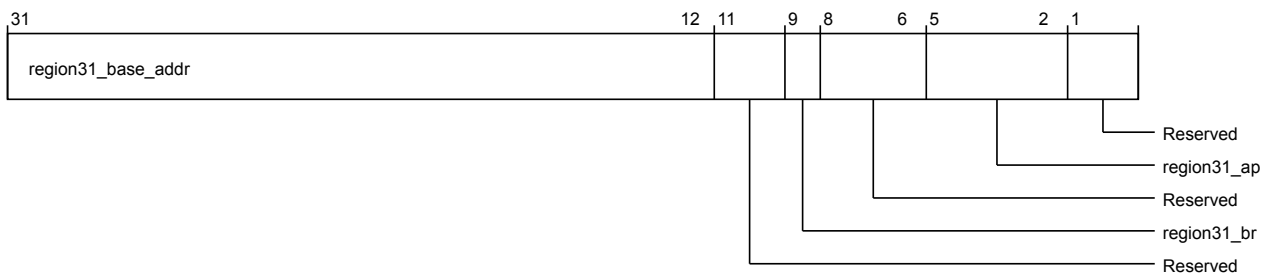


Figure 4-1985 por_mpu_por_mpu_m3_prbar31 (low)

The following table shows the por_mpu_m3_prbar31 lower register bit assignments.

Table 4-2002 por_mpu_por_mpu_m3_prbar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2002 por_mpu_por_mpu_m3_prbar31 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region31_br	Region 31 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region31_ap	Region 31 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m3_prlar31

MPU master 0 programmable limit address register 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1E08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

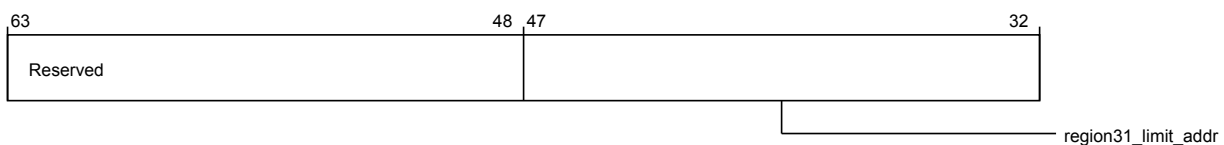


Figure 4-1986 por_mpu_por_mpu_m3_prlar31 (high)

The following table shows the por_mpu_m3_prlar31 higher register bit assignments.

Table 4-2003 por_mpu_por_mpu_m3_prlar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

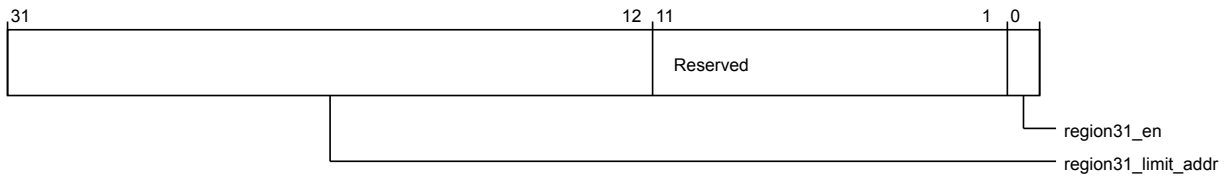


Figure 4-1987 `por_mpu_por_mpu_m3_prlar31` (low)

The following table shows the `por_mpu_m3_prlar31` lower register bit assignments.

Table 4-2004 `por_mpu_por_mpu_m3_prlar31` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region31_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region31_en</code>	Region 31 enable.	RW	1'b0

`por_mpu_m4_ctl`

Functions as the MPU Master 4 control register.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2000

Register reset 64'b010

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

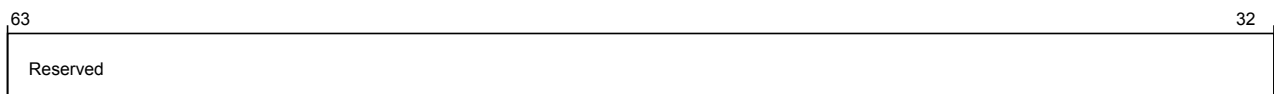


Figure 4-1988 `por_mpu_por_mpu_m4_ctl` (high)

The following table shows the `por_mpu_m4_ctl` higher register bit assignments.

Table 4-2005 `por_mpu_por_mpu_m4_ctl` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

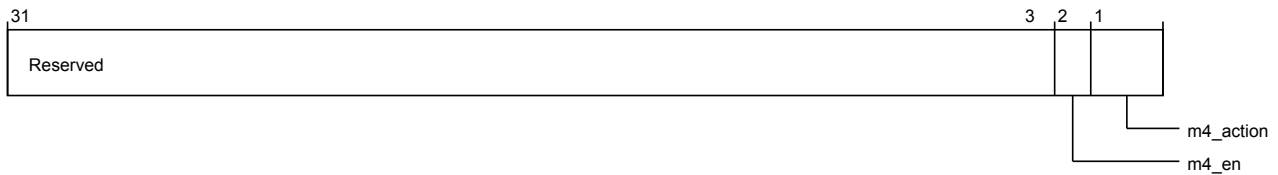


Figure 4-1989 por_mpu_por_mpu_m4_ctl (low)

The following table shows the por_mpu_m4_ctl lower register bit assignments.

Table 4-2006 por_mpu_por_mpu_m4_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	m4_en	MPU master 4 enable.	RW	1'b0
1:0	m4_action	Indicates action HN* should take if no access permission is granted 2'b00: FUSA interrupt 2'b01: Bus error to the originating bus master 2'b10: Both FUSA interrupt and bus error.	RW	2'b10

por_mpu_m4_prbar0

MPU master 0 programmable base address register 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2010

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

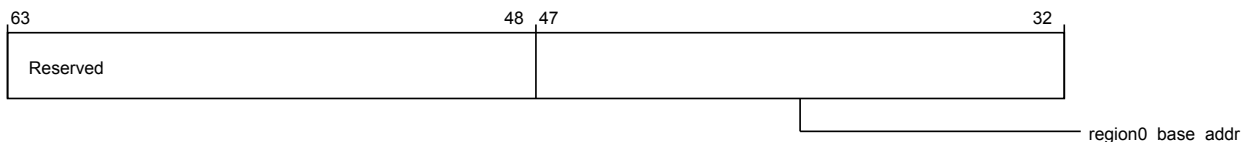


Figure 4-1990 por_mpu_por_mpu_m4_prbar0 (high)

The following table shows the por_mpu_m4_prbar0 higher register bit assignments.

Table 4-2007 por_mpu_por_mpu_m4_prbar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

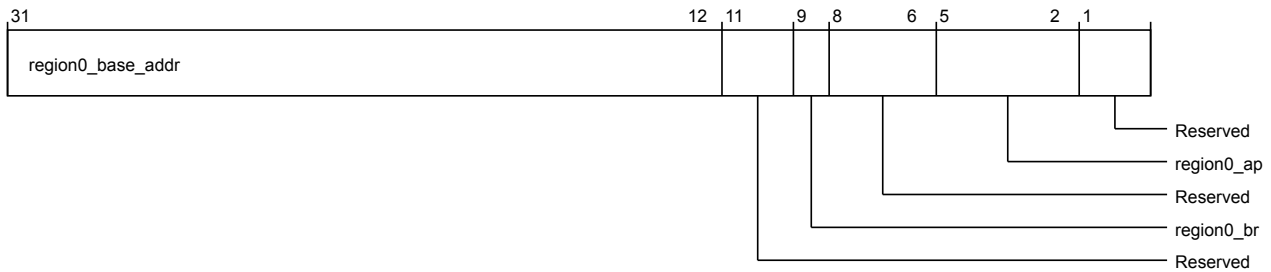


Figure 4-1991 por_mpu_por_mpu_m4_prbar0 (low)

The following table shows the por_mpu_m4_prbar0 lower register bit assignments.

Table 4-2008 por_mpu_por_mpu_m4_prbar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region0_br	Region 0 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region0_ap	Region 0 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar0

MPU master 0 programmable limit address register 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2018
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

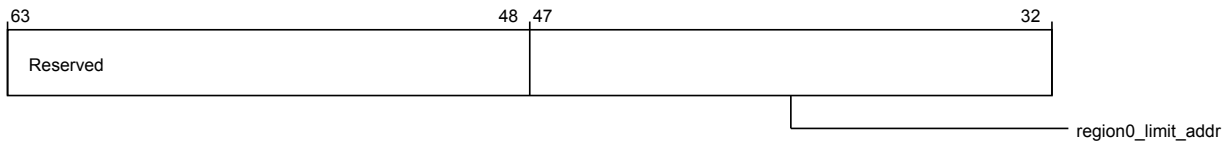


Figure 4-1992 por_mpu_m4_prlar0 (high)

The following table shows the por_mpu_m4_prlar0 higher register bit assignments.

Table 4-2009 por_mpu_m4_prlar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

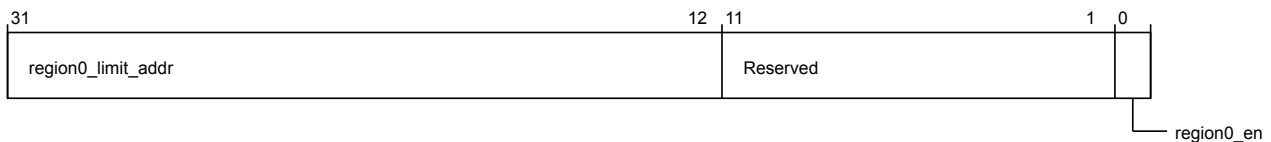


Figure 4-1993 por_mpu_m4_prlar0 (low)

The following table shows the por_mpu_m4_prlar0 lower register bit assignments.

Table 4-2010 por_mpu_m4_prlar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region0_en	Region 0 enable.	RW	1'b0

por_mpu_m4_prbar1

MPU master 0 programmable base address register 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2020
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

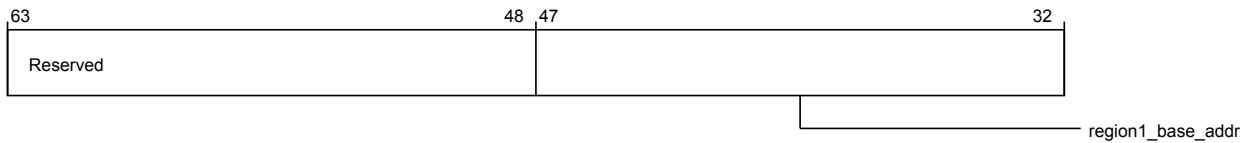


Figure 4-1994 `por_mpu_por_mpu_m4_prbar1` (high)

The following table shows the `por_mpu_m4_prbar1` higher register bit assignments.

Table 4-2011 `por_mpu_por_mpu_m4_prbar1` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region1_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

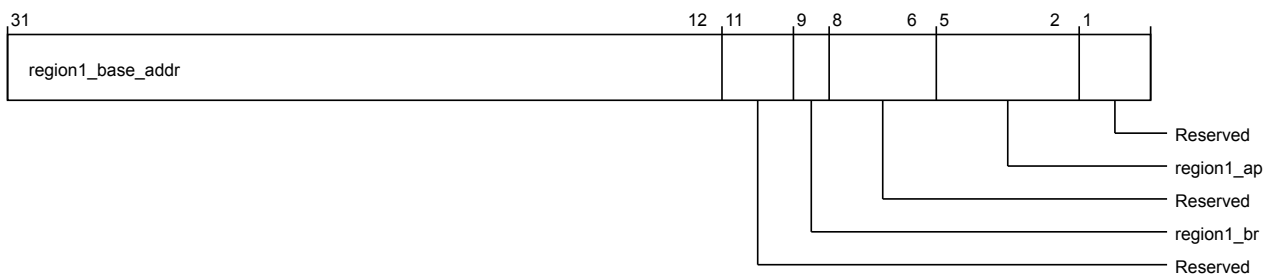


Figure 4-1995 `por_mpu_por_mpu_m4_prbar1` (low)

The following table shows the `por_mpu_m4_prbar1` lower register bit assignments.

Table 4-2012 `por_mpu_por_mpu_m4_prbar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region1_br</code>	Region 1 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-

Table 4-2012 por_mpu_por_mpu_m4_prbar1 (low) (continued)

Bits	Field name	Description	Type	Reset
5:2	region1_ap	Region 1 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar1

MPU master 0 programmable limit address register 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2028

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

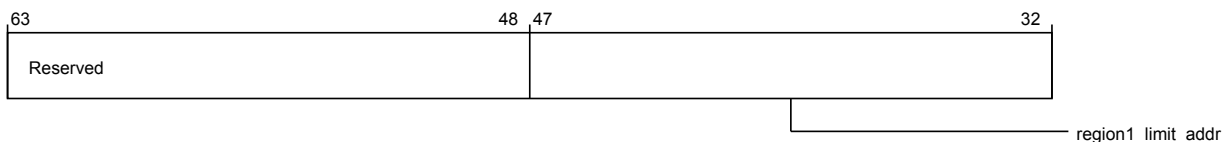


Figure 4-1996 por_mpu_por_mpu_m4_prlar1 (high)

The following table shows the por_mpu_m4_prlar1 higher register bit assignments.

Table 4-2013 por_mpu_por_mpu_m4_prlar1 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region1_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

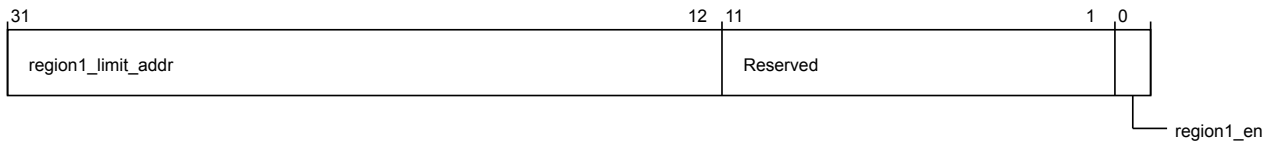


Figure 4-1997 `por_mpu_por_mpu_m4_prlar1` (low)

The following table shows the `por_mpu_m4_prlar1` lower register bit assignments.

Table 4-2014 `por_mpu_por_mpu_m4_prlar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region1_en</code>	Region 1 enable.	RW	1'b0

`por_mpu_m4_prbar2`

MPU master 0 programmable base address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2030

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

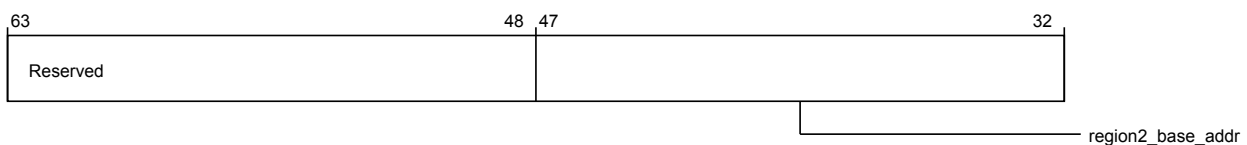


Figure 4-1998 `por_mpu_por_mpu_m4_prbar2` (high)

The following table shows the `por_mpu_m4_prbar2` higher register bit assignments.

Table 4-2015 `por_mpu_por_mpu_m4_prbar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

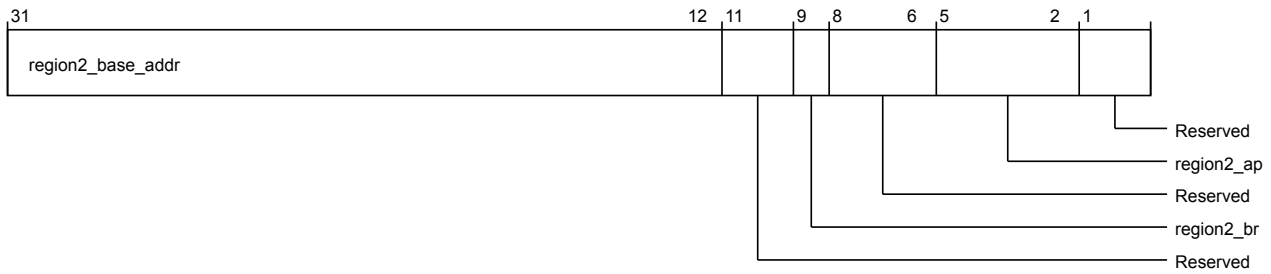


Figure 4-1999 `por_mpu_m4_prbar2` (low)

The following table shows the `por_mpu_m4_prbar2` lower register bit assignments.

Table 4-2016 `por_mpu_m4_prbar2` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region2_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region2_br</code>	Region 2 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region2_ap</code>	Region 2 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m4_prlar2`

MPU master 0 programmable limit address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2038

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

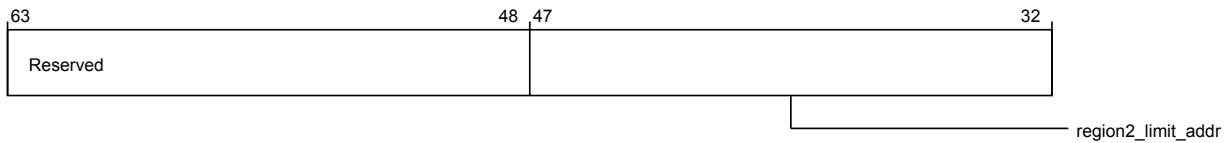


Figure 4-2000 `por_mpu_m4_prlar2` (high)

The following table shows the `por_mpu_m4_prlar2` higher register bit assignments.

Table 4-2017 `por_mpu_m4_prlar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

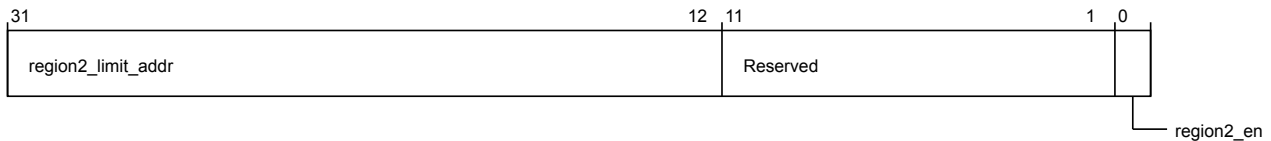


Figure 4-2001 `por_mpu_m4_prlar2` (low)

The following table shows the `por_mpu_m4_prlar2` lower register bit assignments.

Table 4-2018 `por_mpu_m4_prlar2` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region2_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region2_en</code>	Region 2 enable.	RW	1'b0

`por_mpu_m4_prbar3`

MPU master 0 programmable base address register 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2040

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

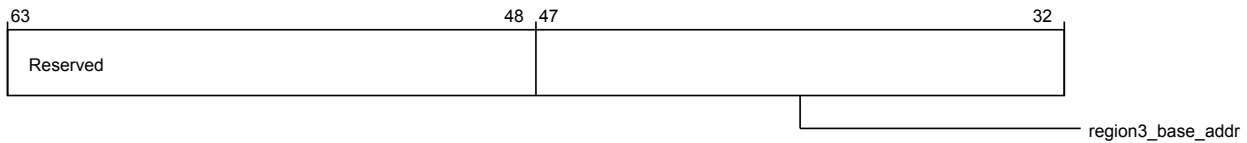


Figure 4-2002 `por_mpu_m4_prbar3` (high)

The following table shows the `por_mpu_m4_prbar3` higher register bit assignments.

Table 4-2019 `por_mpu_m4_prbar3` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

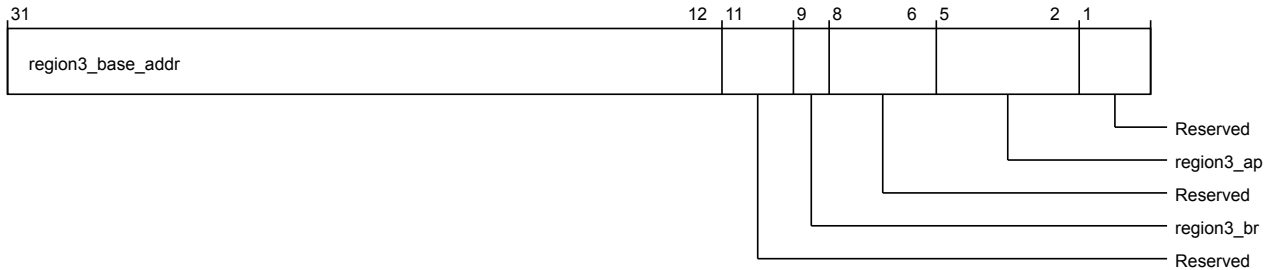


Figure 4-2003 `por_mpu_m4_prbar3` (low)

The following table shows the `por_mpu_m4_prbar3` lower register bit assignments.

Table 4-2020 `por_mpu_m4_prbar3` (low)

Bits	Field name	Description	Type	Reset
31:12	region3_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region3_br	Region 3 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region3_ap	Region 3 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar3

MPU master 0 programmable limit address register 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2048

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

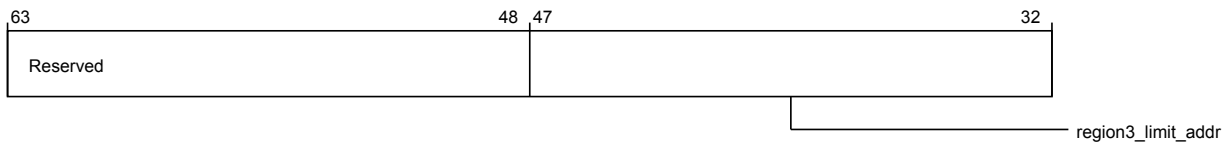


Figure 4-2004 por_mpu_por_mpu_m4_prlar3 (high)

The following table shows the por_mpu_m4_prlar3 higher register bit assignments.

Table 4-2021 por_mpu_por_mpu_m4_prlar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

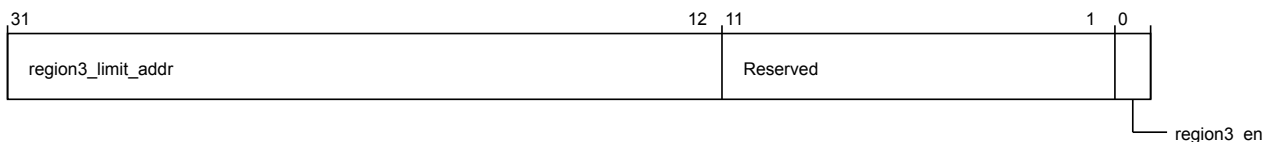


Figure 4-2005 por_mpu_por_mpu_m4_prlar3 (low)

The following table shows the por_mpu_m4_prlar3 lower register bit assignments.

Table 4-2022 por_mpu_por_mpu_m4_prlar3 (low)

Bits	Field name	Description	Type	Reset
31:12	region3_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region3_en	Region 3 enable.	RW	1'b0

por_mpu_m4_prbar4

MPU master 0 programmable base address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2050

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

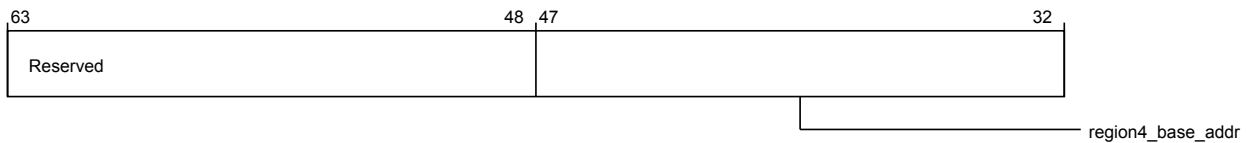


Figure 4-2006 por_mpu_por_mpu_m4_prbar4 (high)

The following table shows the por_mpu_m4_prbar4 higher register bit assignments.

Table 4-2023 por_mpu_por_mpu_m4_prbar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

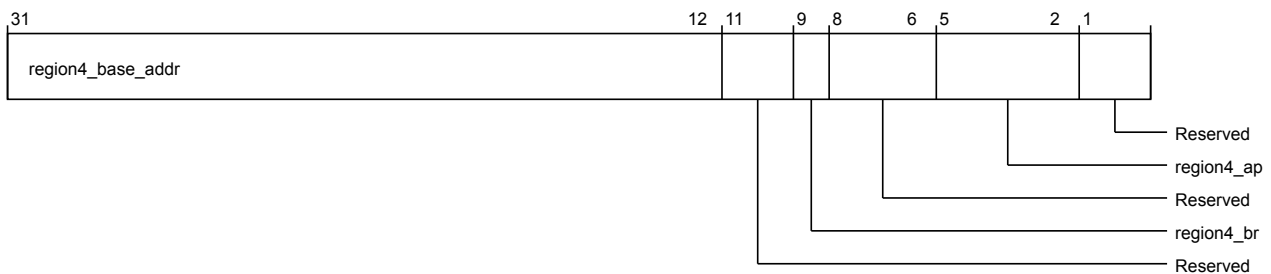


Figure 4-2007 por_mpu_por_mpu_m4_prbar4 (low)

The following table shows the por_mpu_m4_prbar4 lower register bit assignments.

Table 4-2024 por_mpu_por_mpu_m4_prbar4 (low)

Bits	Field name	Description	Type	Reset
31:12	region4_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2024 por_mpu_por_mpu_m4_prbar4 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region4_br	Region 4 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region4_ap	Region 4 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar4

MPU master 0 programmable limit address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2058

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

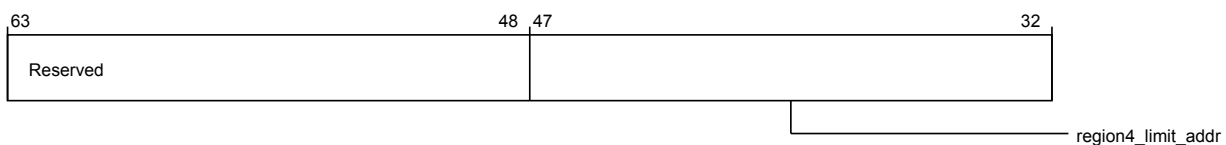


Figure 4-2008 por_mpu_por_mpu_m4_prlar4 (high)

The following table shows the por_mpu_m4_prlar4 higher register bit assignments.

Table 4-2025 por_mpu_por_mpu_m4_prlar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

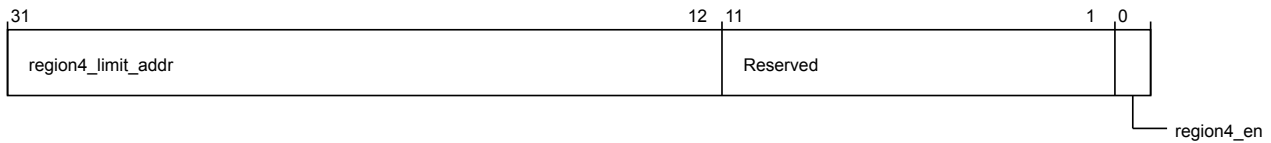


Figure 4-2009 `por_mpu_por_mpu_m4_prlar4` (low)

The following table shows the `por_mpu_m4_prlar4` lower register bit assignments.

Table 4-2026 `por_mpu_por_mpu_m4_prlar4` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region4_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	16'b0
11:1	Reserved	Reserved	RO	-
0	<code>region4_en</code>	Region 4 enable.	RW	1'b0

`por_mpu_m4_prbar5`

MPU master 0 programmable base address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2060

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

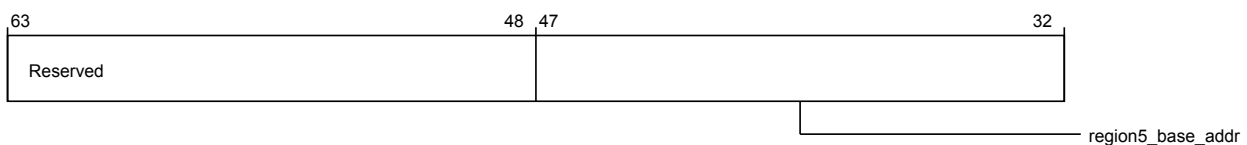


Figure 4-2010 `por_mpu_por_mpu_m4_prbar5` (high)

The following table shows the `por_mpu_m4_prbar5` higher register bit assignments.

Table 4-2027 `por_mpu_por_mpu_m4_prbar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

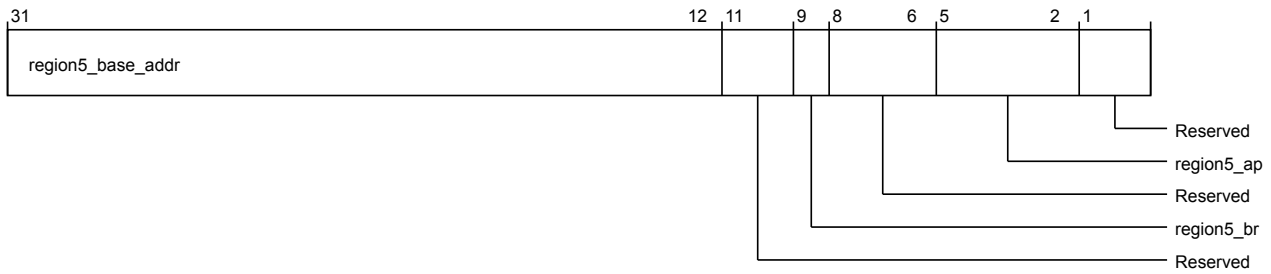


Figure 4-2011 por_mpu_m4_prbar5 (low)

The following table shows the por_mpu_m4_prbar5 lower register bit assignments.

Table 4-2028 por_mpu_m4_prbar5 (low)

Bits	Field name	Description	Type	Reset
31:12	region5_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region5_br	Region 5 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region5_ap	Region 5 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar5

MPU master 0 programmable limit address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2068

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

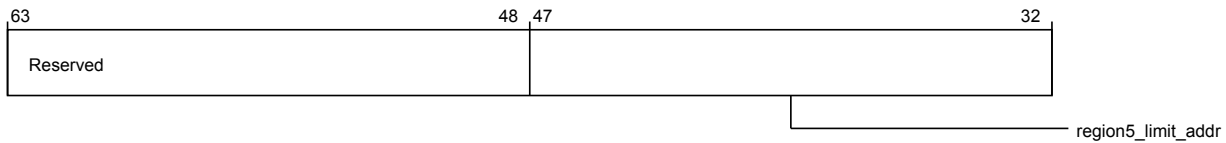


Figure 4-2012 `por_mpu_m4_prlar5` (high)

The following table shows the `por_mpu_m4_prlar5` higher register bit assignments.

Table 4-2029 `por_mpu_m4_prlar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region5_limit_addr	Bits [47:32] of limit address of the range.	RW	316'b0

The following image shows the lower register bit assignments.

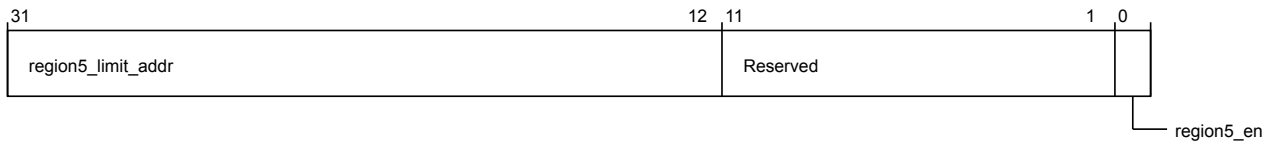


Figure 4-2013 `por_mpu_m4_prlar5` (low)

The following table shows the `por_mpu_m4_prlar5` lower register bit assignments.

Table 4-2030 `por_mpu_m4_prlar5` (low)

Bits	Field name	Description	Type	Reset
31:12	region5_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region5_en	Region 5 enable.	RW	1'b0

`por_mpu_m4_prbar6`

MPU master 0 programmable base address register 6.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2070
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

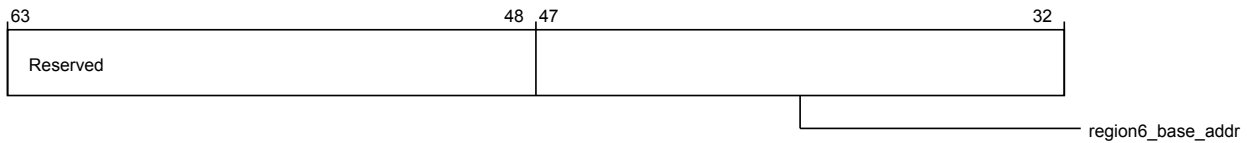


Figure 4-2014 por_mpu_por_mpu_m4_prbar6 (high)

The following table shows the por_mpu_m4_prbar6 higher register bit assignments.

Table 4-2031 por_mpu_por_mpu_m4_prbar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

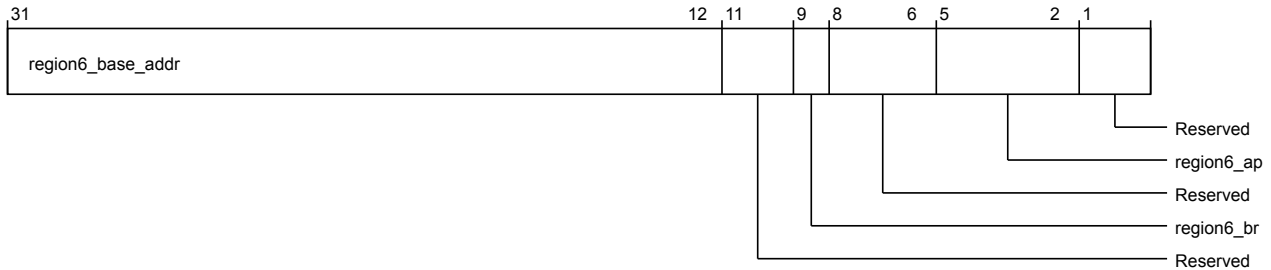


Figure 4-2015 por_mpu_por_mpu_m4_prbar6 (low)

The following table shows the por_mpu_m4_prbar6 lower register bit assignments.

Table 4-2032 por_mpu_por_mpu_m4_prbar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region6_br	Region 6 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region6_ap	Region 6 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar6

MPU master 0 programmable limit address register 6.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2078

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

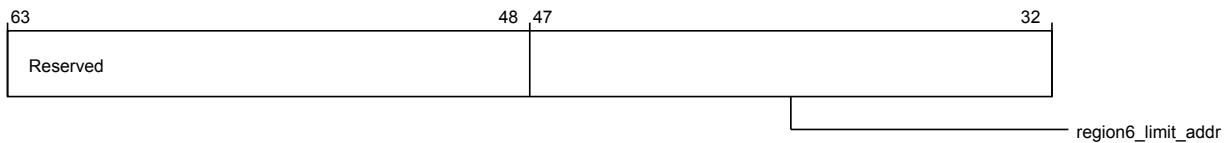


Figure 4-2016 por_mpu_por_mpu_m4_prlar6 (high)

The following table shows the por_mpu_m4_prlar6 higher register bit assignments.

Table 4-2033 por_mpu_por_mpu_m4_prlar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

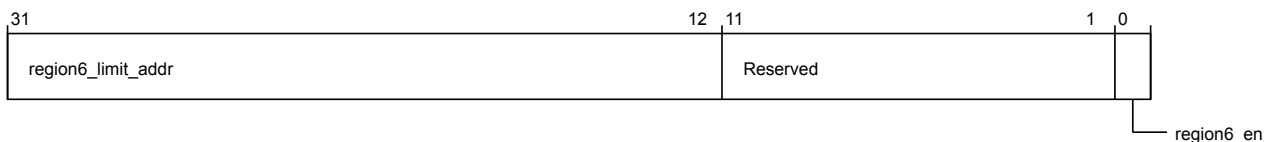


Figure 4-2017 por_mpu_por_mpu_m4_prlar6 (low)

The following table shows the por_mpu_m4_prlar6 lower register bit assignments.

Table 4-2034 por_mpu_por_mpu_m4_prlar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region6_en	Region 6 enable.	RW	1'b0

por_mpu_m4_prbar7

MPU master 0 programmable base address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2080

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

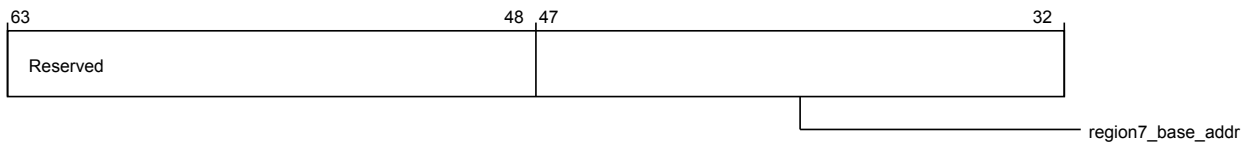


Figure 4-2018 por_mpu_por_mpu_m4_prbar7 (high)

The following table shows the `por_mpu_m4_prbar7` higher register bit assignments.

Table 4-2035 por_mpu_por_mpu_m4_prbar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

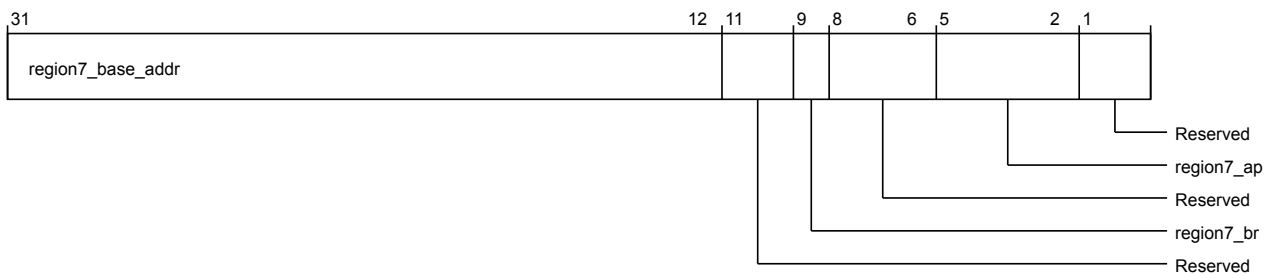


Figure 4-2019 por_mpu_por_mpu_m4_prbar7 (low)

The following table shows the `por_mpu_m4_prbar7` lower register bit assignments.

Table 4-2036 por_mpu_por_mpu_m4_prbar7 (low)

Bits	Field name	Description	Type	Reset
31:12	region7_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2036 por_mpu_por_mpu_m4_prbar7 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region7_br	Region 7 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region7_ap	Region 7 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar7

MPU master 0 programmable limit address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2088

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

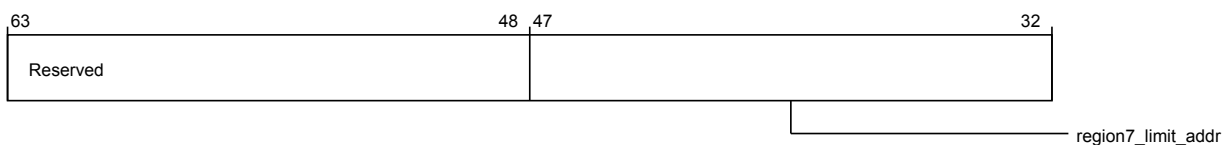


Figure 4-2020 por_mpu_por_mpu_m4_prlar7 (high)

The following table shows the por_mpu_m4_prlar7 higher register bit assignments.

Table 4-2037 por_mpu_por_mpu_m4_prlar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

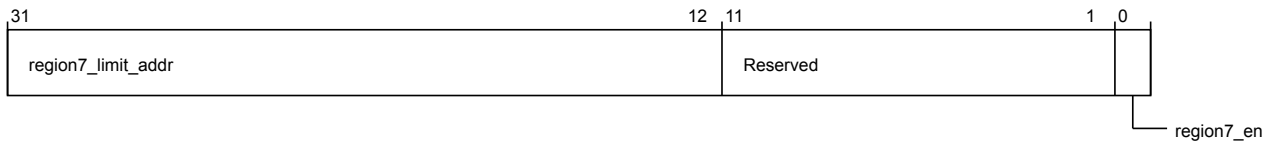


Figure 4-2021 `por_mpu_por_mpu_m4_prlar7` (low)

The following table shows the `por_mpu_m4_prlar7` lower register bit assignments.

Table 4-2038 `por_mpu_por_mpu_m4_prlar7` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region7_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region7_en</code>	Region 7 enable.	RW	1'b0

`por_mpu_m4_prbar8`

MPU master 0 programmable base address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2090

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

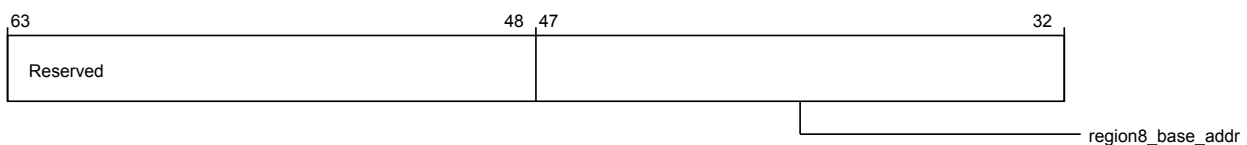


Figure 4-2022 `por_mpu_por_mpu_m4_prbar8` (high)

The following table shows the `por_mpu_m4_prbar8` higher register bit assignments.

Table 4-2039 `por_mpu_por_mpu_m4_prbar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

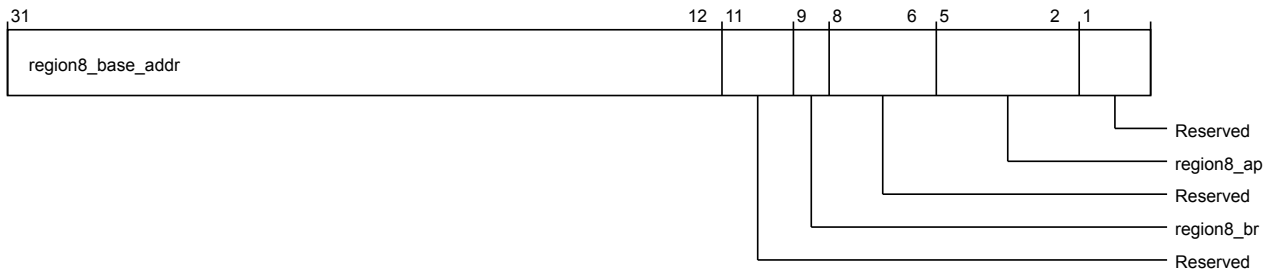


Figure 4-2023 por_mpu_por_mpu_m4_prbar8 (low)

The following table shows the por_mpu_m4_prbar8 lower register bit assignments.

Table 4-2040 por_mpu_por_mpu_m4_prbar8 (low)

Bits	Field name	Description	Type	Reset
31:12	region8_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region8_br	Region 8 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region8_ap	Region 8 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar8

MPU master 0 programmable limit address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2098

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

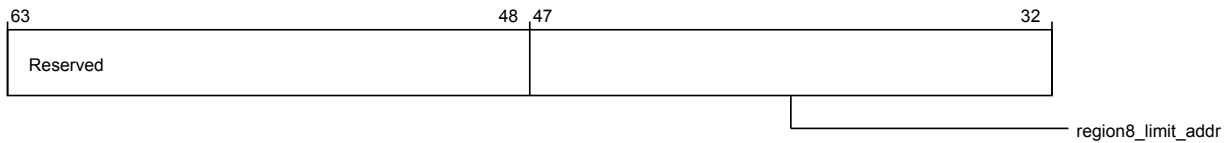


Figure 4-2024 `por_mpu_m4_prlar8` (high)

The following table shows the `por_mpu_m4_prlar8` higher register bit assignments.

Table 4-2041 `por_mpu_m4_prlar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

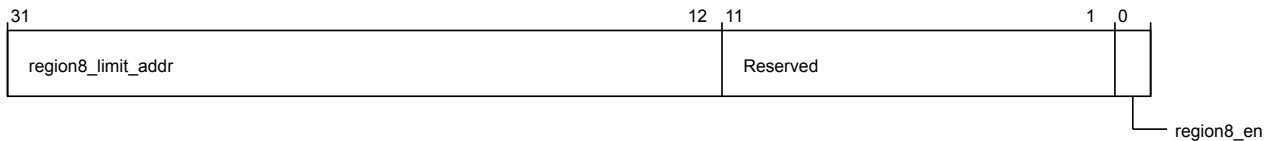


Figure 4-2025 `por_mpu_m4_prlar8` (low)

The following table shows the `por_mpu_m4_prlar8` lower register bit assignments.

Table 4-2042 `por_mpu_m4_prlar8` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region8_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region8_en</code>	Region 8 enable.	RW	1'b0

`por_mpu_m4_prbar9`

MPU master 0 programmable base address register 9.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h20A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

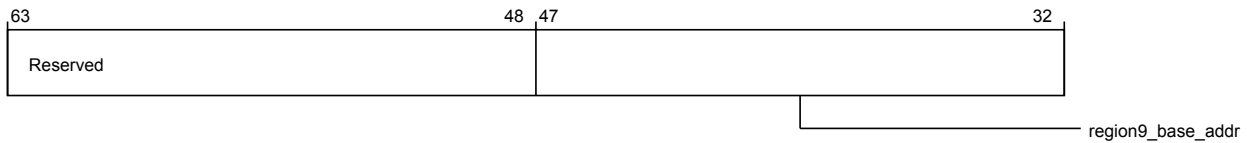


Figure 4-2026 por_mpu_por_mpu_m4_prbar9 (high)

The following table shows the por_mpu_m4_prbar9 higher register bit assignments.

Table 4-2043 por_mpu_por_mpu_m4_prbar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

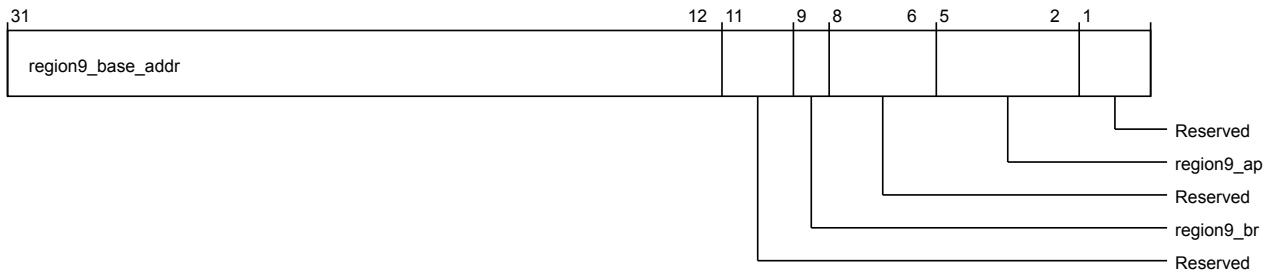


Figure 4-2027 por_mpu_por_mpu_m4_prbar9 (low)

The following table shows the por_mpu_m4_prbar9 lower register bit assignments.

Table 4-2044 por_mpu_por_mpu_m4_prbar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region9_br	Region 9 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region9_ap	Region 9 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar9

MPU master 0 programmable limit address register 9.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h20A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

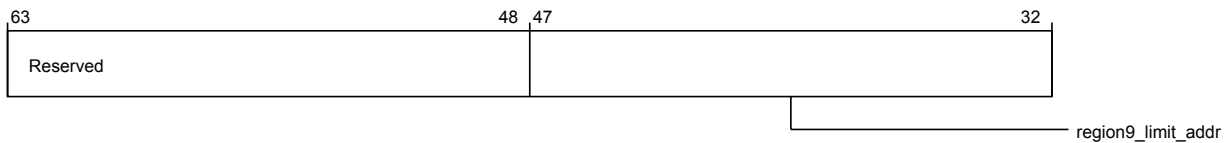


Figure 4-2028 por_mpu_por_mpu_m4_prlar9 (high)

The following table shows the por_mpu_m4_prlar9 higher register bit assignments.

Table 4-2045 por_mpu_por_mpu_m4_prlar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

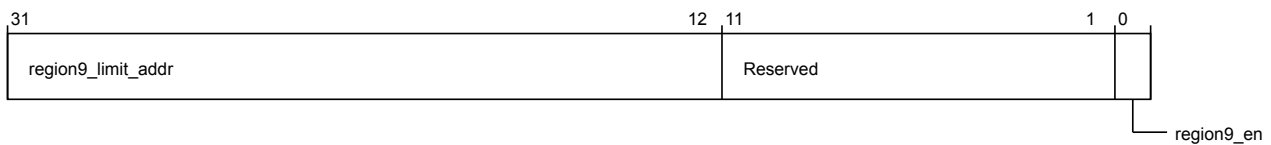


Figure 4-2029 por_mpu_por_mpu_m4_prlar9 (low)

The following table shows the por_mpu_m4_prlar9 lower register bit assignments.

Table 4-2046 por_mpu_por_mpu_m4_prlar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region9_en	Region 9 enable.	RW	1'b0

por_mpu_m4_prbar10

MPU master 0 programmable base address register 10.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h20B0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

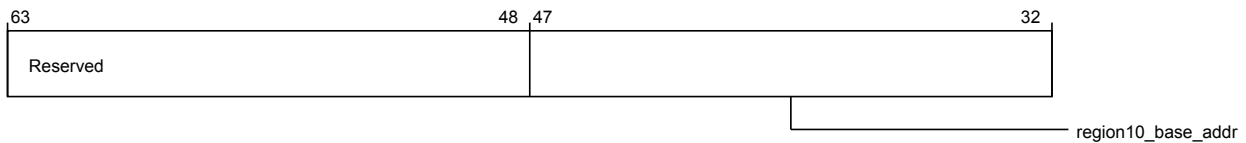


Figure 4-2030 por_mpu_por_mpu_m4_prbar10 (high)

The following table shows the por_mpu_m4_prbar10 higher register bit assignments.

Table 4-2047 por_mpu_por_mpu_m4_prbar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

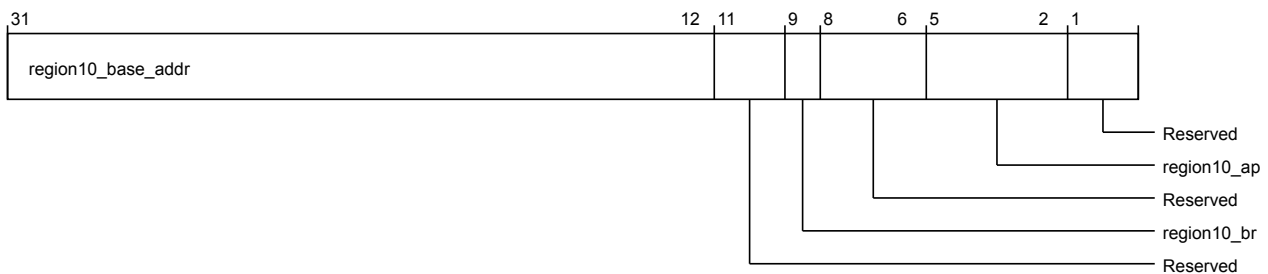


Figure 4-2031 por_mpu_por_mpu_m4_prbar10 (low)

The following table shows the por_mpu_m4_prbar10 lower register bit assignments.

Table 4-2048 por_mpu_por_mpu_m4_prbar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2048 por_mpu_por_mpu_m4_prbar10 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region10_br	Region 10 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region10_ap	Region 10 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar10

MPU master 0 programmable limit address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h20B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

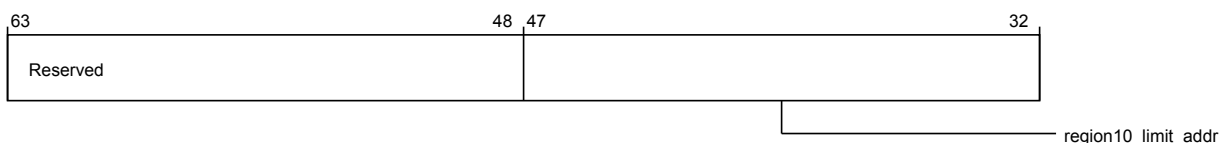


Figure 4-2032 por_mpu_por_mpu_m4_prlar10 (high)

The following table shows the por_mpu_m4_prlar10 higher register bit assignments.

Table 4-2049 por_mpu_por_mpu_m4_prlar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

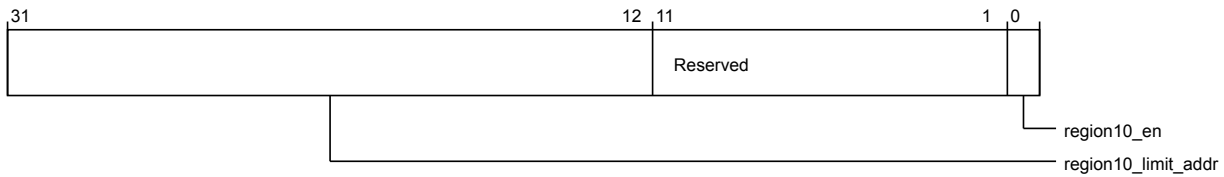


Figure 4-2033 por_mpu_por_mpu_m4_prlar10 (low)

The following table shows the por_mpu_m4_prlar10 lower register bit assignments.

Table 4-2050 por_mpu_por_mpu_m4_prlar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region10_en	Region 10 enable.	RW	1'b0

por_mpu_m4_prbar11

MPU master 0 programmable base address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h20C0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

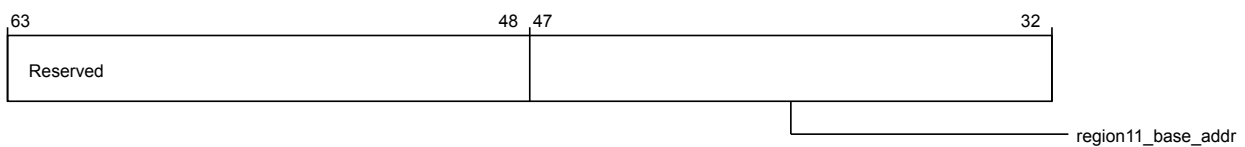


Figure 4-2034 por_mpu_por_mpu_m4_prbar11 (high)

The following table shows the por_mpu_m4_prbar11 higher register bit assignments.

Table 4-2051 por_mpu_por_mpu_m4_prbar11 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

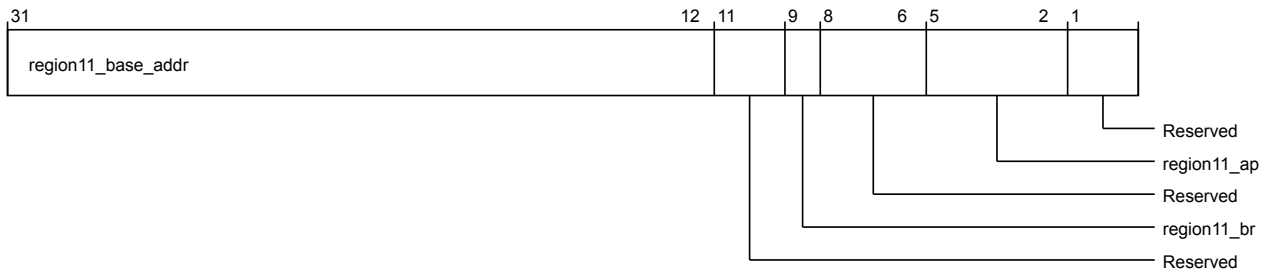


Figure 4-2035 `por_mpu_por_mpu_m4_prbar11` (low)

The following table shows the `por_mpu_m4_prbar11` lower register bit assignments.

Table 4-2052 `por_mpu_por_mpu_m4_prbar11` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region11_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region11_br</code>	Region 11 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region11_ap</code>	Region 11 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m4_prlar11`

MPU master 0 programmable limit address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h20C8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

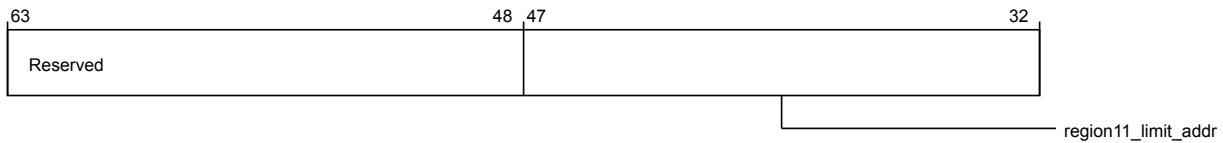


Figure 4-2036 `por_mpu_m4_prlar11` (high)

The following table shows the `por_mpu_m4_prlar11` higher register bit assignments.

Table 4-2053 `por_mpu_m4_prlar11` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_limit_addr	Bits [47:32] of limit address of the range.	RW	20'b0

The following image shows the lower register bit assignments.

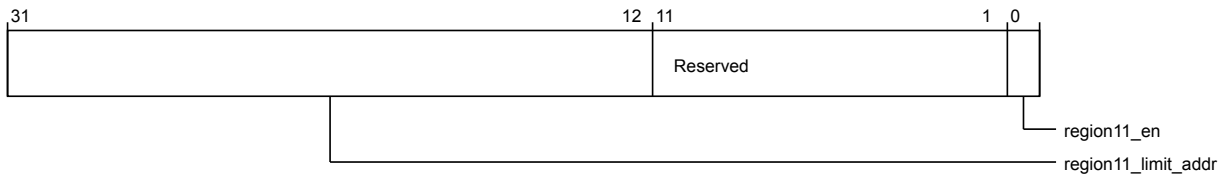


Figure 4-2037 `por_mpu_m4_prlar11` (low)

The following table shows the `por_mpu_m4_prlar11` lower register bit assignments.

Table 4-2054 `por_mpu_m4_prlar11` (low)

Bits	Field name	Description	Type	Reset
31:12	region11_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region11_en	Region 11 enable.	RW	1'b0

`por_mpu_m4_prbar12`

MPU master 0 programmable base address register 12.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h20D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

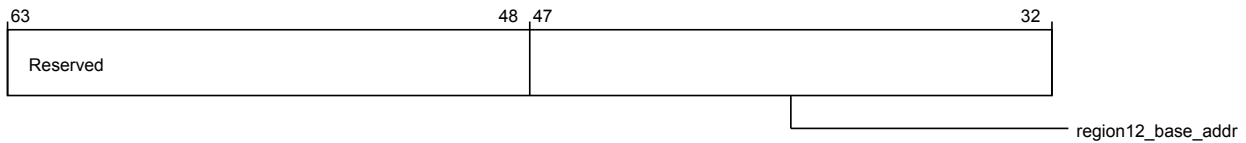


Figure 4-2038 por_mpu_por_mpu_m4_prbar12 (high)

The following table shows the por_mpu_m4_prbar12 higher register bit assignments.

Table 4-2055 por_mpu_por_mpu_m4_prbar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

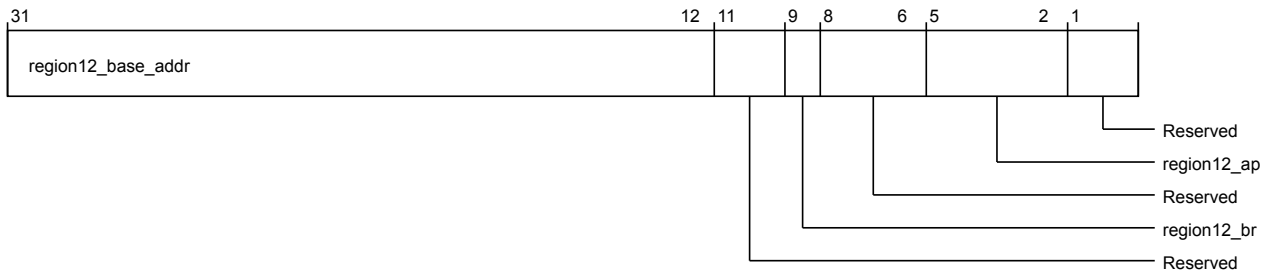


Figure 4-2039 por_mpu_por_mpu_m4_prbar12 (low)

The following table shows the por_mpu_m4_prbar12 lower register bit assignments.

Table 4-2056 por_mpu_por_mpu_m4_prbar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region12_br	Region 12 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region12_ap	Region 12 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar12

MPU master 0 programmable limit address register 12.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h20D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

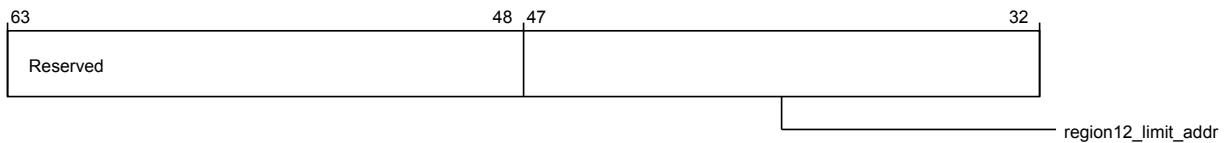


Figure 4-2040 por_mpu_por_mpu_m4_prlar12 (high)

The following table shows the por_mpu_m4_prlar12 higher register bit assignments.

Table 4-2057 por_mpu_por_mpu_m4_prlar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

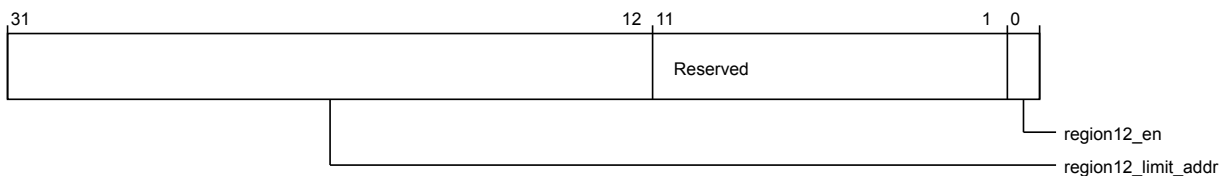


Figure 4-2041 por_mpu_por_mpu_m4_prlar12 (low)

The following table shows the por_mpu_m4_prlar12 lower register bit assignments.

Table 4-2058 por_mpu_por_mpu_m4_prlar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region12_en	Region 12 enable.	RW	1'b0

por_mpu_m4_prbar13

MPU master 0 programmable base address register 13.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h20E0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

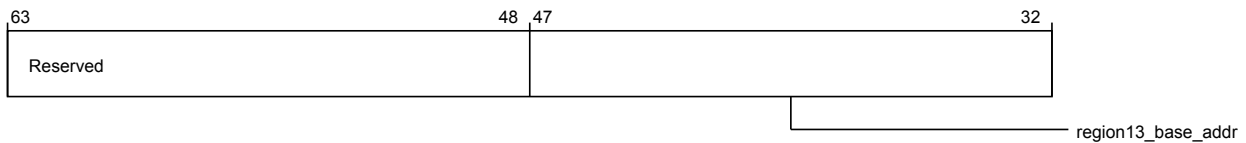


Figure 4-2042 por_mpu_por_mpu_m4_prbar13 (high)

The following table shows the por_mpu_m4_prbar13 higher register bit assignments.

Table 4-2059 por_mpu_por_mpu_m4_prbar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

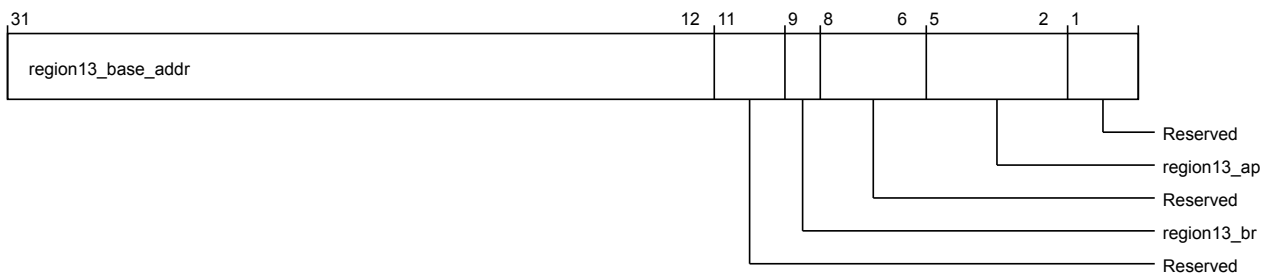


Figure 4-2043 por_mpu_por_mpu_m4_prbar13 (low)

The following table shows the por_mpu_m4_prbar13 lower register bit assignments.

Table 4-2060 por_mpu_por_mpu_m4_prbar13 (low)

Bits	Field name	Description	Type	Reset
31:12	region13_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2060 por_mpu_por_mpu_m4_prbar13 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region13_br	Region 13 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region13_ap	Region 13 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar13

MPU master 0 programmable limit address register 13.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h20E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

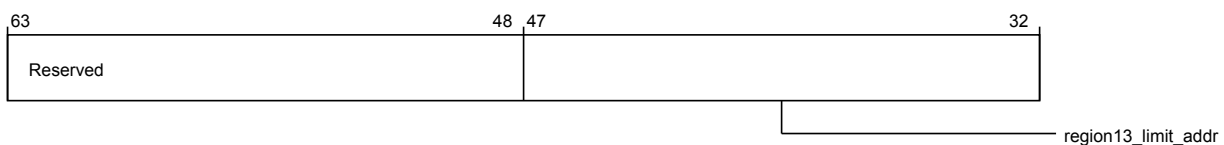


Figure 4-2044 por_mpu_por_mpu_m4_prlar13 (high)

The following table shows the por_mpu_m4_prlar13 higher register bit assignments.

Table 4-2061 por_mpu_por_mpu_m4_prlar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

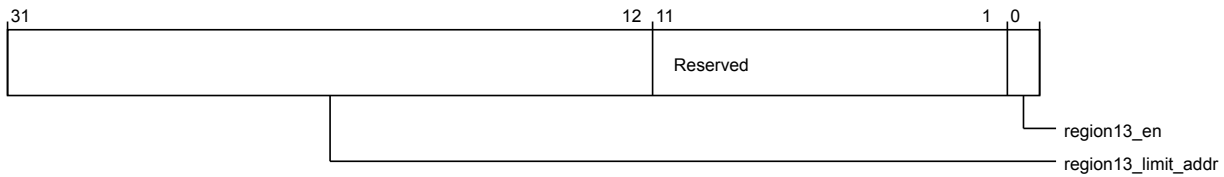


Figure 4-2045 `por_mpu_por_mpu_m4_prlar13` (low)

The following table shows the `por_mpu_m4_prlar13` lower register bit assignments.

Table 4-2062 `por_mpu_por_mpu_m4_prlar13` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region13_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region13_en</code>	Region 13 enable.	RW	1'b0

`por_mpu_m4_prbar14`

MPU master 0 programmable base address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h20F0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

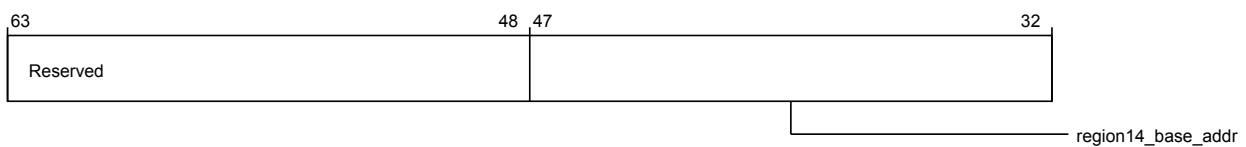


Figure 4-2046 `por_mpu_por_mpu_m4_prbar14` (high)

The following table shows the `por_mpu_m4_prbar14` higher register bit assignments.

Table 4-2063 `por_mpu_por_mpu_m4_prbar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region14_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

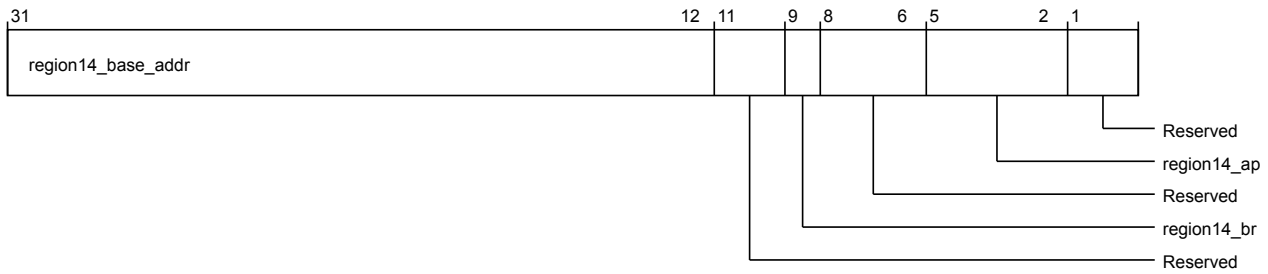


Figure 4-2047 `por_mpu_por_mpu_m4_prbar14` (low)

The following table shows the `por_mpu_m4_prbar14` lower register bit assignments.

Table 4-2064 `por_mpu_por_mpu_m4_prbar14` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region14_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region14_br</code>	Region 14 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region14_ap</code>	Region 14 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m4_prlar14`

MPU master 0 programmable limit address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h20F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

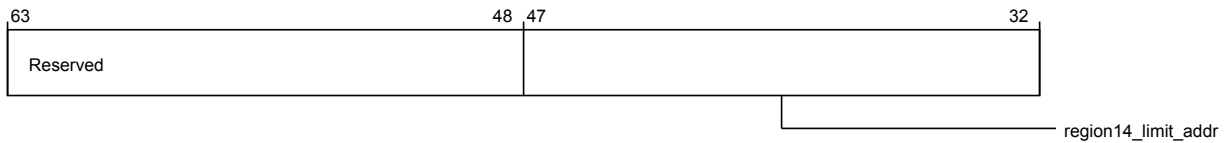


Figure 4-2048 por_mpu_m4_prlar14 (high)

The following table shows the por_mpu_m4_prlar14 higher register bit assignments.

Table 4-2065 por_mpu_m4_prlar14 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region14_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

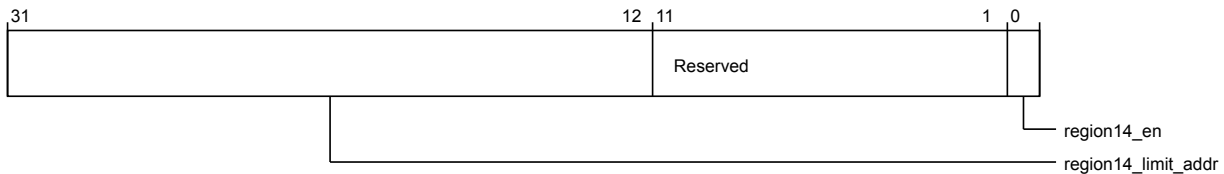


Figure 4-2049 por_mpu_m4_prlar14 (low)

The following table shows the por_mpu_m4_prlar14 lower register bit assignments.

Table 4-2066 por_mpu_m4_prlar14 (low)

Bits	Field name	Description	Type	Reset
31:12	region14_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region14_en	Region 14 enable.	RW	1'b0

por_mpu_m4_prbar15

MPU master 0 programmable base address register 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2100
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

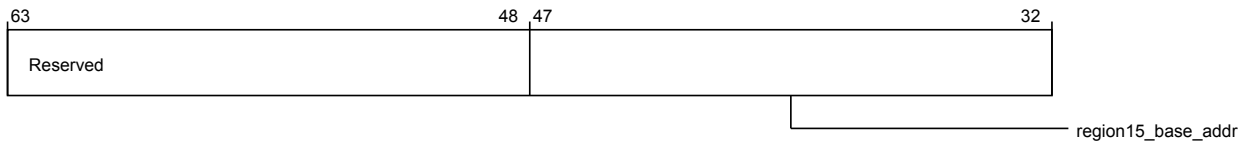


Figure 4-2050 `por_mpu_por_mpu_m4_prbar15` (high)

The following table shows the `por_mpu_m4_prbar15` higher register bit assignments.

Table 4-2067 `por_mpu_por_mpu_m4_prbar15` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

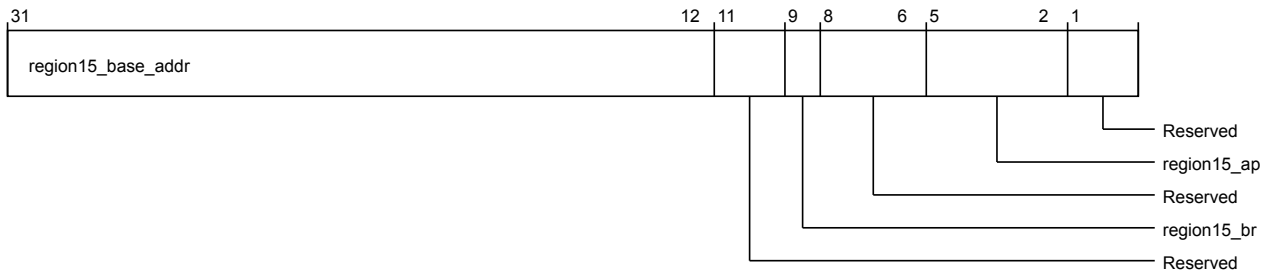


Figure 4-2051 `por_mpu_por_mpu_m4_prbar15` (low)

The following table shows the `por_mpu_m4_prbar15` lower register bit assignments.

Table 4-2068 `por_mpu_por_mpu_m4_prbar15` (low)

Bits	Field name	Description	Type	Reset
31:12	region15_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region15_br	Region 15 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region15_ap	Region 15 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar15

MPU master 0 programmable limit address register 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2108

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

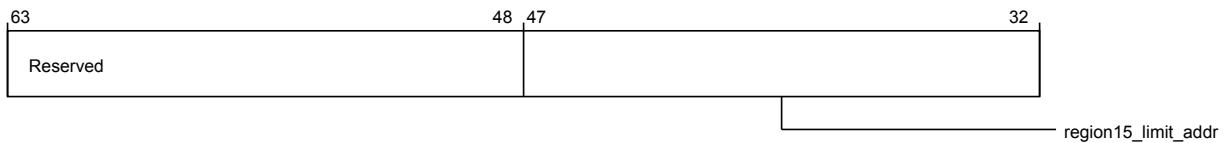


Figure 4-2052 por_mpu_por_mpu_m4_prlar15 (high)

The following table shows the por_mpu_m4_prlar15 higher register bit assignments.

Table 4-2069 por_mpu_por_mpu_m4_prlar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

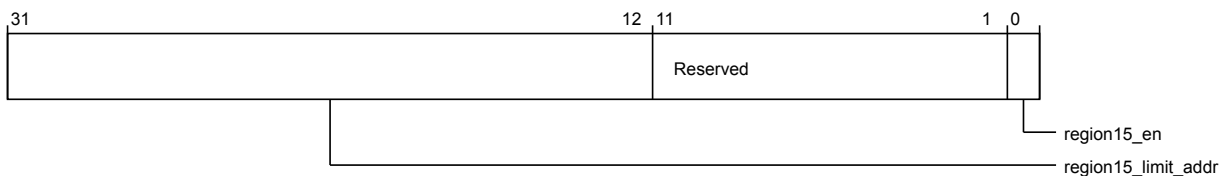


Figure 4-2053 por_mpu_por_mpu_m4_prlar15 (low)

The following table shows the por_mpu_m4_prlar15 lower register bit assignments.

Table 4-2070 por_mpu_por_mpu_m4_prlar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region15_en	Region 15 enable.	RW	1'b0

por_mpu_m4_prbar16

MPU master 0 programmable base address register 16.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2110
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

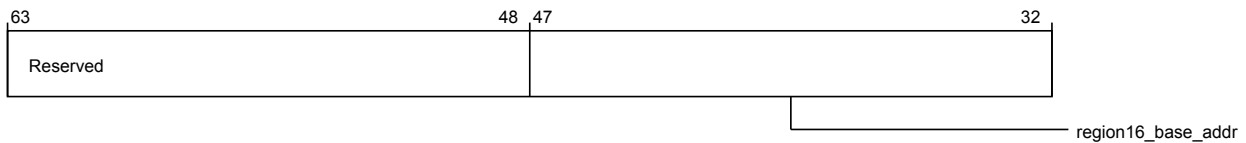


Figure 4-2054 por_mpu_por_mpu_m4_prbar16 (high)

The following table shows the por_mpu_m4_prbar16 higher register bit assignments.

Table 4-2071 por_mpu_por_mpu_m4_prbar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

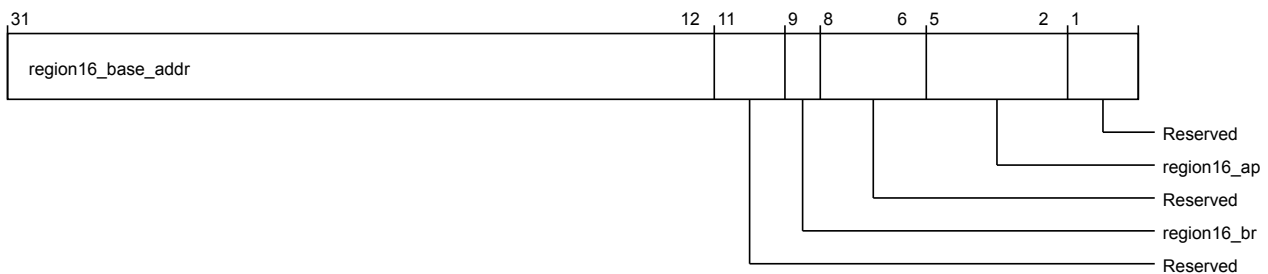


Figure 4-2055 por_mpu_por_mpu_m4_prbar16 (low)

The following table shows the por_mpu_m4_prbar16 lower register bit assignments.

Table 4-2072 por_mpu_por_mpu_m4_prbar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2072 por_mpu_por_mpu_m4_prbar16 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region16_br	Region 16 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region16_ap	Region 16 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar16

MPU master 0 programmable limit address register 16.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2118

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

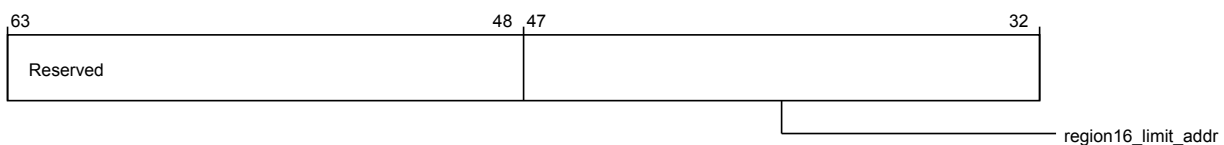


Figure 4-2056 por_mpu_por_mpu_m4_prlar16 (high)

The following table shows the por_mpu_m4_prlar16 higher register bit assignments.

Table 4-2073 por_mpu_por_mpu_m4_prlar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

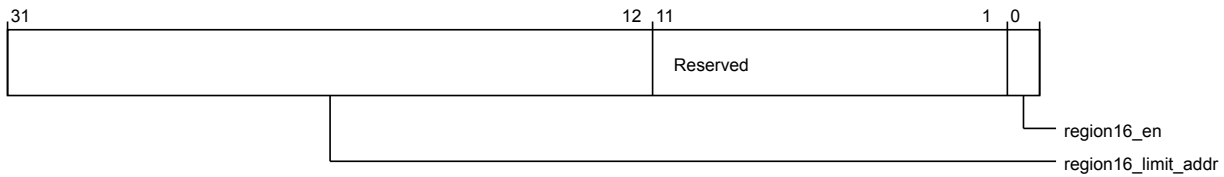


Figure 4-2057 `por_mpu_por_mpu_m4_prlar16` (low)

The following table shows the `por_mpu_m4_prlar16` lower register bit assignments.

Table 4-2074 `por_mpu_por_mpu_m4_prlar16` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region16_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region16_en</code>	Region 16 enable.	RW	1'b0

`por_mpu_m4_prbar17`

MPU master 0 programmable base address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2120

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

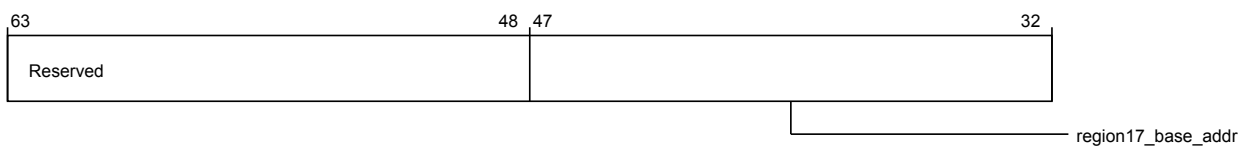


Figure 4-2058 `por_mpu_por_mpu_m4_prbar17` (high)

The following table shows the `por_mpu_m4_prbar17` higher register bit assignments.

Table 4-2075 `por_mpu_por_mpu_m4_prbar17` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region17_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

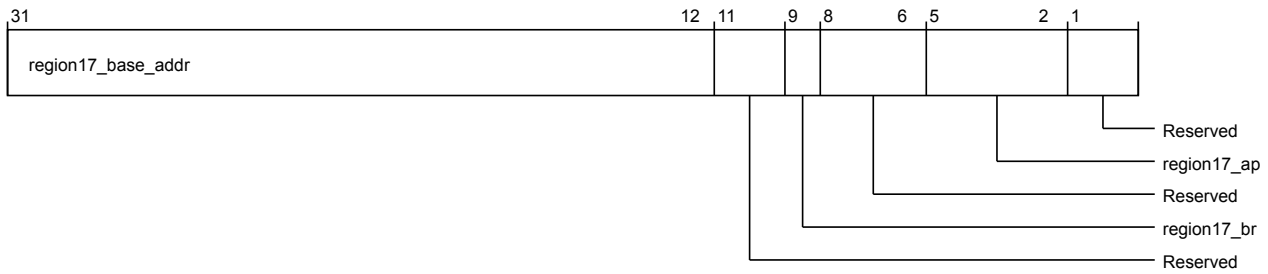


Figure 4-2059 `por_mpu_por_mpu_m4_prbar17` (low)

The following table shows the `por_mpu_m4_prbar17` lower register bit assignments.

Table 4-2076 `por_mpu_por_mpu_m4_prbar17` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region17_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region17_br</code>	Region 17 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region17_ap</code>	Region 17 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m4_prlar17`

MPU master 0 programmable limit address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2128

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

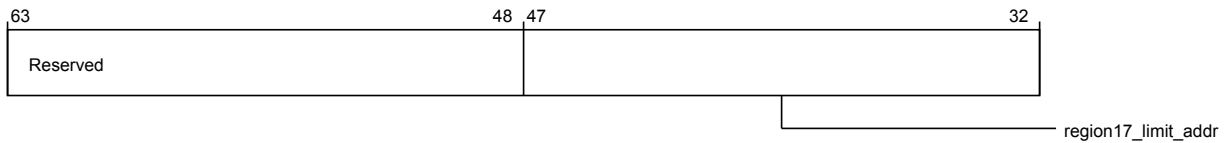


Figure 4-2060 por_mpu_m4_prlar17 (high)

The following table shows the por_mpu_m4_prlar17 higher register bit assignments.

Table 4-2077 por_mpu_m4_prlar17 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

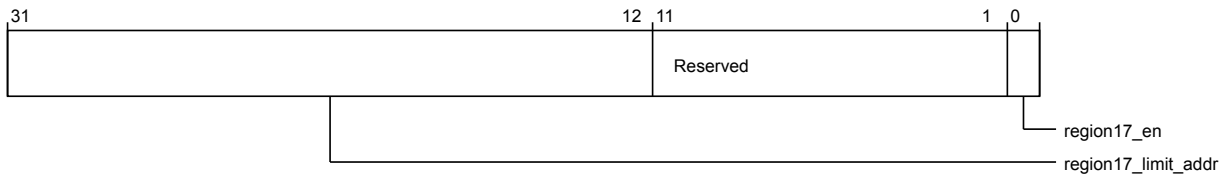


Figure 4-2061 por_mpu_m4_prlar17 (low)

The following table shows the por_mpu_m4_prlar17 lower register bit assignments.

Table 4-2078 por_mpu_m4_prlar17 (low)

Bits	Field name	Description	Type	Reset
31:12	region17_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region17_en	Region 17 enable.	RW	1'b0

por_mpu_m4_prbar18

MPU master 0 programmable base address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2130
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

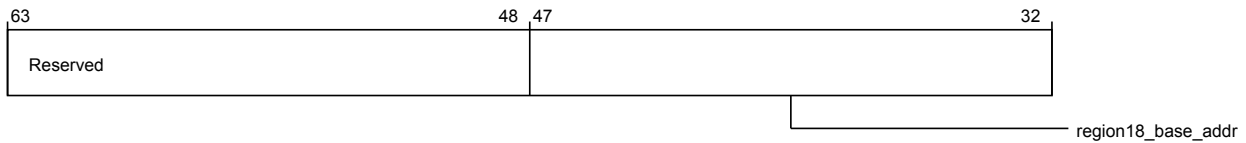


Figure 4-2062 por_mpu_por_mpu_m4_prbar18 (high)

The following table shows the por_mpu_m4_prbar18 higher register bit assignments.

Table 4-2079 por_mpu_por_mpu_m4_prbar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

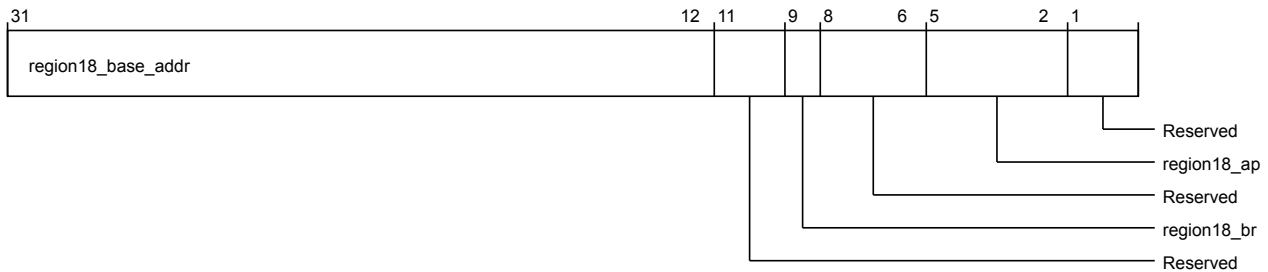


Figure 4-2063 por_mpu_por_mpu_m4_prbar18 (low)

The following table shows the por_mpu_m4_prbar18 lower register bit assignments.

Table 4-2080 por_mpu_por_mpu_m4_prbar18 (low)

Bits	Field name	Description	Type	Reset
31:12	region18_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region18_br	Region 18 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region18_ap	Region 18 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar18

MPU master 0 programmable limit address register 18.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2138

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

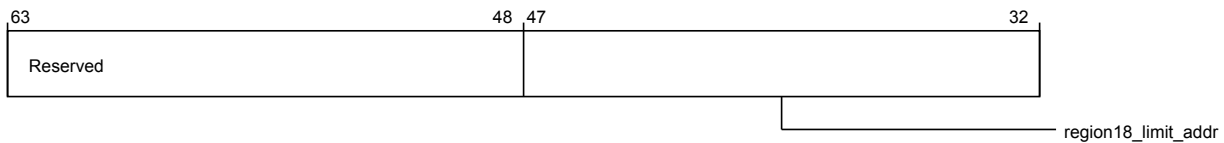


Figure 4-2064 `por_mpu_por_mpu_m4_prlar18` (high)

The following table shows the `por_mpu_m4_prlar18` higher register bit assignments.

Table 4-2081 `por_mpu_por_mpu_m4_prlar18` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region18_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

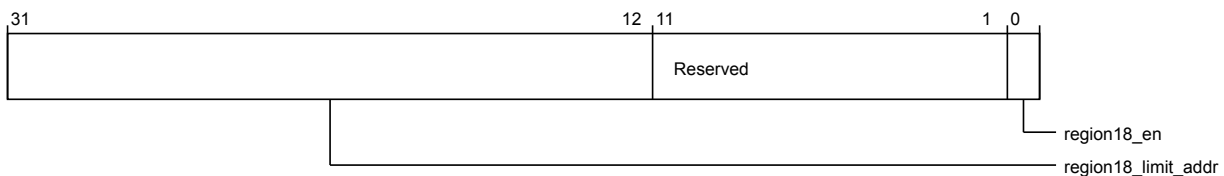


Figure 4-2065 `por_mpu_por_mpu_m4_prlar18` (low)

The following table shows the `por_mpu_m4_prlar18` lower register bit assignments.

Table 4-2082 `por_mpu_por_mpu_m4_prlar18` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region18_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region18_en</code>	Region 18 enable.	RW	1'b0

por_mpu_m4_prbar19

MPU master 0 programmable base address register 19.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2140
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

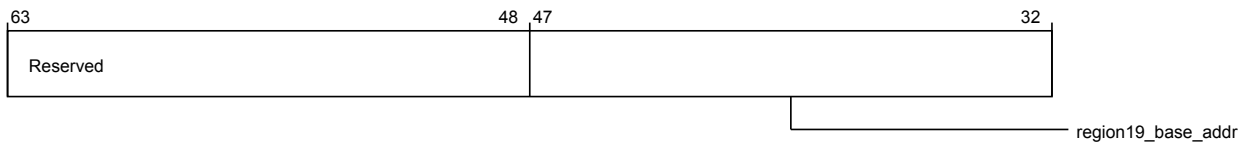


Figure 4-2066 por_mpu_por_mpu_m4_prbar19 (high)

The following table shows the por_mpu_m4_prbar19 higher register bit assignments.

Table 4-2083 por_mpu_por_mpu_m4_prbar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

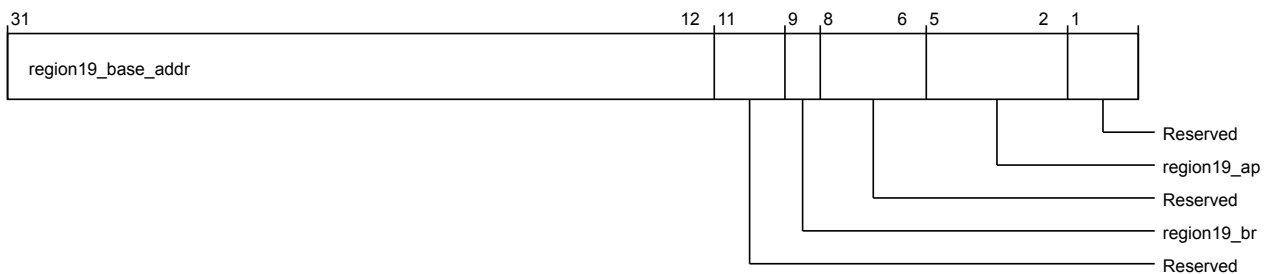


Figure 4-2067 por_mpu_por_mpu_m4_prbar19 (low)

The following table shows the por_mpu_m4_prbar19 lower register bit assignments.

Table 4-2084 por_mpu_por_mpu_m4_prbar19 (low)

Bits	Field name	Description	Type	Reset
31:12	region19_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2084 por_mpu_por_mpu_m4_prbar19 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region19_br	Region 19 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region19_ap	Region 19 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar19

MPU master 0 programmable limit address register 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2148

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

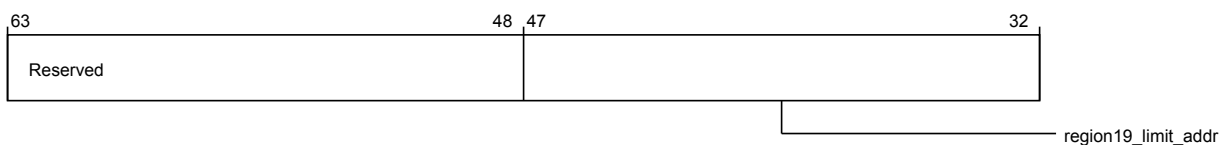


Figure 4-2068 por_mpu_por_mpu_m4_prlar19 (high)

The following table shows the por_mpu_m4_prlar19 higher register bit assignments.

Table 4-2085 por_mpu_por_mpu_m4_prlar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

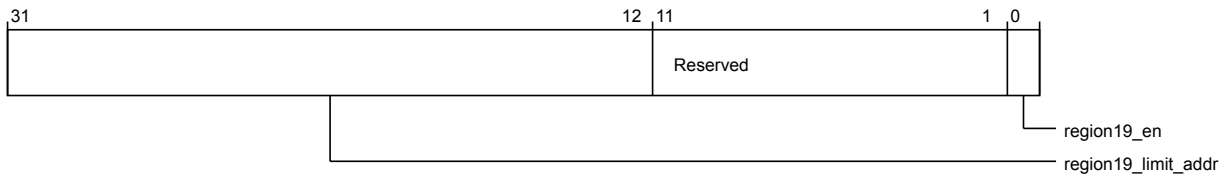


Figure 4-2069 `por_mpu_por_mpu_m4_prlar19` (low)

The following table shows the `por_mpu_m4_prlar19` lower register bit assignments.

Table 4-2086 `por_mpu_por_mpu_m4_prlar19` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region19_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region19_en</code>	Region 19 enable.	RW	1'b0

`por_mpu_m4_prbar20`

MPU master 0 programmable base address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2150

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

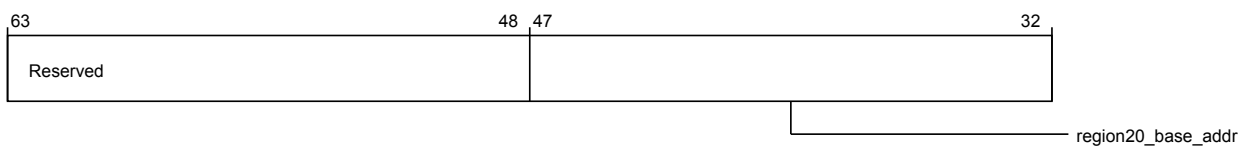


Figure 4-2070 `por_mpu_por_mpu_m4_prbar20` (high)

The following table shows the `por_mpu_m4_prbar20` higher register bit assignments.

Table 4-2087 `por_mpu_por_mpu_m4_prbar20` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region20_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

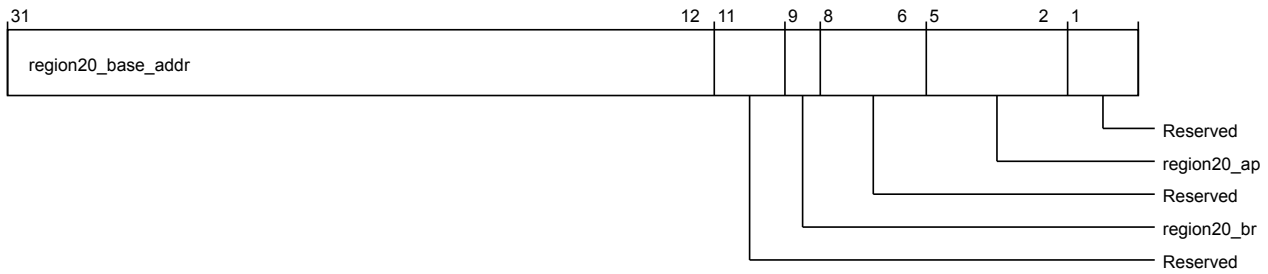


Figure 4-2071 `por_mpu_por_mpu_m4_prbar20` (low)

The following table shows the `por_mpu_m4_prbar20` lower register bit assignments.

Table 4-2088 `por_mpu_por_mpu_m4_prbar20` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region20_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region20_br</code>	Region 20 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region20_ap</code>	Region 20 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m4_prlar20`

MPU master 0 programmable limit address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2158

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

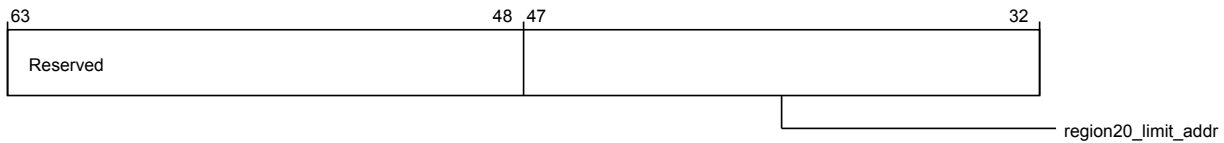


Figure 4-2072 por_mpu_m4_prlar20 (high)

The following table shows the por_mpu_m4_prlar20 higher register bit assignments.

Table 4-2089 por_mpu_m4_prlar20 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region20_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

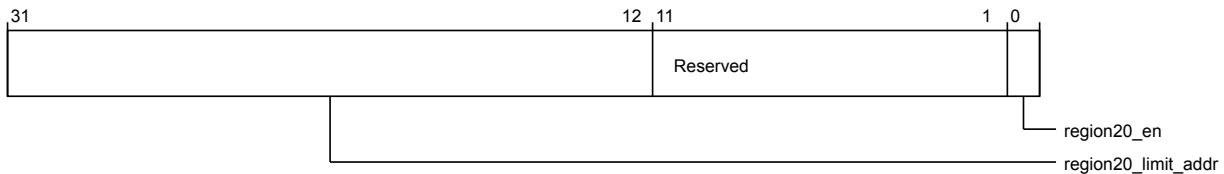


Figure 4-2073 por_mpu_m4_prlar20 (low)

The following table shows the por_mpu_m4_prlar20 lower register bit assignments.

Table 4-2090 por_mpu_m4_prlar20 (low)

Bits	Field name	Description	Type	Reset
31:12	region20_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region20_en	Region 20 enable.	RW	1'b0

por_mpu_m4_prbar21

MPU master 0 programmable base address register 21.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2160
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

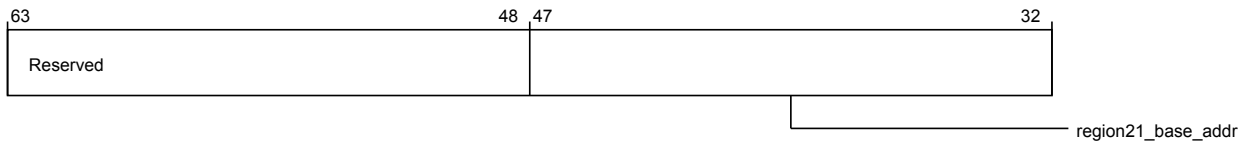


Figure 4-2074 `por_mpu_por_mpu_m4_prbar21` (high)

The following table shows the `por_mpu_m4_prbar21` higher register bit assignments.

Table 4-2091 `por_mpu_por_mpu_m4_prbar21` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

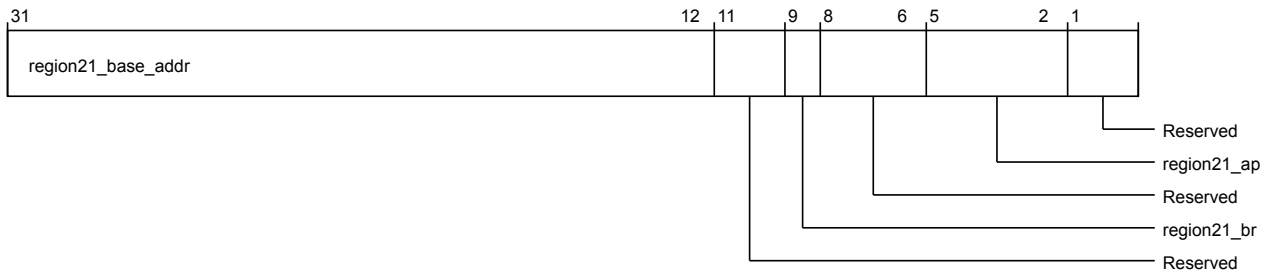


Figure 4-2075 `por_mpu_por_mpu_m4_prbar21` (low)

The following table shows the `por_mpu_m4_prbar21` lower register bit assignments.

Table 4-2092 `por_mpu_por_mpu_m4_prbar21` (low)

Bits	Field name	Description	Type	Reset
31:12	region21_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region21_br	Region 21 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region21_ap	Region 21 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar21

MPU master 0 programmable limit address register 21.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2168

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

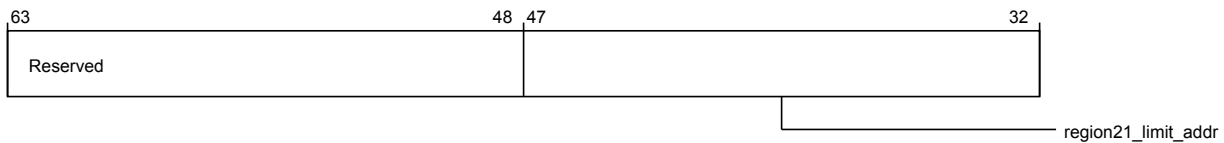


Figure 4-2076 por_mpu_por_mpu_m4_prlar21 (high)

The following table shows the `por_mpu_m4_prlar21` higher register bit assignments.

Table 4-2093 por_mpu_por_mpu_m4_prlar21 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

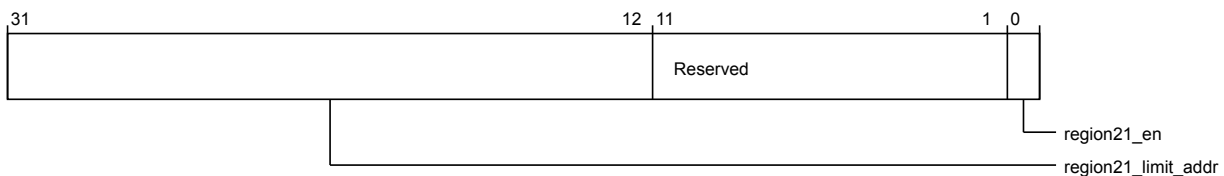


Figure 4-2077 por_mpu_por_mpu_m4_prlar21 (low)

The following table shows the `por_mpu_m4_prlar21` lower register bit assignments.

Table 4-2094 por_mpu_por_mpu_m4_prlar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region21_en	Region 21 enable.	RW	1'b0

por_mpu_m4_prbar22

MPU master 0 programmable base address register 22.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2170
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

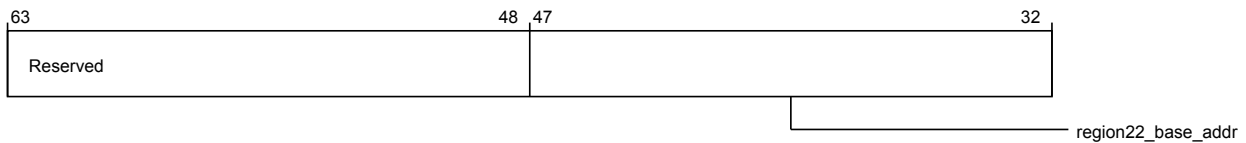


Figure 4-2078 por_mpu_por_mpu_m4_prbar22 (high)

The following table shows the por_mpu_m4_prbar22 higher register bit assignments.

Table 4-2095 por_mpu_por_mpu_m4_prbar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

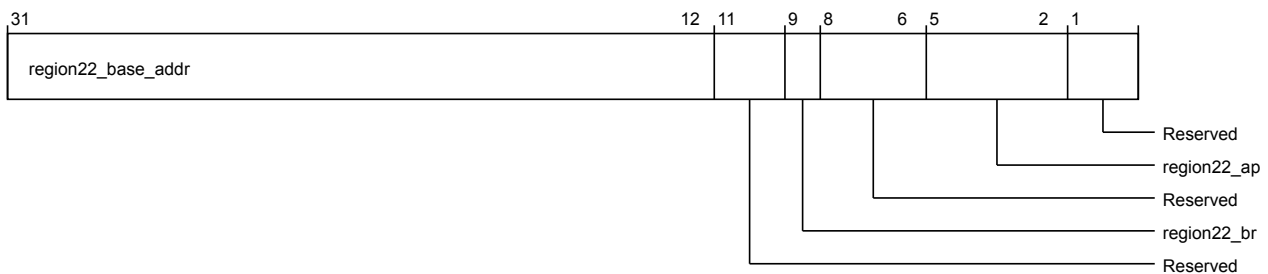


Figure 4-2079 por_mpu_por_mpu_m4_prbar22 (low)

The following table shows the por_mpu_m4_prbar22 lower register bit assignments.

Table 4-2096 por_mpu_por_mpu_m4_prbar22 (low)

Bits	Field name	Description	Type	Reset
31:12	region22_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2096 por_mpu_por_mpu_m4_prbar22 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region22_br	Region 22 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region22_ap	Region 22 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar22

MPU master 0 programmable limit address register 22.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2178

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

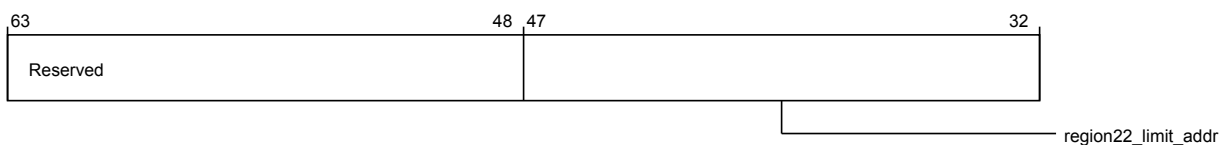


Figure 4-2080 por_mpu_por_mpu_m4_prlar22 (high)

The following table shows the por_mpu_m4_prlar22 higher register bit assignments.

Table 4-2097 por_mpu_por_mpu_m4_prlar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

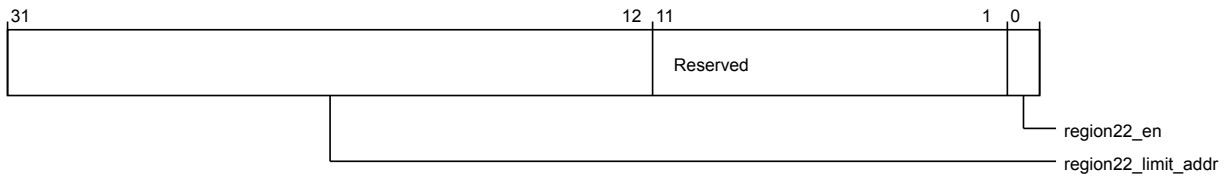


Figure 4-2081 `por_mpu_por_mpu_m4_prlar22` (low)

The following table shows the `por_mpu_m4_prlar22` lower register bit assignments.

Table 4-2098 `por_mpu_por_mpu_m4_prlar22` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region22_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region22_en</code>	Region 22 enable.	RW	1'b0

`por_mpu_m4_prbar23`

MPU master 0 programmable base address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2180

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

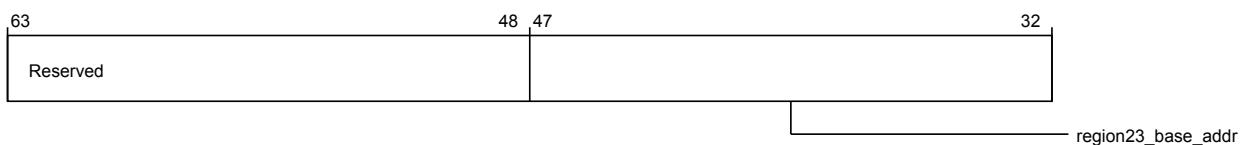


Figure 4-2082 `por_mpu_por_mpu_m4_prbar23` (high)

The following table shows the `por_mpu_m4_prbar23` higher register bit assignments.

Table 4-2099 `por_mpu_por_mpu_m4_prbar23` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region23_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

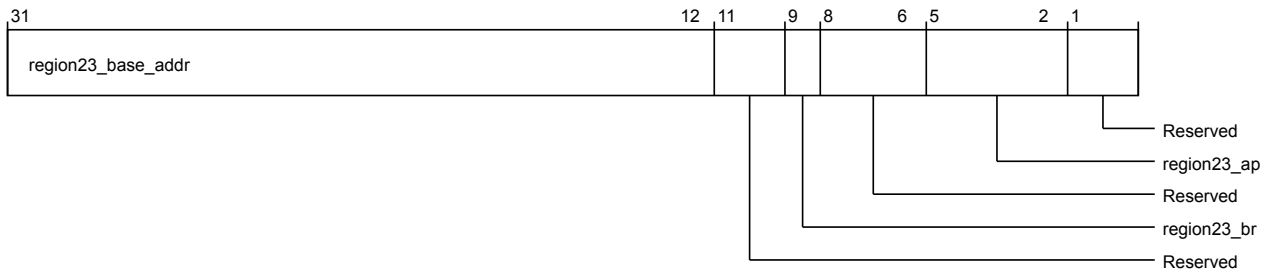


Figure 4-2083 por_mpu_por_mpu_m4_prbar23 (low)

The following table shows the por_mpu_m4_prbar23 lower register bit assignments.

Table 4-2100 por_mpu_por_mpu_m4_prbar23 (low)

Bits	Field name	Description	Type	Reset
31:12	region23_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region23_br	Region 23 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region23_ap	Region 23 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar23

MPU master 0 programmable limit address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2188

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

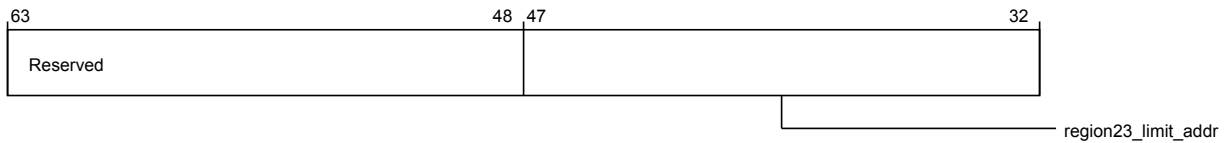


Figure 4-2084 `por_mpu_m4_prlar23` (high)

The following table shows the `por_mpu_m4_prlar23` higher register bit assignments.

Table 4-2101 `por_mpu_m4_prlar23` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region23_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

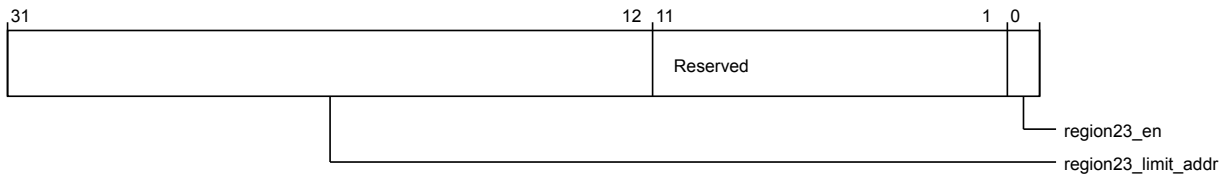


Figure 4-2085 `por_mpu_m4_prlar23` (low)

The following table shows the `por_mpu_m4_prlar23` lower register bit assignments.

Table 4-2102 `por_mpu_m4_prlar23` (low)

Bits	Field name	Description	Type	Reset
31:12	region23_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region23_en	Region 23 enable.	RW	1'b0

`por_mpu_m4_prbar24`

MPU master 0 programmable base address register 24.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2190
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

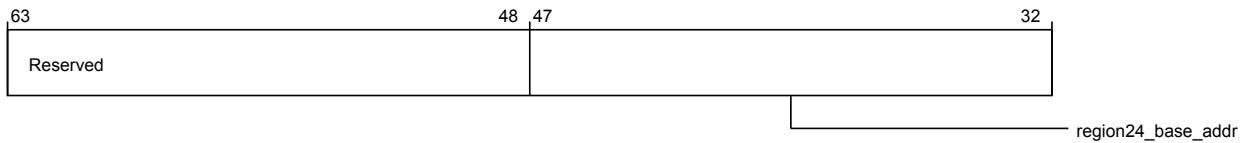


Figure 4-2086 por_mpu_por_mpu_m4_prbar24 (high)

The following table shows the por_mpu_m4_prbar24 higher register bit assignments.

Table 4-2103 por_mpu_por_mpu_m4_prbar24 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

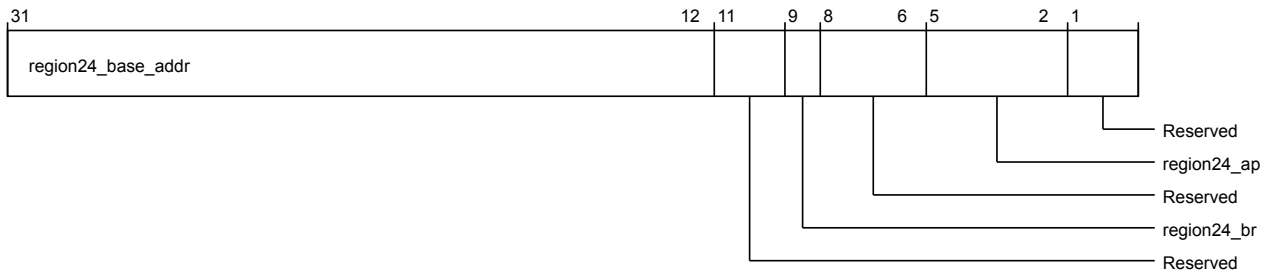


Figure 4-2087 por_mpu_por_mpu_m4_prbar24 (low)

The following table shows the por_mpu_m4_prbar24 lower register bit assignments.

Table 4-2104 por_mpu_por_mpu_m4_prbar24 (low)

Bits	Field name	Description	Type	Reset
31:12	region24_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region24_br	Region 24 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region24_ap	Region 24 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar24

MPU master 0 programmable limit address register 24.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2198

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

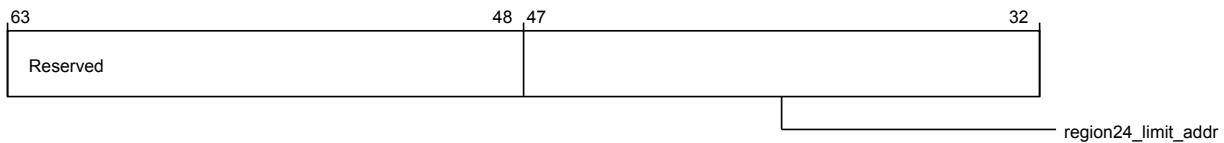


Figure 4-2088 `por_mpu_m4_prlar24` (high)

The following table shows the `por_mpu_m4_prlar24` higher register bit assignments.

Table 4-2105 `por_mpu_m4_prlar24` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region24_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

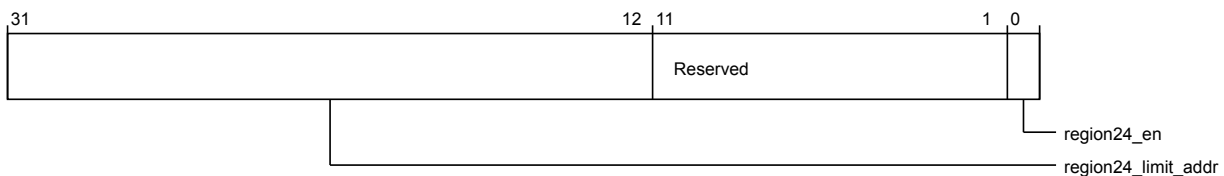


Figure 4-2089 `por_mpu_m4_prlar24` (low)

The following table shows the `por_mpu_m4_prlar24` lower register bit assignments.

Table 4-2106 `por_mpu_m4_prlar24` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region24_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region24_en</code>	Region 24 enable.	RW	1'b0

por_mpu_m4_prbar25

MPU master 0 programmable base address register 25.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

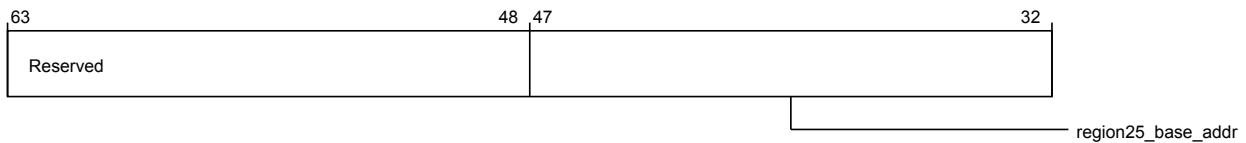


Figure 4-2090 por_mpu_por_mpu_m4_prbar25 (high)

The following table shows the por_mpu_m4_prbar25 higher register bit assignments.

Table 4-2107 por_mpu_por_mpu_m4_prbar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

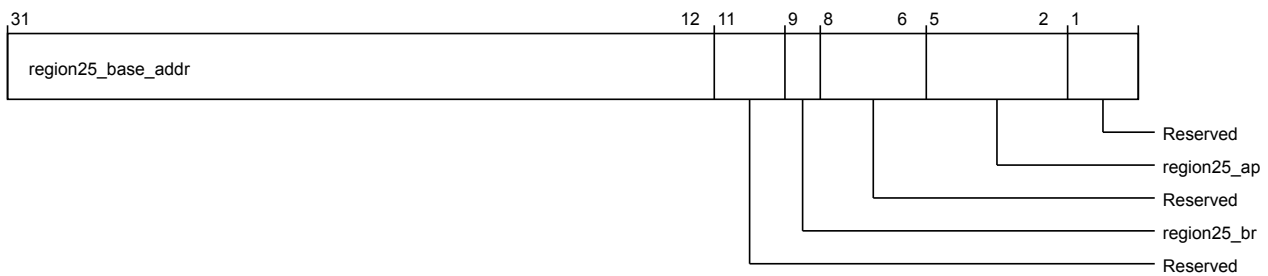


Figure 4-2091 por_mpu_por_mpu_m4_prbar25 (low)

The following table shows the por_mpu_m4_prbar25 lower register bit assignments.

Table 4-2108 por_mpu_por_mpu_m4_prbar25 (low)

Bits	Field name	Description	Type	Reset
31:12	region25_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2108 por_mpu_por_mpu_m4_prbar25 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region25_br	Region 25 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region25_ap	Region 25 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar25

MPU master 0 programmable limit address register 25.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h21A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

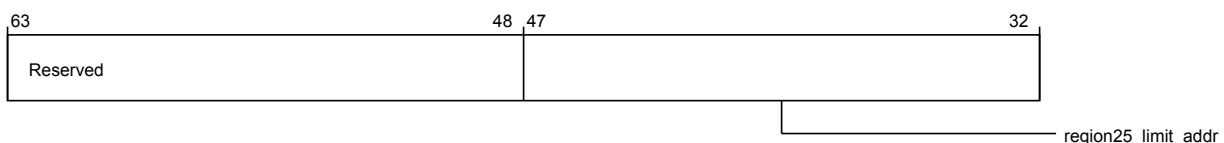


Figure 4-2092 por_mpu_por_mpu_m4_prlar25 (high)

The following table shows the por_mpu_m4_prlar25 higher register bit assignments.

Table 4-2109 por_mpu_por_mpu_m4_prlar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

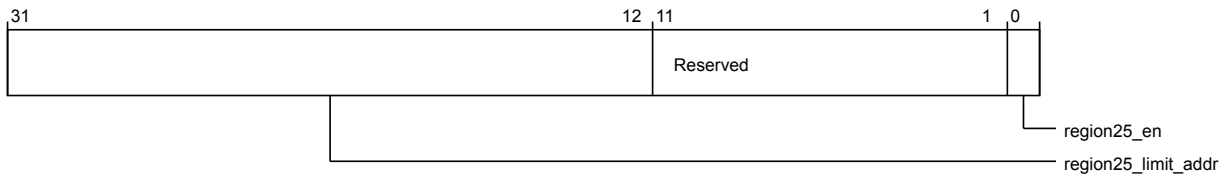


Figure 4-2093 `por_mpu_por_mpu_m4_prlar25` (low)

The following table shows the `por_mpu_m4_prlar25` lower register bit assignments.

Table 4-2110 `por_mpu_por_mpu_m4_prlar25` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region25_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region25_en</code>	Region 25 enable.	RW	1'b0

`por_mpu_m4_prbar26`

MPU master 0 programmable base address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h21B0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

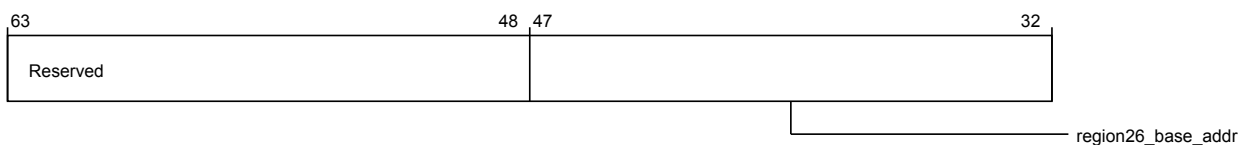


Figure 4-2094 `por_mpu_por_mpu_m4_prbar26` (high)

The following table shows the `por_mpu_m4_prbar26` higher register bit assignments.

Table 4-2111 `por_mpu_por_mpu_m4_prbar26` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region26_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

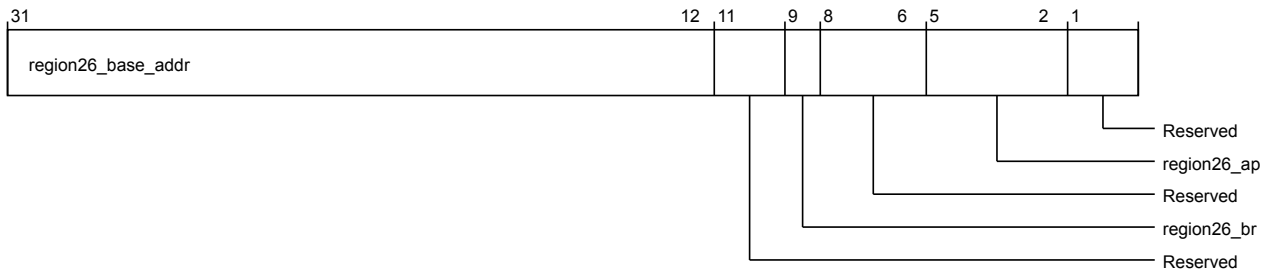


Figure 4-2095 `por_mpu_por_mpu_m4_prbar26` (low)

The following table shows the `por_mpu_m4_prbar26` lower register bit assignments.

Table 4-2112 `por_mpu_por_mpu_m4_prbar26` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region26_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region26_br</code>	Region 26 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region26_ap</code>	Region 26 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m4_prlar26`

MPU master 0 programmable limit address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h21B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

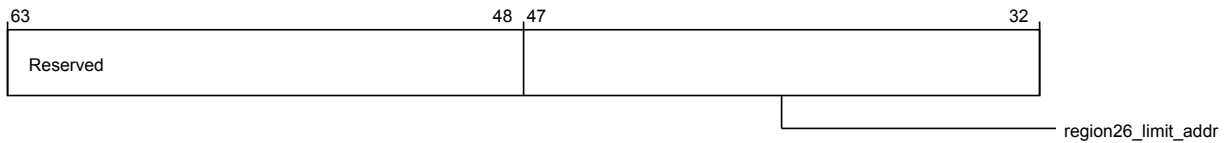


Figure 4-2096 `por_mpu_m4_prlar26` (high)

The following table shows the `por_mpu_m4_prlar26` higher register bit assignments.

Table 4-2113 `por_mpu_m4_prlar26` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region26_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

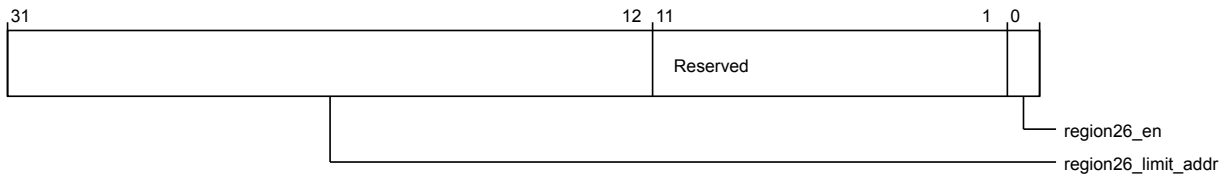


Figure 4-2097 `por_mpu_m4_prlar26` (low)

The following table shows the `por_mpu_m4_prlar26` lower register bit assignments.

Table 4-2114 `por_mpu_m4_prlar26` (low)

Bits	Field name	Description	Type	Reset
31:12	region26_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region26_en	Region 26 enable.	RW	1'b0

`por_mpu_m4_prbar27`

MPU master 0 programmable base address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21C0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

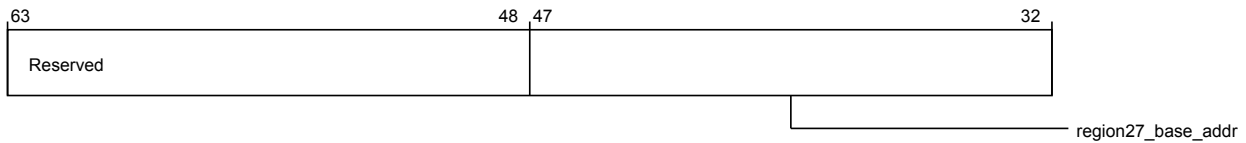


Figure 4-2098 por_mpu_por_mpu_m4_prbar27 (high)

The following table shows the por_mpu_m4_prbar27 higher register bit assignments.

Table 4-2115 por_mpu_por_mpu_m4_prbar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

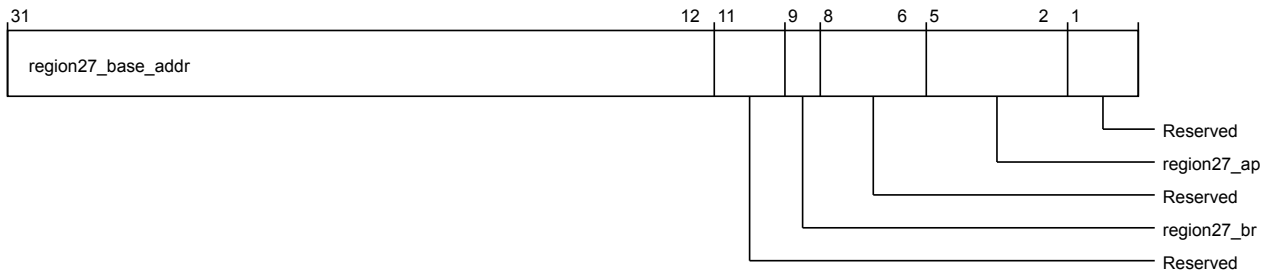


Figure 4-2099 por_mpu_por_mpu_m4_prbar27 (low)

The following table shows the por_mpu_m4_prbar27 lower register bit assignments.

Table 4-2116 por_mpu_por_mpu_m4_prbar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region27_br	Region 27 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region27_ap	Region 27 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar27

MPU master 0 programmable limit address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21C8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

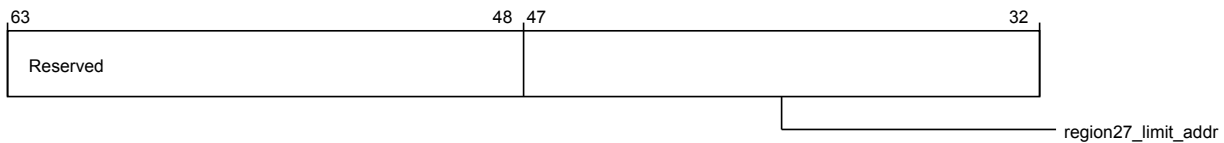


Figure 4-2100 por_mpu_por_mpu_m4_prlar27 (high)

The following table shows the `por_mpu_m4_prlar27` higher register bit assignments.

Table 4-2117 por_mpu_por_mpu_m4_prlar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

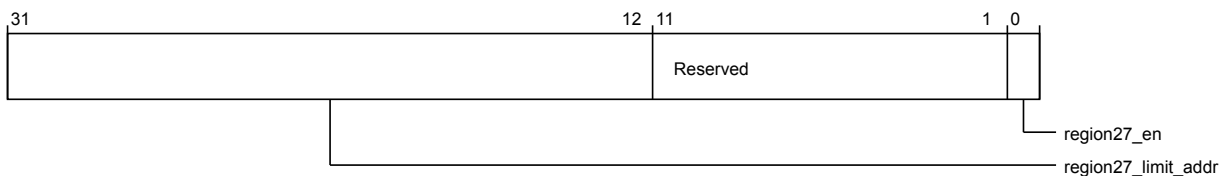


Figure 4-2101 por_mpu_por_mpu_m4_prlar27 (low)

The following table shows the `por_mpu_m4_prlar27` lower register bit assignments.

Table 4-2118 por_mpu_por_mpu_m4_prlar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region27_en	Region 27 enable.	RW	1'b0

por_mpu_m4_prbar28

MPU master 0 programmable base address register 28.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h21D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

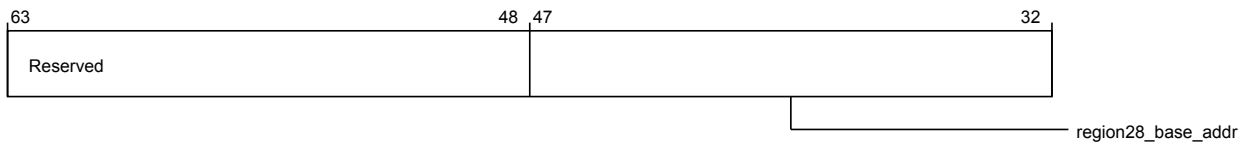


Figure 4-2102 por_mpu_por_mpu_m4_prbar28 (high)

The following table shows the por_mpu_m4_prbar28 higher register bit assignments.

Table 4-2119 por_mpu_por_mpu_m4_prbar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

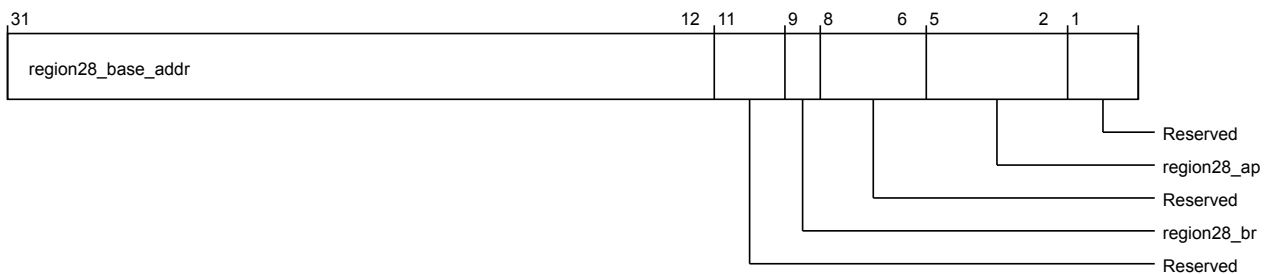


Figure 4-2103 por_mpu_por_mpu_m4_prbar28 (low)

The following table shows the por_mpu_m4_prbar28 lower register bit assignments.

Table 4-2120 por_mpu_por_mpu_m4_prbar28 (low)

Bits	Field name	Description	Type	Reset
31:12	region28_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2120 `por_mpu_por_mpu_m4_prbar28` (low) (continued)

Bits	Field name	Description	Type	Reset
9	region28_br	Region 28 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region28_ap	Region 28 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m4_prlar28`

MPU master 0 programmable limit address register 28.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h21D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

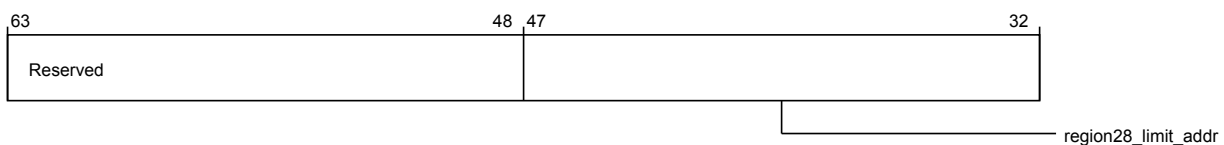


Figure 4-2104 `por_mpu_por_mpu_m4_prlar28` (high)

The following table shows the `por_mpu_m4_prlar28` higher register bit assignments.

Table 4-2121 `por_mpu_por_mpu_m4_prlar28` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

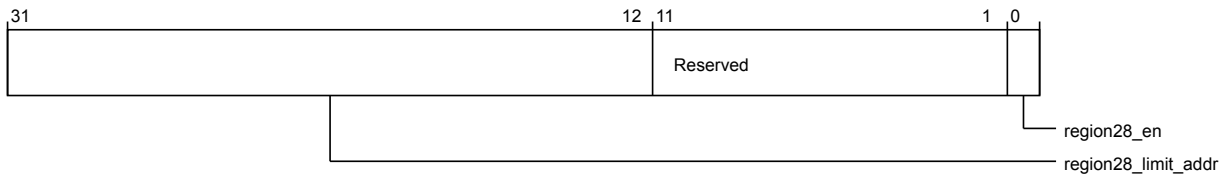


Figure 4-2105 `por_mpu_por_mpu_m4_prlar28` (low)

The following table shows the `por_mpu_m4_prlar28` lower register bit assignments.

Table 4-2122 `por_mpu_por_mpu_m4_prlar28` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region28_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region28_en</code>	Region 28 enable.	RW	1'b0

`por_mpu_m4_prbar29`

MPU master 0 programmable base address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h21E0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

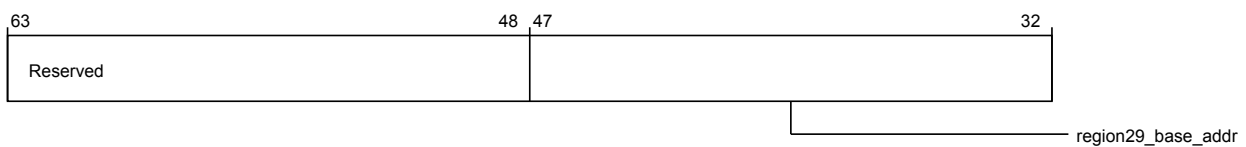


Figure 4-2106 `por_mpu_por_mpu_m4_prbar29` (high)

The following table shows the `por_mpu_m4_prbar29` higher register bit assignments.

Table 4-2123 `por_mpu_por_mpu_m4_prbar29` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region29_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

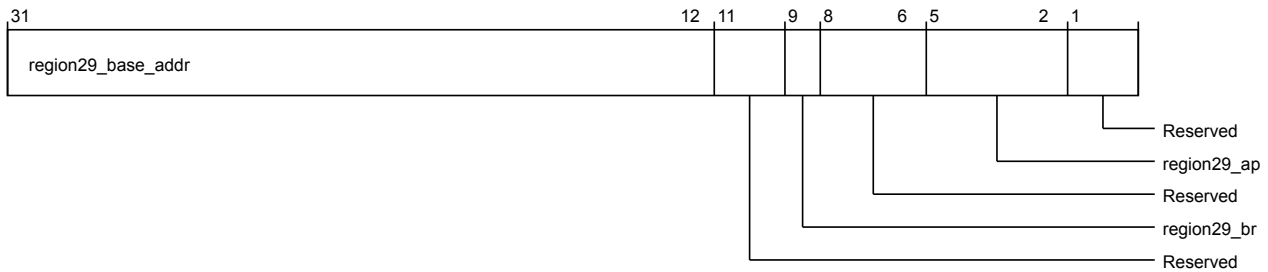


Figure 4-2107 por_mpu_por_mpu_m4_prbar29 (low)

The following table shows the por_mpu_m4_prbar29 lower register bit assignments.

Table 4-2124 por_mpu_por_mpu_m4_prbar29 (low)

Bits	Field name	Description	Type	Reset
31:12	region29_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region29_br	Region 29 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region29_ap	Region 29 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar29

MPU master 0 programmable limit address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h21E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

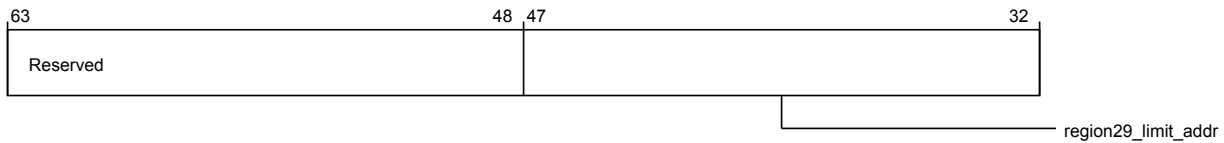


Figure 4-2108 por_mpu_m4_prlar29 (high)

The following table shows the por_mpu_m4_prlar29 higher register bit assignments.

Table 4-2125 por_mpu_m4_prlar29 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region29_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

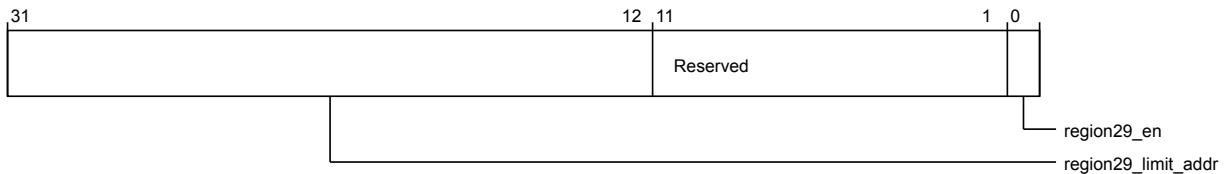


Figure 4-2109 por_mpu_m4_prlar29 (low)

The following table shows the por_mpu_m4_prlar29 lower register bit assignments.

Table 4-2126 por_mpu_m4_prlar29 (low)

Bits	Field name	Description	Type	Reset
31:12	region29_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region29_en	Region 29 enable.	RW	1'b0

por_mpu_m4_prbar30

MPU master 0 programmable base address register 30.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h21F0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

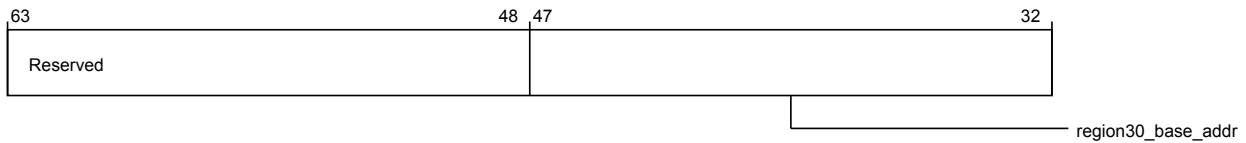


Figure 4-2110 por_mpu_por_mpu_m4_prbar30 (high)

The following table shows the por_mpu_m4_prbar30 higher register bit assignments.

Table 4-2127 por_mpu_por_mpu_m4_prbar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

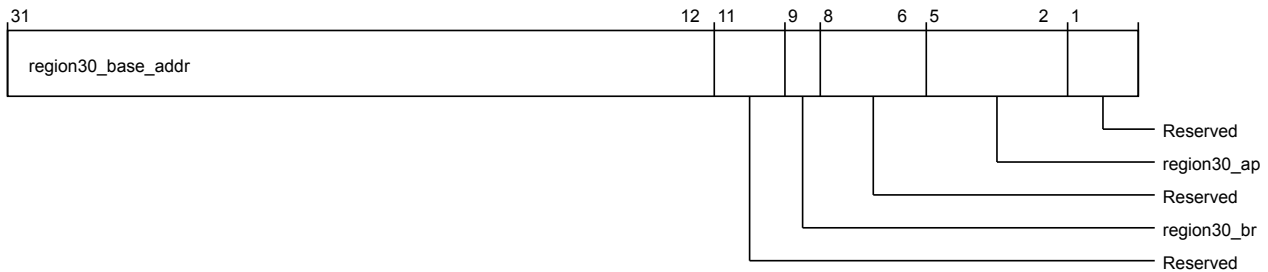


Figure 4-2111 por_mpu_por_mpu_m4_prbar30 (low)

The following table shows the por_mpu_m4_prbar30 lower register bit assignments.

Table 4-2128 por_mpu_por_mpu_m4_prbar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region30_br	Region 30 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region30_ap	Region 30 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar30

MPU master 0 programmable limit address register 30.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h21F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

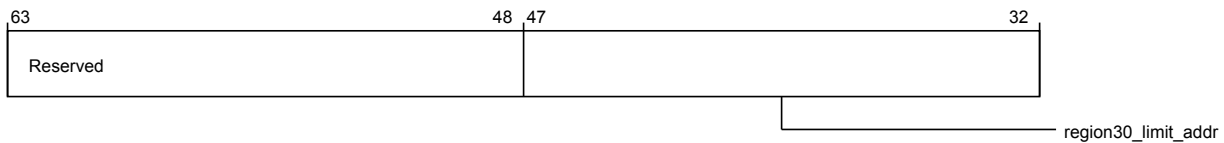


Figure 4-2112 por_mpu_por_mpu_m4_prlar30 (high)

The following table shows the por_mpu_m4_prlar30 higher register bit assignments.

Table 4-2129 por_mpu_por_mpu_m4_prlar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

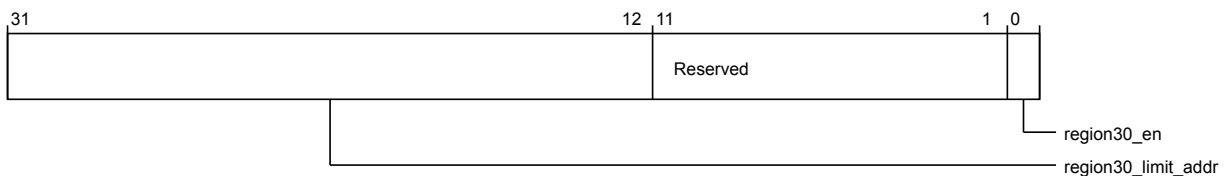


Figure 4-2113 por_mpu_por_mpu_m4_prlar30 (low)

The following table shows the por_mpu_m4_prlar30 lower register bit assignments.

Table 4-2130 por_mpu_por_mpu_m4_prlar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region30_en	Region 30 enable.	RW	1'b0

por_mpu_m4_prbar31

MPU master 0 programmable base address register 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2200
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

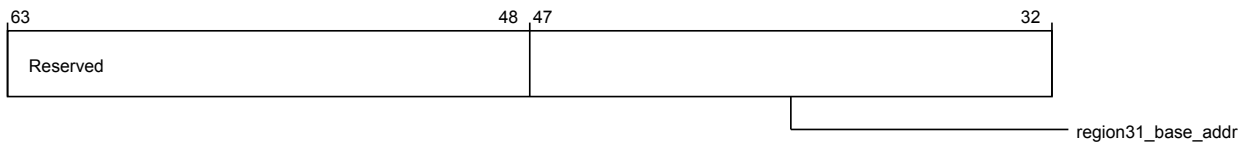


Figure 4-2114 por_mpu_por_mpu_m4_prbar31 (high)

The following table shows the por_mpu_m4_prbar31 higher register bit assignments.

Table 4-2131 por_mpu_por_mpu_m4_prbar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

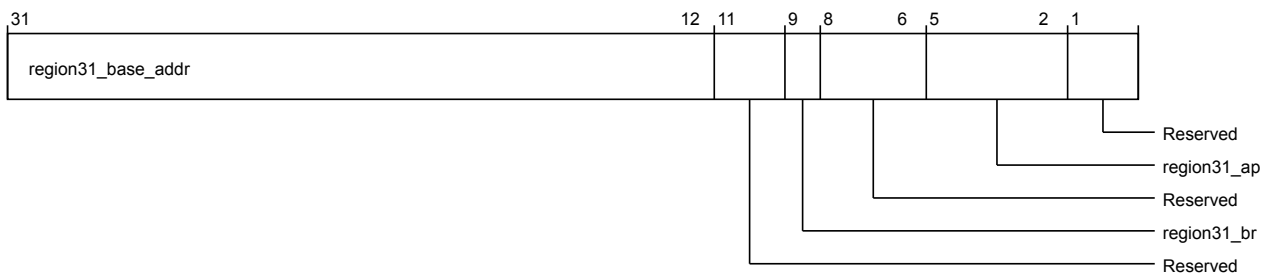


Figure 4-2115 por_mpu_por_mpu_m4_prbar31 (low)

The following table shows the por_mpu_m4_prbar31 lower register bit assignments.

Table 4-2132 por_mpu_por_mpu_m4_prbar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2132 por_mpu_por_mpu_m4_prbar31 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region31_br	Region 31 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region31_ap	Region 31 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m4_prlar31

MPU master 0 programmable limit address register 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2208

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

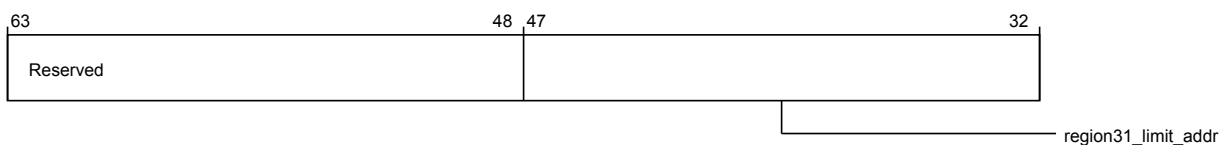


Figure 4-2116 por_mpu_por_mpu_m4_prlar31 (high)

The following table shows the por_mpu_m4_prlar31 higher register bit assignments.

Table 4-2133 por_mpu_por_mpu_m4_prlar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

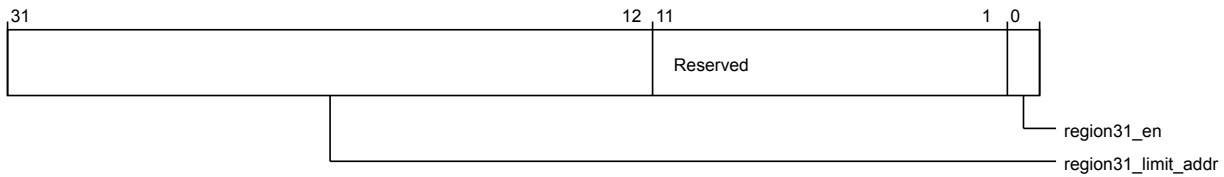


Figure 4-2117 `por_mpu_por_mpu_m4_prlar31` (low)

The following table shows the `por_mpu_m4_prlar31` lower register bit assignments.

Table 4-2134 `por_mpu_por_mpu_m4_prlar31` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region31_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region31_en</code>	Region 31 enable.	RW	1'b0

`por_mpu_m5_ctl`

Functions as the MPU Master 5 control register.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2400

Register reset 64'b010

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

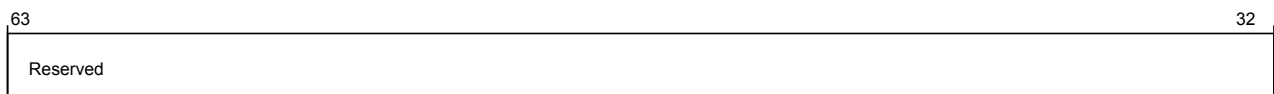


Figure 4-2118 `por_mpu_por_mpu_m5_ctl` (high)

The following table shows the `por_mpu_m5_ctl` higher register bit assignments.

Table 4-2135 `por_mpu_por_mpu_m5_ctl` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

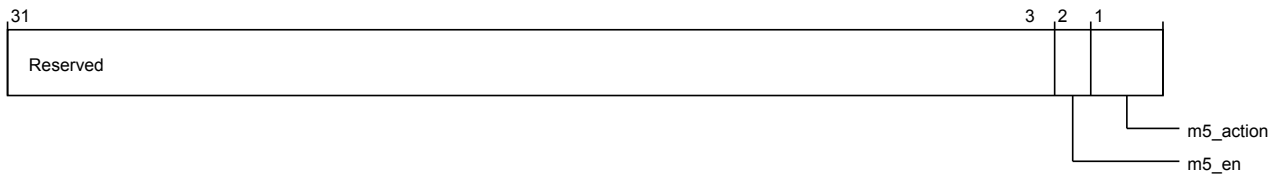


Figure 4-2119 por_mpu_por_mpu_m5_ctl (low)

The following table shows the por_mpu_m5_ctl lower register bit assignments.

Table 4-2136 por_mpu_por_mpu_m5_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	m5_en	MPU master 5 enable.	RW	1'b0
1:0	m5_action	Indicates action HN* should take if no access permission is granted 2'b00: FUSA interrupt 2'b01: Bus error to the originating bus master 2'b10: Both FUSA interrupt and bus error.	RW	2'b10

por_mpu_m5_prbar0

MPU master 0 programmable base address register 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2410

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

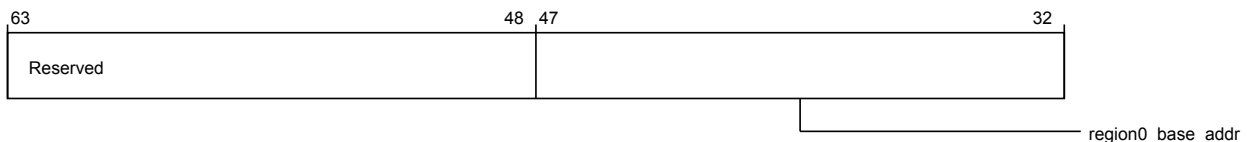


Figure 4-2120 por_mpu_por_mpu_m5_prbar0 (high)

The following table shows the por_mpu_m5_prbar0 higher register bit assignments.

Table 4-2137 por_mpu_por_mpu_m5_prbar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

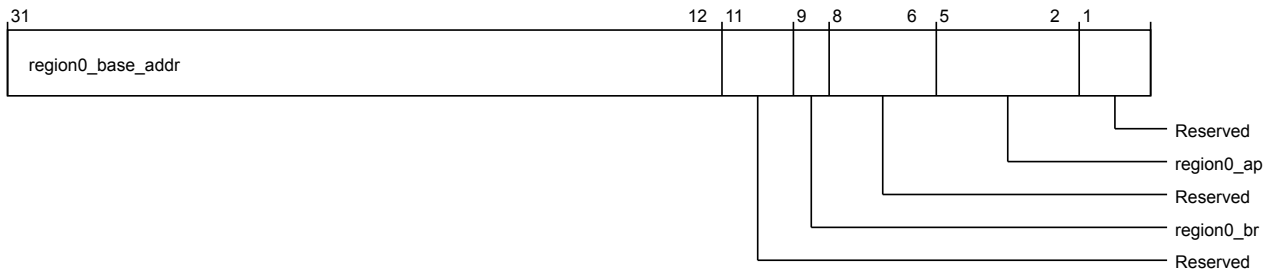


Figure 4-2121 por_mpu_por_mpu_m5_prbar0 (low)

The following table shows the por_mpu_m5_prbar0 lower register bit assignments.

Table 4-2138 por_mpu_por_mpu_m5_prbar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region0_br	Region 0 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region0_ap	Region 0 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar0

MPU master 0 programmable limit address register 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2418
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

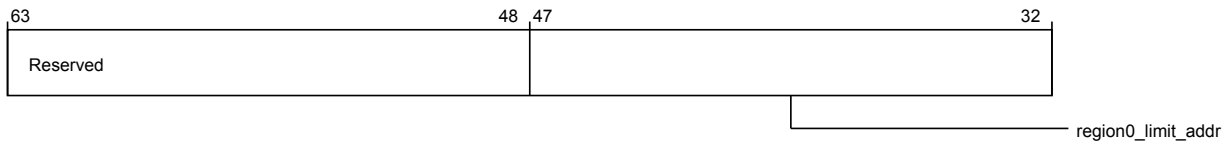


Figure 4-2122 por_mpu_m5_prlar0 (high)

The following table shows the por_mpu_m5_prlar0 higher register bit assignments.

Table 4-2139 por_mpu_m5_prlar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

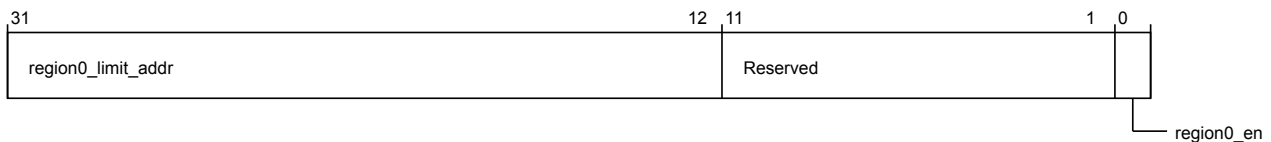


Figure 4-2123 por_mpu_m5_prlar0 (low)

The following table shows the por_mpu_m5_prlar0 lower register bit assignments.

Table 4-2140 por_mpu_m5_prlar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region0_en	Region 0 enable.	RW	1'b0

por_mpu_m5_prbar1

MPU master 0 programmable base address register 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2420
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

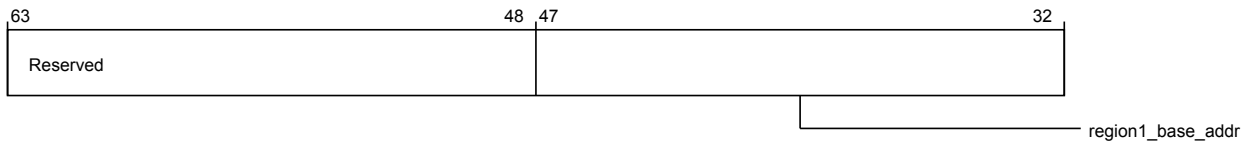


Figure 4-2124 por_mpu_por_mpu_m5_prbar1 (high)

The following table shows the por_mpu_m5_prbar1 higher register bit assignments.

Table 4-2141 por_mpu_por_mpu_m5_prbar1 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region1_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

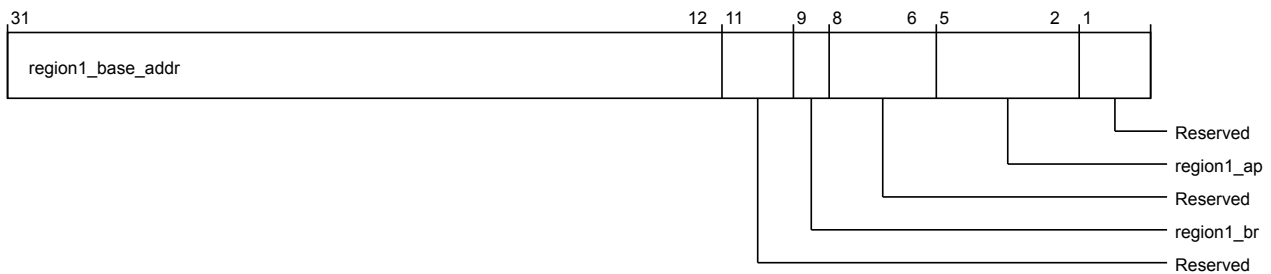


Figure 4-2125 por_mpu_por_mpu_m5_prbar1 (low)

The following table shows the por_mpu_m5_prbar1 lower register bit assignments.

Table 4-2142 por_mpu_por_mpu_m5_prbar1 (low)

Bits	Field name	Description	Type	Reset
31:12	region1_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region1_br	Region 1 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-

Table 4-2142 por_mpu_por_mpu_m5_prbar1 (low) (continued)

Bits	Field name	Description	Type	Reset
5:2	region1_ap	Region 1 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar1

MPU master 0 programmable limit address register 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2428

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

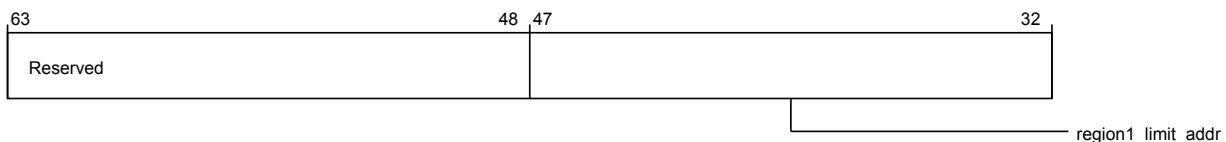


Figure 4-2126 por_mpu_por_mpu_m5_prlar1 (high)

The following table shows the por_mpu_m5_prlar1 higher register bit assignments.

Table 4-2143 por_mpu_por_mpu_m5_prlar1 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region1_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

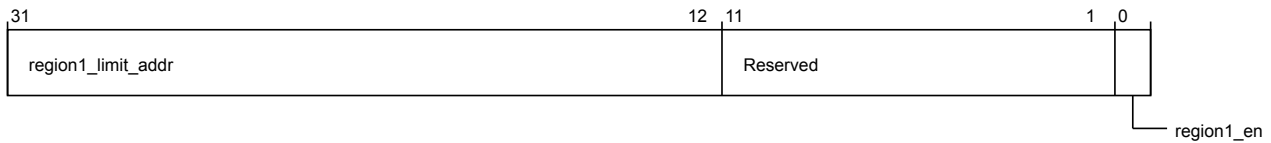


Figure 4-2127 `por_mpu_por_mpu_m5_prlar1` (low)

The following table shows the `por_mpu_m5_prlar1` lower register bit assignments.

Table 4-2144 `por_mpu_por_mpu_m5_prlar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region1_en</code>	Region 1 enable.	RW	1'b0

`por_mpu_m5_prbar2`

MPU master 0 programmable base address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2430

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

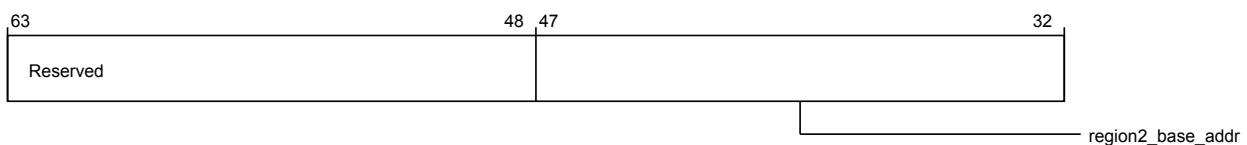


Figure 4-2128 `por_mpu_por_mpu_m5_prbar2` (high)

The following table shows the `por_mpu_m5_prbar2` higher register bit assignments.

Table 4-2145 `por_mpu_por_mpu_m5_prbar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

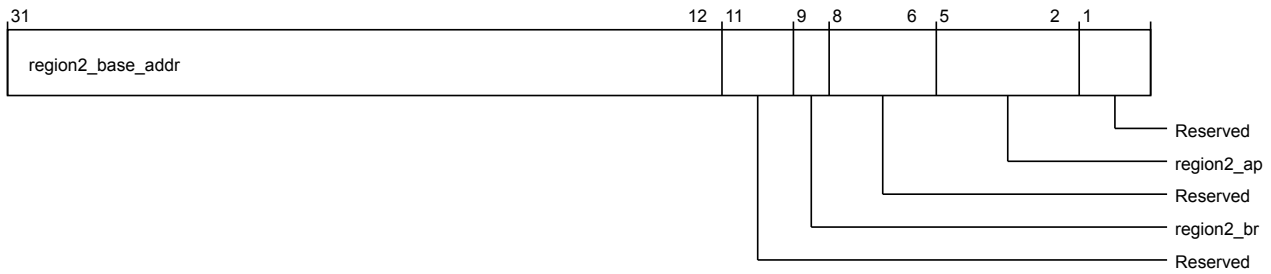


Figure 4-2129 por_mpu_por_mpu_m5_prbar2 (low)

The following table shows the por_mpu_m5_prbar2 lower register bit assignments.

Table 4-2146 por_mpu_por_mpu_m5_prbar2 (low)

Bits	Field name	Description	Type	Reset
31:12	region2_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region2_br	Region 2 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region2_ap	Region 2 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar2

MPU master 0 programmable limit address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2438

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

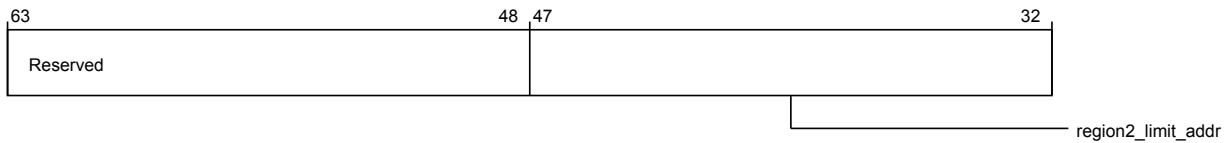


Figure 4-2130 `por_mpu_m5_prlar2` (high)

The following table shows the `por_mpu_m5_prlar2` higher register bit assignments.

Table 4-2147 `por_mpu_m5_prlar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

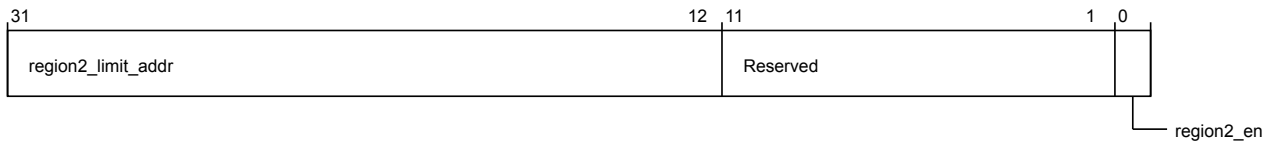


Figure 4-2131 `por_mpu_m5_prlar2` (low)

The following table shows the `por_mpu_m5_prlar2` lower register bit assignments.

Table 4-2148 `por_mpu_m5_prlar2` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region2_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region2_en</code>	Region 2 enable.	RW	1'b0

`por_mpu_m5_prbar3`

MPU master 0 programmable base address register 3.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2440
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

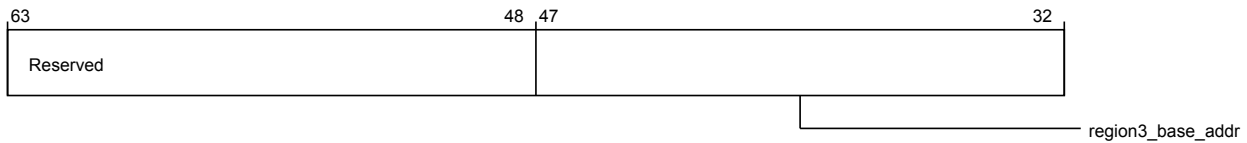


Figure 4-2132 `por_mpu_m5_prbar3` (high)

The following table shows the `por_mpu_m5_prbar3` higher register bit assignments.

Table 4-2149 `por_mpu_m5_prbar3` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

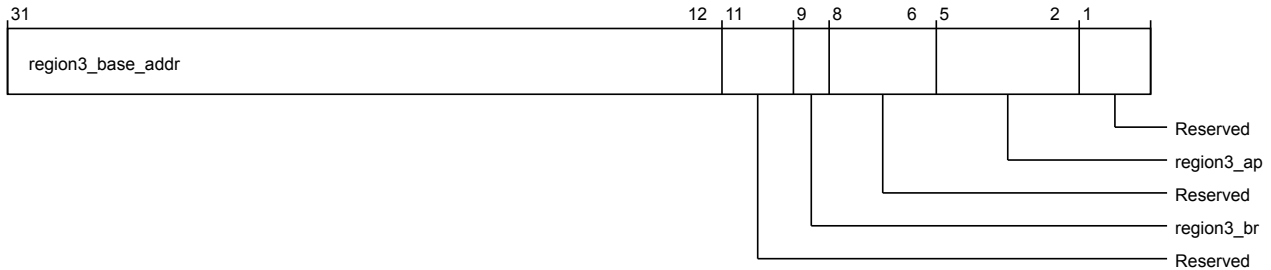


Figure 4-2133 `por_mpu_m5_prbar3` (low)

The following table shows the `por_mpu_m5_prbar3` lower register bit assignments.

Table 4-2150 `por_mpu_m5_prbar3` (low)

Bits	Field name	Description	Type	Reset
31:12	region3_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region3_br	Region 3 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region3_ap	Region 3 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar3

MPU master 0 programmable limit address register 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2448

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

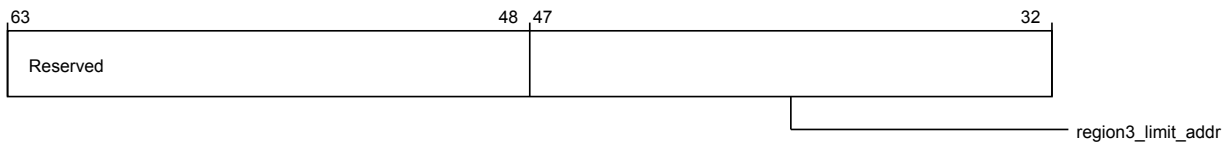


Figure 4-2134 por_mpu_por_mpu_m5_prlar3 (high)

The following table shows the por_mpu_m5_prlar3 higher register bit assignments.

Table 4-2151 por_mpu_por_mpu_m5_prlar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

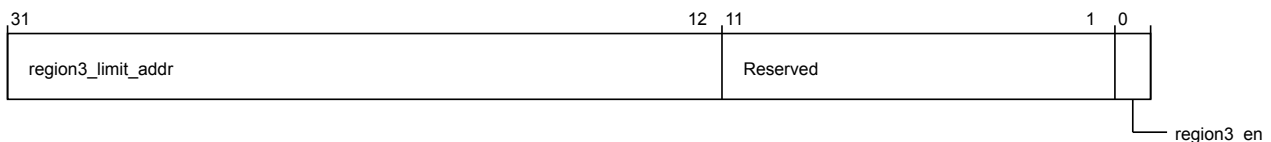


Figure 4-2135 por_mpu_por_mpu_m5_prlar3 (low)

The following table shows the por_mpu_m5_prlar3 lower register bit assignments.

Table 4-2152 por_mpu_por_mpu_m5_prlar3 (low)

Bits	Field name	Description	Type	Reset
31:12	region3_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region3_en	Region 3 enable.	RW	1'b0

por_mpu_m5_prbar4

MPU master 0 programmable base address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2450

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

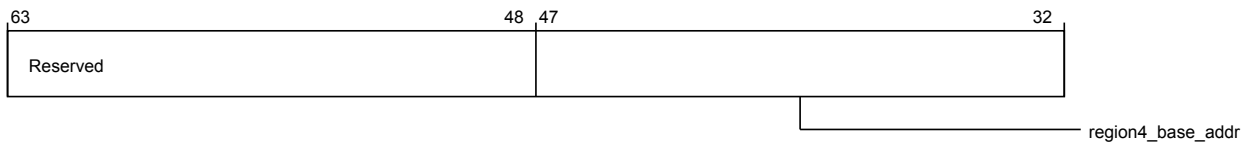


Figure 4-2136 por_mpu_por_mpu_m5_prbar4 (high)

The following table shows the por_mpu_m5_prbar4 higher register bit assignments.

Table 4-2153 por_mpu_por_mpu_m5_prbar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

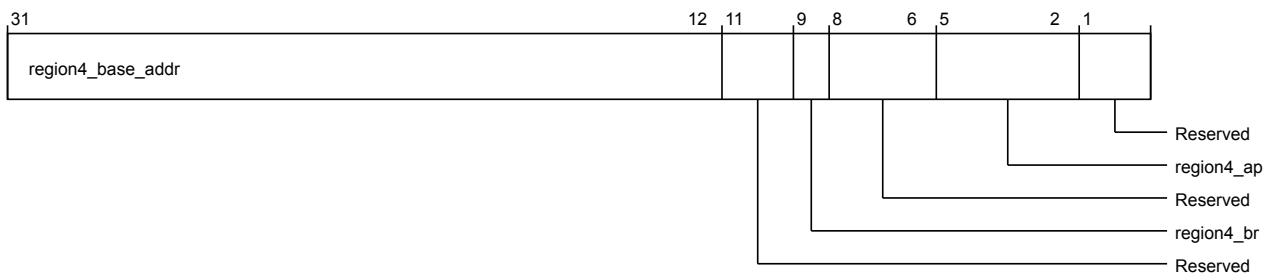


Figure 4-2137 por_mpu_por_mpu_m5_prbar4 (low)

The following table shows the por_mpu_m5_prbar4 lower register bit assignments.

Table 4-2154 por_mpu_por_mpu_m5_prbar4 (low)

Bits	Field name	Description	Type	Reset
31:12	region4_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2154 por_mpu_por_mpu_m5_prbar4 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region4_br	Region 4 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region4_ap	Region 4 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar4

MPU master 0 programmable limit address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2458

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

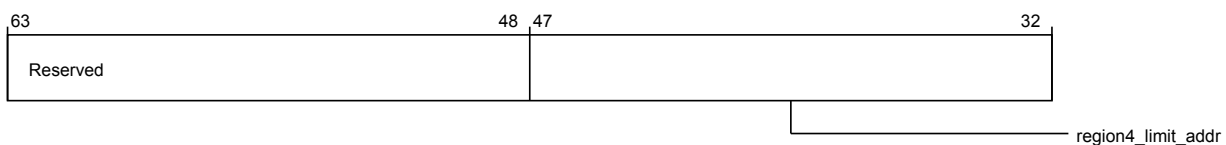


Figure 4-2138 por_mpu_por_mpu_m5_prlar4 (high)

The following table shows the por_mpu_m5_prlar4 higher register bit assignments.

Table 4-2155 por_mpu_por_mpu_m5_prlar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

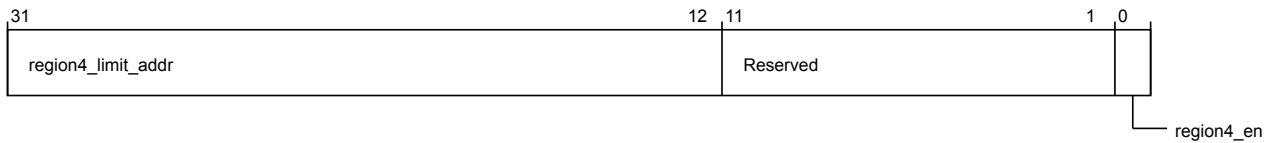


Figure 4-2139 `por_mpu_por_mpu_m5_prlar4` (low)

The following table shows the `por_mpu_m5_prlar4` lower register bit assignments.

Table 4-2156 `por_mpu_por_mpu_m5_prlar4` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region4_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region4_en</code>	Region 4 enable.	RW	1'b0

`por_mpu_m5_prbar5`

MPU master 0 programmable base address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2460

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

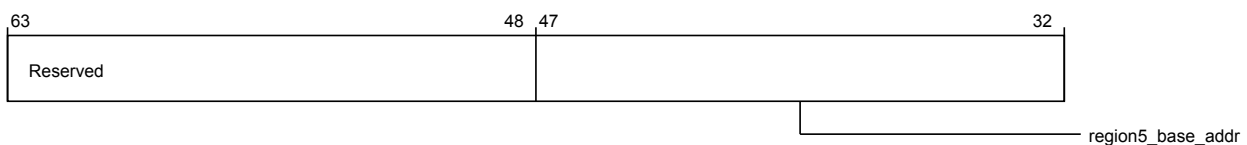


Figure 4-2140 `por_mpu_por_mpu_m5_prbar5` (high)

The following table shows the `por_mpu_m5_prbar5` higher register bit assignments.

Table 4-2157 `por_mpu_por_mpu_m5_prbar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

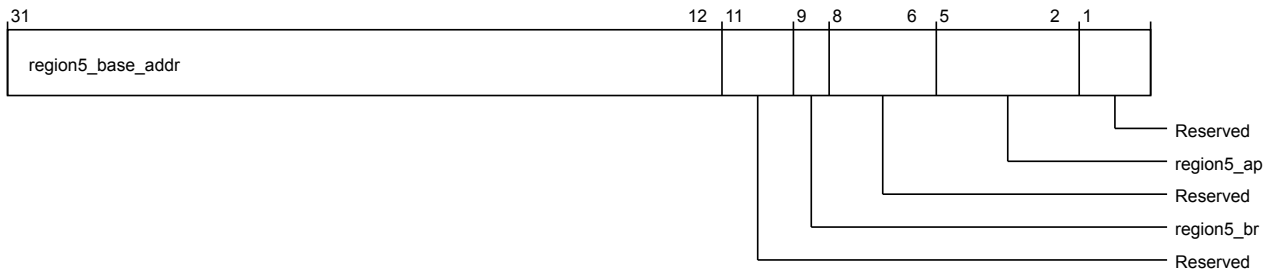


Figure 4-2141 por_mpu_por_mpu_m5_prbar5 (low)

The following table shows the por_mpu_m5_prbar5 lower register bit assignments.

Table 4-2158 por_mpu_por_mpu_m5_prbar5 (low)

Bits	Field name	Description	Type	Reset
31:12	region5_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region5_br	Region 5 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region5_ap	Region 5 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar5

MPU master 0 programmable limit address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2468

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

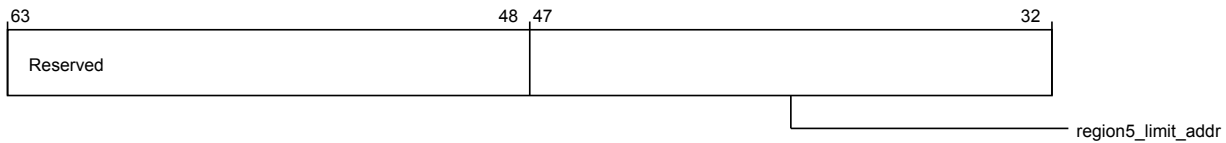


Figure 4-2142 `por_mpu_m5_prlar5` (high)

The following table shows the `por_mpu_m5_prlar5` higher register bit assignments.

Table 4-2159 `por_mpu_m5_prlar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

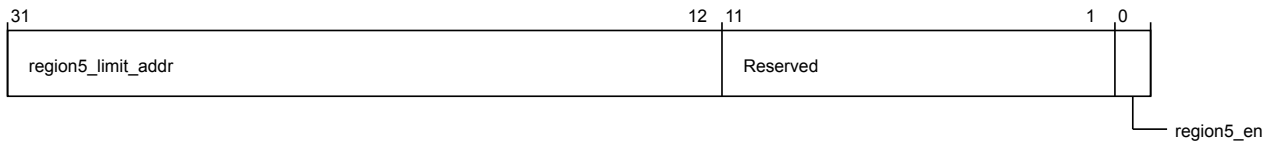


Figure 4-2143 `por_mpu_m5_prlar5` (low)

The following table shows the `por_mpu_m5_prlar5` lower register bit assignments.

Table 4-2160 `por_mpu_m5_prlar5` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region5_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region5_en</code>	Region 5 enable.	RW	1'b0

`por_mpu_m5_prbar6`

MPU master 0 programmable base address register 6.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2470
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

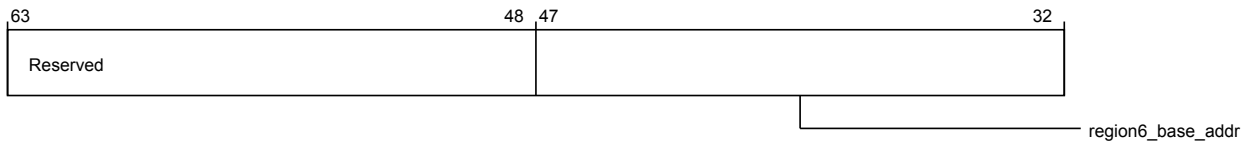


Figure 4-2144 `por_mpu_por_mpu_m5_prbar6` (high)

The following table shows the `por_mpu_m5_prbar6` higher register bit assignments.

Table 4-2161 `por_mpu_por_mpu_m5_prbar6` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_base_addr	Bits [47:31] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

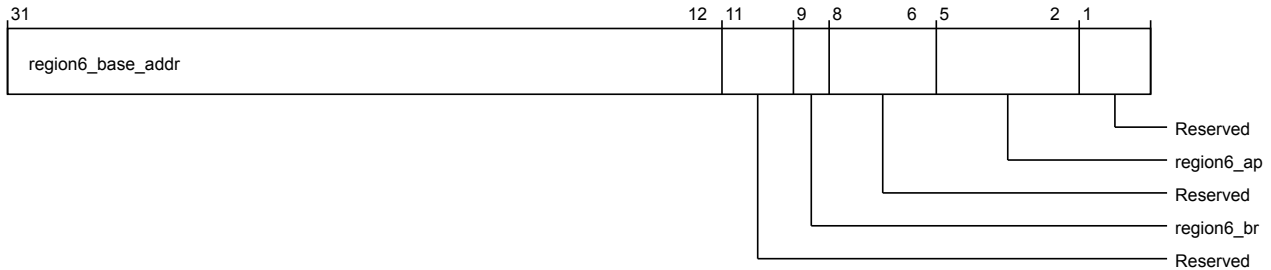


Figure 4-2145 `por_mpu_por_mpu_m5_prbar6` (low)

The following table shows the `por_mpu_m5_prbar6` lower register bit assignments.

Table 4-2162 `por_mpu_por_mpu_m5_prbar6` (low)

Bits	Field name	Description	Type	Reset
31:12	region6_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region6_br	Region 6 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region6_ap	Region 6 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar6

MPU master 0 programmable limit address register 6.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2478

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

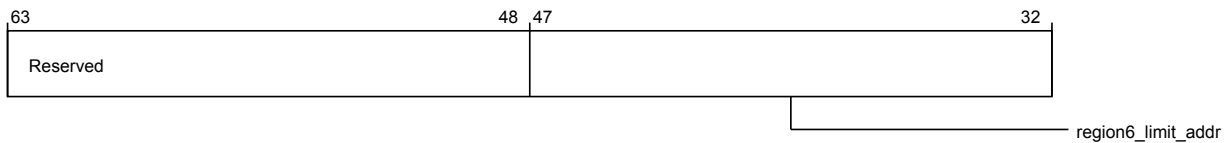


Figure 4-2146 por_mpu_por_mpu_m5_prlar6 (high)

The following table shows the por_mpu_m5_prlar6 higher register bit assignments.

Table 4-2163 por_mpu_por_mpu_m5_prlar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_limit_addr	Bits [47:32] of limit address of the range.	RW	20'b0

The following image shows the lower register bit assignments.

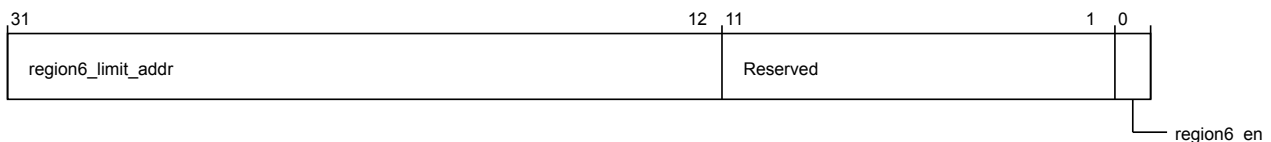


Figure 4-2147 por_mpu_por_mpu_m5_prlar6 (low)

The following table shows the por_mpu_m5_prlar6 lower register bit assignments.

Table 4-2164 por_mpu_por_mpu_m5_prlar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region6_en	Region 6 enable.	RW	1'b0

por_mpu_m5_prbar7

MPU master 0 programmable base address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2480

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

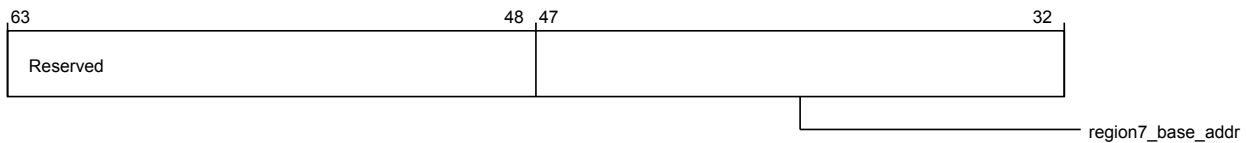


Figure 4-2148 por_mpu_m5_prbar7 (high)

The following table shows the por_mpu_m5_prbar7 higher register bit assignments.

Table 4-2165 por_mpu_m5_prbar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

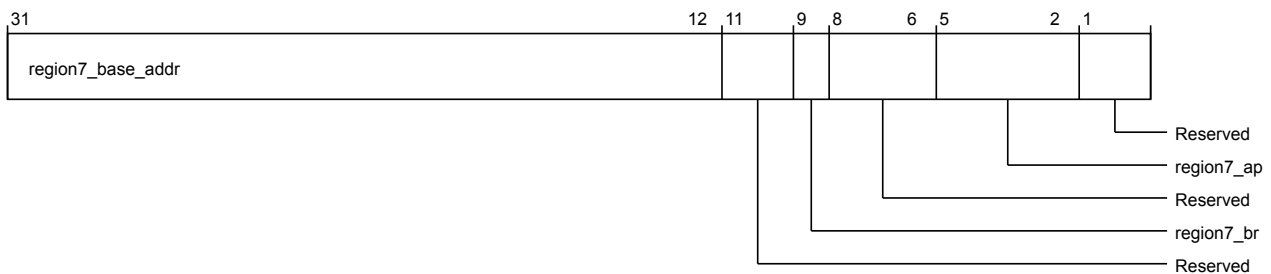


Figure 4-2149 por_mpu_m5_prbar7 (low)

The following table shows the por_mpu_m5_prbar7 lower register bit assignments.

Table 4-2166 por_mpu_m5_prbar7 (low)

Bits	Field name	Description	Type	Reset
31:12	region7_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2166 por_mpu_por_mpu_m5_prbar7 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region7_br	Region 7 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region7_ap	Region 7 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar7

MPU master 0 programmable limit address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2488

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

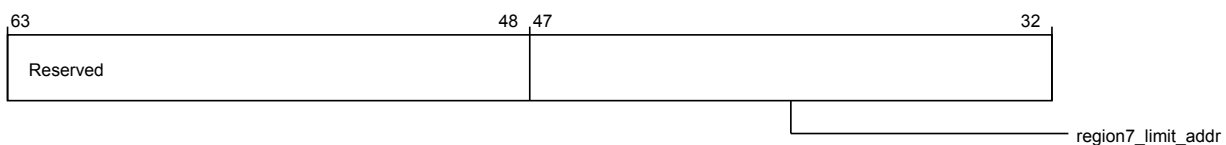


Figure 4-2150 por_mpu_por_mpu_m5_prlar7 (high)

The following table shows the por_mpu_m5_prlar7 higher register bit assignments.

Table 4-2167 por_mpu_por_mpu_m5_prlar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

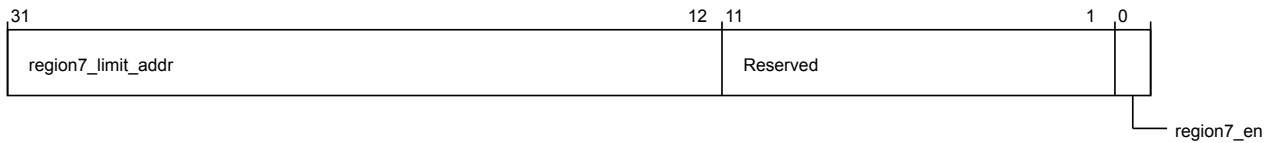


Figure 4-2151 `por_mpu_por_mpu_m5_prlar7` (low)

The following table shows the `por_mpu_m5_prlar7` lower register bit assignments.

Table 4-2168 `por_mpu_por_mpu_m5_prlar7` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region7_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region7_en</code>	Region 7 enable.	RW	1'b0

`por_mpu_m5_prbar8`

MPU master 0 programmable base address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2490

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

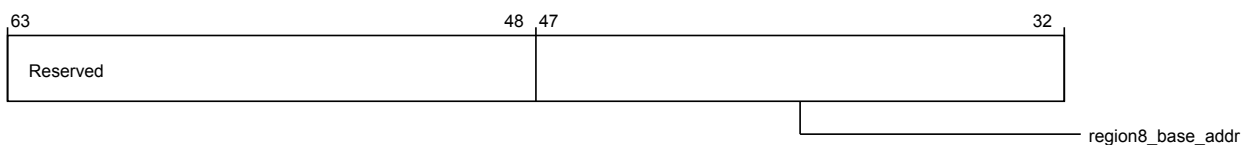


Figure 4-2152 `por_mpu_por_mpu_m5_prbar8` (high)

The following table shows the `por_mpu_m5_prbar8` higher register bit assignments.

Table 4-2169 `por_mpu_por_mpu_m5_prbar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

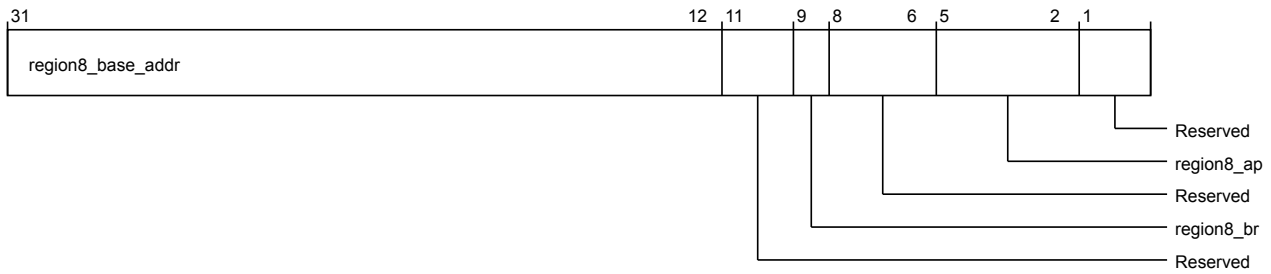


Figure 4-2153 por_mpu_por_mpu_m5_prbar8 (low)

The following table shows the por_mpu_m5_prbar8 lower register bit assignments.

Table 4-2170 por_mpu_por_mpu_m5_prbar8 (low)

Bits	Field name	Description	Type	Reset
31:12	region8_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region8_br	Region 8 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region8_ap	Region 8 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar8

MPU master 0 programmable limit address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2498

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

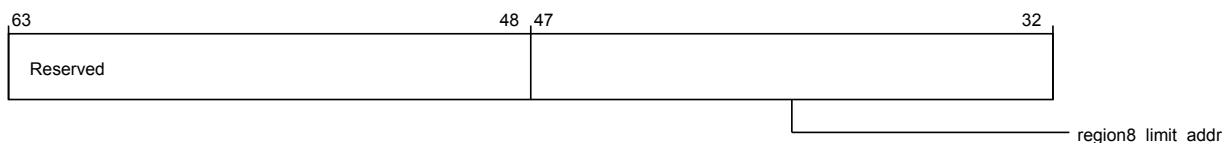


Figure 4-2154 `por_mpu_m5_prlar8` (high)

The following table shows the `por_mpu_m5_prlar8` higher register bit assignments.

Table 4-2171 `por_mpu_m5_prlar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

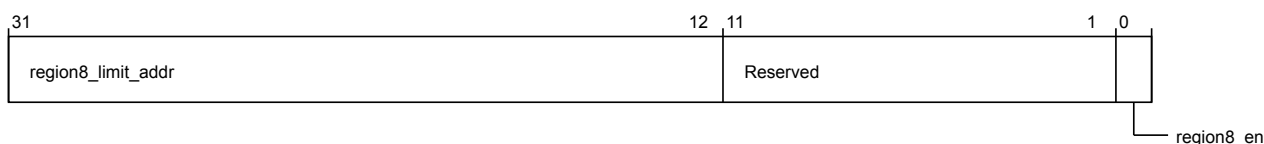


Figure 4-2155 `por_mpu_m5_prlar8` (low)

The following table shows the `por_mpu_m5_prlar8` lower register bit assignments.

Table 4-2172 `por_mpu_m5_prlar8` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region8_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region8_en</code>	Region 8 enable.	RW	1'b0

`por_mpu_m5_prbar9`

MPU master 0 programmable base address register 9.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h24A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

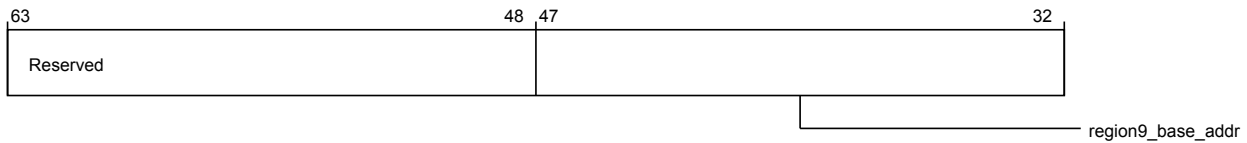


Figure 4-2156 `por_mpu_por_mpu_m5_prbar9` (high)

The following table shows the `por_mpu_m5_prbar9` higher register bit assignments.

Table 4-2173 `por_mpu_por_mpu_m5_prbar9` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

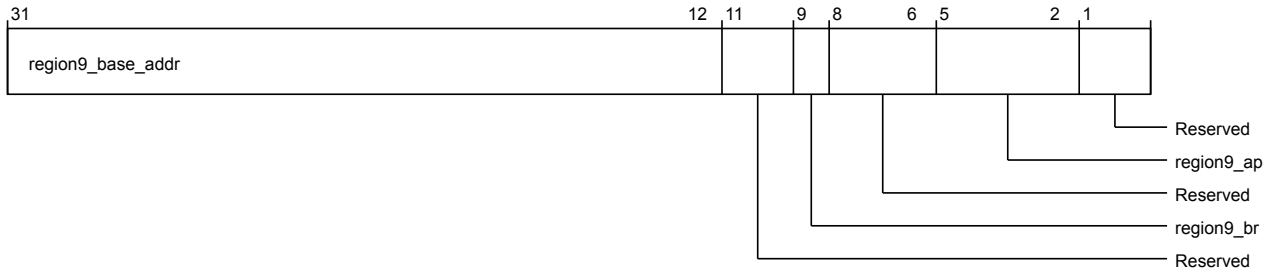


Figure 4-2157 `por_mpu_por_mpu_m5_prbar9` (low)

The following table shows the `por_mpu_m5_prbar9` lower register bit assignments.

Table 4-2174 `por_mpu_por_mpu_m5_prbar9` (low)

Bits	Field name	Description	Type	Reset
31:12	region9_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region9_br	Region 9 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region9_ap	Region 9 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar9

MPU master 0 programmable limit address register 9.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h24A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

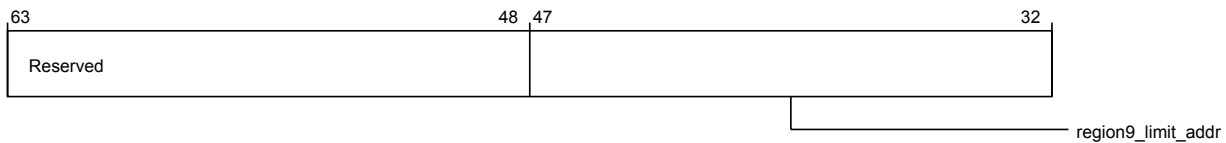


Figure 4-2158 por_mpu_por_mpu_m5_prlar9 (high)

The following table shows the por_mpu_m5_prlar9 higher register bit assignments.

Table 4-2175 por_mpu_por_mpu_m5_prlar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

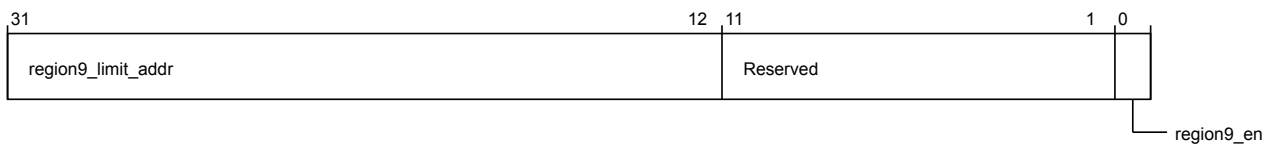


Figure 4-2159 por_mpu_por_mpu_m5_prlar9 (low)

The following table shows the por_mpu_m5_prlar9 lower register bit assignments.

Table 4-2176 por_mpu_por_mpu_m5_prlar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region9_en	Region 9 enable.	RW	1'b0

por_mpu_m5_prbar10

MPU master 0 programmable base address register 10.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h24B0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

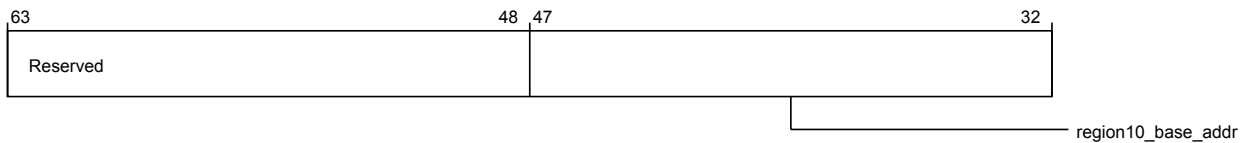


Figure 4-2160 por_mpu_por_mpu_m5_prbar10 (high)

The following table shows the por_mpu_m5_prbar10 higher register bit assignments.

Table 4-2177 por_mpu_por_mpu_m5_prbar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

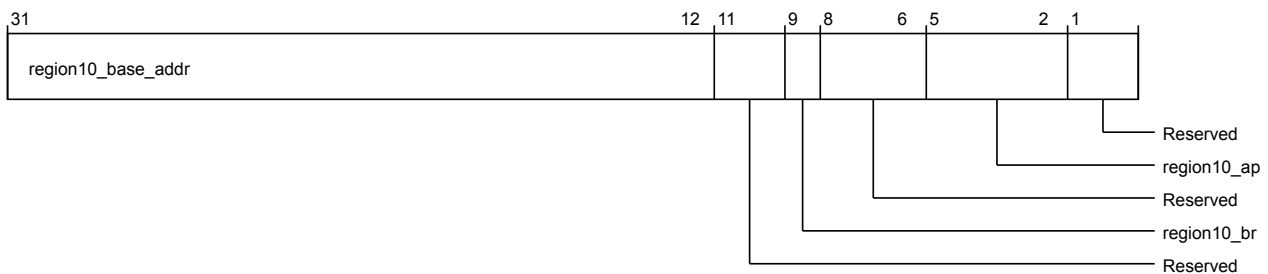


Figure 4-2161 por_mpu_por_mpu_m5_prbar10 (low)

The following table shows the por_mpu_m5_prbar10 lower register bit assignments.

Table 4-2178 por_mpu_por_mpu_m5_prbar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2178 `por_mpu_por_mpu_m5_prbar10` (low) (continued)

Bits	Field name	Description	Type	Reset
9	region10_br	Region 10 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region10_ap	Region 10 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m5_prlar10`

MPU master 0 programmable limit address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h24B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

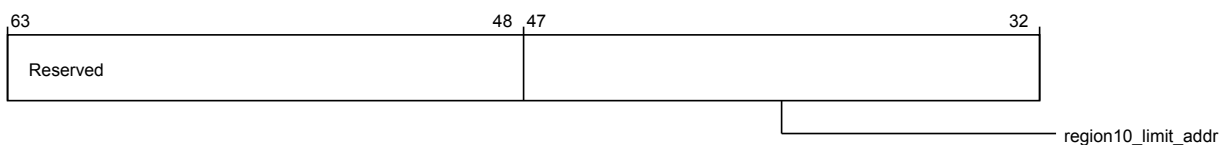


Figure 4-2162 `por_mpu_por_mpu_m5_prlar10` (high)

The following table shows the `por_mpu_m5_prlar10` higher register bit assignments.

Table 4-2179 `por_mpu_por_mpu_m5_prlar10` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

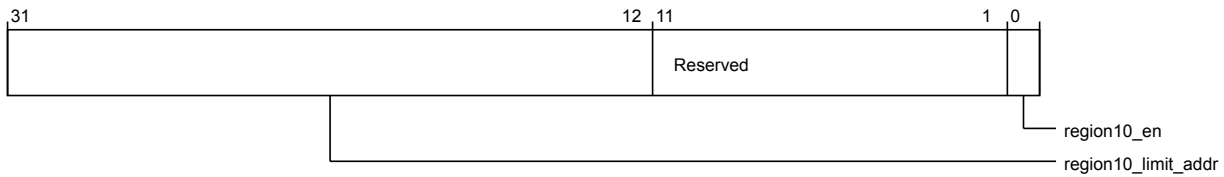


Figure 4-2163 por_mpu_por_mpu_m5_prlar10 (low)

The following table shows the por_mpu_m5_prlar10 lower register bit assignments.

Table 4-2180 por_mpu_por_mpu_m5_prlar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region10_en	Region 10 enable.	RW	1'b0

por_mpu_m5_prbar11

MPU master 0 programmable base address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h24C0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

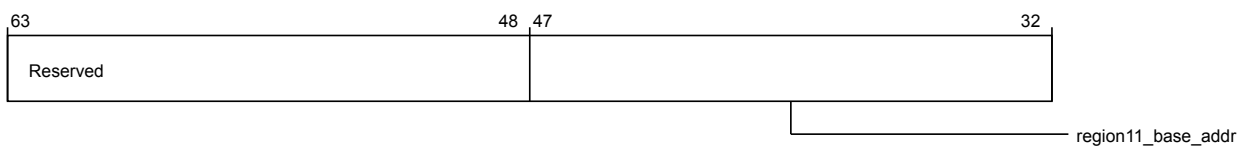


Figure 4-2164 por_mpu_por_mpu_m5_prbar11 (high)

The following table shows the por_mpu_m5_prbar11 higher register bit assignments.

Table 4-2181 por_mpu_por_mpu_m5_prbar11 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

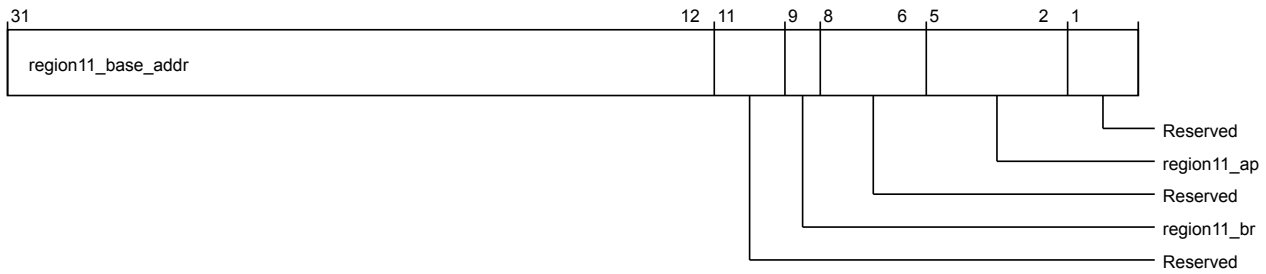


Figure 4-2165 `por_mpu_por_mpu_m5_prbar11` (low)

The following table shows the `por_mpu_m5_prbar11` lower register bit assignments.

Table 4-2182 `por_mpu_por_mpu_m5_prbar11` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region11_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region11_br</code>	Region 11 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region11_ap</code>	Region 11 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m5_prlar11`

MPU master 0 programmable limit address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h24C8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

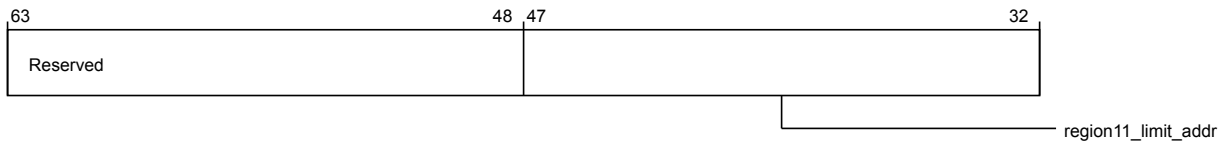


Figure 4-2166 por_mpu_por_mpu_m5_prlar11 (high)

The following table shows the por_mpu_m5_prlar11 higher register bit assignments.

Table 4-2183 por_mpu_por_mpu_m5_prlar11 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

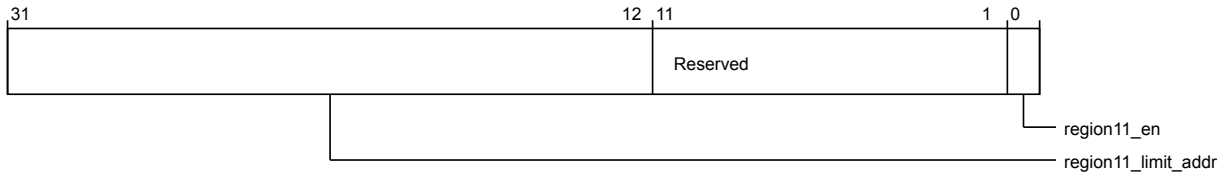


Figure 4-2167 por_mpu_por_mpu_m5_prlar11 (low)

The following table shows the por_mpu_m5_prlar11 lower register bit assignments.

Table 4-2184 por_mpu_por_mpu_m5_prlar11 (low)

Bits	Field name	Description	Type	Reset
31:12	region11_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region11_en	Region 11 enable.	RW	1'b0

por_mpu_m5_prbar12

MPU master 0 programmable base address register 12.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h24D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

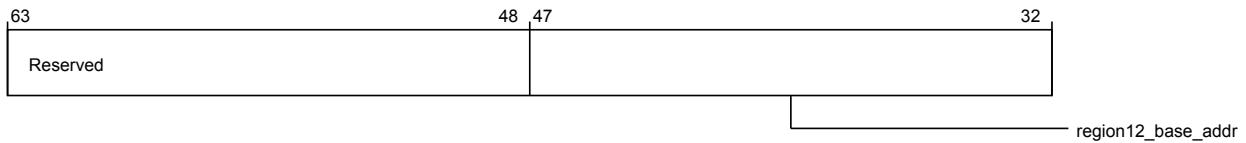


Figure 4-2168 `por_mpu_por_mpu_m5_prbar12` (high)

The following table shows the `por_mpu_m5_prbar12` higher register bit assignments.

Table 4-2185 `por_mpu_por_mpu_m5_prbar12` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

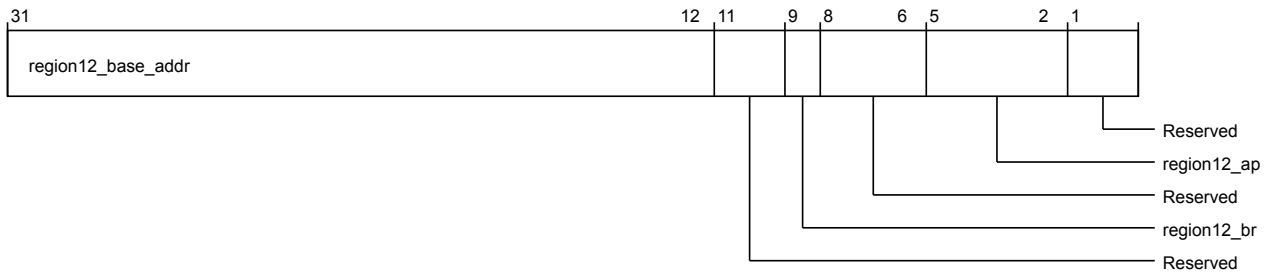


Figure 4-2169 `por_mpu_por_mpu_m5_prbar12` (low)

The following table shows the `por_mpu_m5_prbar12` lower register bit assignments.

Table 4-2186 `por_mpu_por_mpu_m5_prbar12` (low)

Bits	Field name	Description	Type	Reset
31:12	region12_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region12_br	Region 12 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region12_ap	Region 12 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar12

MPU master 0 programmable limit address register 12.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h24D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

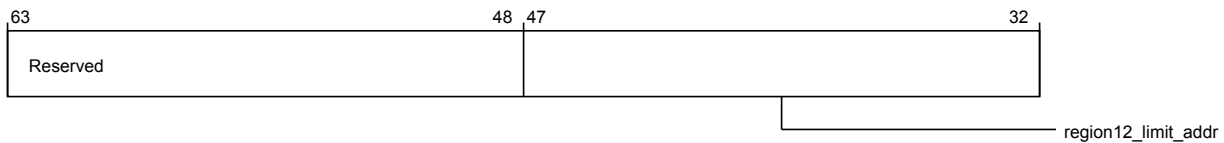


Figure 4-2170 por_mpu_por_mpu_m5_prlar12 (high)

The following table shows the `por_mpu_m5_prlar12` higher register bit assignments.

Table 4-2187 por_mpu_por_mpu_m5_prlar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

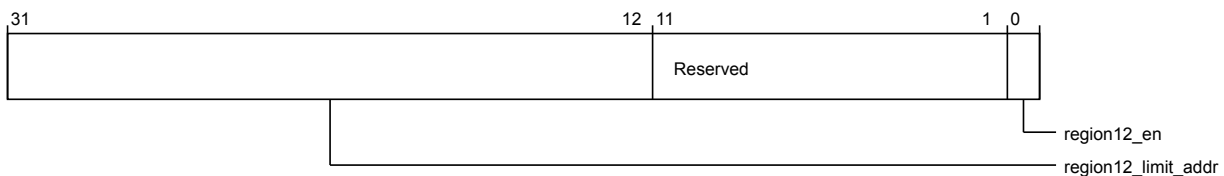


Figure 4-2171 por_mpu_por_mpu_m5_prlar12 (low)

The following table shows the `por_mpu_m5_prlar12` lower register bit assignments.

Table 4-2188 por_mpu_por_mpu_m5_prlar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region12_en	Region 12 enable.	RW	1'b0

por_mpu_m5_prbar13

MPU master 0 programmable base address register 13.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h24E0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

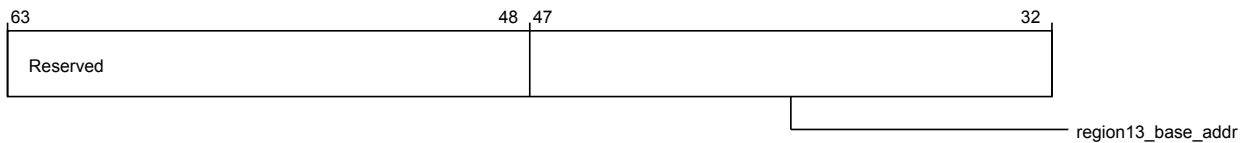


Figure 4-2172 por_mpu_por_mpu_m5_prbar13 (high)

The following table shows the por_mpu_m5_prbar13 higher register bit assignments.

Table 4-2189 por_mpu_por_mpu_m5_prbar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

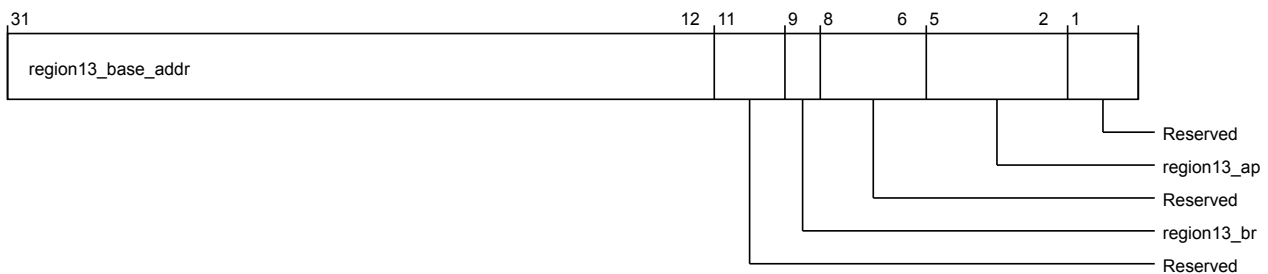


Figure 4-2173 por_mpu_por_mpu_m5_prbar13 (low)

The following table shows the por_mpu_m5_prbar13 lower register bit assignments.

Table 4-2190 por_mpu_por_mpu_m5_prbar13 (low)

Bits	Field name	Description	Type	Reset
31:12	region13_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2190 por_mpu_por_mpu_m5_prbar13 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region13_br	Region 13 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region13_ap	Region 13 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar13

MPU master 0 programmable limit address register 13.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h24E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

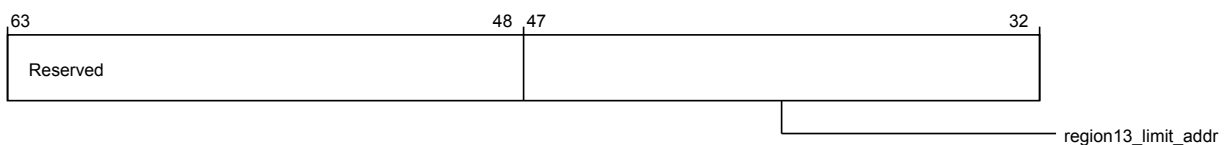


Figure 4-2174 por_mpu_por_mpu_m5_prlar13 (high)

The following table shows the por_mpu_m5_prlar13 higher register bit assignments.

Table 4-2191 por_mpu_por_mpu_m5_prlar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

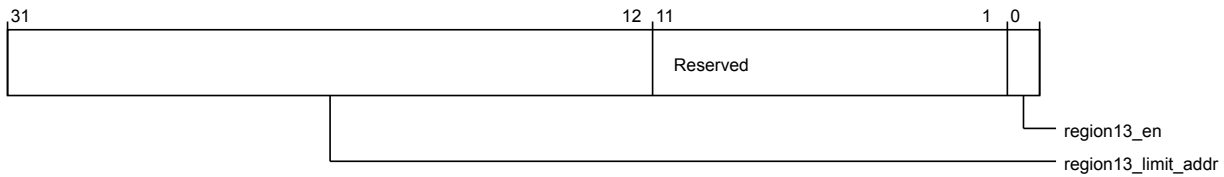


Figure 4-2175 `por_mpu_por_mpu_m5_prlar13` (low)

The following table shows the `por_mpu_m5_prlar13` lower register bit assignments.

Table 4-2192 `por_mpu_por_mpu_m5_prlar13` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region13_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region13_en</code>	Region 13 enable.	RW	1'b0

`por_mpu_m5_prbar14`

MPU master 0 programmable base address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h24F0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

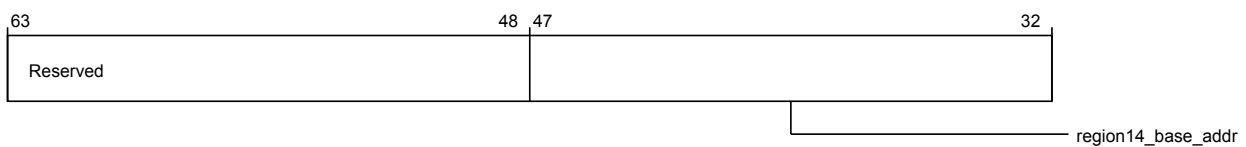


Figure 4-2176 `por_mpu_por_mpu_m5_prbar14` (high)

The following table shows the `por_mpu_m5_prbar14` higher register bit assignments.

Table 4-2193 `por_mpu_por_mpu_m5_prbar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region14_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

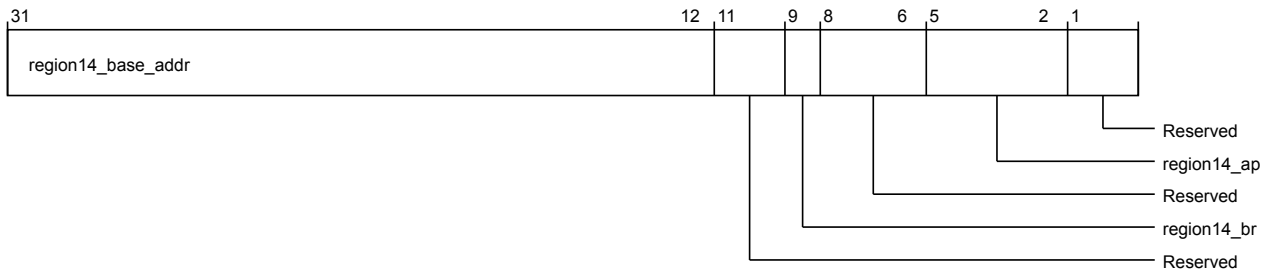


Figure 4-2177 por_mpu_por_mpu_m5_prbar14 (low)

The following table shows the por_mpu_m5_prbar14 lower register bit assignments.

Table 4-2194 por_mpu_por_mpu_m5_prbar14 (low)

Bits	Field name	Description	Type	Reset
31:12	region14_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region14_br	Region 14 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region14_ap	Region 14 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar14

MPU master 0 programmable limit address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h24F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

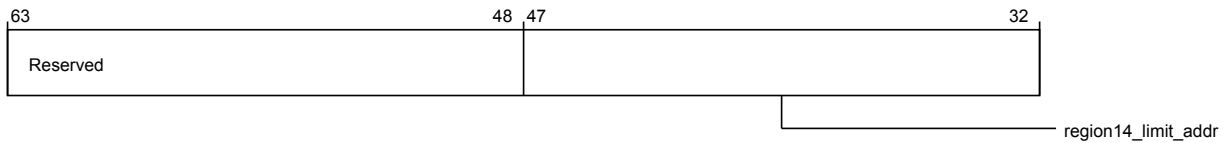


Figure 4-2178 `por_mpu_m5_prlar14` (high)

The following table shows the `por_mpu_m5_prlar14` higher register bit assignments.

Table 4-2195 `por_mpu_m5_prlar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region14_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

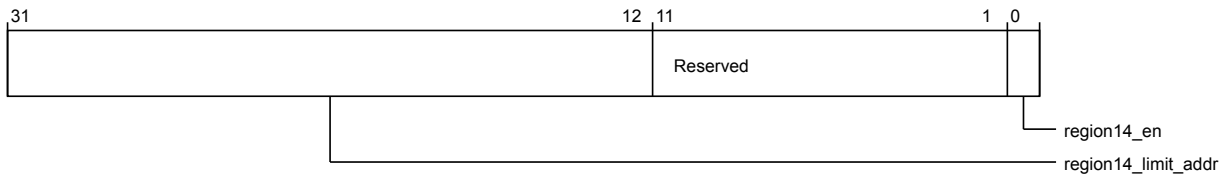


Figure 4-2179 `por_mpu_m5_prlar14` (low)

The following table shows the `por_mpu_m5_prlar14` lower register bit assignments.

Table 4-2196 `por_mpu_m5_prlar14` (low)

Bits	Field name	Description	Type	Reset
31:12	region14_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region14_en	Region 14 enable.	RW	1'b0

`por_mpu_m5_prbar15`

MPU master 0 programmable base address register 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2500
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

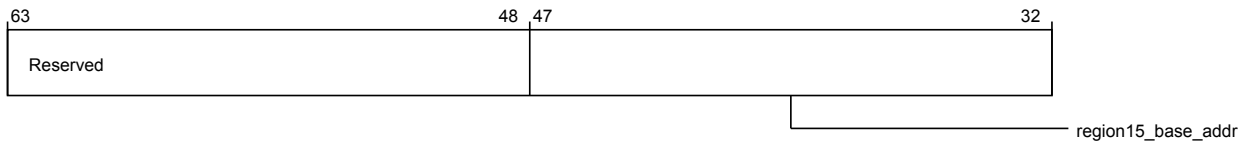


Figure 4-2180 por_mpu_por_mpu_m5_prbar15 (high)

The following table shows the por_mpu_m5_prbar15 higher register bit assignments.

Table 4-2197 por_mpu_por_mpu_m5_prbar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

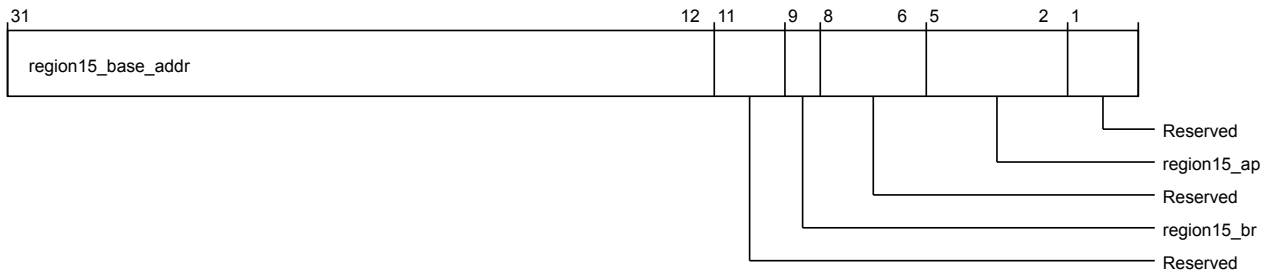


Figure 4-2181 por_mpu_por_mpu_m5_prbar15 (low)

The following table shows the por_mpu_m5_prbar15 lower register bit assignments.

Table 4-2198 por_mpu_por_mpu_m5_prbar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region15_br	Region 15 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region15_ap	Region 15 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar15

MPU master 0 programmable limit address register 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2508

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

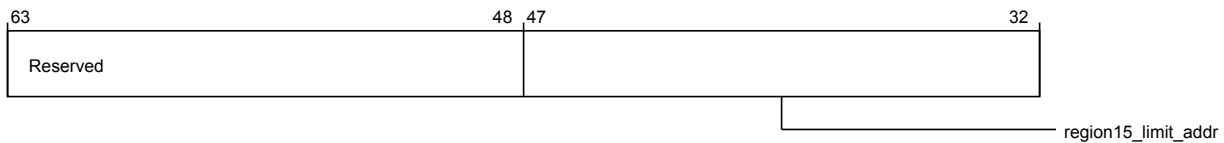


Figure 4-2182 por_mpu_por_mpu_m5_prlar15 (high)

The following table shows the por_mpu_m5_prlar15 higher register bit assignments.

Table 4-2199 por_mpu_por_mpu_m5_prlar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

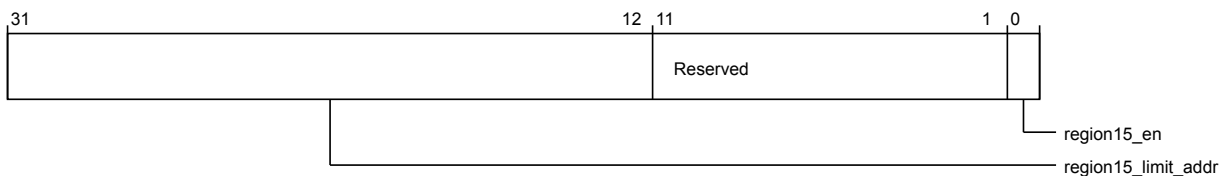


Figure 4-2183 por_mpu_por_mpu_m5_prlar15 (low)

The following table shows the por_mpu_m5_prlar15 lower register bit assignments.

Table 4-2200 por_mpu_por_mpu_m5_prlar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region15_en	Region 15 enable.	RW	1'b0

por_mpu_m5_prbar16

MPU master 0 programmable base address register 16.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2510
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

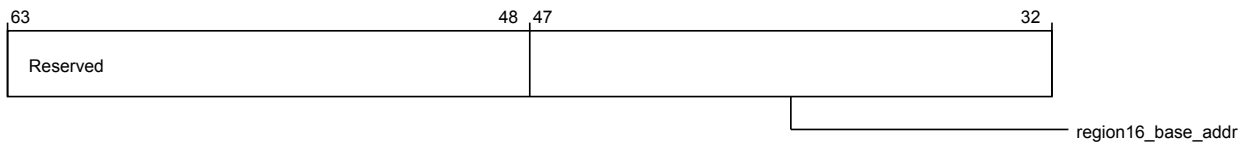


Figure 4-2184 por_mpu_por_mpu_m5_prbar16 (high)

The following table shows the por_mpu_m5_prbar16 higher register bit assignments.

Table 4-2201 por_mpu_por_mpu_m5_prbar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

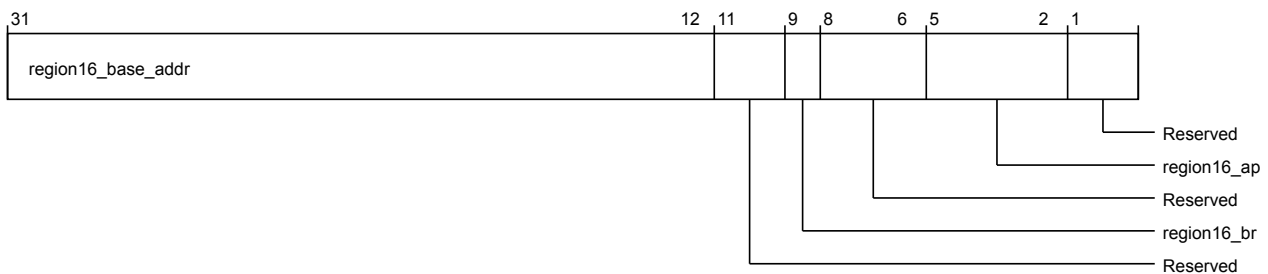


Figure 4-2185 por_mpu_por_mpu_m5_prbar16 (low)

The following table shows the por_mpu_m5_prbar16 lower register bit assignments.

Table 4-2202 por_mpu_por_mpu_m5_prbar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2202 por_mpu_por_mpu_m5_prbar16 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region16_br	Region 16 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region16_ap	Region 16 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar16

MPU master 0 programmable limit address register 16.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2518

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

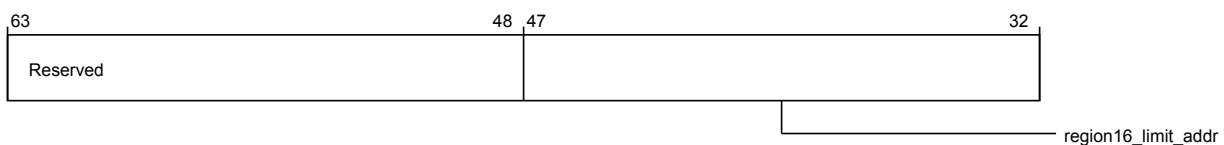


Figure 4-2186 por_mpu_por_mpu_m5_prlar16 (high)

The following table shows the por_mpu_m5_prlar16 higher register bit assignments.

Table 4-2203 por_mpu_por_mpu_m5_prlar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

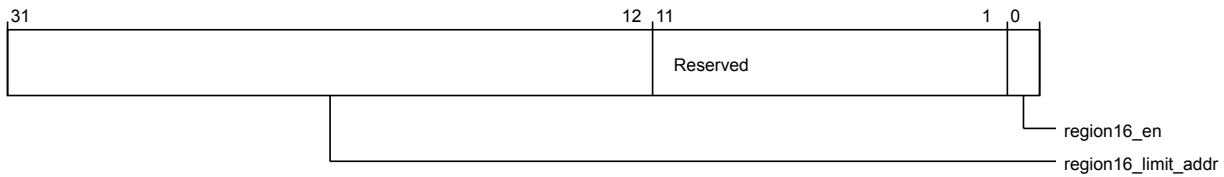


Figure 4-2187 `por_mpu_por_mpu_m5_prlar16` (low)

The following table shows the `por_mpu_m5_prlar16` lower register bit assignments.

Table 4-2204 `por_mpu_por_mpu_m5_prlar16` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region16_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region16_en</code>	Region 16 enable.	RW	1'b0

`por_mpu_m5_prbar17`

MPU master 0 programmable base address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2520

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

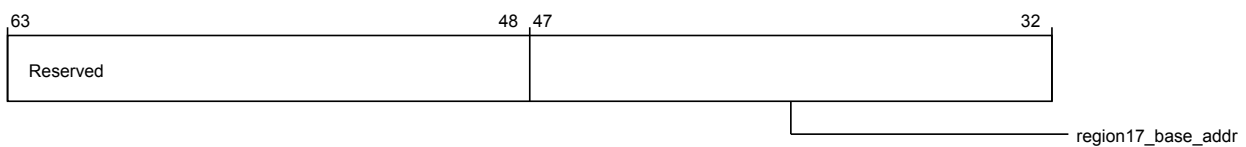


Figure 4-2188 `por_mpu_por_mpu_m5_prbar17` (high)

The following table shows the `por_mpu_m5_prbar17` higher register bit assignments.

Table 4-2205 `por_mpu_por_mpu_m5_prbar17` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region17_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

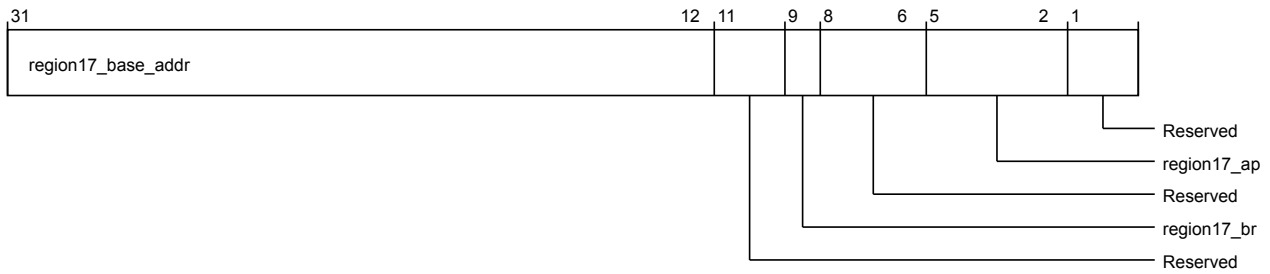


Figure 4-2189 `por_mpu_por_mpu_m5_prbar17` (low)

The following table shows the `por_mpu_m5_prbar17` lower register bit assignments.

Table 4-2206 `por_mpu_por_mpu_m5_prbar17` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region17_base_addr</code>	Bits [32:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region17_br</code>	Region 17 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region17_ap</code>	Region 17 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m5_prlar17`

MPU master 0 programmable limit address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2528

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

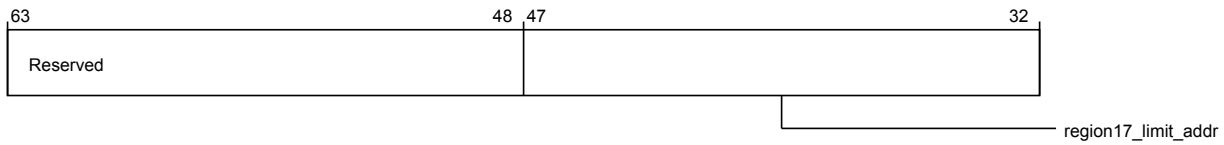


Figure 4-2190 por_mpu_m5_prlar17 (high)

The following table shows the por_mpu_m5_prlar17 higher register bit assignments.

Table 4-2207 por_mpu_m5_prlar17 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

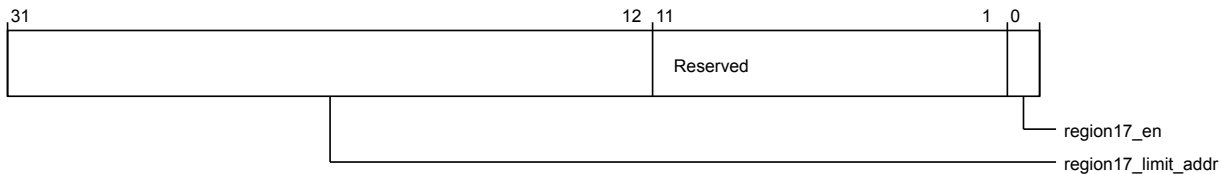


Figure 4-2191 por_mpu_m5_prlar17 (low)

The following table shows the por_mpu_m5_prlar17 lower register bit assignments.

Table 4-2208 por_mpu_m5_prlar17 (low)

Bits	Field name	Description	Type	Reset
31:12	region17_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region17_en	Region 17 enable.	RW	1'b0

por_mpu_m5_prbar18

MPU master 0 programmable base address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2530
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

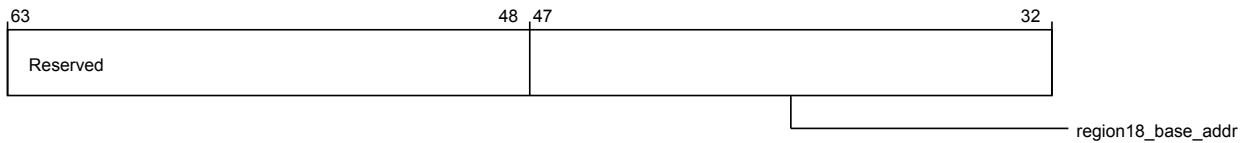


Figure 4-2192 por_mpu_por_mpu_m5_prbar18 (high)

The following table shows the por_mpu_m5_prbar18 higher register bit assignments.

Table 4-2209 por_mpu_por_mpu_m5_prbar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

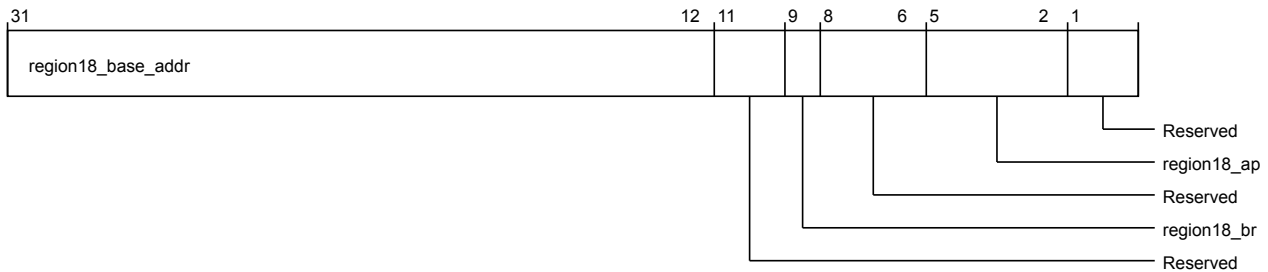


Figure 4-2193 por_mpu_por_mpu_m5_prbar18 (low)

The following table shows the por_mpu_m5_prbar18 lower register bit assignments.

Table 4-2210 por_mpu_por_mpu_m5_prbar18 (low)

Bits	Field name	Description	Type	Reset
31:12	region18_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region18_br	Region 18 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region18_ap	Region 18 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar18

MPU master 0 programmable limit address register 18.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2538

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

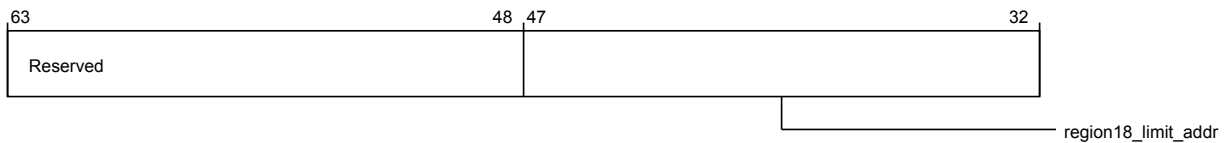


Figure 4-2194 por_mpu_por_mpu_m5_prlar18 (high)

The following table shows the por_mpu_m5_prlar18 higher register bit assignments.

Table 4-2211 por_mpu_por_mpu_m5_prlar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

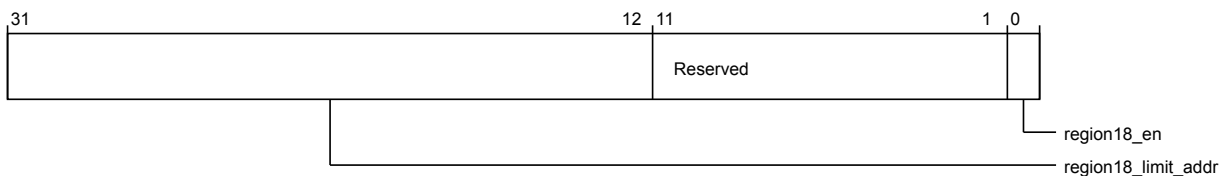


Figure 4-2195 por_mpu_por_mpu_m5_prlar18 (low)

The following table shows the por_mpu_m5_prlar18 lower register bit assignments.

Table 4-2212 por_mpu_por_mpu_m5_prlar18 (low)

Bits	Field name	Description	Type	Reset
31:12	region18_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region18_en	Region 18 enable.	RW	1'b0

por_mpu_m5_prbar19

MPU master 0 programmable base address register 19.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2540
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

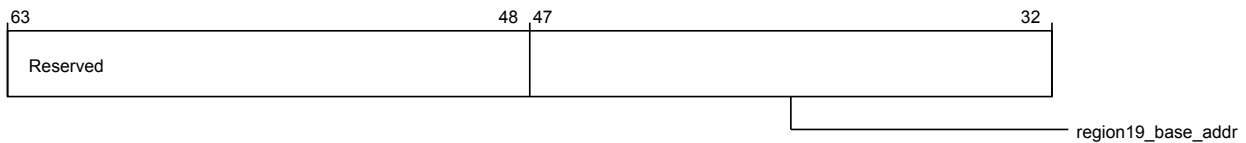


Figure 4-2196 por_mpu_por_mpu_m5_prbar19 (high)

The following table shows the por_mpu_m5_prbar19 higher register bit assignments.

Table 4-2213 por_mpu_por_mpu_m5_prbar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

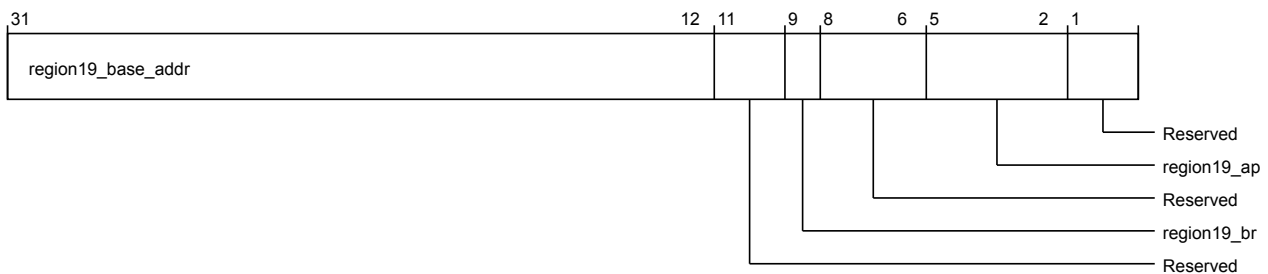


Figure 4-2197 por_mpu_por_mpu_m5_prbar19 (low)

The following table shows the por_mpu_m5_prbar19 lower register bit assignments.

Table 4-2214 por_mpu_por_mpu_m5_prbar19 (low)

Bits	Field name	Description	Type	Reset
31:12	region19_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2214 por_mpu_por_mpu_m5_prbar19 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region19_br	Region 19 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region19_ap	Region 19 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar19

MPU master 0 programmable limit address register 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2548

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

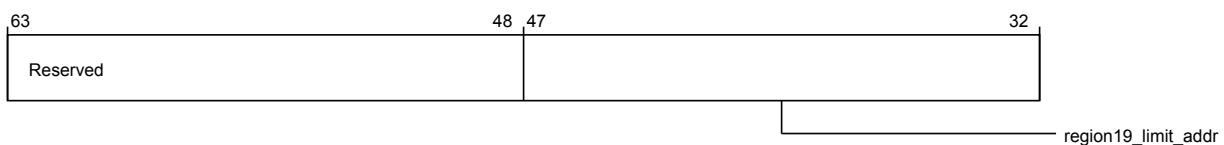


Figure 4-2198 por_mpu_por_mpu_m5_prlar19 (high)

The following table shows the por_mpu_m5_prlar19 higher register bit assignments.

Table 4-2215 por_mpu_por_mpu_m5_prlar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

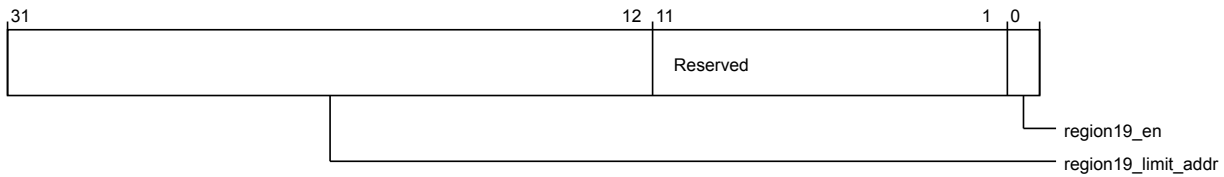


Figure 4-2199 `por_mpu_por_mpu_m5_prlar19` (low)

The following table shows the `por_mpu_m5_prlar19` lower register bit assignments.

Table 4-2216 `por_mpu_por_mpu_m5_prlar19` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region19_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region19_en</code>	Region 19 enable.	RW	1'b0

`por_mpu_m5_prbar20`

MPU master 0 programmable base address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2550

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

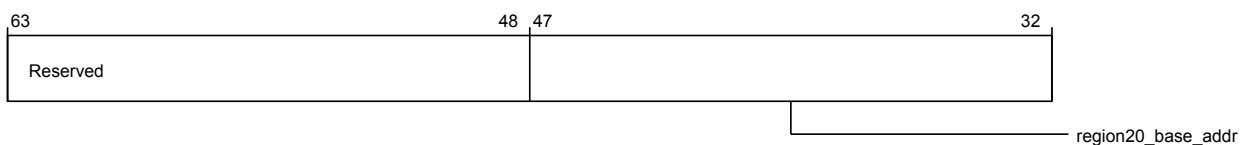


Figure 4-2200 `por_mpu_por_mpu_m5_prbar20` (high)

The following table shows the `por_mpu_m5_prbar20` higher register bit assignments.

Table 4-2217 `por_mpu_por_mpu_m5_prbar20` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region20_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

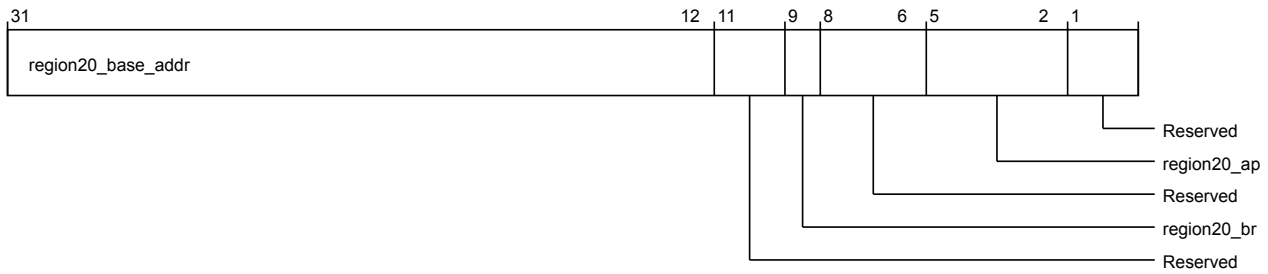


Figure 4-2201 por_mpu_m5_prbar20 (low)

The following table shows the por_mpu_m5_prbar20 lower register bit assignments.

Table 4-2218 por_mpu_m5_prbar20 (low)

Bits	Field name	Description	Type	Reset
31:12	region20_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region20_br	Region 20 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region20_ap	Region 20 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar20

MPU master 0 programmable limit address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2558

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

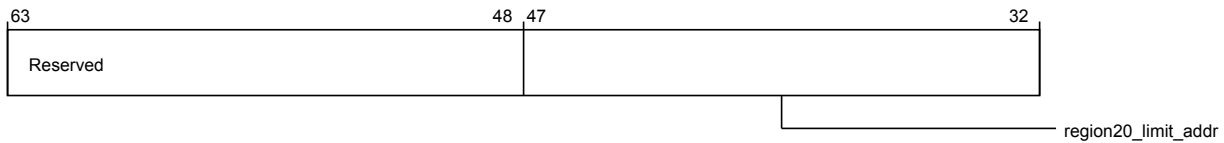


Figure 4-2202 por_mpu_por_mpu_m5_prlar20 (high)

The following table shows the por_mpu_m5_prlar20 higher register bit assignments.

Table 4-2219 por_mpu_por_mpu_m5_prlar20 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region20_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

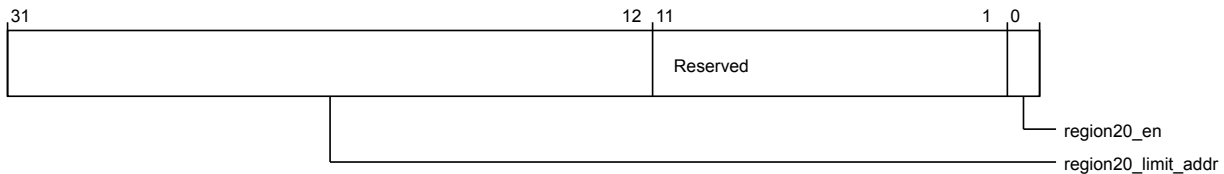


Figure 4-2203 por_mpu_por_mpu_m5_prlar20 (low)

The following table shows the por_mpu_m5_prlar20 lower register bit assignments.

Table 4-2220 por_mpu_por_mpu_m5_prlar20 (low)

Bits	Field name	Description	Type	Reset
31:12	region20_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region20_en	Region 20 enable.	RW	1'b0

por_mpu_m5_prbar21

MPU master 0 programmable base address register 21.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2560
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

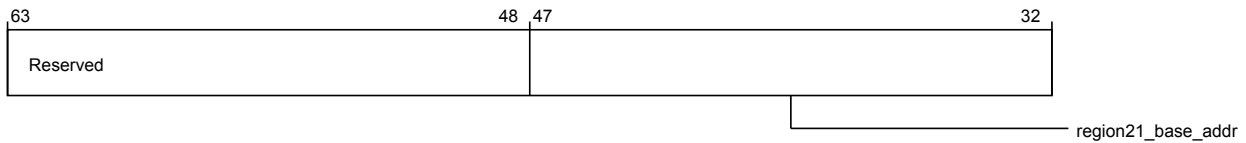


Figure 4-2204 por_mpu_por_mpu_m5_prbar21 (high)

The following table shows the por_mpu_m5_prbar21 higher register bit assignments.

Table 4-2221 por_mpu_por_mpu_m5_prbar21 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

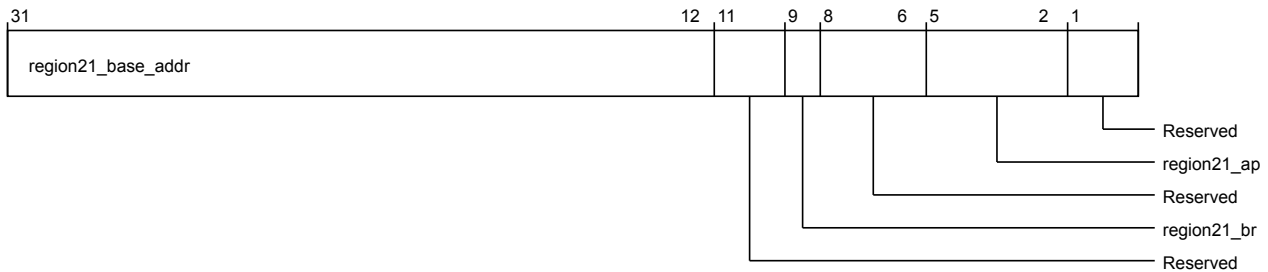


Figure 4-2205 por_mpu_por_mpu_m5_prbar21 (low)

The following table shows the por_mpu_m5_prbar21 lower register bit assignments.

Table 4-2222 por_mpu_por_mpu_m5_prbar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region21_br	Region 21 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region21_ap	Region 21 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar21

MPU master 0 programmable limit address register 21.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2568

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

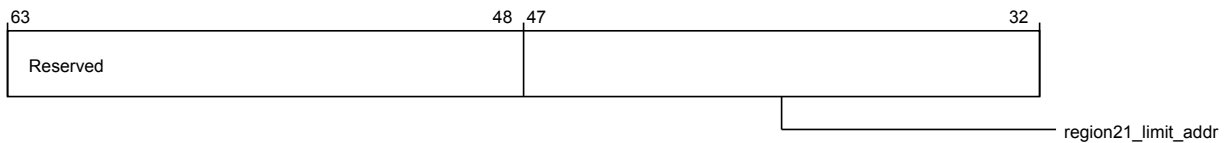


Figure 4-2206 `por_mpu_m5_prlar21` (high)

The following table shows the `por_mpu_m5_prlar21` higher register bit assignments.

Table 4-2223 `por_mpu_m5_prlar21` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

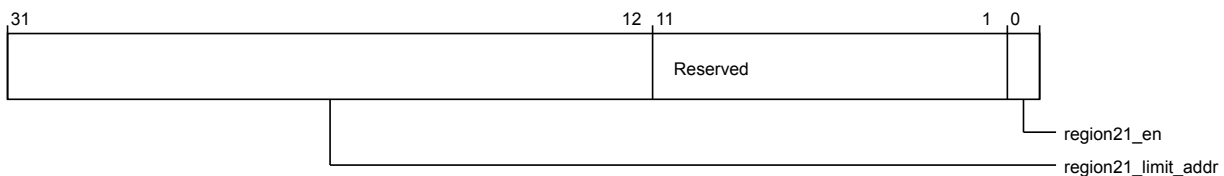


Figure 4-2207 `por_mpu_m5_prlar21` (low)

The following table shows the `por_mpu_m5_prlar21` lower register bit assignments.

Table 4-2224 `por_mpu_m5_prlar21` (low)

Bits	Field name	Description	Type	Reset
31:12	region21_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region21_en	Region 21 enable.	RW	1'b0

por_mpu_m5_prbar22

MPU master 0 programmable base address register 22.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2570
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

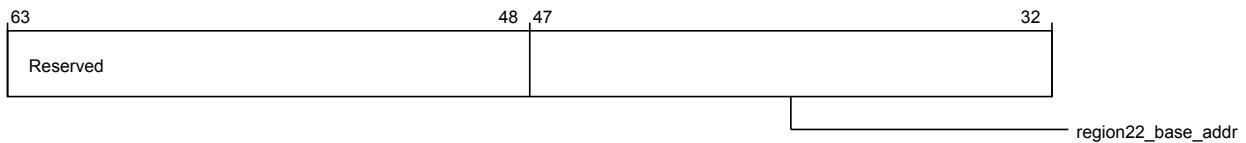


Figure 4-2208 por_mpu_por_mpu_m5_prbar22 (high)

The following table shows the por_mpu_m5_prbar22 higher register bit assignments.

Table 4-2225 por_mpu_por_mpu_m5_prbar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

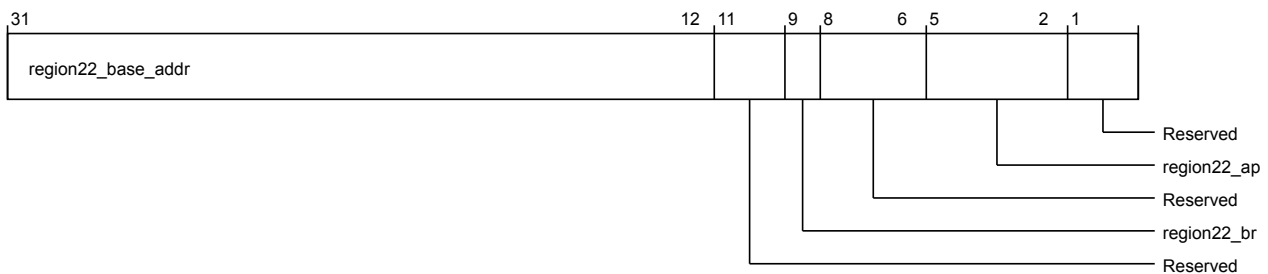


Figure 4-2209 por_mpu_por_mpu_m5_prbar22 (low)

The following table shows the por_mpu_m5_prbar22 lower register bit assignments.

Table 4-2226 por_mpu_por_mpu_m5_prbar22 (low)

Bits	Field name	Description	Type	Reset
31:12	region22_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2226 por_mpu_por_mpu_m5_prbar22 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region22_br	Region 22 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region22_ap	Region 22 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar22

MPU master 0 programmable limit address register 22.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2578

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

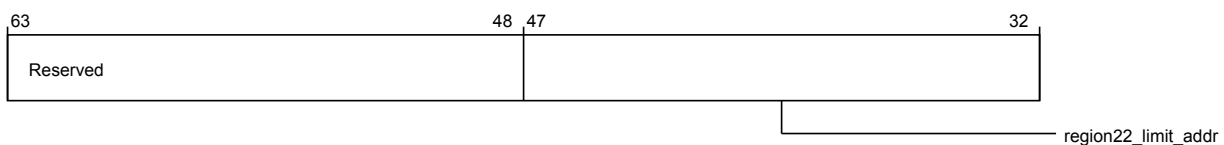


Figure 4-2210 por_mpu_por_mpu_m5_prlar22 (high)

The following table shows the por_mpu_m5_prlar22 higher register bit assignments.

Table 4-2227 por_mpu_por_mpu_m5_prlar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

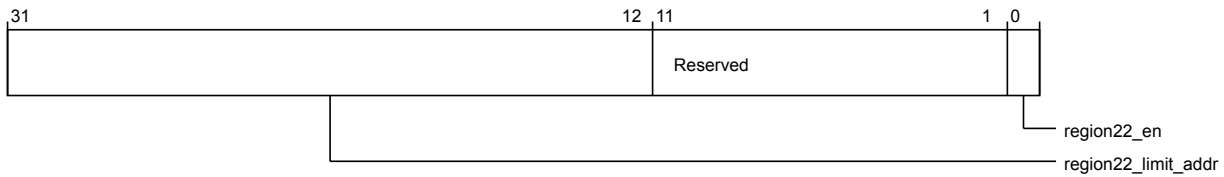


Figure 4-2211 `por_mpu_por_mpu_m5_prlar22` (low)

The following table shows the `por_mpu_m5_prlar22` lower register bit assignments.

Table 4-2228 `por_mpu_por_mpu_m5_prlar22` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region22_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region22_en</code>	Region 22 enable.	RW	1'b0

`por_mpu_m5_prbar23`

MPU master 0 programmable base address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2580

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

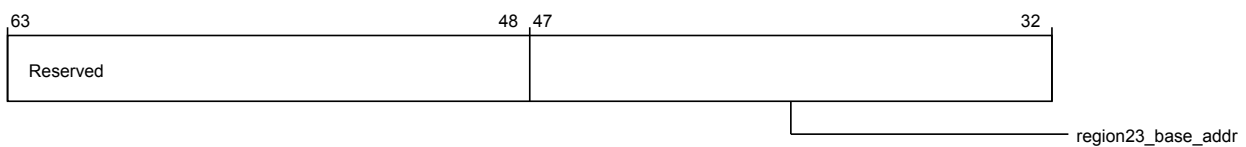


Figure 4-2212 `por_mpu_por_mpu_m5_prbar23` (high)

The following table shows the `por_mpu_m5_prbar23` higher register bit assignments.

Table 4-2229 `por_mpu_por_mpu_m5_prbar23` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region23_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

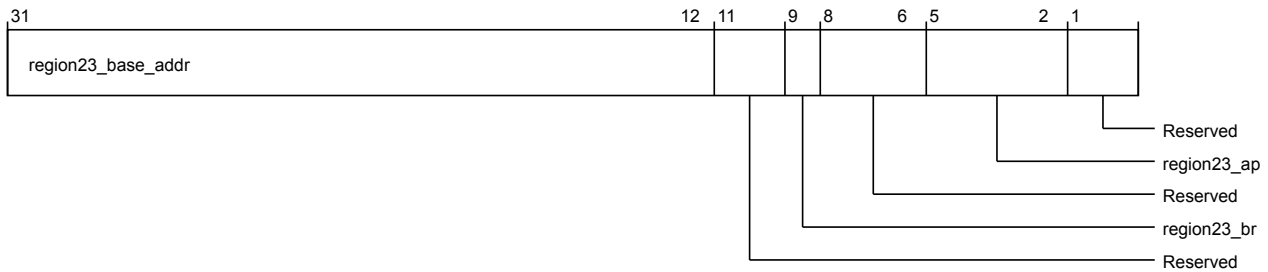


Figure 4-2213 `por_mpu_por_mpu_m5_prbar23` (low)

The following table shows the `por_mpu_m5_prbar23` lower register bit assignments.

Table 4-2230 `por_mpu_por_mpu_m5_prbar23` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region23_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region23_br</code>	Region 23 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region23_ap</code>	Region 23 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m5_prlar23`

MPU master 0 programmable limit address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2588

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

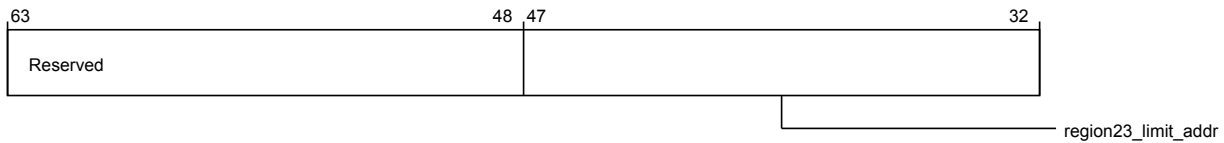


Figure 4-2214 `por_mpu_m5_prlar23` (high)

The following table shows the `por_mpu_m5_prlar23` higher register bit assignments.

Table 4-2231 `por_mpu_m5_prlar23` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region23_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

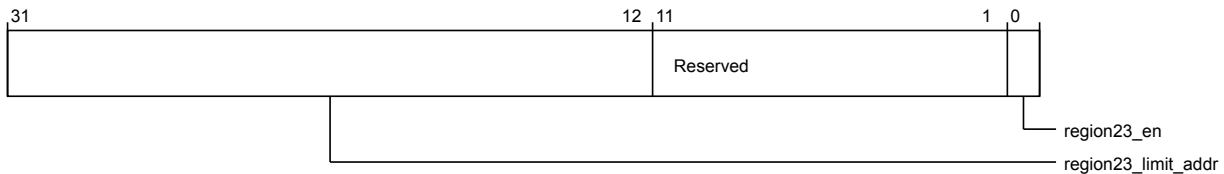


Figure 4-2215 `por_mpu_m5_prlar23` (low)

The following table shows the `por_mpu_m5_prlar23` lower register bit assignments.

Table 4-2232 `por_mpu_m5_prlar23` (low)

Bits	Field name	Description	Type	Reset
31:12	region23_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region23_en	Region 23 enable.	RW	1'b0

`por_mpu_m5_prbar24`

MPU master 0 programmable base address register 24.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2590
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

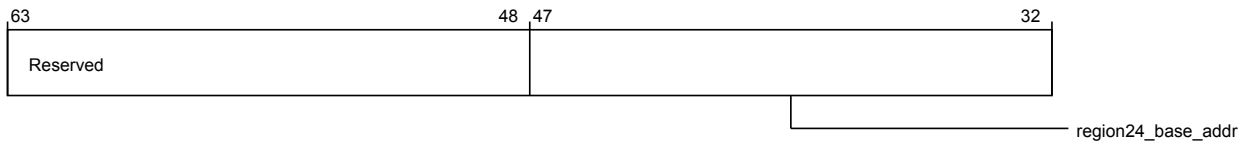


Figure 4-2216 `por_mpu_por_mpu_m5_prbar24` (high)

The following table shows the `por_mpu_m5_prbar24` higher register bit assignments.

Table 4-2233 `por_mpu_por_mpu_m5_prbar24` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

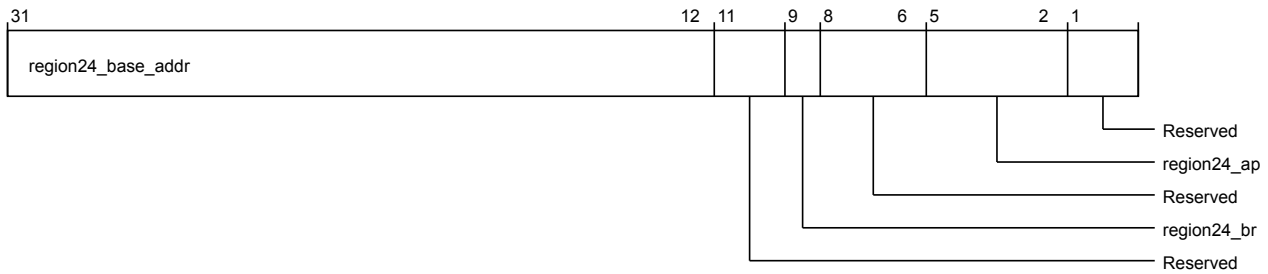


Figure 4-2217 `por_mpu_por_mpu_m5_prbar24` (low)

The following table shows the `por_mpu_m5_prbar24` lower register bit assignments.

Table 4-2234 `por_mpu_por_mpu_m5_prbar24` (low)

Bits	Field name	Description	Type	Reset
31:12	region24_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region24_br	Region 24 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region24_ap	Region 24 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar24

MPU master 0 programmable limit address register 24.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2598

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

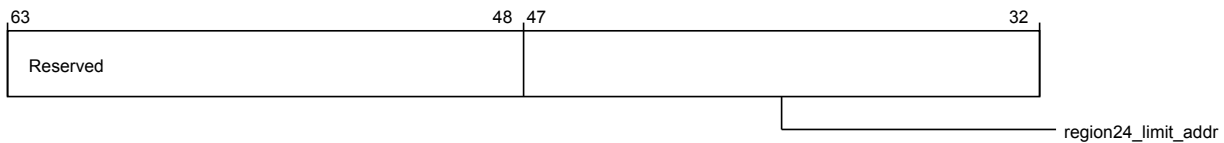


Figure 4-2218 por_mpu_por_mpu_m5_prlar24 (high)

The following table shows the por_mpu_m5_prlar24 higher register bit assignments.

Table 4-2235 por_mpu_por_mpu_m5_prlar24 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

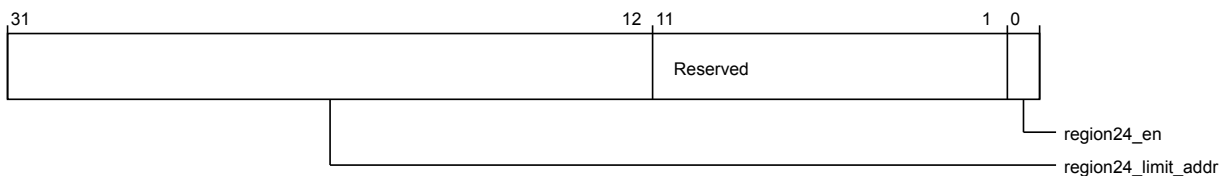


Figure 4-2219 por_mpu_por_mpu_m5_prlar24 (low)

The following table shows the por_mpu_m5_prlar24 lower register bit assignments.

Table 4-2236 por_mpu_por_mpu_m5_prlar24 (low)

Bits	Field name	Description	Type	Reset
31:12	region24_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region24_en	Region 24 enable.	RW	1'b0

por_mpu_m5_prbar25

MPU master 0 programmable base address register 25.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h25A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

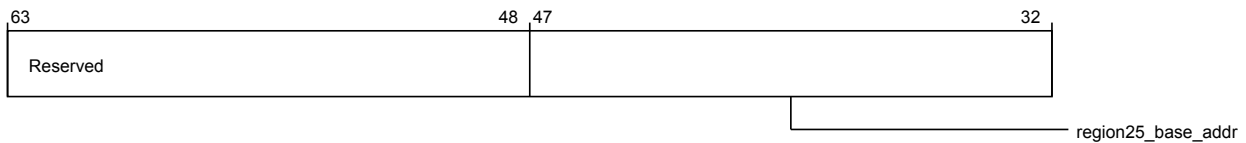


Figure 4-2220 por_mpu_por_mpu_m5_prbar25 (high)

The following table shows the por_mpu_m5_prbar25 higher register bit assignments.

Table 4-2237 por_mpu_por_mpu_m5_prbar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

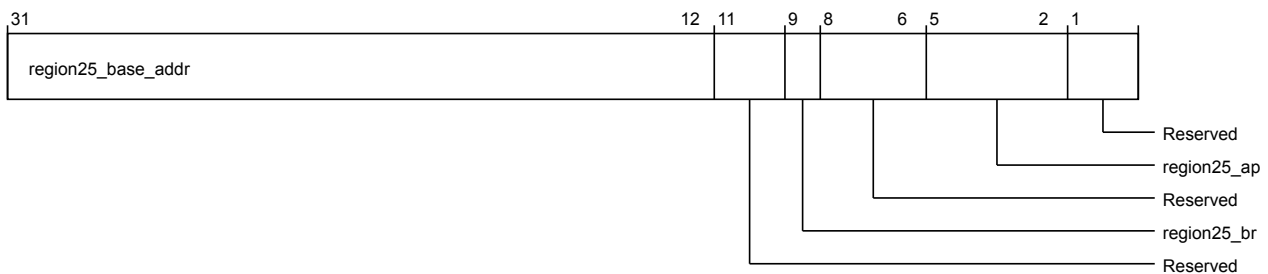


Figure 4-2221 por_mpu_por_mpu_m5_prbar25 (low)

The following table shows the por_mpu_m5_prbar25 lower register bit assignments.

Table 4-2238 por_mpu_por_mpu_m5_prbar25 (low)

Bits	Field name	Description	Type	Reset
31:12	region25_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2238 por_mpu_por_mpu_m5_prbar25 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region25_br	Region 25 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region25_ap	Region 25 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar25

MPU master 0 programmable limit address register 25.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h25A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

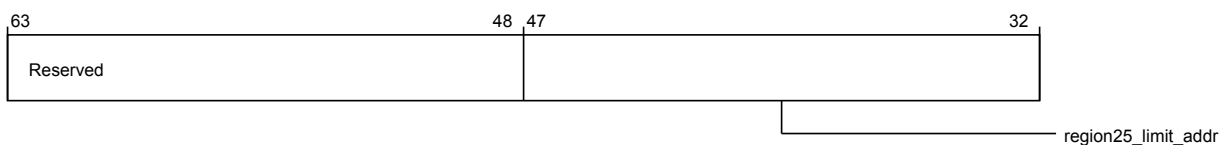


Figure 4-2222 por_mpu_por_mpu_m5_prlar25 (high)

The following table shows the por_mpu_m5_prlar25 higher register bit assignments.

Table 4-2239 por_mpu_por_mpu_m5_prlar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

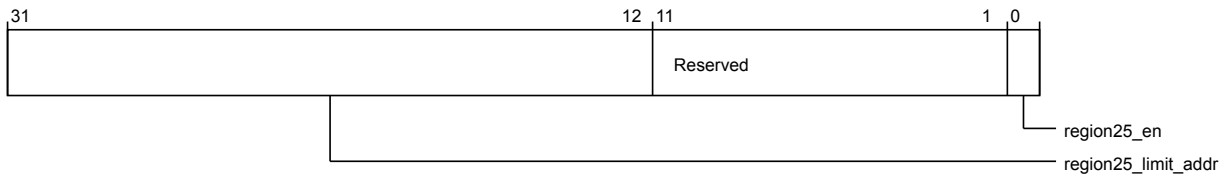


Figure 4-2223 `por_mpu_por_mpu_m5_prlar25` (low)

The following table shows the `por_mpu_m5_prlar25` lower register bit assignments.

Table 4-2240 `por_mpu_por_mpu_m5_prlar25` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region25_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region25_en</code>	Region 25 enable.	RW	1'b0

`por_mpu_m5_prbar26`

MPU master 0 programmable base address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h25B0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

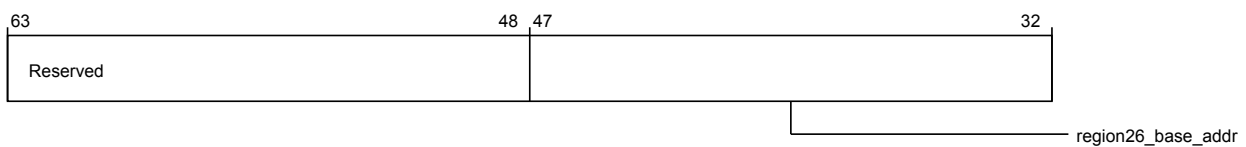


Figure 4-2224 `por_mpu_por_mpu_m5_prbar26` (high)

The following table shows the `por_mpu_m5_prbar26` higher register bit assignments.

Table 4-2241 `por_mpu_por_mpu_m5_prbar26` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region26_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

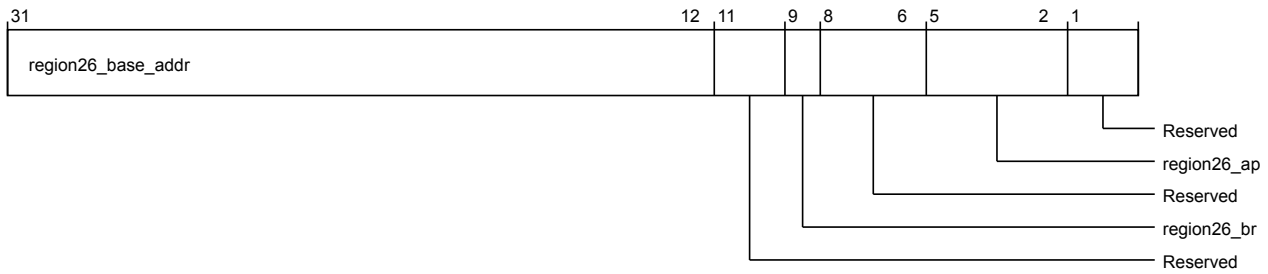


Figure 4-2225 por_mpu_m5_prbar26 (low)

The following table shows the por_mpu_m5_prbar26 lower register bit assignments.

Table 4-2242 por_mpu_m5_prbar26 (low)

Bits	Field name	Description	Type	Reset
31:12	region26_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region26_br	Region 26 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region26_ap	Region 26 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar26

MPU master 0 programmable limit address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h25B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

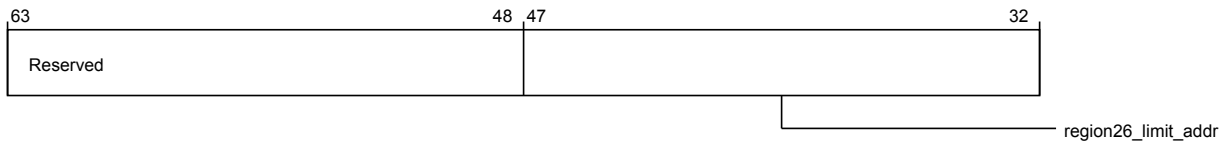


Figure 4-2226 por_mpu_m5_prlar26 (high)

The following table shows the por_mpu_m5_prlar26 higher register bit assignments.

Table 4-2243 por_mpu_m5_prlar26 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region26_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

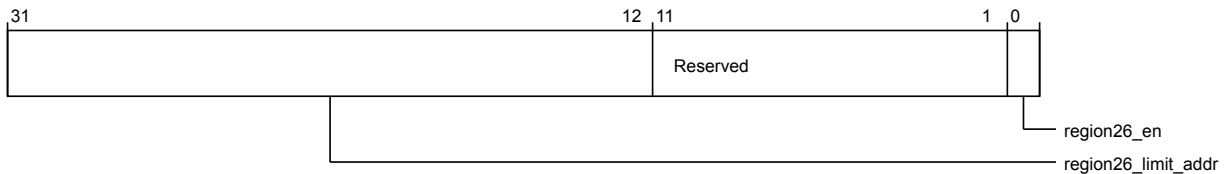


Figure 4-2227 por_mpu_m5_prlar26 (low)

The following table shows the por_mpu_m5_prlar26 lower register bit assignments.

Table 4-2244 por_mpu_m5_prlar26 (low)

Bits	Field name	Description	Type	Reset
31:12	region26_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region26_en	Region 26 enable.	RW	1'b0

por_mpu_m5_prbar27

MPU master 0 programmable base address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h25C0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

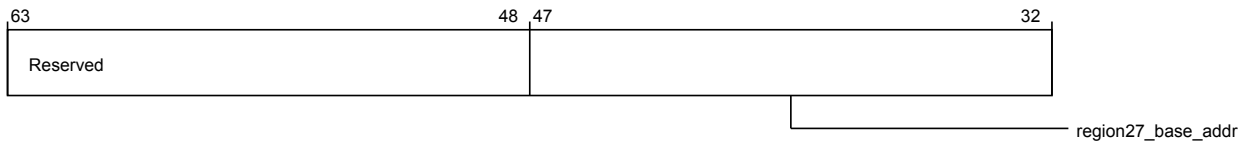


Figure 4-2228 `por_mpu_por_mpu_m5_prbar27` (high)

The following table shows the `por_mpu_m5_prbar27` higher register bit assignments.

Table 4-2245 `por_mpu_por_mpu_m5_prbar27` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

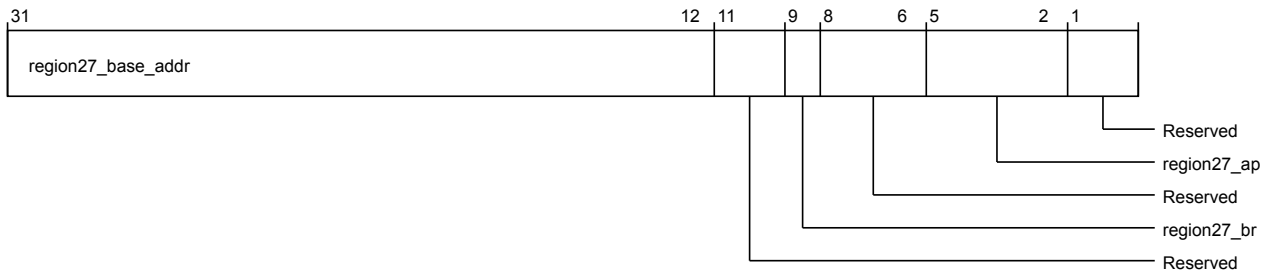


Figure 4-2229 `por_mpu_por_mpu_m5_prbar27` (low)

The following table shows the `por_mpu_m5_prbar27` lower register bit assignments.

Table 4-2246 `por_mpu_por_mpu_m5_prbar27` (low)

Bits	Field name	Description	Type	Reset
31:12	region27_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region27_br	Region 27 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region27_ap	Region 27 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar27

MPU master 0 programmable limit address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h25C8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

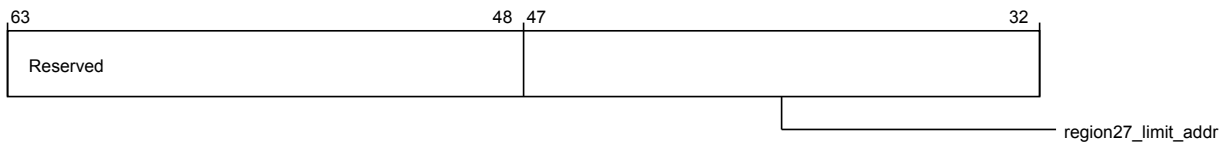


Figure 4-2230 por_mpu_por_mpu_m5_prlar27 (high)

The following table shows the por_mpu_m5_prlar27 higher register bit assignments.

Table 4-2247 por_mpu_por_mpu_m5_prlar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

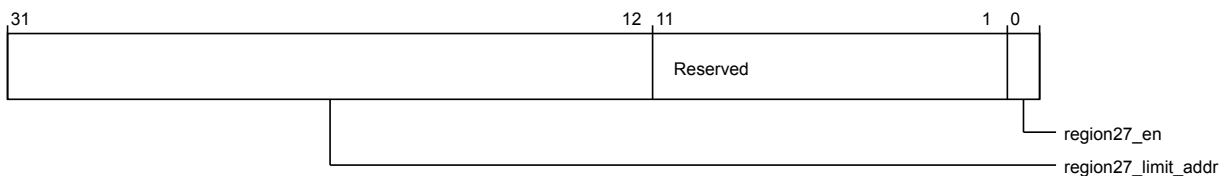


Figure 4-2231 por_mpu_por_mpu_m5_prlar27 (low)

The following table shows the por_mpu_m5_prlar27 lower register bit assignments.

Table 4-2248 por_mpu_por_mpu_m5_prlar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region27_en	Region 27 enable.	RW	1'b0

por_mpu_m5_prbar28

MPU master 0 programmable base address register 28.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h25D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

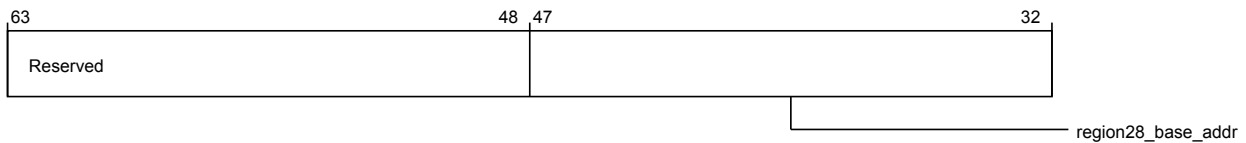


Figure 4-2232 por_mpu_por_mpu_m5_prbar28 (high)

The following table shows the por_mpu_m5_prbar28 higher register bit assignments.

Table 4-2249 por_mpu_por_mpu_m5_prbar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

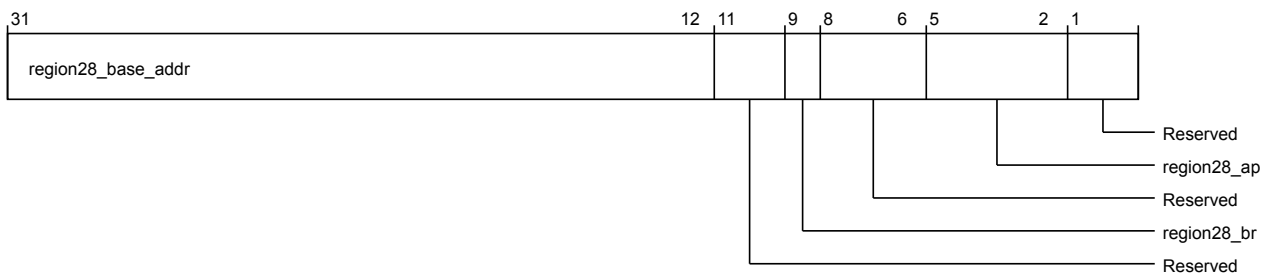


Figure 4-2233 por_mpu_por_mpu_m5_prbar28 (low)

The following table shows the por_mpu_m5_prbar28 lower register bit assignments.

Table 4-2250 por_mpu_por_mpu_m5_prbar28 (low)

Bits	Field name	Description	Type	Reset
31:12	region28_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2250 `por_mpu_por_mpu_m5_prbar28` (low) (continued)

Bits	Field name	Description	Type	Reset
9	region28_br	Region 28 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region28_ap	Region 28 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m5_prlar28`

MPU master 0 programmable limit address register 28.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h25D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

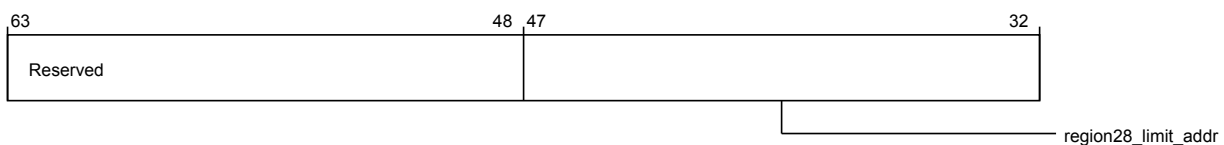


Figure 4-2234 `por_mpu_por_mpu_m5_prlar28` (high)

The following table shows the `por_mpu_m5_prlar28` higher register bit assignments.

Table 4-2251 `por_mpu_por_mpu_m5_prlar28` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

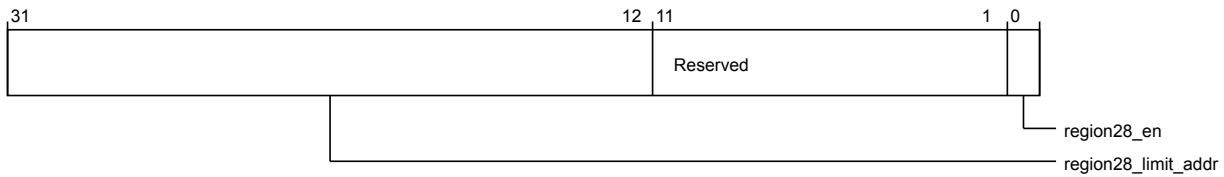


Figure 4-2235 `por_mpu_por_mpu_m5_prlar28` (low)

The following table shows the `por_mpu_m5_prlar28` lower register bit assignments.

Table 4-2252 `por_mpu_por_mpu_m5_prlar28` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region28_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region28_en</code>	Region 28 enable.	RW	1'b0

`por_mpu_m5_prbar29`

MPU master 0 programmable base address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h25E0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

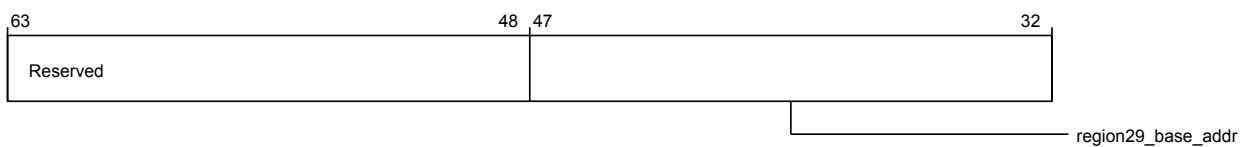


Figure 4-2236 `por_mpu_por_mpu_m5_prbar29` (high)

The following table shows the `por_mpu_m5_prbar29` higher register bit assignments.

Table 4-2253 `por_mpu_por_mpu_m5_prbar29` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region29_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

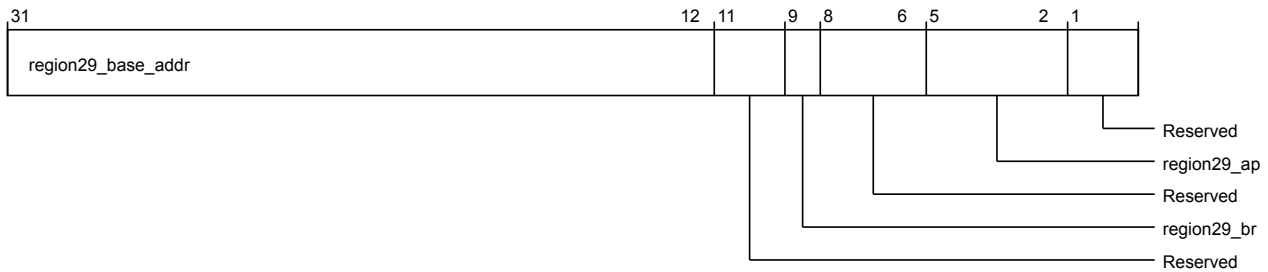


Figure 4-2237 `por_mpu_por_mpu_m5_prbar29` (low)

The following table shows the `por_mpu_m5_prbar29` lower register bit assignments.

Table 4-2254 `por_mpu_por_mpu_m5_prbar29` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region29_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region29_br</code>	Region 29 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region29_ap</code>	Region 29 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m5_prlar29`

MPU master 0 programmable limit address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h25E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

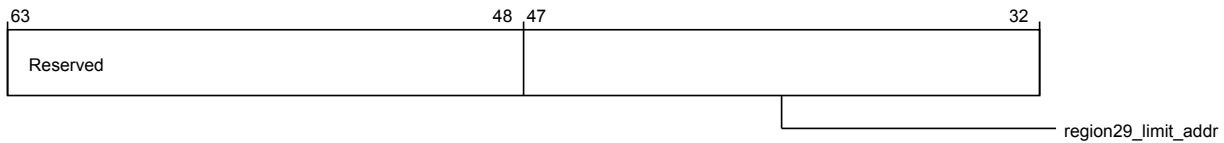


Figure 4-2238 por_mpu_m5_prlar29 (high)

The following table shows the por_mpu_m5_prlar29 higher register bit assignments.

Table 4-2255 por_mpu_m5_prlar29 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region29_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

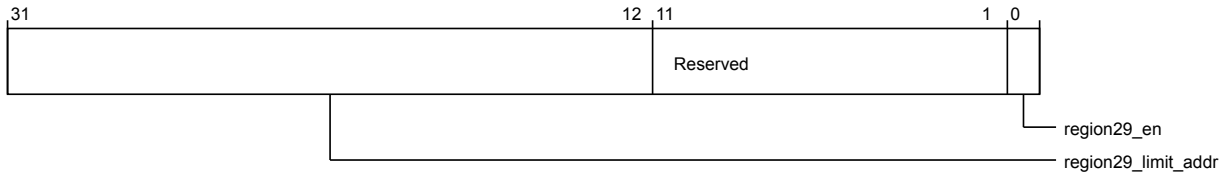


Figure 4-2239 por_mpu_m5_prlar29 (low)

The following table shows the por_mpu_m5_prlar29 lower register bit assignments.

Table 4-2256 por_mpu_m5_prlar29 (low)

Bits	Field name	Description	Type	Reset
31:12	region29_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region29_en	Region 29 enable.	RW	1'b0

por_mpu_m5_prbar30

MPU master 0 programmable base address register 30.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h25F0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

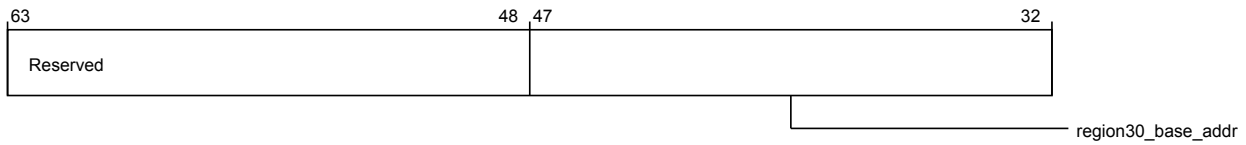


Figure 4-2240 por_mpu_por_mpu_m5_prbar30 (high)

The following table shows the por_mpu_m5_prbar30 higher register bit assignments.

Table 4-2257 por_mpu_por_mpu_m5_prbar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

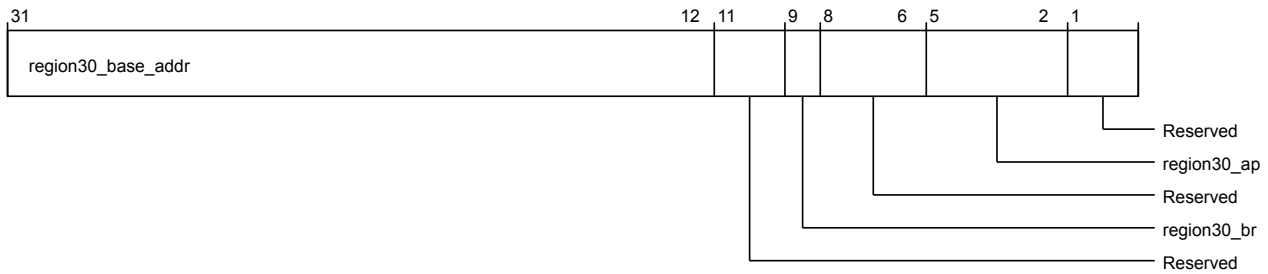


Figure 4-2241 por_mpu_por_mpu_m5_prbar30 (low)

The following table shows the por_mpu_m5_prbar30 lower register bit assignments.

Table 4-2258 por_mpu_por_mpu_m5_prbar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region30_br	Region 30 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region30_ap	Region 30 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar30

MPU master 0 programmable limit address register 30.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h25F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

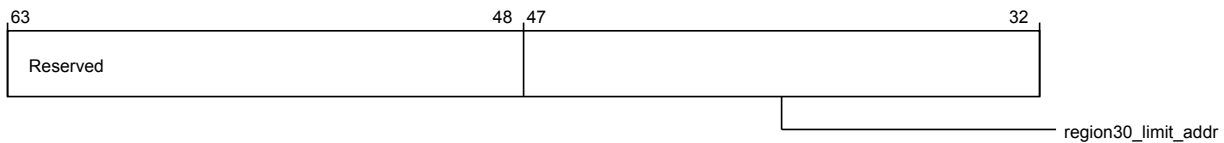


Figure 4-2242 por_mpu_por_mpu_m5_prlar30 (high)

The following table shows the por_mpu_m5_prlar30 higher register bit assignments.

Table 4-2259 por_mpu_por_mpu_m5_prlar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

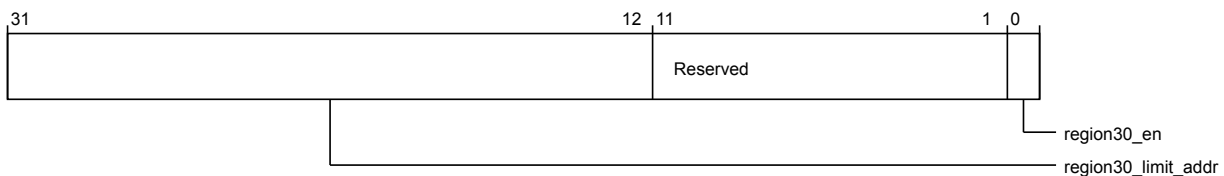


Figure 4-2243 por_mpu_por_mpu_m5_prlar30 (low)

The following table shows the por_mpu_m5_prlar30 lower register bit assignments.

Table 4-2260 por_mpu_por_mpu_m5_prlar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region30_en	Region 30 enable.	RW	1'b0

por_mpu_m5_prbar31

MPU master 0 programmable base address register 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2600
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

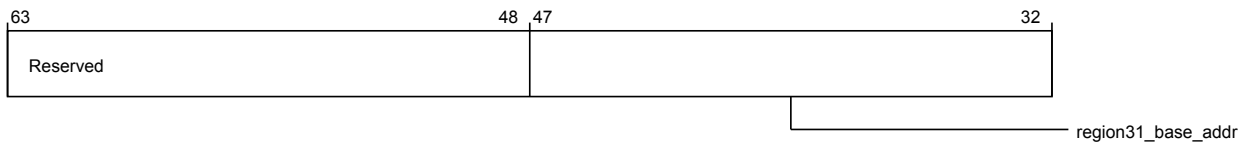


Figure 4-2244 por_mpu_por_mpu_m5_prbar31 (high)

The following table shows the por_mpu_m5_prbar31 higher register bit assignments.

Table 4-2261 por_mpu_por_mpu_m5_prbar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

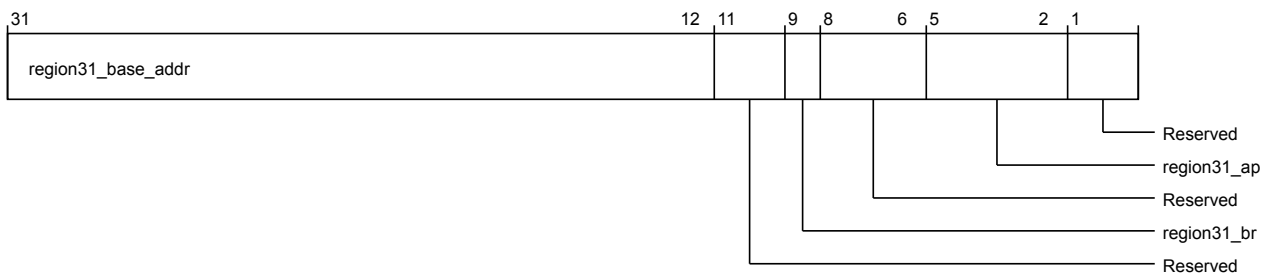


Figure 4-2245 por_mpu_por_mpu_m5_prbar31 (low)

The following table shows the por_mpu_m5_prbar31 lower register bit assignments.

Table 4-2262 por_mpu_por_mpu_m5_prbar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2262 por_mpu_por_mpu_m5_prbar31 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region31_br	Region 31 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region31_ap	Region 31 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m5_prlar31

MPU master 0 programmable limit address register 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2608

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

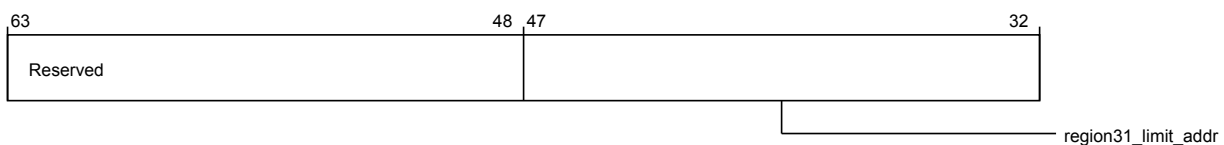


Figure 4-2246 por_mpu_por_mpu_m5_prlar31 (high)

The following table shows the por_mpu_m5_prlar31 higher register bit assignments.

Table 4-2263 por_mpu_por_mpu_m5_prlar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

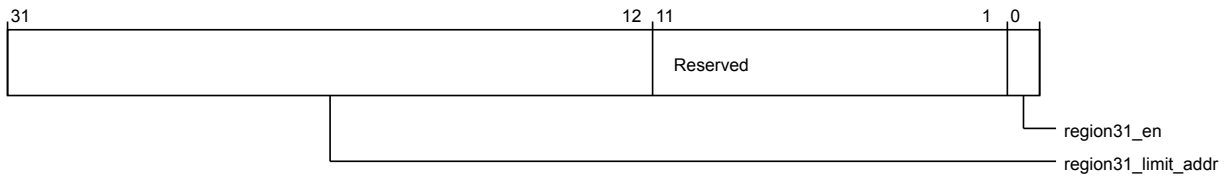


Figure 4-2247 por_mpu_por_mpu_m5_prlar31 (low)

The following table shows the por_mpu_m5_prlar31 lower register bit assignments.

Table 4-2264 por_mpu_por_mpu_m5_prlar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region31_en	Region 31 enable.	RW	1'b0

por_mpu_m6_ctl

Functions as the MPU Master 6 control register.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2800

Register reset 64'b010

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

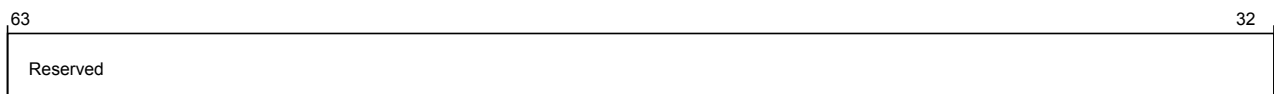


Figure 4-2248 por_mpu_por_mpu_m6_ctl (high)

The following table shows the por_mpu_m6_ctl higher register bit assignments.

Table 4-2265 por_mpu_por_mpu_m6_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

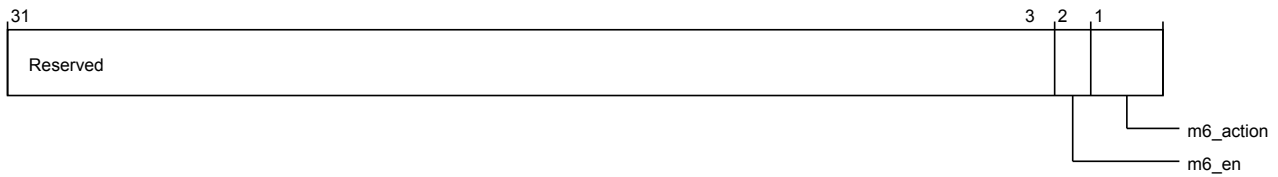


Figure 4-2249 por_mpu_por_mpu_m6_ctl (low)

The following table shows the por_mpu_m6_ctl lower register bit assignments.

Table 4-2266 por_mpu_por_mpu_m6_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	m6_en	MPU master 6 enable.	RW	1'b0
1:0	m6_action	Indicates action HN* should take if no access permission is granted 2'b00: FUSA interrupt 2'b01: Bus error to the originating bus master 2'b10: Both FUSA interrupt and bus error.	RW	2'b10

por_mpu_m6_prbar0

MPU master 0 programmable base address register 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2810

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

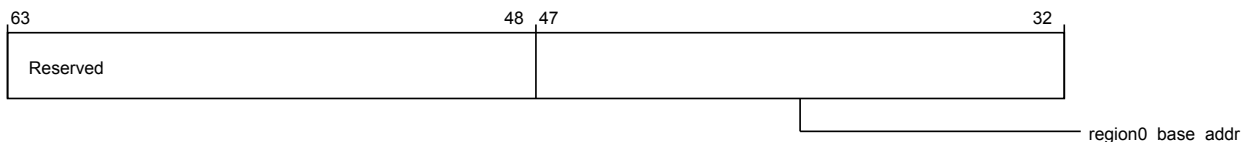


Figure 4-2250 por_mpu_por_mpu_m6_prbar0 (high)

The following table shows the por_mpu_m6_prbar0 higher register bit assignments.

Table 4-2267 por_mpu_por_mpu_m6_prbar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

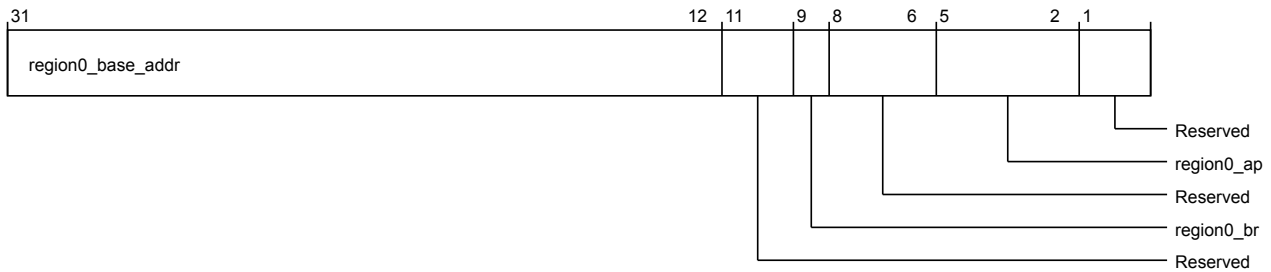


Figure 4-2251 por_mpu_por_mpu_m6_prbar0 (low)

The following table shows the por_mpu_m6_prbar0 lower register bit assignments.

Table 4-2268 por_mpu_por_mpu_m6_prbar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region0_br	Region 0 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region0_ap	Region 0 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar0

MPU master 0 programmable limit address register 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2818
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

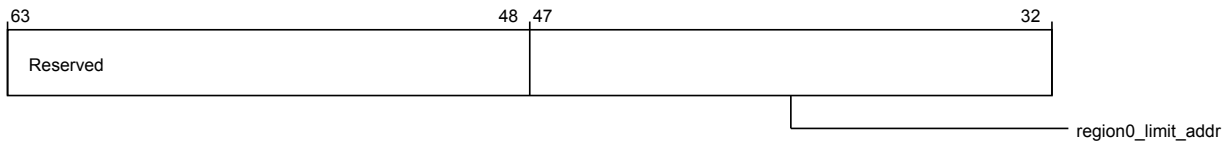


Figure 4-2252 por_mpu_por_mpu_m6_prlar0 (high)

The following table shows the por_mpu_m6_prlar0 higher register bit assignments.

Table 4-2269 por_mpu_por_mpu_m6_prlar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

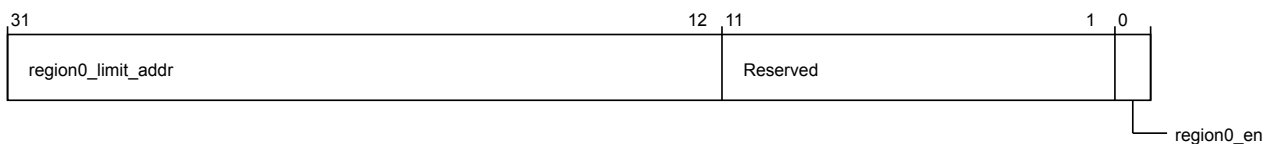


Figure 4-2253 por_mpu_por_mpu_m6_prlar0 (low)

The following table shows the por_mpu_m6_prlar0 lower register bit assignments.

Table 4-2270 por_mpu_por_mpu_m6_prlar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region0_en	Region 0 enable.	RW	1'b0

por_mpu_m6_prbar1

MPU master 0 programmable base address register 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2820
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

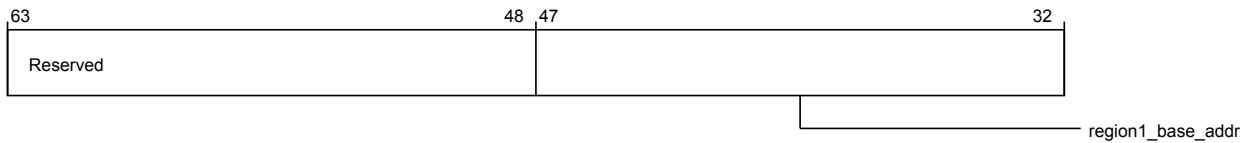


Figure 4-2254 `por_mpu_por_mpu_m6_prbar1` (high)

The following table shows the `por_mpu_m6_prbar1` higher register bit assignments.

Table 4-2271 `por_mpu_por_mpu_m6_prbar1` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region1_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

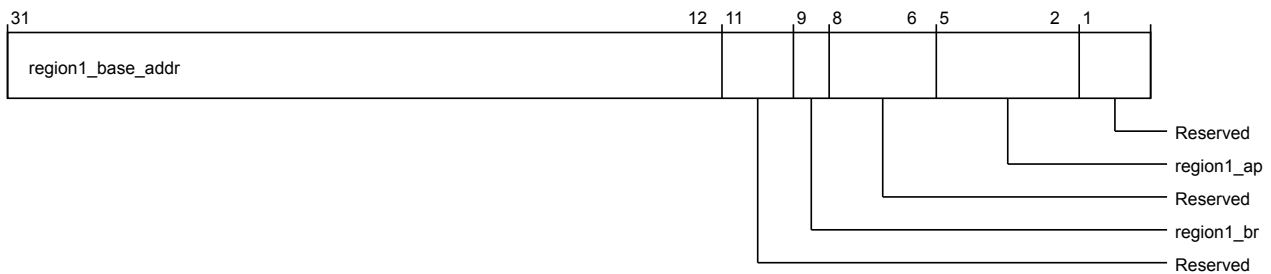


Figure 4-2255 `por_mpu_por_mpu_m6_prbar1` (low)

The following table shows the `por_mpu_m6_prbar1` lower register bit assignments.

Table 4-2272 `por_mpu_por_mpu_m6_prbar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region1_br</code>	Region 1 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-

Table 4-2272 por_mpu_por_mpu_m6_prbar1 (low) (continued)

Bits	Field name	Description	Type	Reset
5:2	region1_ap	Region 1 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar1

MPU master 0 programmable limit address register 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2828

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

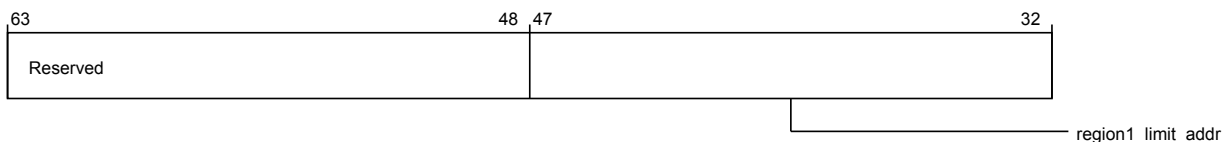


Figure 4-2256 por_mpu_por_mpu_m6_prlar1 (high)

The following table shows the por_mpu_m6_prlar1 higher register bit assignments.

Table 4-2273 por_mpu_por_mpu_m6_prlar1 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region1_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

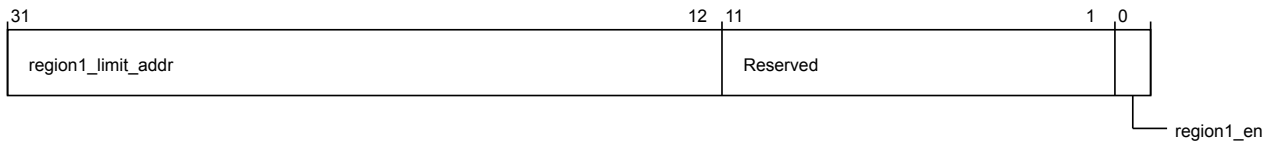


Figure 4-2257 `por_mpu_por_mpu_m6_prlar1` (low)

The following table shows the `por_mpu_m6_prlar1` lower register bit assignments.

Table 4-2274 `por_mpu_por_mpu_m6_prlar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region1_en</code>	Region 1 enable.	RW	1'b0

`por_mpu_m6_prbar2`

MPU master 0 programmable base address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2830

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

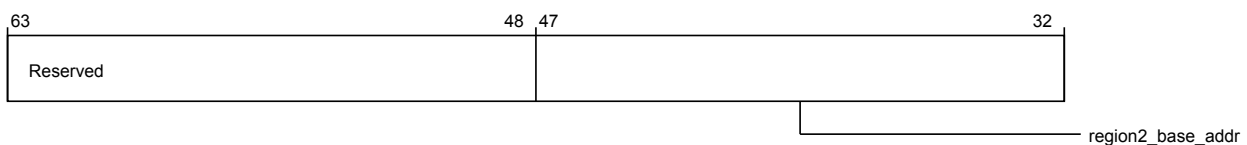


Figure 4-2258 `por_mpu_por_mpu_m6_prbar2` (high)

The following table shows the `por_mpu_m6_prbar2` higher register bit assignments.

Table 4-2275 `por_mpu_por_mpu_m6_prbar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

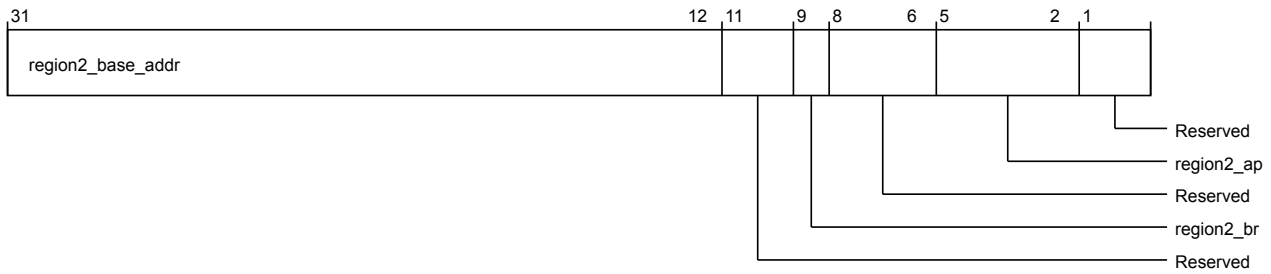


Figure 4-2259 por_mpu_por_mpu_m6_prbar2 (low)

The following table shows the por_mpu_m6_prbar2 lower register bit assignments.

Table 4-2276 por_mpu_por_mpu_m6_prbar2 (low)

Bits	Field name	Description	Type	Reset
31:12	region2_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region2_br	Region 2 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region2_ap	Region 2 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar2

MPU master 0 programmable limit address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2838

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

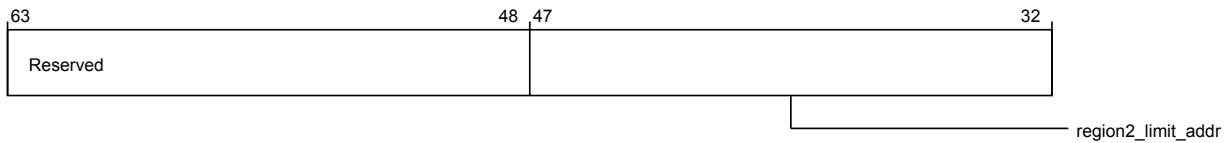


Figure 4-2260 `por_mpu_por_mpu_m6_prlar2` (high)

The following table shows the `por_mpu_m6_prlar2` higher register bit assignments.

Table 4-2277 `por_mpu_por_mpu_m6_prlar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

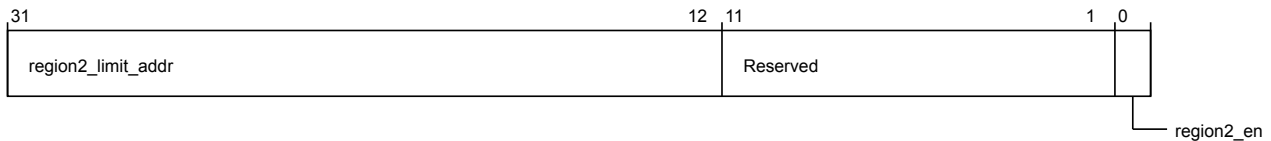


Figure 4-2261 `por_mpu_por_mpu_m6_prlar2` (low)

The following table shows the `por_mpu_m6_prlar2` lower register bit assignments.

Table 4-2278 `por_mpu_por_mpu_m6_prlar2` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region2_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region2_en</code>	Region 2 enable.	RW	1'b0

`por_mpu_m6_prbar3`

MPU master 0 programmable base address register 3.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2840
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

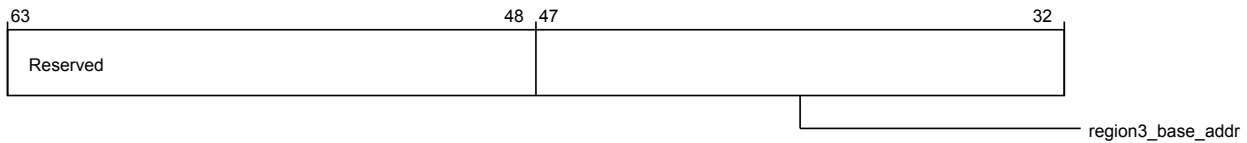


Figure 4-2262 por_mpu_por_mpu_m6_prbar3 (high)

The following table shows the por_mpu_m6_prbar3 higher register bit assignments.

Table 4-2279 por_mpu_por_mpu_m6_prbar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

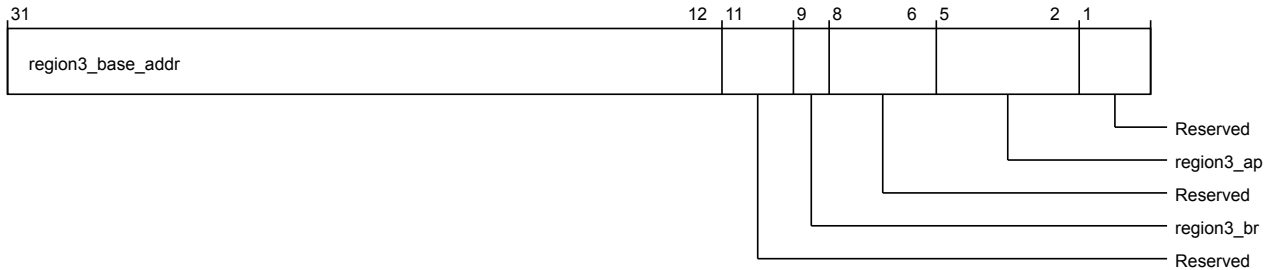


Figure 4-2263 por_mpu_por_mpu_m6_prbar3 (low)

The following table shows the por_mpu_m6_prbar3 lower register bit assignments.

Table 4-2280 por_mpu_por_mpu_m6_prbar3 (low)

Bits	Field name	Description	Type	Reset
31:12	region3_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region3_br	Region 3 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region3_ap	Region 3 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar3

MPU master 0 programmable limit address register 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2848

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

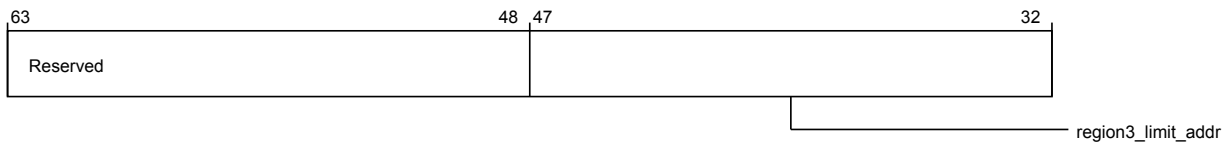


Figure 4-2264 por_mpu_por_mpu_m6_prlar3 (high)

The following table shows the por_mpu_m6_prlar3 higher register bit assignments.

Table 4-2281 por_mpu_por_mpu_m6_prlar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

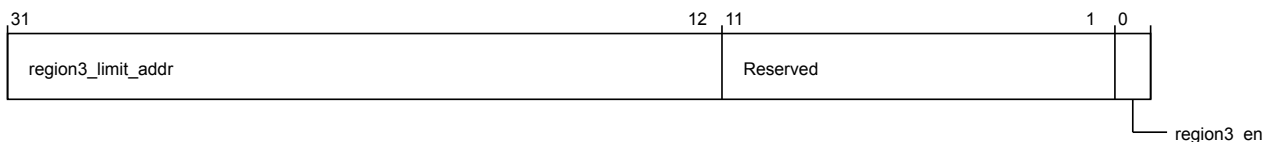


Figure 4-2265 por_mpu_por_mpu_m6_prlar3 (low)

The following table shows the por_mpu_m6_prlar3 lower register bit assignments.

Table 4-2282 por_mpu_por_mpu_m6_prlar3 (low)

Bits	Field name	Description	Type	Reset
31:12	region3_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region3_en	Region 3 enable.	RW	1'b0

por_mpu_m6_prbar4

MPU master 0 programmable base address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2850

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

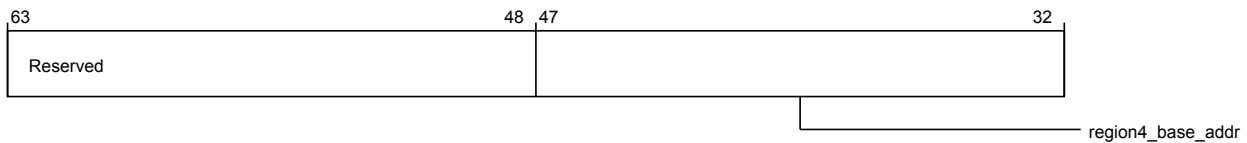


Figure 4-2266 por_mpu_por_mpu_m6_prbar4 (high)

The following table shows the por_mpu_m6_prbar4 higher register bit assignments.

Table 4-2283 por_mpu_por_mpu_m6_prbar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

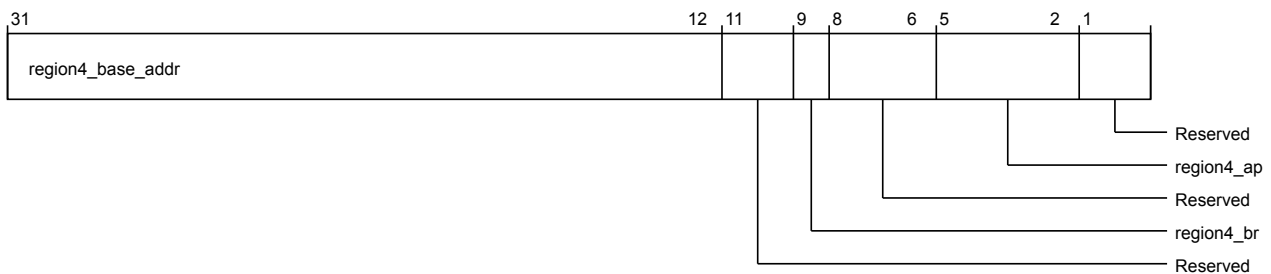


Figure 4-2267 por_mpu_por_mpu_m6_prbar4 (low)

The following table shows the por_mpu_m6_prbar4 lower register bit assignments.

Table 4-2284 por_mpu_por_mpu_m6_prbar4 (low)

Bits	Field name	Description	Type	Reset
31:12	region4_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2284 por_mpu_por_mpu_m6_prbar4 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region4_br	Region 4 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region4_ap	Region 4 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar4

MPU master 0 programmable limit address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2858

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

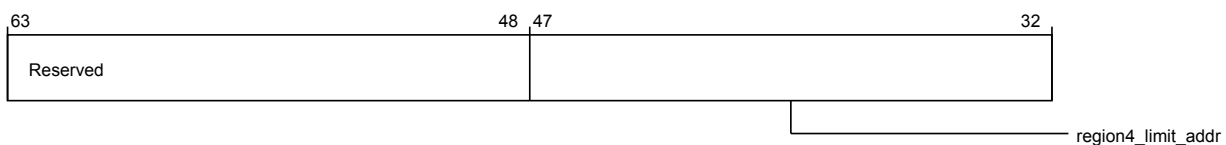


Figure 4-2268 por_mpu_por_mpu_m6_prlar4 (high)

The following table shows the por_mpu_m6_prlar4 higher register bit assignments.

Table 4-2285 por_mpu_por_mpu_m6_prlar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

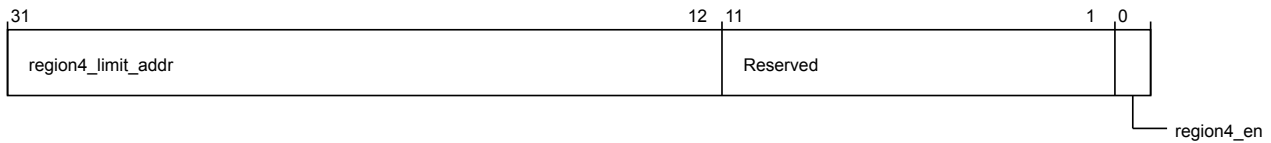


Figure 4-2269 `por_mpu_por_mpu_m6_prlar4` (low)

The following table shows the `por_mpu_m6_prlar4` lower register bit assignments.

Table 4-2286 `por_mpu_por_mpu_m6_prlar4` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region4_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region4_en</code>	Region 4 enable.	RW	1'b0

`por_mpu_m6_prbar5`

MPU master 0 programmable base address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2860

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

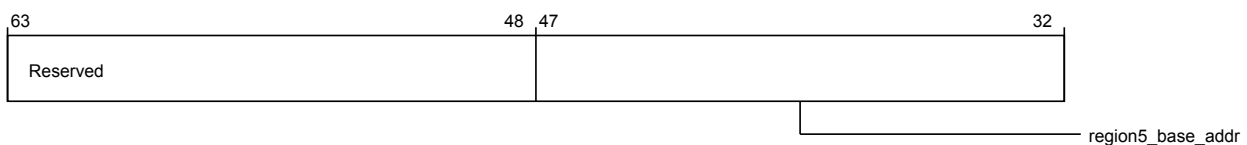


Figure 4-2270 `por_mpu_por_mpu_m6_prbar5` (high)

The following table shows the `por_mpu_m6_prbar5` higher register bit assignments.

Table 4-2287 `por_mpu_por_mpu_m6_prbar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

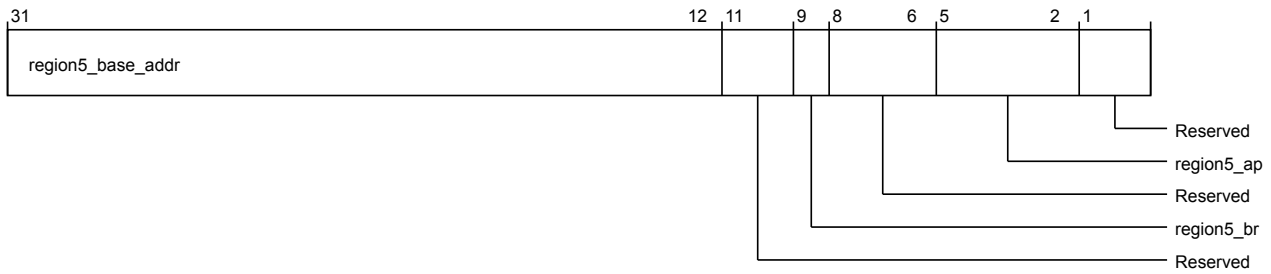


Figure 4-2271 por_mpu_por_mpu_m6_prbar5 (low)

The following table shows the por_mpu_m6_prbar5 lower register bit assignments.

Table 4-2288 por_mpu_por_mpu_m6_prbar5 (low)

Bits	Field name	Description	Type	Reset
31:12	region5_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region5_br	Region 5 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region5_ap	Region 5 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar5

MPU master 0 programmable limit address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2868

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

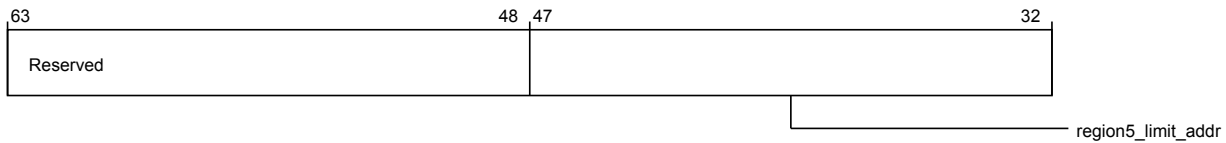


Figure 4-2272 `por_mpu_m6_prlar5` (high)

The following table shows the `por_mpu_m6_prlar5` higher register bit assignments.

Table 4-2289 `por_mpu_m6_prlar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

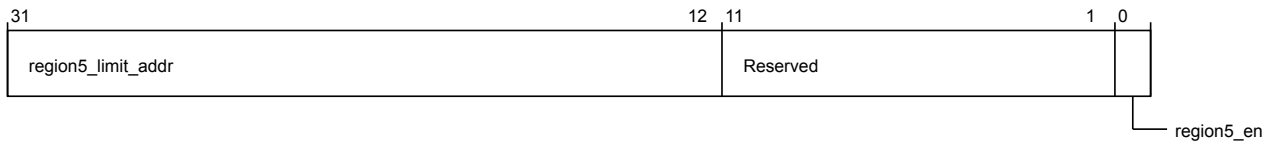


Figure 4-2273 `por_mpu_m6_prlar5` (low)

The following table shows the `por_mpu_m6_prlar5` lower register bit assignments.

Table 4-2290 `por_mpu_m6_prlar5` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region5_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region5_en</code>	Region 5 enable.	RW	1'b0

`por_mpu_m6_prbar6`

MPU master 0 programmable base address register 6.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2870
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

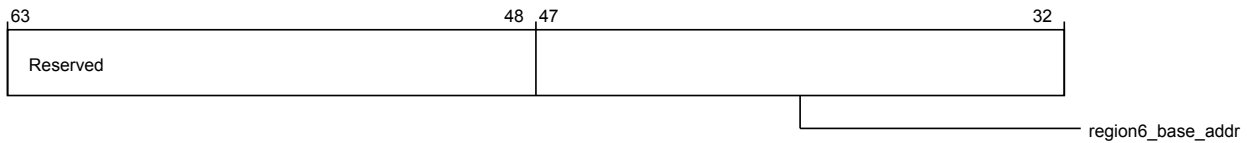


Figure 4-2274 `por_mpu_por_mpu_m6_prbar6` (high)

The following table shows the `por_mpu_m6_prbar6` higher register bit assignments.

Table 4-2291 `por_mpu_por_mpu_m6_prbar6` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

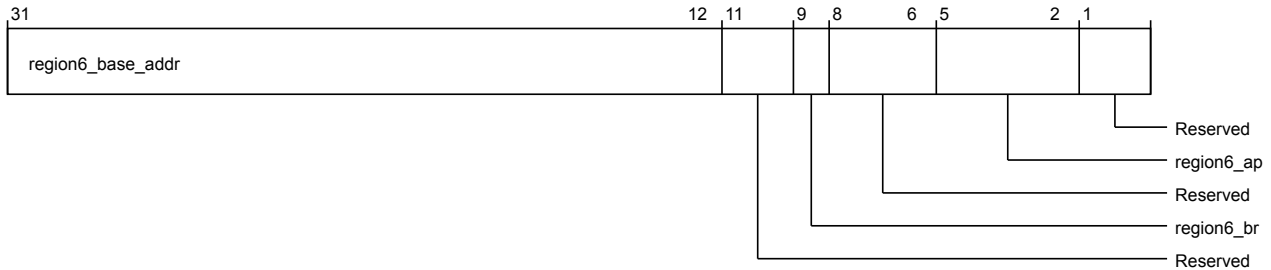


Figure 4-2275 `por_mpu_por_mpu_m6_prbar6` (low)

The following table shows the `por_mpu_m6_prbar6` lower register bit assignments.

Table 4-2292 `por_mpu_por_mpu_m6_prbar6` (low)

Bits	Field name	Description	Type	Reset
31:12	region6_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region6_br	Region 6 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region6_ap	Region 6 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar6

MPU master 0 programmable limit address register 6.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2878

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

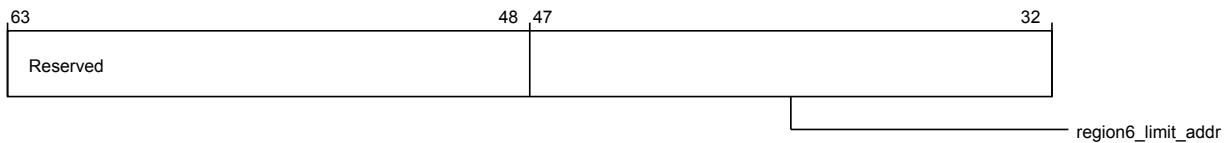


Figure 4-2276 por_mpu_por_mpu_m6_prlar6 (high)

The following table shows the por_mpu_m6_prlar6 higher register bit assignments.

Table 4-2293 por_mpu_por_mpu_m6_prlar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

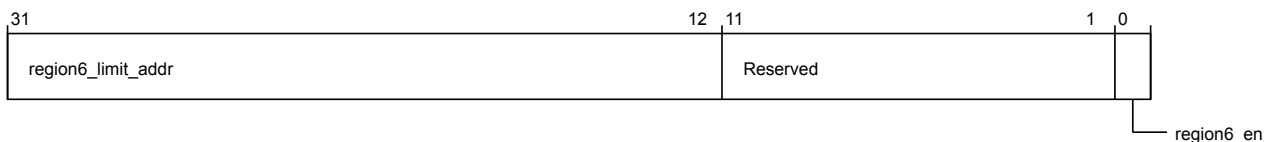


Figure 4-2277 por_mpu_por_mpu_m6_prlar6 (low)

The following table shows the por_mpu_m6_prlar6 lower register bit assignments.

Table 4-2294 por_mpu_por_mpu_m6_prlar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region6_en	Region 6 enable.	RW	1'b0

por_mpu_m6_prbar7

MPU master 0 programmable base address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2880

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

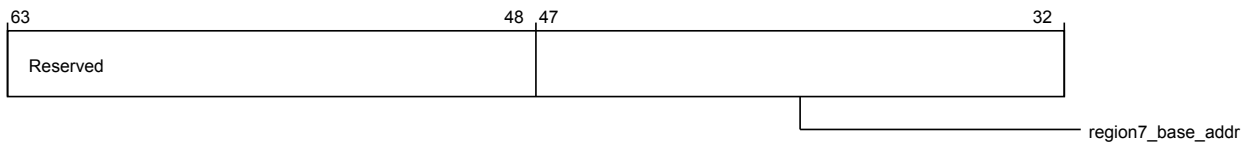


Figure 4-2278 `por_mpu_m6_prbar7` (high)

The following table shows the `por_mpu_m6_prbar7` higher register bit assignments.

Table 4-2295 `por_mpu_m6_prbar7` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

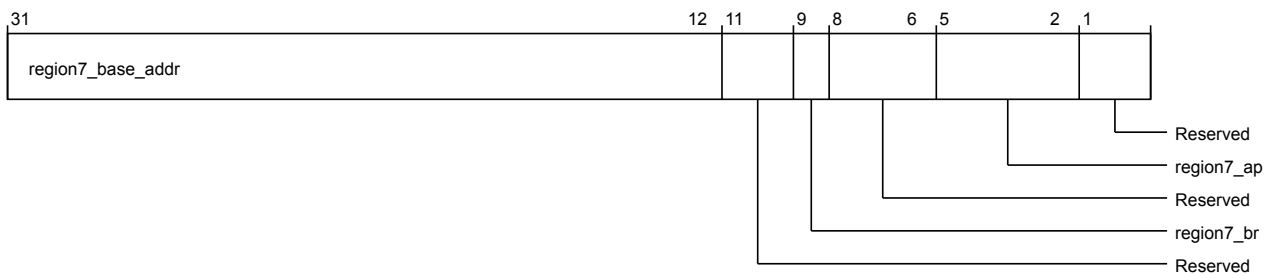


Figure 4-2279 `por_mpu_m6_prbar7` (low)

The following table shows the `por_mpu_m6_prbar7` lower register bit assignments.

Table 4-2296 `por_mpu_m6_prbar7` (low)

Bits	Field name	Description	Type	Reset
31:12	region7_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2296 por_mpu_por_mpu_m6_prbar7 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region7_br	Region 7 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region7_ap	Region 7 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar7

MPU master 0 programmable limit address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2888

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

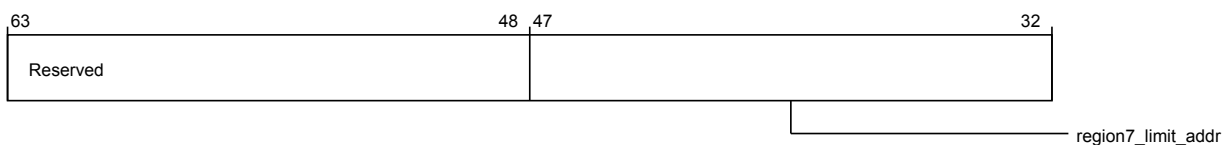


Figure 4-2280 por_mpu_por_mpu_m6_prlar7 (high)

The following table shows the por_mpu_m6_prlar7 higher register bit assignments.

Table 4-2297 por_mpu_por_mpu_m6_prlar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

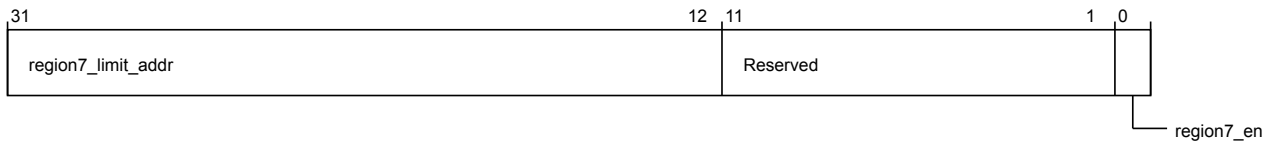


Figure 4-2281 por_mpu_por_mpu_m6_prlar7 (low)

The following table shows the por_mpu_m6_prlar7 lower register bit assignments.

Table 4-2298 por_mpu_por_mpu_m6_prlar7 (low)

Bits	Field name	Description	Type	Reset
31:12	region7_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region7_en	Region 7 enable.	RW	1'b0

por_mpu_m6_prbar8

MPU master 0 programmable base address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2890

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

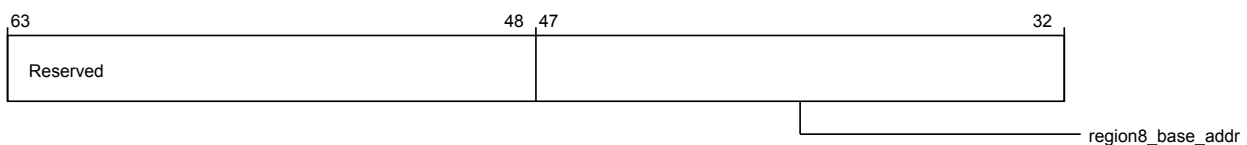


Figure 4-2282 por_mpu_por_mpu_m6_prbar8 (high)

The following table shows the por_mpu_m6_prbar8 higher register bit assignments.

Table 4-2299 por_mpu_por_mpu_m6_prbar8 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region8_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

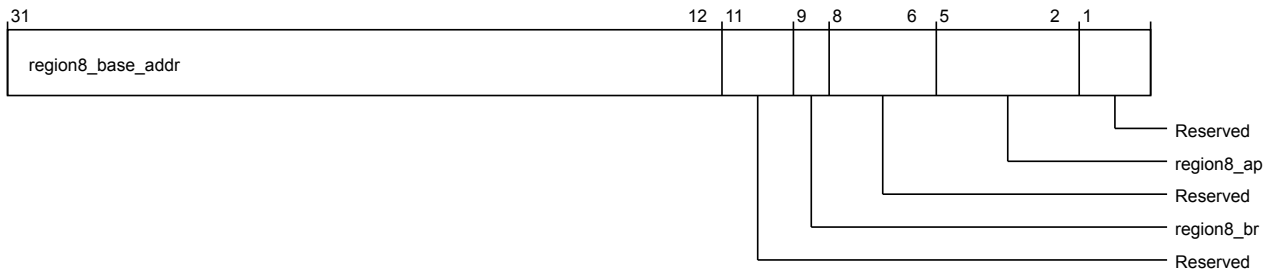


Figure 4-2283 por_mpu_por_mpu_m6_prbar8 (low)

The following table shows the por_mpu_m6_prbar8 lower register bit assignments.

Table 4-2300 por_mpu_por_mpu_m6_prbar8 (low)

Bits	Field name	Description	Type	Reset
31:12	region8_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region8_br	Region 8 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region8_ap	Region 8 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar8

MPU master 0 programmable limit address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2898

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

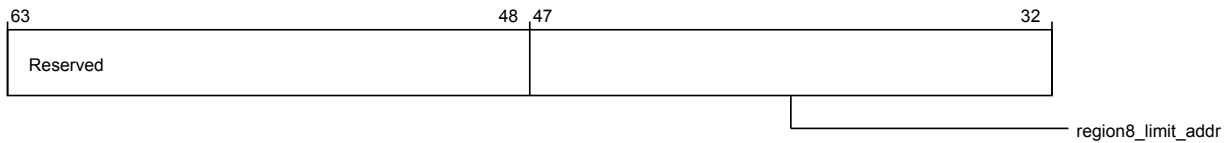


Figure 4-2284 `por_mpu_m6_prlar8` (high)

The following table shows the `por_mpu_m6_prlar8` higher register bit assignments.

Table 4-2301 `por_mpu_m6_prlar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

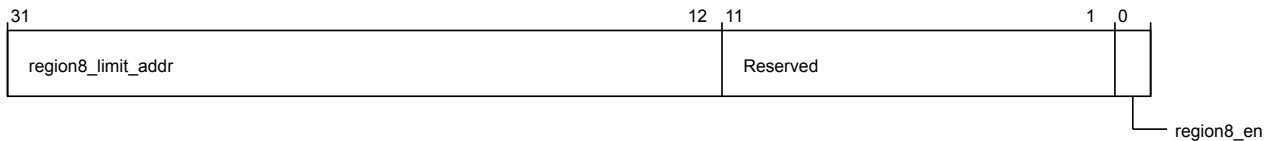


Figure 4-2285 `por_mpu_m6_prlar8` (low)

The following table shows the `por_mpu_m6_prlar8` lower register bit assignments.

Table 4-2302 `por_mpu_m6_prlar8` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region8_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region8_en</code>	Region 8 enable.	RW	1'b0

`por_mpu_m6_prbar9`

MPU master 0 programmable base address register 9.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h28A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

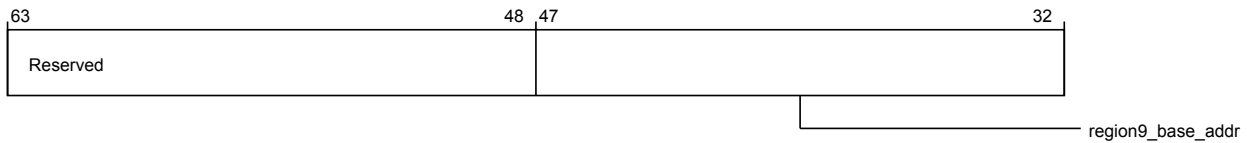


Figure 4-2286 `por_mpu_por_mpu_m6_prbar9` (high)

The following table shows the `por_mpu_m6_prbar9` higher register bit assignments.

Table 4-2303 `por_mpu_por_mpu_m6_prbar9` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region9_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

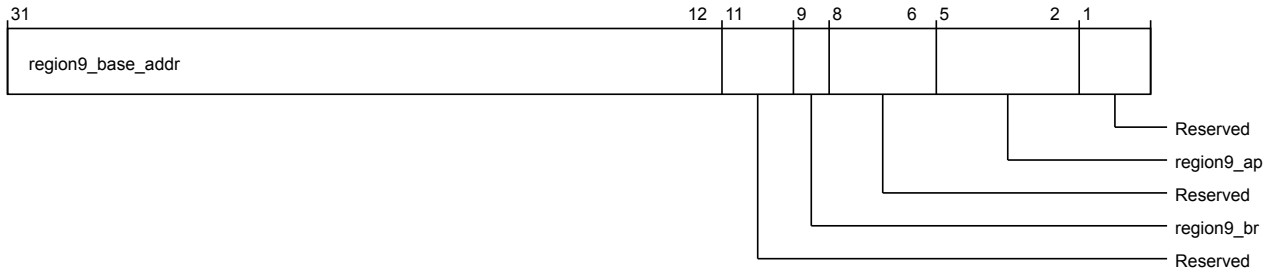


Figure 4-2287 `por_mpu_por_mpu_m6_prbar9` (low)

The following table shows the `por_mpu_m6_prbar9` lower register bit assignments.

Table 4-2304 `por_mpu_por_mpu_m6_prbar9` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region9_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region9_br</code>	Region 9 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region9_ap</code>	Region 9 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar9

MPU master 0 programmable limit address register 9.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h28A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

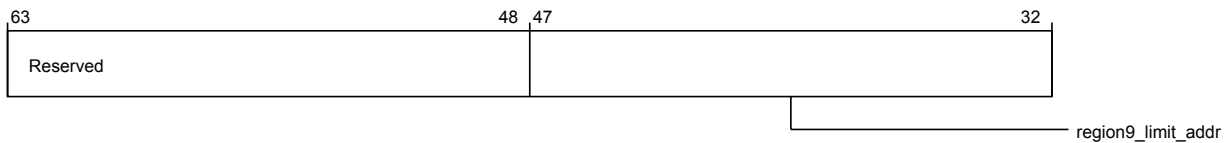


Figure 4-2288 por_mpu_por_mpu_m6_prlar9 (high)

The following table shows the por_mpu_m6_prlar9 higher register bit assignments.

Table 4-2305 por_mpu_por_mpu_m6_prlar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

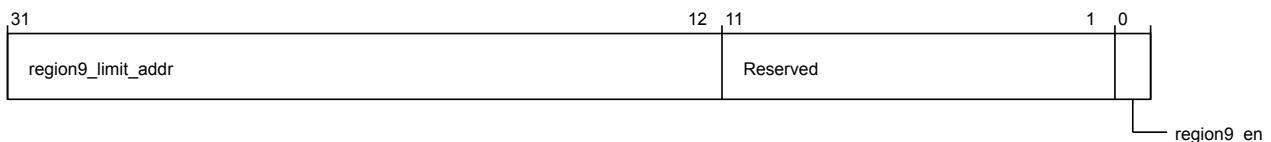


Figure 4-2289 por_mpu_por_mpu_m6_prlar9 (low)

The following table shows the por_mpu_m6_prlar9 lower register bit assignments.

Table 4-2306 por_mpu_por_mpu_m6_prlar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region9_en	Region 9 enable.	RW	1'b0

por_mpu_m6_prbar10

MPU master 0 programmable base address register 10.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h28B0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

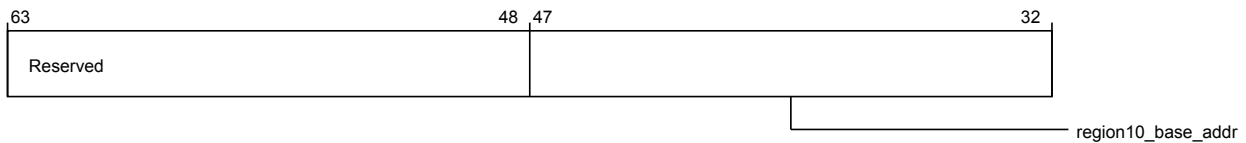


Figure 4-2290 por_mpu_por_mpu_m6_prbar10 (high)

The following table shows the por_mpu_m6_prbar10 higher register bit assignments.

Table 4-2307 por_mpu_por_mpu_m6_prbar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

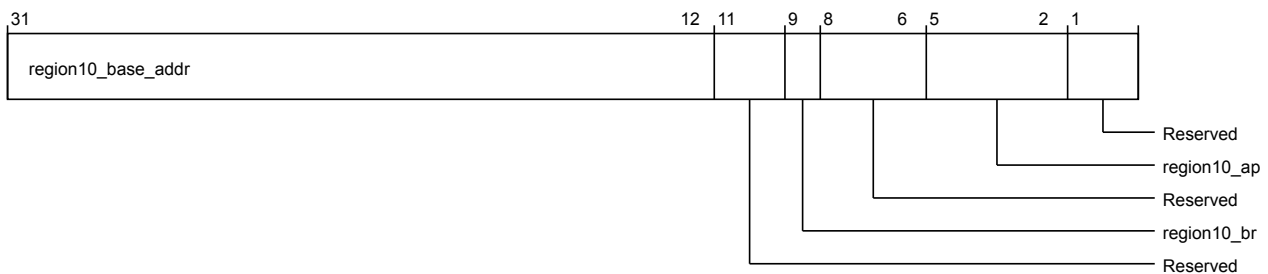


Figure 4-2291 por_mpu_por_mpu_m6_prbar10 (low)

The following table shows the por_mpu_m6_prbar10 lower register bit assignments.

Table 4-2308 por_mpu_por_mpu_m6_prbar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2308 `por_mpu_por_mpu_m6_prbar10` (low) (continued)

Bits	Field name	Description	Type	Reset
9	region10_br	Region 10 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region10_ap	Region 10 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m6_prlar10`

MPU master 0 programmable limit address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h28B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

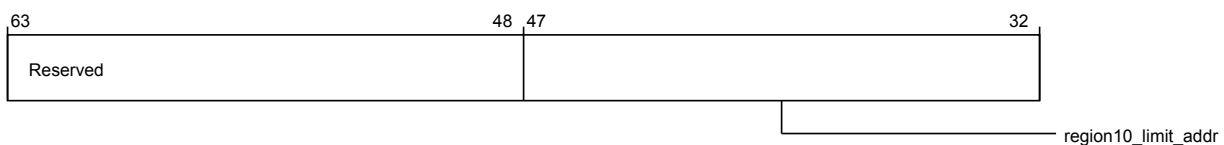


Figure 4-2292 `por_mpu_por_mpu_m6_prlar10` (high)

The following table shows the `por_mpu_m6_prlar10` higher register bit assignments.

Table 4-2309 `por_mpu_por_mpu_m6_prlar10` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

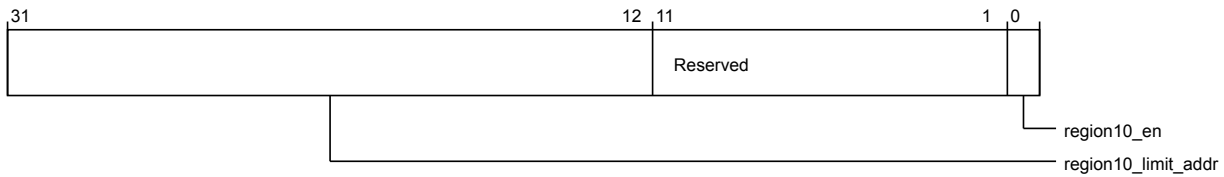


Figure 4-2293 `por_mpu_por_mpu_m6_prlar10` (low)

The following table shows the `por_mpu_m6_prlar10` lower register bit assignments.

Table 4-2310 `por_mpu_por_mpu_m6_prlar10` (low)

Bits	Field name	Description	Type	Reset
31:12	region10_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region10_en	Region 10 enable.	RW	1'b0

`por_mpu_m6_prbar11`

MPU master 0 programmable base address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h28C0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

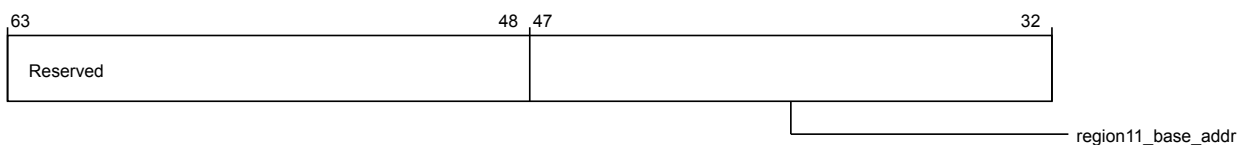


Figure 4-2294 `por_mpu_por_mpu_m6_prbar11` (high)

The following table shows the `por_mpu_m6_prbar11` higher register bit assignments.

Table 4-2311 `por_mpu_por_mpu_m6_prbar11` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

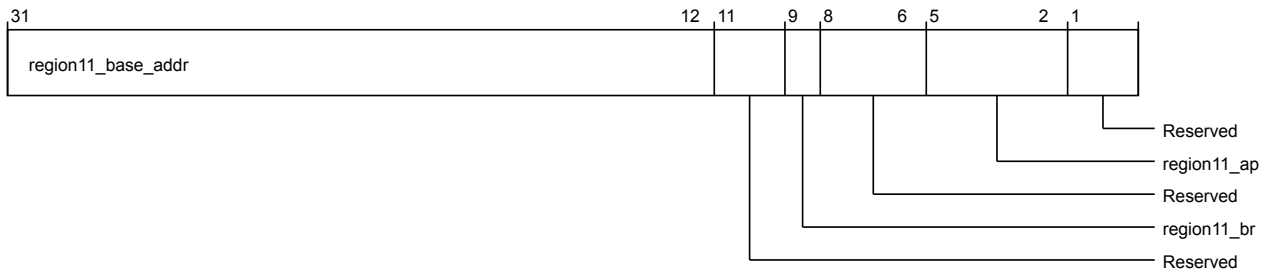


Figure 4-2295 `por_mpu_por_mpu_m6_prbar11` (low)

The following table shows the `por_mpu_m6_prbar11` lower register bit assignments.

Table 4-2312 `por_mpu_por_mpu_m6_prbar11` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region11_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region11_br</code>	Region 11 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region11_ap</code>	Region 11 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m6_prlar11`

MPU master 0 programmable limit address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h28C8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

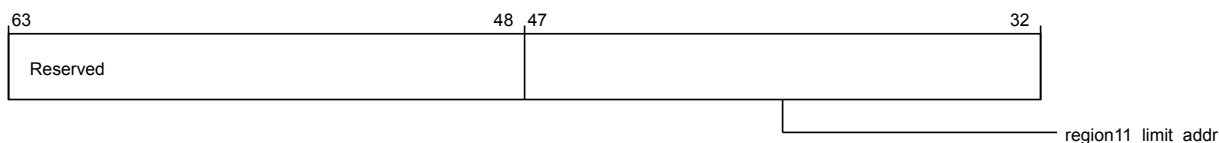


Figure 4-2296 `por_mpu_m6_prlar11` (high)

The following table shows the `por_mpu_m6_prlar11` higher register bit assignments.

Table 4-2313 `por_mpu_m6_prlar11` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

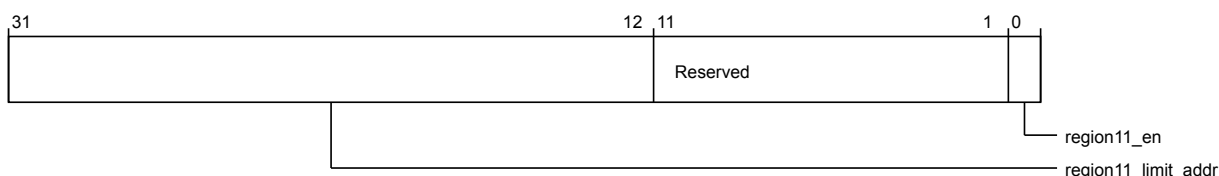


Figure 4-2297 `por_mpu_m6_prlar11` (low)

The following table shows the `por_mpu_m6_prlar11` lower register bit assignments.

Table 4-2314 `por_mpu_m6_prlar11` (low)

Bits	Field name	Description	Type	Reset
31:12	region11_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region11_en	Region 11 enable.	RW	1'b0

`por_mpu_m6_prbar12`

MPU master 0 programmable base address register 12.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h28D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

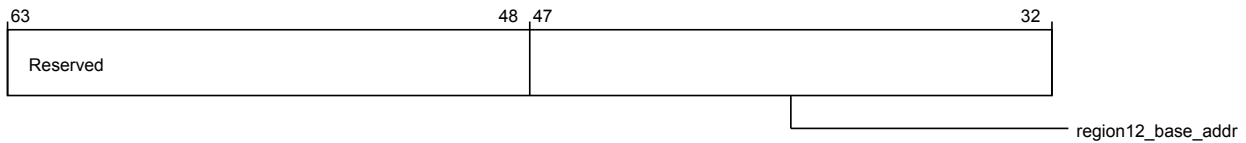


Figure 4-2298 `por_mpu_por_mpu_m6_prbar12` (high)

The following table shows the `por_mpu_m6_prbar12` higher register bit assignments.

Table 4-2315 `por_mpu_por_mpu_m6_prbar12` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

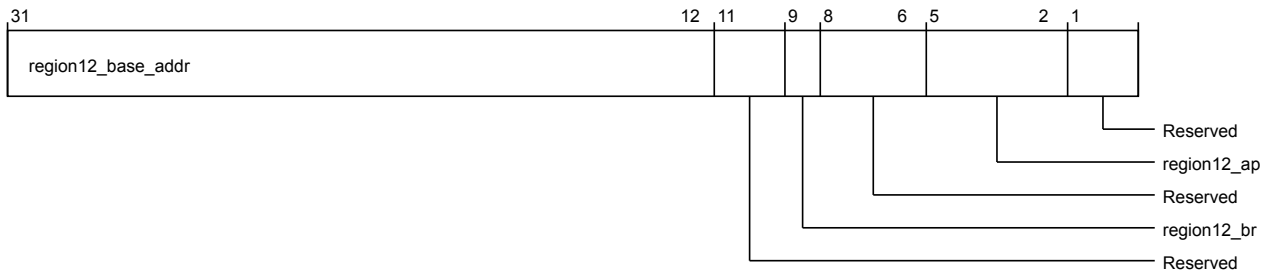


Figure 4-2299 `por_mpu_por_mpu_m6_prbar12` (low)

The following table shows the `por_mpu_m6_prbar12` lower register bit assignments.

Table 4-2316 `por_mpu_por_mpu_m6_prbar12` (low)

Bits	Field name	Description	Type	Reset
31:12	region12_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region12_br	Region 12 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region12_ap	Region 12 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar12

MPU master 0 programmable limit address register 12.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h28D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

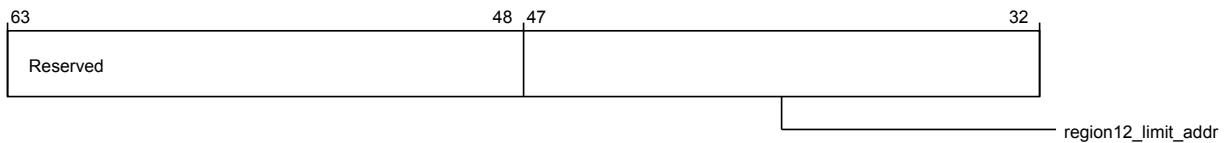


Figure 4-2300 por_mpu_por_mpu_m6_prlar12 (high)

The following table shows the por_mpu_m6_prlar12 higher register bit assignments.

Table 4-2317 por_mpu_por_mpu_m6_prlar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

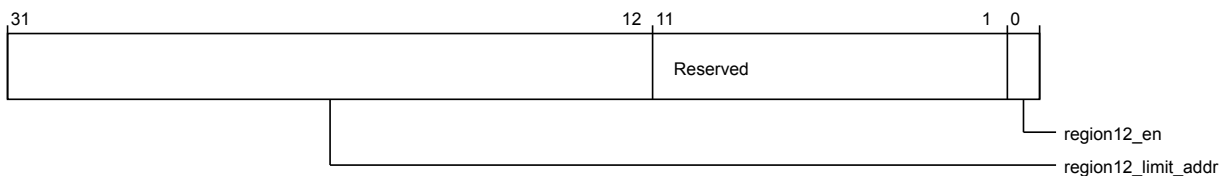


Figure 4-2301 por_mpu_por_mpu_m6_prlar12 (low)

The following table shows the por_mpu_m6_prlar12 lower register bit assignments.

Table 4-2318 por_mpu_por_mpu_m6_prlar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region12_en	Region 12 enable.	RW	1'b0

por_mpu_m6_prbar13

MPU master 0 programmable base address register 13.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h28E0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

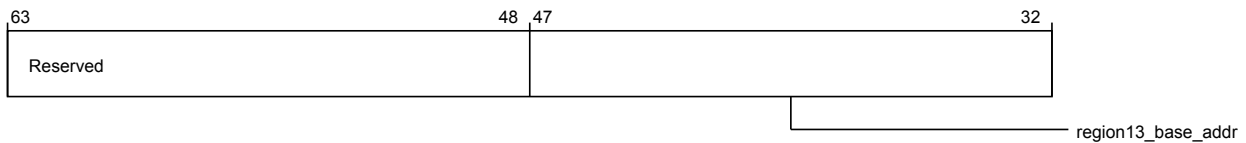


Figure 4-2302 por_mpu_por_mpu_m6_prbar13 (high)

The following table shows the por_mpu_m6_prbar13 higher register bit assignments.

Table 4-2319 por_mpu_por_mpu_m6_prbar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

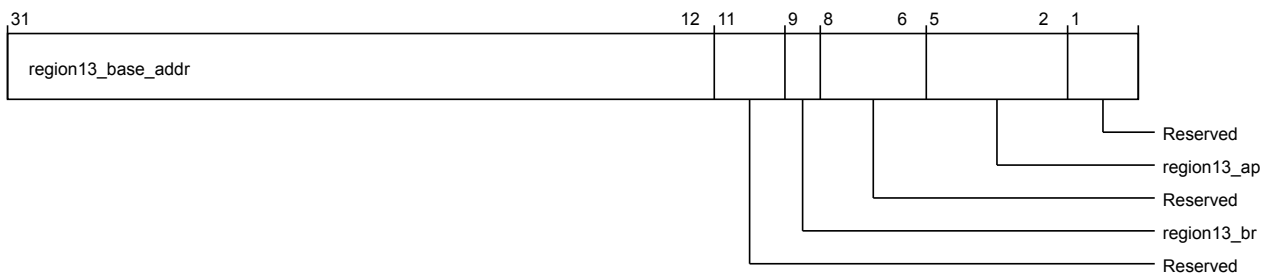


Figure 4-2303 por_mpu_por_mpu_m6_prbar13 (low)

The following table shows the por_mpu_m6_prbar13 lower register bit assignments.

Table 4-2320 por_mpu_por_mpu_m6_prbar13 (low)

Bits	Field name	Description	Type	Reset
31:12	region13_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2320 por_mpu_por_mpu_m6_prbar13 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region13_br	Region 13 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region13_ap	Region 13 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar13

MPU master 0 programmable limit address register 13.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h28E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

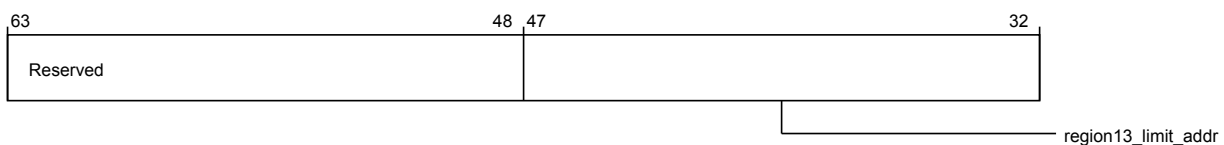


Figure 4-2304 por_mpu_por_mpu_m6_prlar13 (high)

The following table shows the por_mpu_m6_prlar13 higher register bit assignments.

Table 4-2321 por_mpu_por_mpu_m6_prlar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

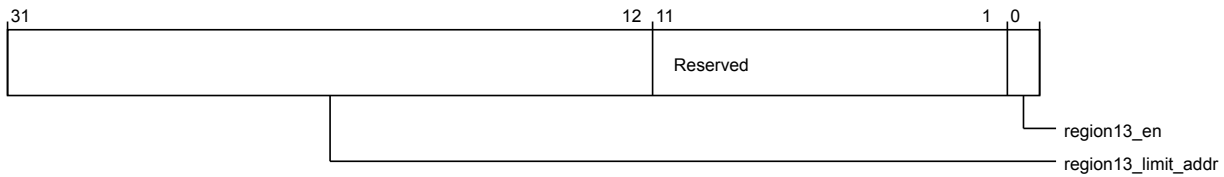


Figure 4-2305 `por_mpu_por_mpu_m6_prlar13` (low)

The following table shows the `por_mpu_m6_prlar13` lower register bit assignments.

Table 4-2322 `por_mpu_por_mpu_m6_prlar13` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region13_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region13_en</code>	Region 13 enable.	RW	1'b0

`por_mpu_m6_prbar14`

MPU master 0 programmable base address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h28F0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

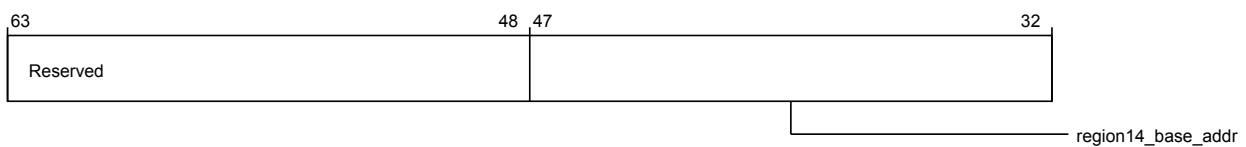


Figure 4-2306 `por_mpu_por_mpu_m6_prbar14` (high)

The following table shows the `por_mpu_m6_prbar14` higher register bit assignments.

Table 4-2323 `por_mpu_por_mpu_m6_prbar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region14_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

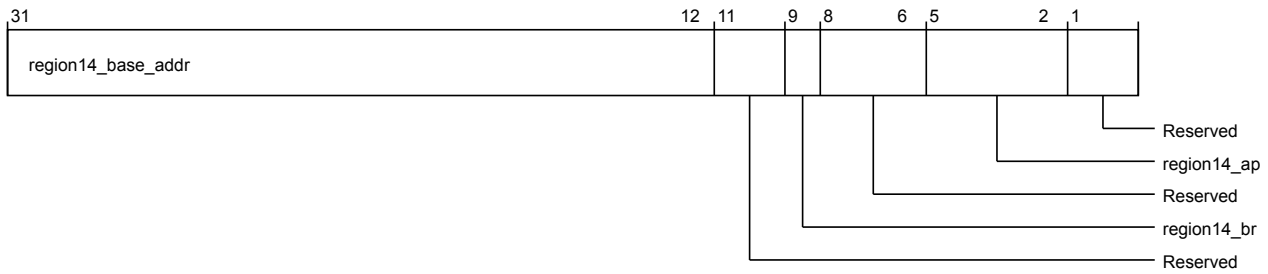


Figure 4-2307 por_mpu_por_mpu_m6_prbar14 (low)

The following table shows the por_mpu_m6_prbar14 lower register bit assignments.

Table 4-2324 por_mpu_por_mpu_m6_prbar14 (low)

Bits	Field name	Description	Type	Reset
31:12	region14_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region14_br	Region 14 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region14_ap	Region 14 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar14

MPU master 0 programmable limit address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h28F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

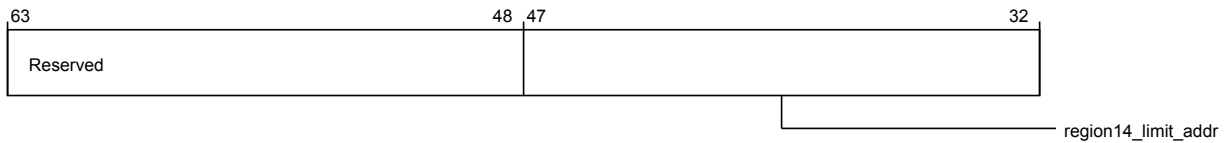


Figure 4-2308 `por_mpu_m6_prlar14` (high)

The following table shows the `por_mpu_m6_prlar14` higher register bit assignments.

Table 4-2325 `por_mpu_m6_prlar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region14_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

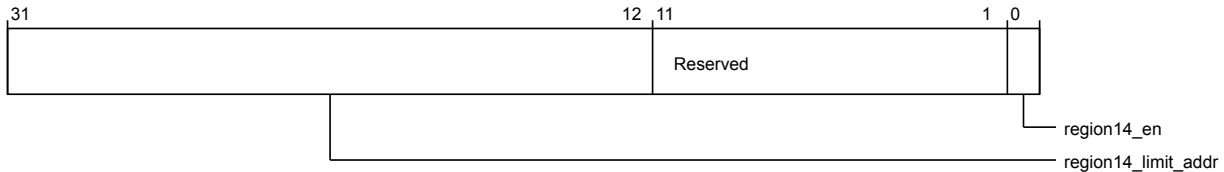


Figure 4-2309 `por_mpu_m6_prlar14` (low)

The following table shows the `por_mpu_m6_prlar14` lower register bit assignments.

Table 4-2326 `por_mpu_m6_prlar14` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region14_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region14_en</code>	Region 14 enable.	RW	1'b0

`por_mpu_m6_prbar15`

MPU master 0 programmable base address register 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2900
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

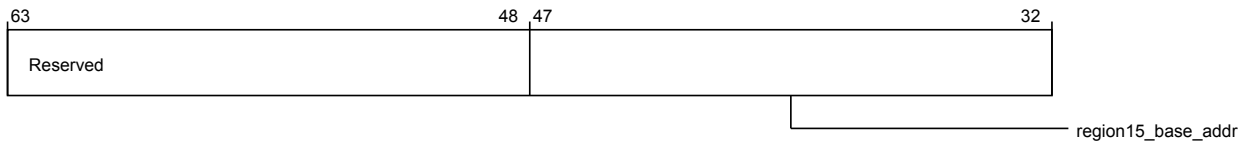


Figure 4-2310 por_mpu_por_mpu_m6_prbar15 (high)

The following table shows the por_mpu_m6_prbar15 higher register bit assignments.

Table 4-2327 por_mpu_por_mpu_m6_prbar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

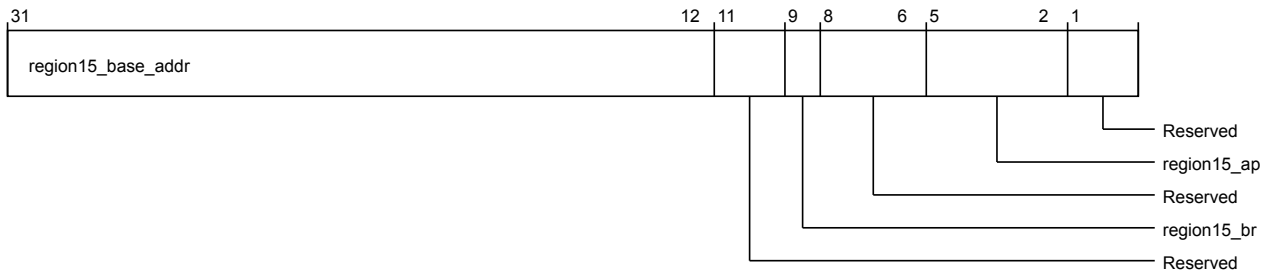


Figure 4-2311 por_mpu_por_mpu_m6_prbar15 (low)

The following table shows the por_mpu_m6_prbar15 lower register bit assignments.

Table 4-2328 por_mpu_por_mpu_m6_prbar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region15_br	Region 15 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region15_ap	Region 15 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar15

MPU master 0 programmable limit address register 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2908

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

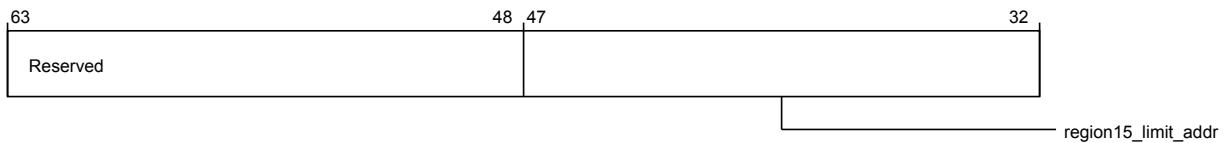


Figure 4-2312 por_mpu_por_mpu_m6_prlar15 (high)

The following table shows the por_mpu_m6_prlar15 higher register bit assignments.

Table 4-2329 por_mpu_por_mpu_m6_prlar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

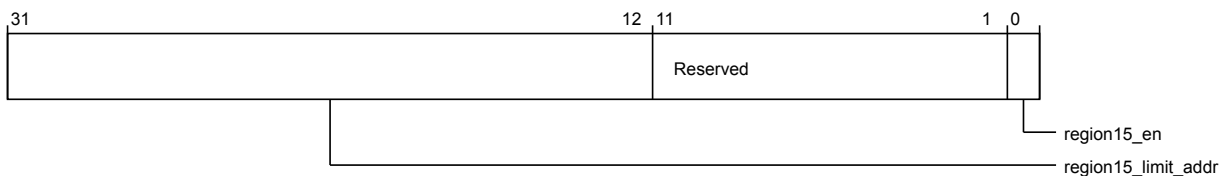


Figure 4-2313 por_mpu_por_mpu_m6_prlar15 (low)

The following table shows the por_mpu_m6_prlar15 lower register bit assignments.

Table 4-2330 por_mpu_por_mpu_m6_prlar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region15_en	Region 15 enable.	RW	1'b0

por_mpu_m6_prbar16

MPU master 0 programmable base address register 16.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2910
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

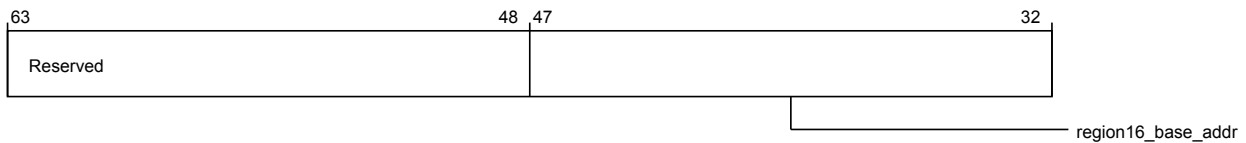


Figure 4-2314 por_mpu_por_mpu_m6_prbar16 (high)

The following table shows the por_mpu_m6_prbar16 higher register bit assignments.

Table 4-2331 por_mpu_por_mpu_m6_prbar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

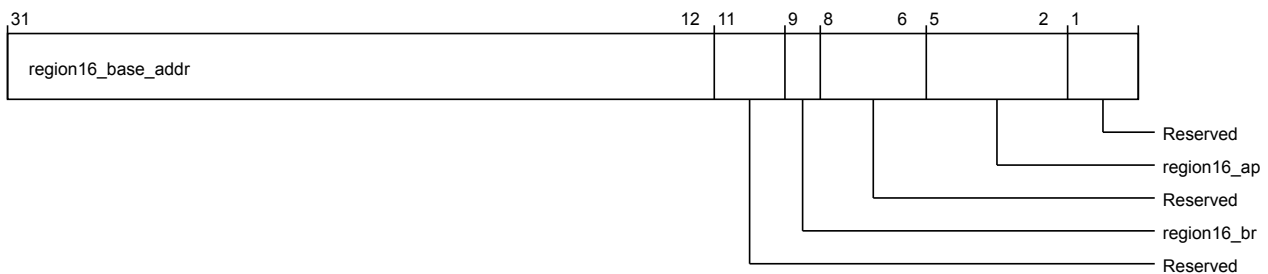


Figure 4-2315 por_mpu_por_mpu_m6_prbar16 (low)

The following table shows the por_mpu_m6_prbar16 lower register bit assignments.

Table 4-2332 por_mpu_por_mpu_m6_prbar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2332 por_mpu_por_mpu_m6_prbar16 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region16_br	Region 16 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region16_ap	Region 16 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar16

MPU master 0 programmable limit address register 16.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2918

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

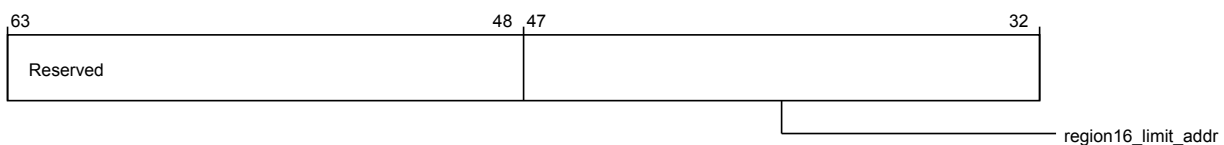


Figure 4-2316 por_mpu_por_mpu_m6_prlar16 (high)

The following table shows the por_mpu_m6_prlar16 higher register bit assignments.

Table 4-2333 por_mpu_por_mpu_m6_prlar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

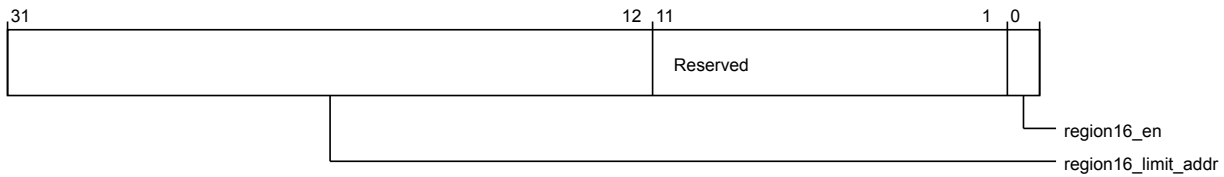


Figure 4-2317 `por_mpu_por_mpu_m6_prlar16` (low)

The following table shows the `por_mpu_m6_prlar16` lower register bit assignments.

Table 4-2334 `por_mpu_por_mpu_m6_prlar16` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region16_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region16_en</code>	Region 16 enable.	RW	1'b0

`por_mpu_m6_prbar17`

MPU master 0 programmable base address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2920

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

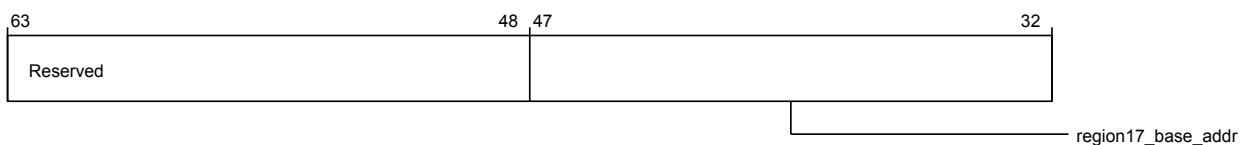


Figure 4-2318 `por_mpu_por_mpu_m6_prbar17` (high)

The following table shows the `por_mpu_m6_prbar17` higher register bit assignments.

Table 4-2335 `por_mpu_por_mpu_m6_prbar17` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region17_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

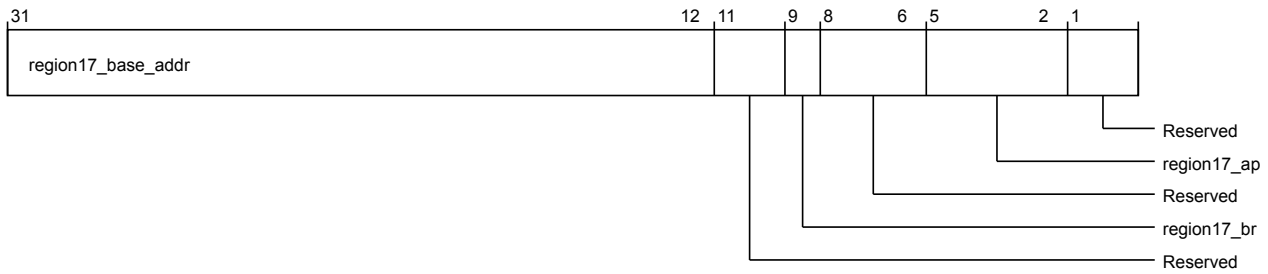


Figure 4-2319 `por_mpu_por_mpu_m6_prbar17` (low)

The following table shows the `por_mpu_m6_prbar17` lower register bit assignments.

Table 4-2336 `por_mpu_por_mpu_m6_prbar17` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region17_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region17_br</code>	Region 17 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region17_ap</code>	Region 17 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m6_prlar17`

MPU master 0 programmable limit address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2928

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

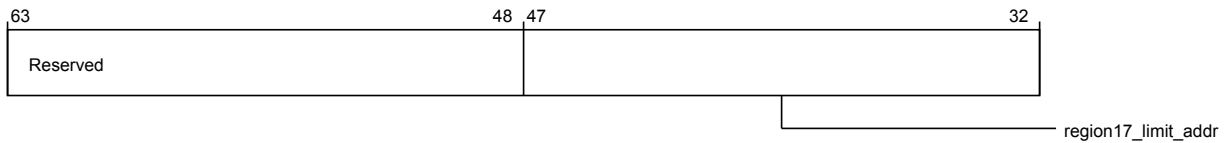


Figure 4-2320 `por_mpu_m6_prlar17` (high)

The following table shows the `por_mpu_m6_prlar17` higher register bit assignments.

Table 4-2337 `por_mpu_m6_prlar17` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

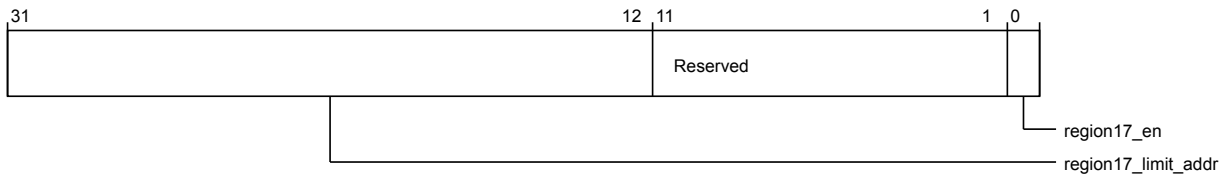


Figure 4-2321 `por_mpu_m6_prlar17` (low)

The following table shows the `por_mpu_m6_prlar17` lower register bit assignments.

Table 4-2338 `por_mpu_m6_prlar17` (low)

Bits	Field name	Description	Type	Reset
31:12	region17_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region17_en	Region 17 enable.	RW	1'b0

`por_mpu_m6_prbar18`

MPU master 0 programmable base address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2930
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

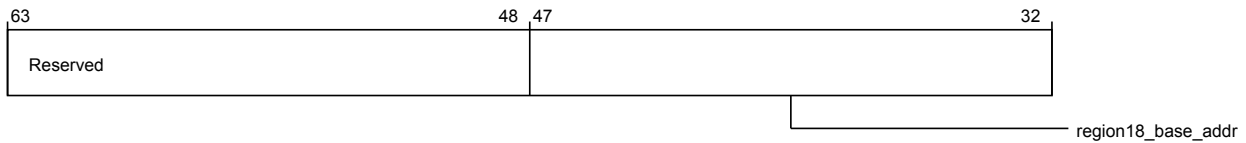


Figure 4-2322 `por_mpu_por_mpu_m6_prbar18` (high)

The following table shows the `por_mpu_m6_prbar18` higher register bit assignments.

Table 4-2339 `por_mpu_por_mpu_m6_prbar18` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_base_addr	Bits [47:32] of base address of the range.	RW	61'b0

The following image shows the lower register bit assignments.

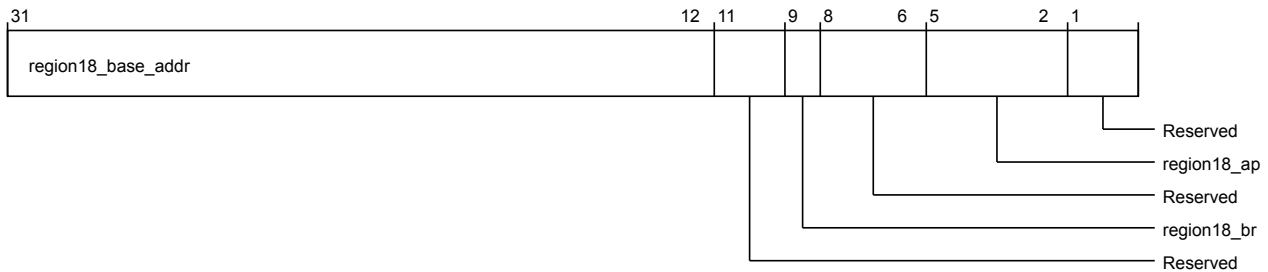


Figure 4-2323 `por_mpu_por_mpu_m6_prbar18` (low)

The following table shows the `por_mpu_m6_prbar18` lower register bit assignments.

Table 4-2340 `por_mpu_por_mpu_m6_prbar18` (low)

Bits	Field name	Description	Type	Reset
31:12	region18_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region18_br	Region 18 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region18_ap	Region 18 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar18

MPU master 0 programmable limit address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2938
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

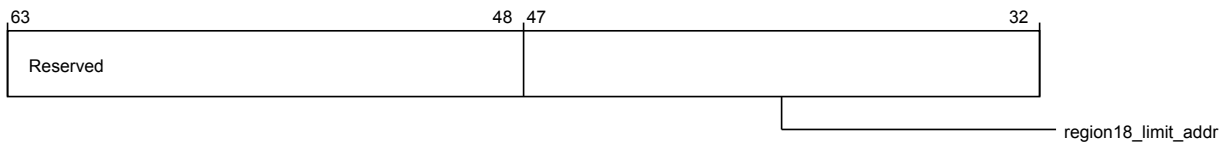


Figure 4-2324 por_mpu_por_mpu_m6_prlar18 (high)

The following table shows the por_mpu_m6_prlar18 higher register bit assignments.

Table 4-2341 por_mpu_por_mpu_m6_prlar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

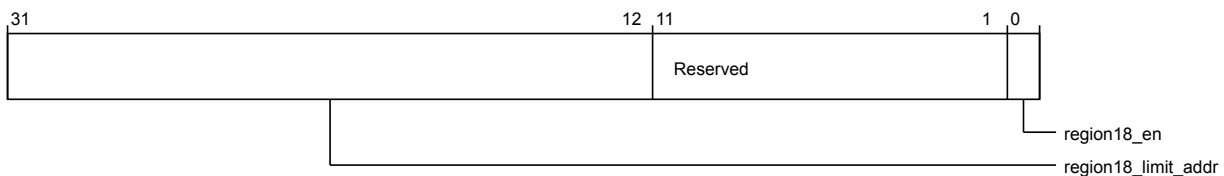


Figure 4-2325 por_mpu_por_mpu_m6_prlar18 (low)

The following table shows the por_mpu_m6_prlar18 lower register bit assignments.

Table 4-2342 por_mpu_por_mpu_m6_prlar18 (low)

Bits	Field name	Description	Type	Reset
31:12	region18_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region18_en	Region 18 enable.	RW	1'b0

por_mpu_m6_prbar19

MPU master 0 programmable base address register 19.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2940
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

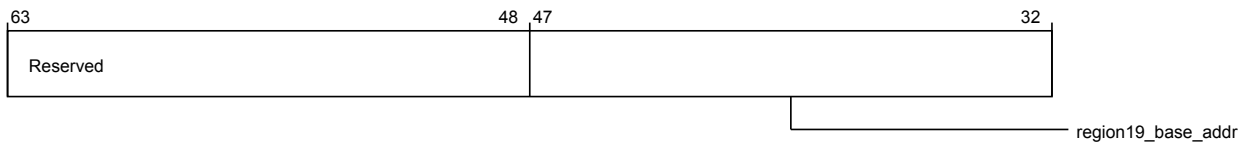


Figure 4-2326 por_mpu_por_mpu_m6_prbar19 (high)

The following table shows the por_mpu_m6_prbar19 higher register bit assignments.

Table 4-2343 por_mpu_por_mpu_m6_prbar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

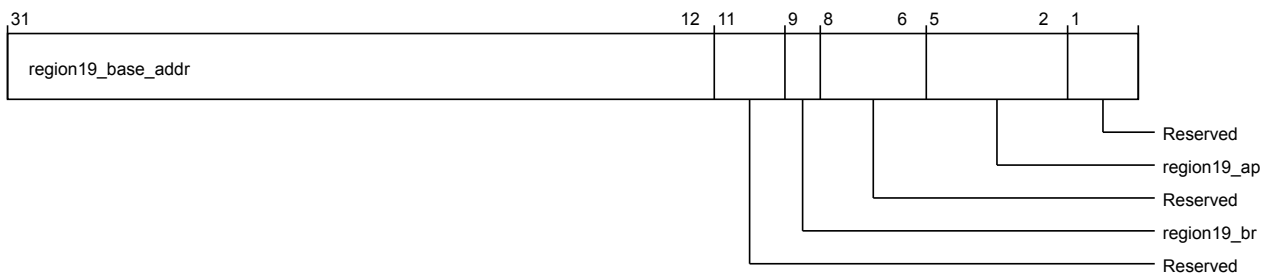


Figure 4-2327 por_mpu_por_mpu_m6_prbar19 (low)

The following table shows the por_mpu_m6_prbar19 lower register bit assignments.

Table 4-2344 por_mpu_por_mpu_m6_prbar19 (low)

Bits	Field name	Description	Type	Reset
31:12	region19_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2344 por_mpu_por_mpu_m6_prbar19 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region19_br	Region 19 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region19_ap	Region 19 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar19

MPU master 0 programmable limit address register 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2948

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

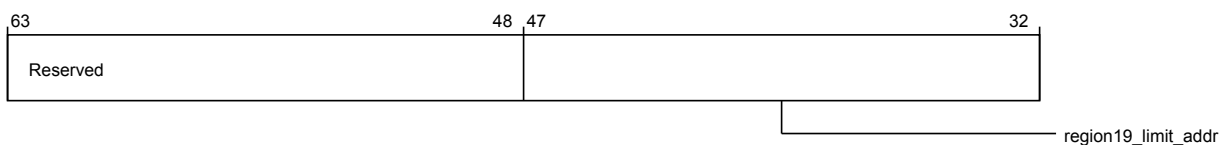


Figure 4-2328 por_mpu_por_mpu_m6_prlar19 (high)

The following table shows the por_mpu_m6_prlar19 higher register bit assignments.

Table 4-2345 por_mpu_por_mpu_m6_prlar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

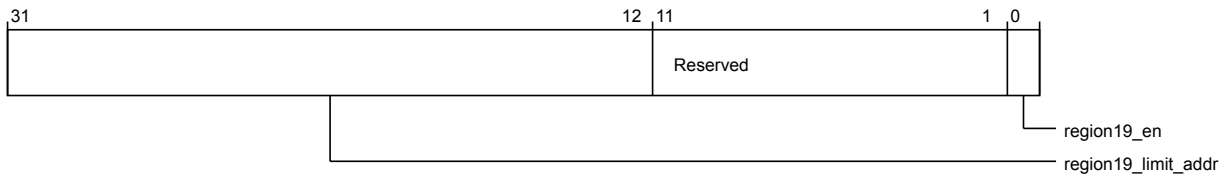


Figure 4-2329 por_mpu_por_mpu_m6_prlar19 (low)

The following table shows the por_mpu_m6_prlar19 lower register bit assignments.

Table 4-2346 por_mpu_por_mpu_m6_prlar19 (low)

Bits	Field name	Description	Type	Reset
31:12	region19_limit_addr	Bits [31:12] of limit address of the range.	RW	16'b0
11:1	Reserved	Reserved	RO	-
0	region19_en	Region 19 enable.	RW	1'b0

por_mpu_m6_prbar20

MPU master 0 programmable base address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2950

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

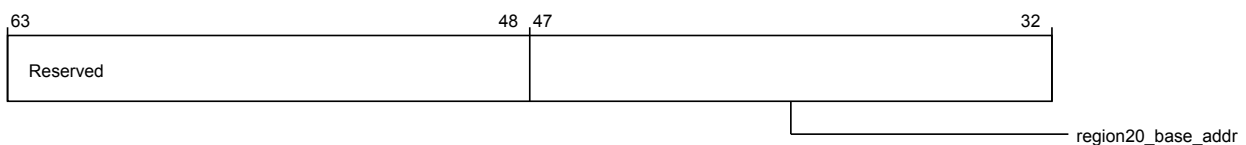


Figure 4-2330 por_mpu_por_mpu_m6_prbar20 (high)

The following table shows the por_mpu_m6_prbar20 higher register bit assignments.

Table 4-2347 por_mpu_por_mpu_m6_prbar20 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region20_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

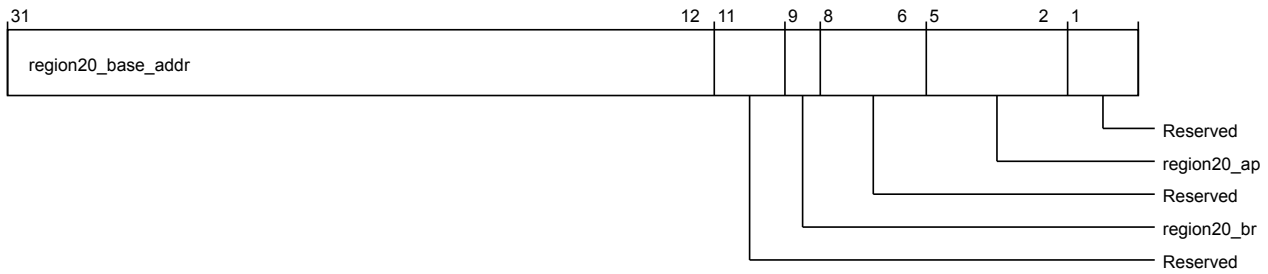


Figure 4-2331 `por_mpu_por_mpu_m6_prbar20` (low)

The following table shows the `por_mpu_m6_prbar20` lower register bit assignments.

Table 4-2348 `por_mpu_por_mpu_m6_prbar20` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region20_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region20_br</code>	Region 20 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region20_ap</code>	Region 20 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m6_prlar20`

MPU master 0 programmable limit address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2958

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

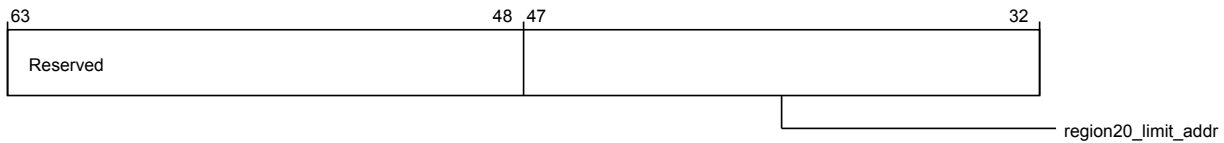


Figure 4-2332 `por_mpu_m6_prlar20` (high)

The following table shows the `por_mpu_m6_prlar20` higher register bit assignments.

Table 4-2349 `por_mpu_m6_prlar20` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region20_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

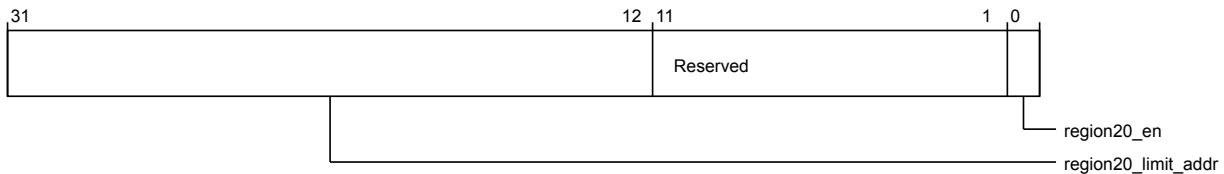


Figure 4-2333 `por_mpu_m6_prlar20` (low)

The following table shows the `por_mpu_m6_prlar20` lower register bit assignments.

Table 4-2350 `por_mpu_m6_prlar20` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region20_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region20_en</code>	Region 20 enable.	RW	1'b0

`por_mpu_m6_prbar21`

MPU master 0 programmable base address register 21.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2960
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

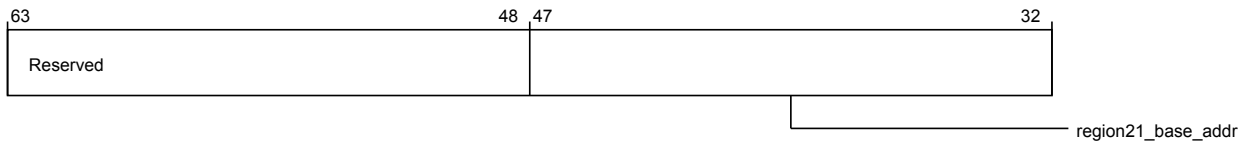


Figure 4-2334 `por_mpu_por_mpu_m6_prbar21` (high)

The following table shows the `por_mpu_m6_prbar21` higher register bit assignments.

Table 4-2351 `por_mpu_por_mpu_m6_prbar21` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

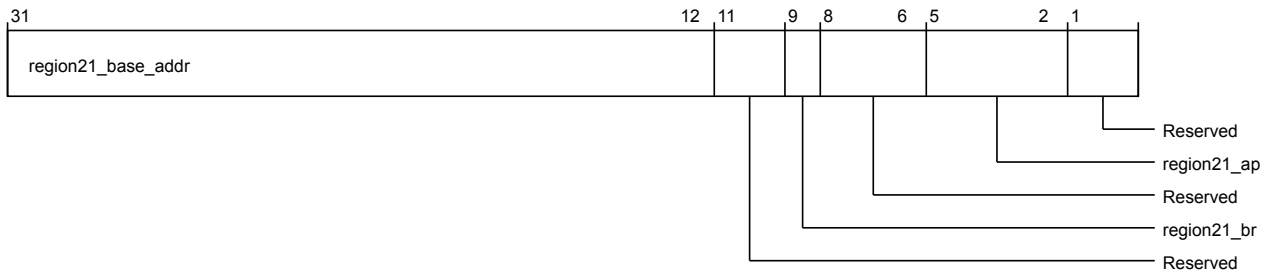


Figure 4-2335 `por_mpu_por_mpu_m6_prbar21` (low)

The following table shows the `por_mpu_m6_prbar21` lower register bit assignments.

Table 4-2352 `por_mpu_por_mpu_m6_prbar21` (low)

Bits	Field name	Description	Type	Reset
31:12	region21_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region21_br	Region 21 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region21_ap	Region 21 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar21

MPU master 0 programmable limit address register 21.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2968

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

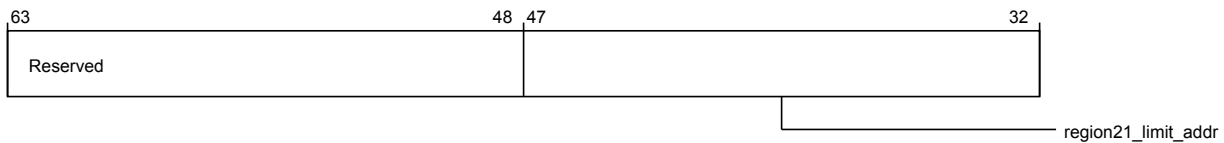


Figure 4-2336 por_mpu_por_mpu_m6_prlar21 (high)

The following table shows the `por_mpu_m6_prlar21` higher register bit assignments.

Table 4-2353 por_mpu_por_mpu_m6_prlar21 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

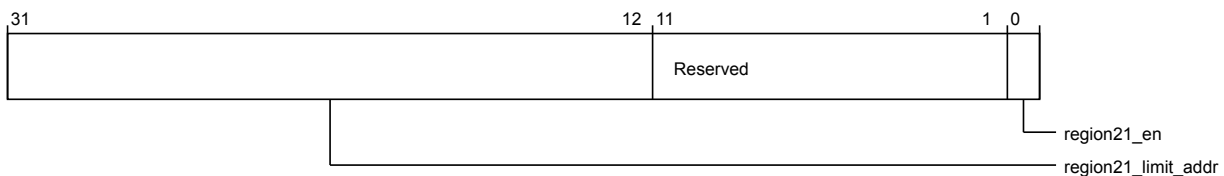


Figure 4-2337 por_mpu_por_mpu_m6_prlar21 (low)

The following table shows the `por_mpu_m6_prlar21` lower register bit assignments.

Table 4-2354 por_mpu_por_mpu_m6_prlar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region21_en	Region 21 enable.	RW	1'b0

por_mpu_m6_prbar22

MPU master 0 programmable base address register 22.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2970
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

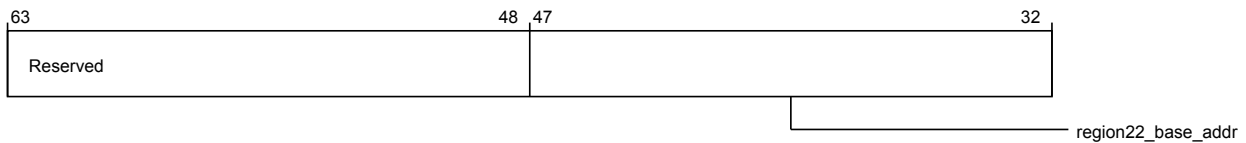


Figure 4-2338 por_mpu_por_mpu_m6_prbar22 (high)

The following table shows the por_mpu_m6_prbar22 higher register bit assignments.

Table 4-2355 por_mpu_por_mpu_m6_prbar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

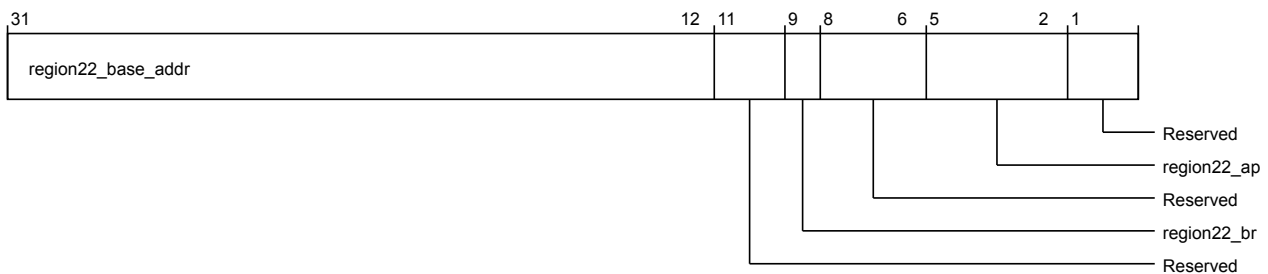


Figure 4-2339 por_mpu_por_mpu_m6_prbar22 (low)

The following table shows the por_mpu_m6_prbar22 lower register bit assignments.

Table 4-2356 por_mpu_por_mpu_m6_prbar22 (low)

Bits	Field name	Description	Type	Reset
31:12	region22_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2356 por_mpu_por_mpu_m6_prbar22 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region22_br	Region 22 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region22_ap	Region 22 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar22

MPU master 0 programmable limit address register 22.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2978

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

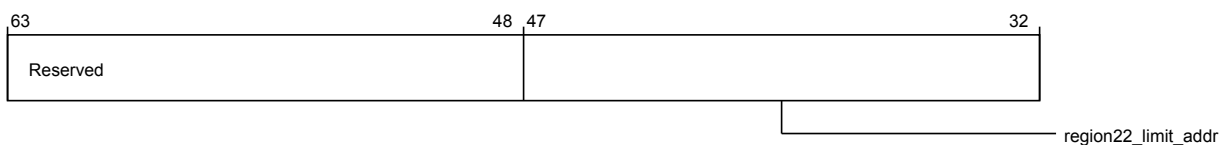


Figure 4-2340 por_mpu_por_mpu_m6_prlar22 (high)

The following table shows the por_mpu_m6_prlar22 higher register bit assignments.

Table 4-2357 por_mpu_por_mpu_m6_prlar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

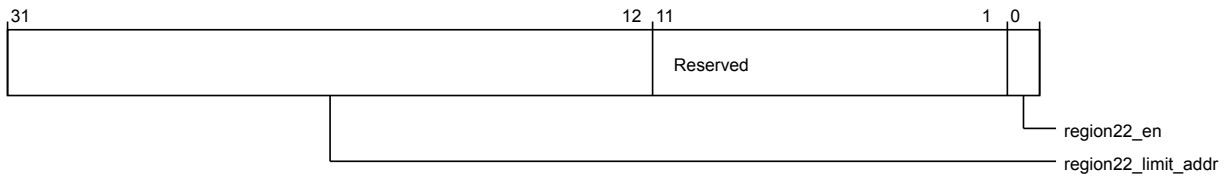


Figure 4-2341 `por_mpu_por_mpu_m6_prlar22` (low)

The following table shows the `por_mpu_m6_prlar22` lower register bit assignments.

Table 4-2358 `por_mpu_por_mpu_m6_prlar22` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region22_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region22_en</code>	Region 22 enable.	RW	1'b0

`por_mpu_m6_prbar23`

MPU master 0 programmable base address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

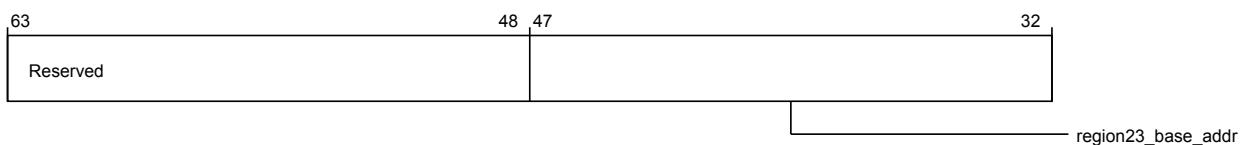


Figure 4-2342 `por_mpu_por_mpu_m6_prbar23` (high)

The following table shows the `por_mpu_m6_prbar23` higher register bit assignments.

Table 4-2359 `por_mpu_por_mpu_m6_prbar23` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region23_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

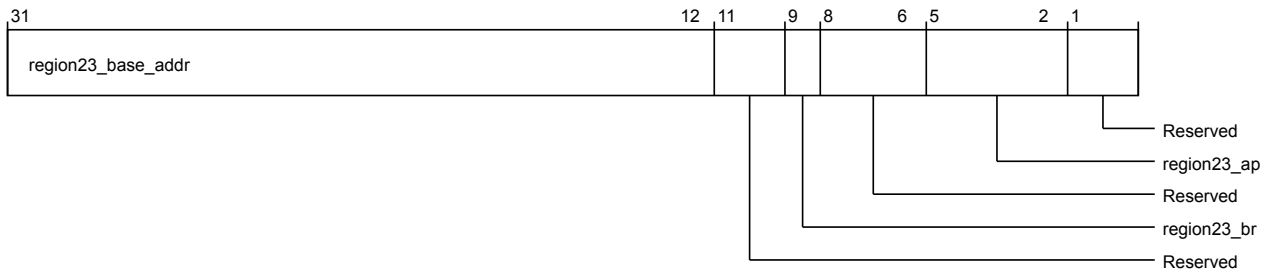


Figure 4-2343 por_mpu_por_mpu_m6_prbar23 (low)

The following table shows the por_mpu_m6_prbar23 lower register bit assignments.

Table 4-2360 por_mpu_por_mpu_m6_prbar23 (low)

Bits	Field name	Description	Type	Reset
31:12	region23_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region23_br	Region 23 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region23_ap	Region 23 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar23

MPU master 0 programmable limit address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2988

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

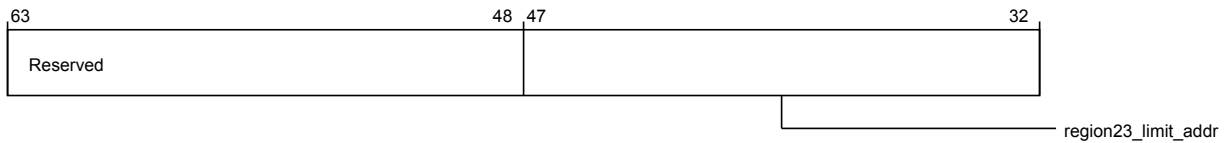


Figure 4-2344 `por_mpu_m6_prlar23` (high)

The following table shows the `por_mpu_m6_prlar23` higher register bit assignments.

Table 4-2361 `por_mpu_m6_prlar23` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region23_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

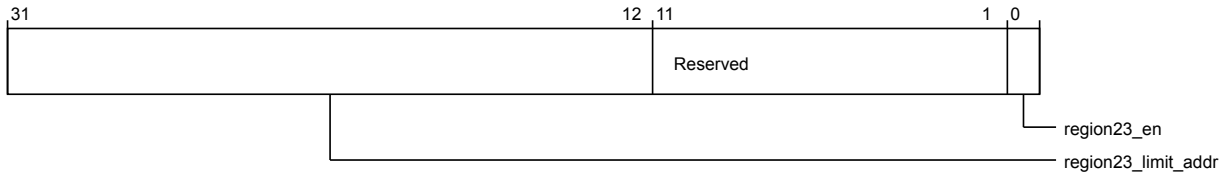


Figure 4-2345 `por_mpu_m6_prlar23` (low)

The following table shows the `por_mpu_m6_prlar23` lower register bit assignments.

Table 4-2362 `por_mpu_m6_prlar23` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region23_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region23_en</code>	Region 23 enable.	RW	1'b0

`por_mpu_m6_prbar24`

MPU master 0 programmable base address register 24.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2990
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

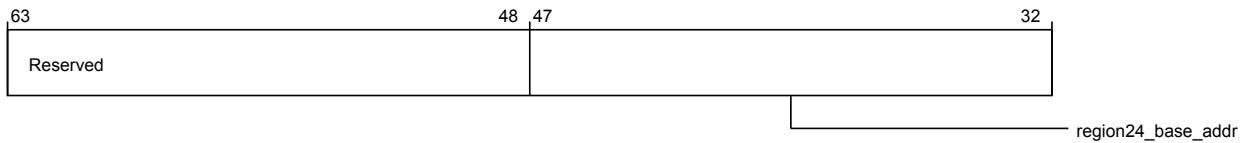


Figure 4-2346 por_mpu_por_mpu_m6_prbar24 (high)

The following table shows the por_mpu_m6_prbar24 higher register bit assignments.

Table 4-2363 por_mpu_por_mpu_m6_prbar24 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

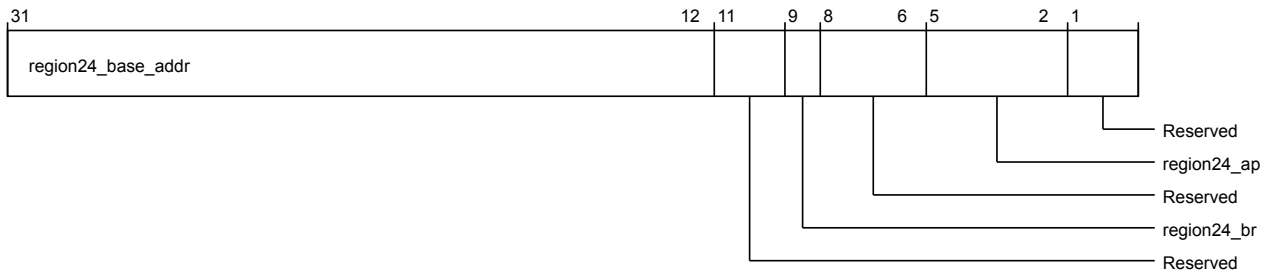


Figure 4-2347 por_mpu_por_mpu_m6_prbar24 (low)

The following table shows the por_mpu_m6_prbar24 lower register bit assignments.

Table 4-2364 por_mpu_por_mpu_m6_prbar24 (low)

Bits	Field name	Description	Type	Reset
31:12	region24_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region24_br	Region 24 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region24_ap	Region 24 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar24

MPU master 0 programmable limit address register 24.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2998

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

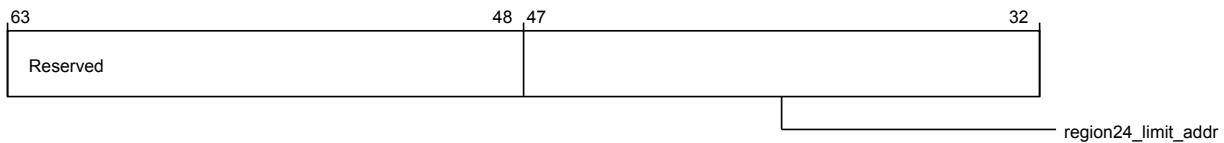


Figure 4-2348 por_mpu_por_mpu_m6_prlar24 (high)

The following table shows the `por_mpu_m6_prlar24` higher register bit assignments.

Table 4-2365 por_mpu_por_mpu_m6_prlar24 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

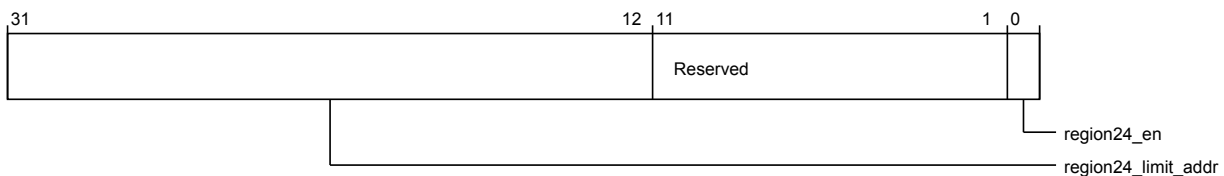


Figure 4-2349 por_mpu_por_mpu_m6_prlar24 (low)

The following table shows the `por_mpu_m6_prlar24` lower register bit assignments.

Table 4-2366 por_mpu_por_mpu_m6_prlar24 (low)

Bits	Field name	Description	Type	Reset
31:12	region24_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region24_en	Region 24 enable.	RW	1'b0

por_mpu_m6_prbar25

MPU master 0 programmable base address register 25.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h29A0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

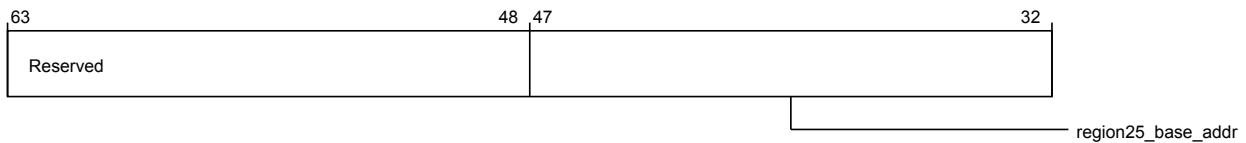


Figure 4-2350 por_mpu_por_mpu_m6_prbar25 (high)

The following table shows the por_mpu_m6_prbar25 higher register bit assignments.

Table 4-2367 por_mpu_por_mpu_m6_prbar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

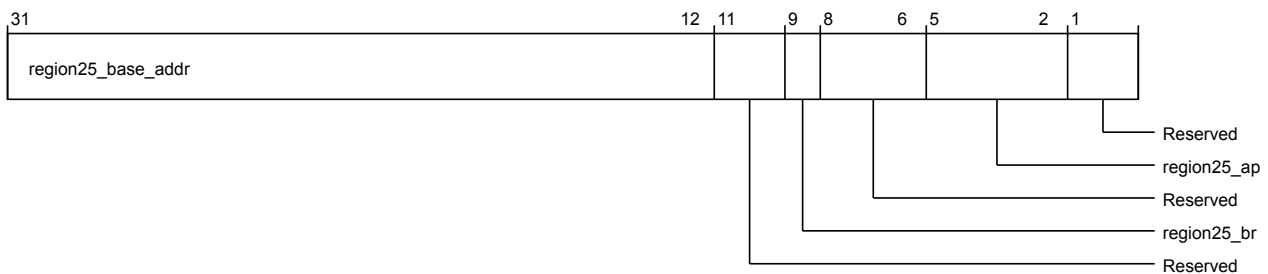


Figure 4-2351 por_mpu_por_mpu_m6_prbar25 (low)

The following table shows the por_mpu_m6_prbar25 lower register bit assignments.

Table 4-2368 por_mpu_por_mpu_m6_prbar25 (low)

Bits	Field name	Description	Type	Reset
31:12	region25_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2368 por_mpu_por_mpu_m6_prbar25 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region25_br	Region 25 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region25_ap	Region 25 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar25

MPU master 0 programmable limit address register 25.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h29A8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

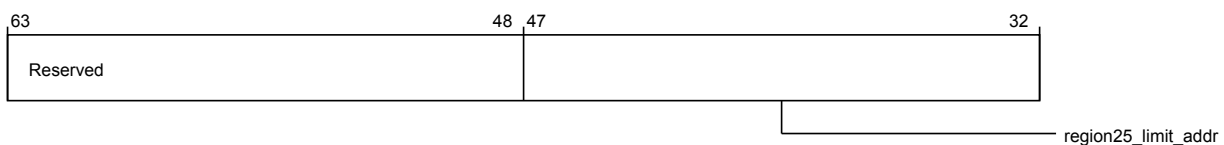


Figure 4-2352 por_mpu_por_mpu_m6_prlar25 (high)

The following table shows the por_mpu_m6_prlar25 higher register bit assignments.

Table 4-2369 por_mpu_por_mpu_m6_prlar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

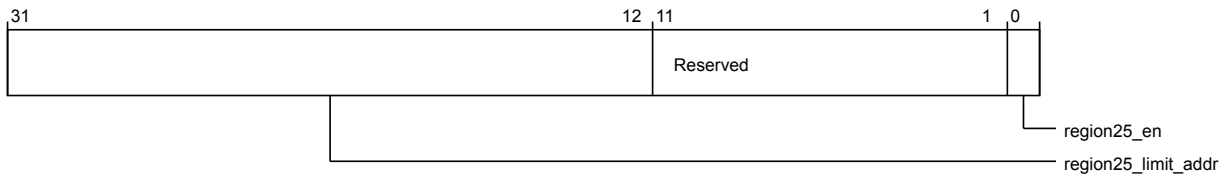


Figure 4-2353 `por_mpu_por_mpu_m6_prlar25` (low)

The following table shows the `por_mpu_m6_prlar25` lower register bit assignments.

Table 4-2370 `por_mpu_por_mpu_m6_prlar25` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region25_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region25_en</code>	Region 25 enable.	RW	1'b0

`por_mpu_m6_prbar26`

MPU master 0 programmable base address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h29B0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

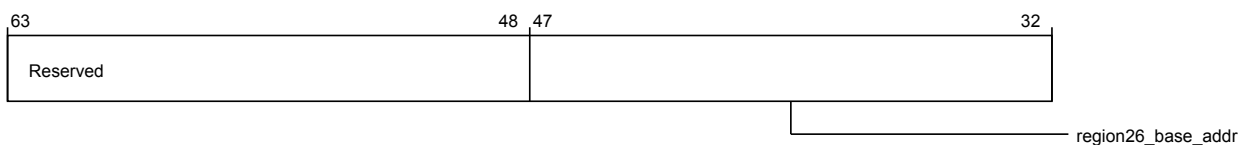


Figure 4-2354 `por_mpu_por_mpu_m6_prbar26` (high)

The following table shows the `por_mpu_m6_prbar26` higher register bit assignments.

Table 4-2371 `por_mpu_por_mpu_m6_prbar26` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region26_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

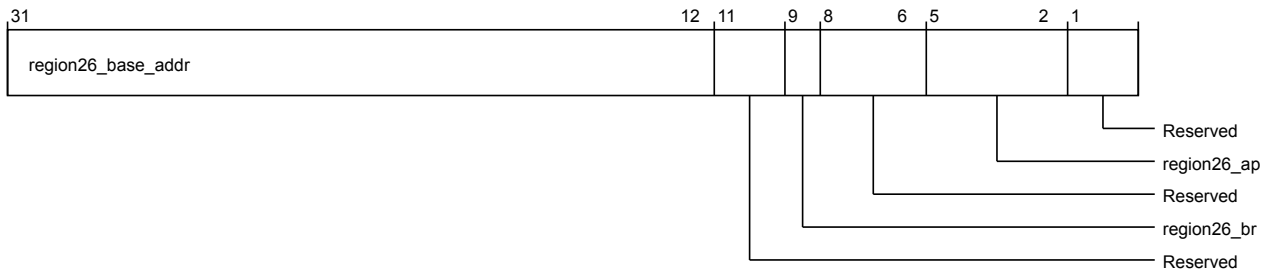


Figure 4-2355 por_mpu_por_mpu_m6_prbar26 (low)

The following table shows the por_mpu_m6_prbar26 lower register bit assignments.

Table 4-2372 por_mpu_por_mpu_m6_prbar26 (low)

Bits	Field name	Description	Type	Reset
31:12	region26_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region26_br	Region 26 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region26_ap	Region 26 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar26

MPU master 0 programmable limit address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h29B8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

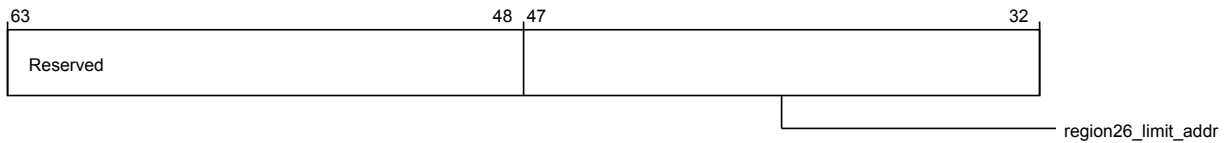


Figure 4-2356 por_mpu_m6_prlar26 (high)

The following table shows the por_mpu_m6_prlar26 higher register bit assignments.

Table 4-2373 por_mpu_m6_prlar26 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region26_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

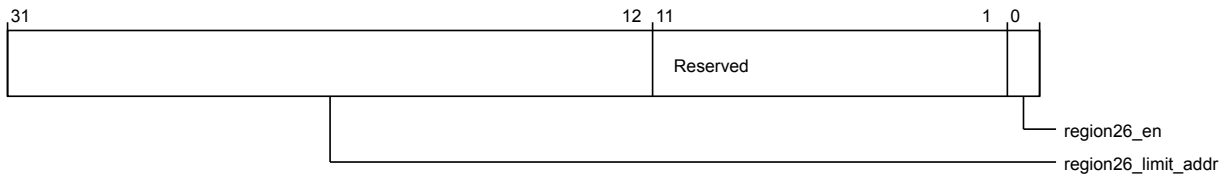


Figure 4-2357 por_mpu_m6_prlar26 (low)

The following table shows the por_mpu_m6_prlar26 lower register bit assignments.

Table 4-2374 por_mpu_m6_prlar26 (low)

Bits	Field name	Description	Type	Reset
31:12	region26_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region26_en	Region 26 enable.	RW	1'b0

por_mpu_m6_prbar27

MPU master 0 programmable base address register 27.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h29C0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

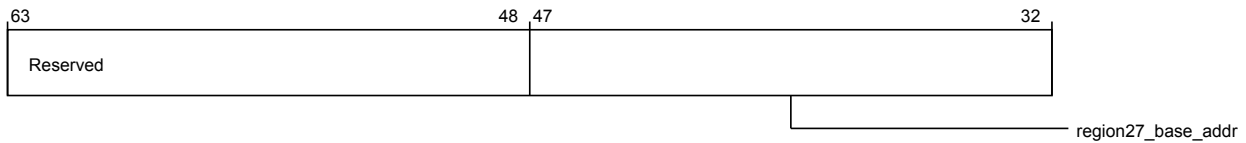


Figure 4-2358 por_mpu_por_mpu_m6_prbar27 (high)

The following table shows the por_mpu_m6_prbar27 higher register bit assignments.

Table 4-2375 por_mpu_por_mpu_m6_prbar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

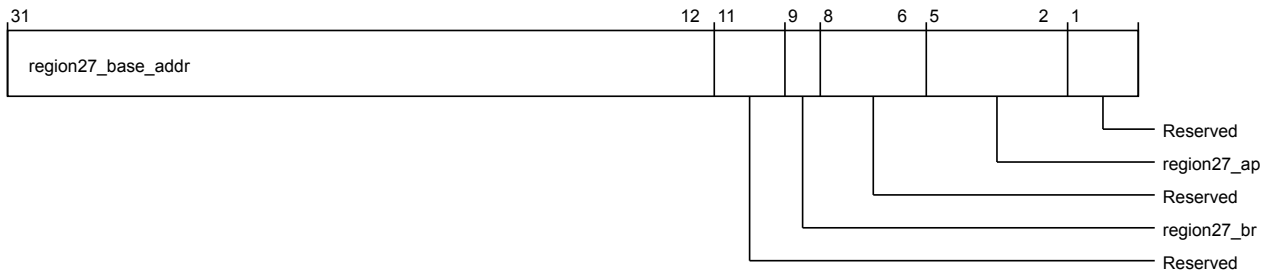


Figure 4-2359 por_mpu_por_mpu_m6_prbar27 (low)

The following table shows the por_mpu_m6_prbar27 lower register bit assignments.

Table 4-2376 por_mpu_por_mpu_m6_prbar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region27_br	Region 27 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region27_ap	Region 27 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar27

MPU master 0 programmable limit address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h29C8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

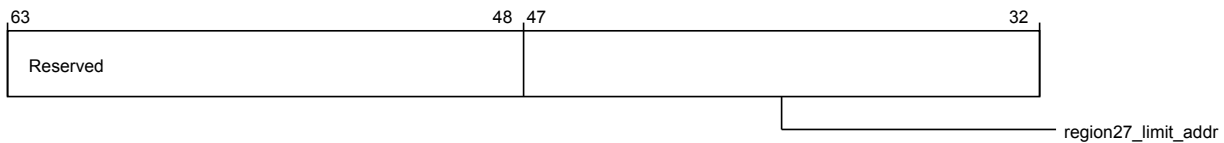


Figure 4-2360 por_mpu_por_mpu_m6_prlar27 (high)

The following table shows the `por_mpu_m6_prlar27` higher register bit assignments.

Table 4-2377 por_mpu_por_mpu_m6_prlar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

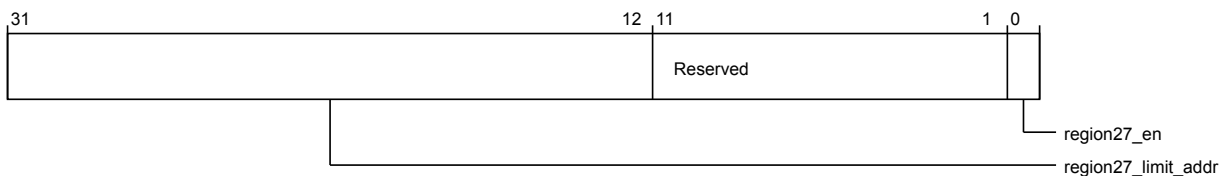


Figure 4-2361 por_mpu_por_mpu_m6_prlar27 (low)

The following table shows the `por_mpu_m6_prlar27` lower register bit assignments.

Table 4-2378 por_mpu_por_mpu_m6_prlar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region27_en	Region 27 enable.	RW	1'b0

por_mpu_m6_prbar28

MPU master 0 programmable base address register 28.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h29D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

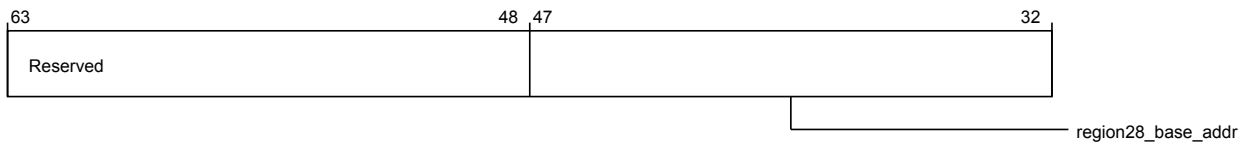


Figure 4-2362 por_mpu_por_mpu_m6_prbar28 (high)

The following table shows the por_mpu_m6_prbar28 higher register bit assignments.

Table 4-2379 por_mpu_por_mpu_m6_prbar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

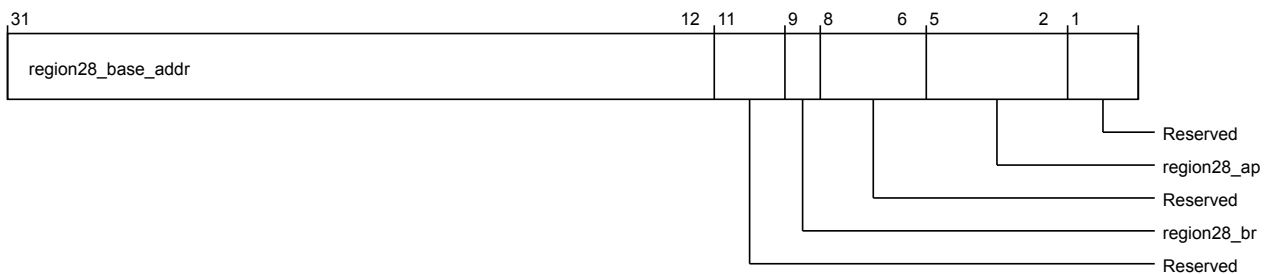


Figure 4-2363 por_mpu_por_mpu_m6_prbar28 (low)

The following table shows the por_mpu_m6_prbar28 lower register bit assignments.

Table 4-2380 por_mpu_por_mpu_m6_prbar28 (low)

Bits	Field name	Description	Type	Reset
31:12	region28_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2380 por_mpu_por_mpu_m6_prbar28 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region28_br	Region 28 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region28_ap	Region 28 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar28

MPU master 0 programmable limit address register 28.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h29D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

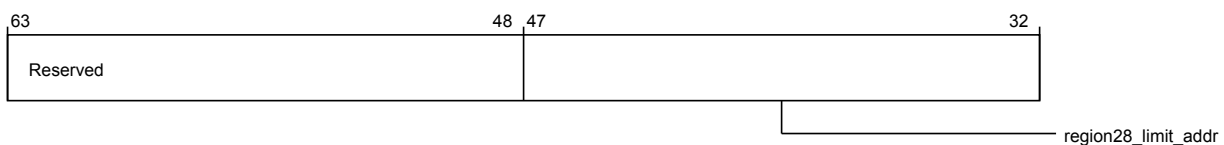


Figure 4-2364 por_mpu_por_mpu_m6_prlar28 (high)

The following table shows the por_mpu_m6_prlar28 higher register bit assignments.

Table 4-2381 por_mpu_por_mpu_m6_prlar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

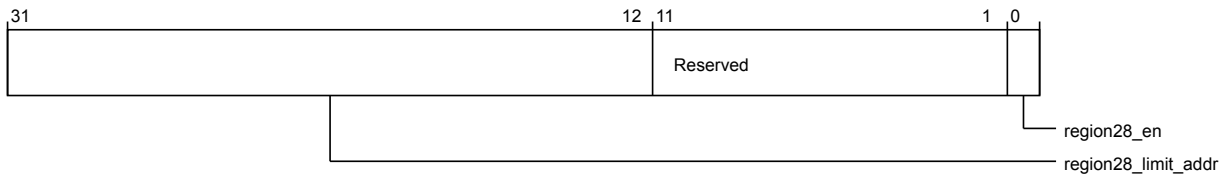


Figure 4-2365 `por_mpu_por_mpu_m6_prlar28` (low)

The following table shows the `por_mpu_m6_prlar28` lower register bit assignments.

Table 4-2382 `por_mpu_por_mpu_m6_prlar28` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region28_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region28_en</code>	Region 28 enable.	RW	1'b0

`por_mpu_m6_prbar29`

MPU master 0 programmable base address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h29E0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

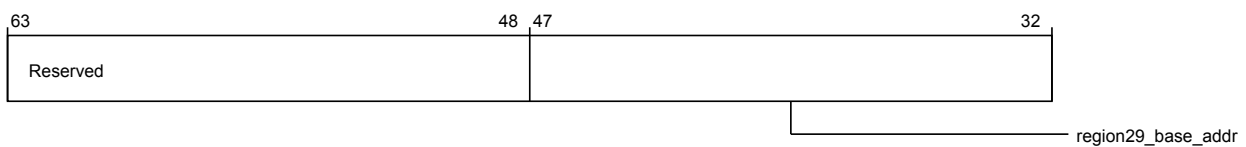


Figure 4-2366 `por_mpu_por_mpu_m6_prbar29` (high)

The following table shows the `por_mpu_m6_prbar29` higher register bit assignments.

Table 4-2383 `por_mpu_por_mpu_m6_prbar29` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region29_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

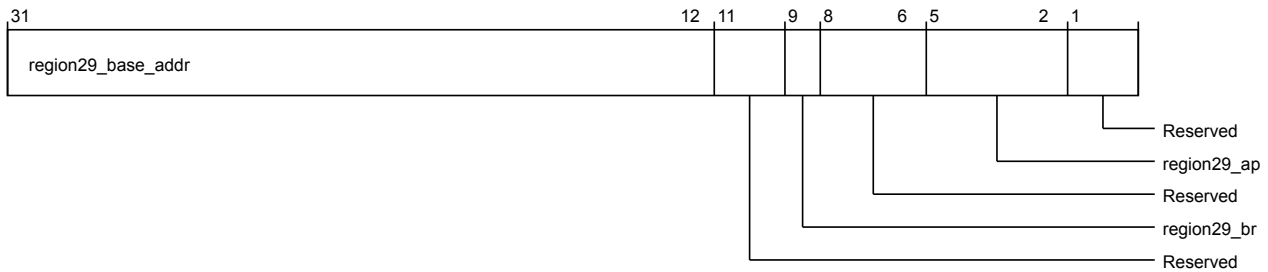


Figure 4-2367 `por_mpu_m6_prbar29` (low)

The following table shows the `por_mpu_m6_prbar29` lower register bit assignments.

Table 4-2384 `por_mpu_m6_prbar29` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region29_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region29_br</code>	Region 29 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region29_ap</code>	Region 29 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m6_prlar29`

MPU master 0 programmable limit address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h29E8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

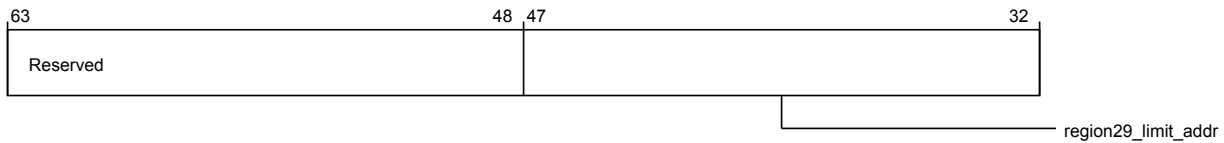


Figure 4-2368 `por_mpu_m6_prlar29` (high)

The following table shows the `por_mpu_m6_prlar29` higher register bit assignments.

Table 4-2385 `por_mpu_m6_prlar29` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region29_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

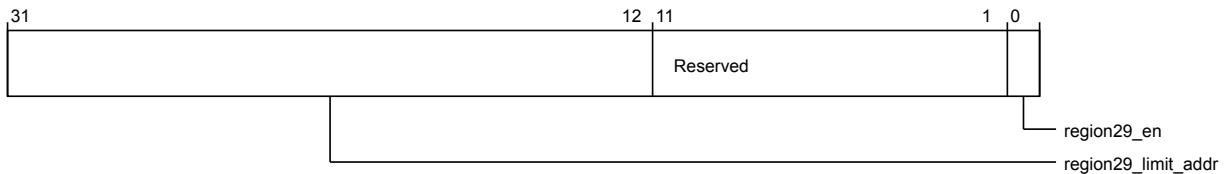


Figure 4-2369 `por_mpu_m6_prlar29` (low)

The following table shows the `por_mpu_m6_prlar29` lower register bit assignments.

Table 4-2386 `por_mpu_m6_prlar29` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region29_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region29_en</code>	Region 29 enable.	RW	1'b0

`por_mpu_m6_prbar30`

MPU master 0 programmable base address register 30.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h29F0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

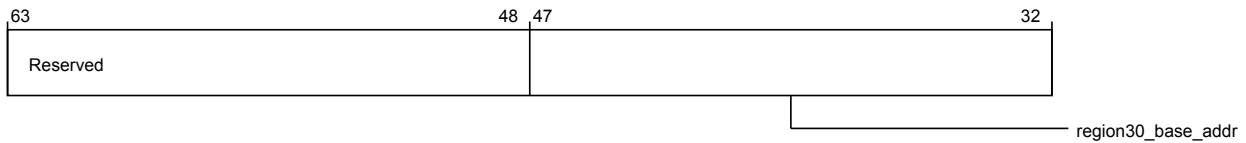


Figure 4-2370 por_mpu_por_mpu_m6_prbar30 (high)

The following table shows the por_mpu_m6_prbar30 higher register bit assignments.

Table 4-2387 por_mpu_por_mpu_m6_prbar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

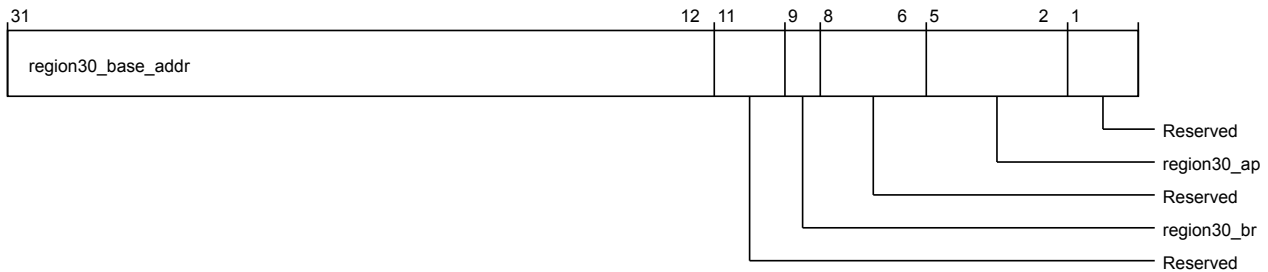


Figure 4-2371 por_mpu_por_mpu_m6_prbar30 (low)

The following table shows the por_mpu_m6_prbar30 lower register bit assignments.

Table 4-2388 por_mpu_por_mpu_m6_prbar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region30_br	Region 30 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region30_ap	Region 30 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar30

MPU master 0 programmable limit address register 30.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h29F8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

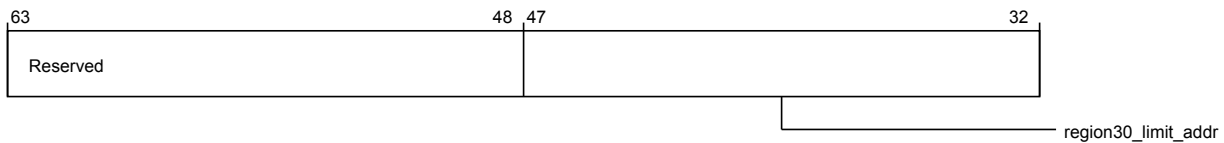


Figure 4-2372 por_mpu_por_mpu_m6_prlar30 (high)

The following table shows the `por_mpu_m6_prlar30` higher register bit assignments.

Table 4-2389 por_mpu_por_mpu_m6_prlar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

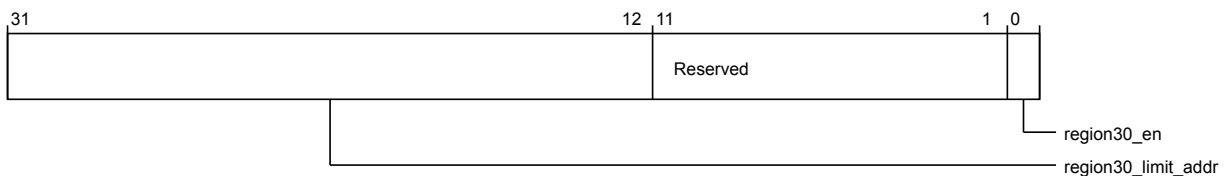


Figure 4-2373 por_mpu_por_mpu_m6_prlar30 (low)

The following table shows the `por_mpu_m6_prlar30` lower register bit assignments.

Table 4-2390 por_mpu_por_mpu_m6_prlar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region30_en	Region 30 enable.	RW	1'b0

por_mpu_m6_prbar31

MPU master 0 programmable base address register 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2A00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

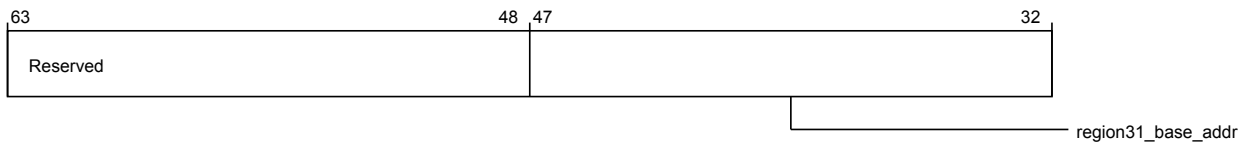


Figure 4-2374 por_mpu_por_mpu_m6_prbar31 (high)

The following table shows the por_mpu_m6_prbar31 higher register bit assignments.

Table 4-2391 por_mpu_por_mpu_m6_prbar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

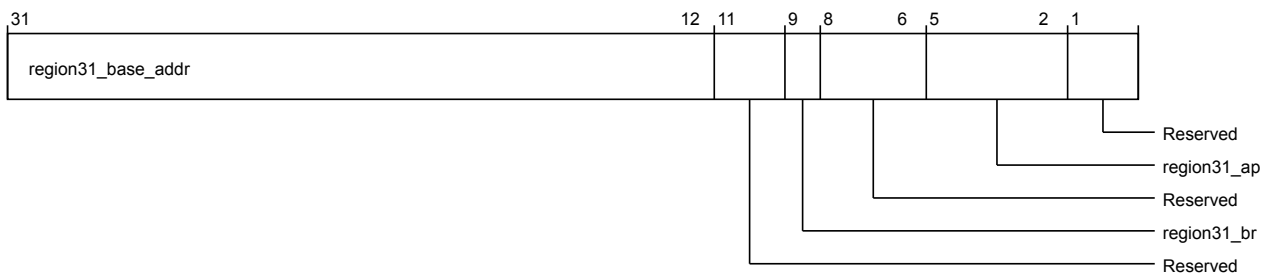


Figure 4-2375 por_mpu_por_mpu_m6_prbar31 (low)

The following table shows the por_mpu_m6_prbar31 lower register bit assignments.

Table 4-2392 por_mpu_por_mpu_m6_prbar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2392 por_mpu_por_mpu_m6_prbar31 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region31_br	Region 31 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region31_ap	Region 31 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m6_prlar31

MPU master 0 programmable limit address register 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2A08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

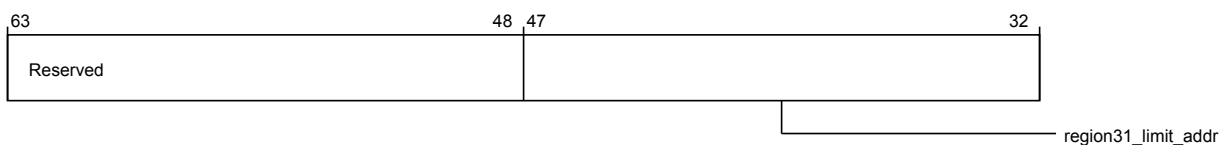


Figure 4-2376 por_mpu_por_mpu_m6_prlar31 (high)

The following table shows the por_mpu_m6_prlar31 higher register bit assignments.

Table 4-2393 por_mpu_por_mpu_m6_prlar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

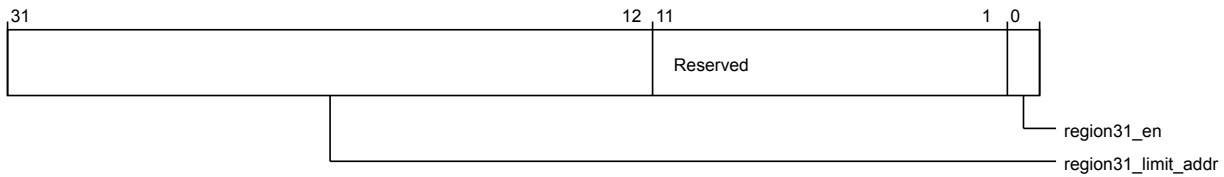


Figure 4-2377 por_mpu_por_mpu_m6_prlar31 (low)

The following table shows the por_mpu_m6_prlar31 lower register bit assignments.

Table 4-2394 por_mpu_por_mpu_m6_prlar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region31_en	Region 31 enable.	RW	1'b0

por_mpu_m7_ctl

Functions as the MPU Master 7 control register.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C00

Register reset 64'b010

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

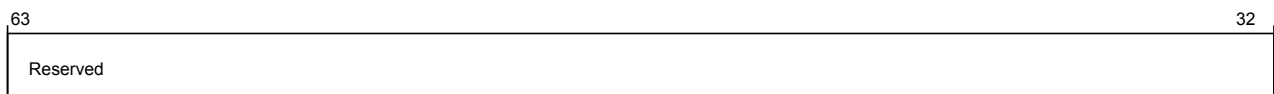


Figure 4-2378 por_mpu_por_mpu_m7_ctl (high)

The following table shows the por_mpu_m7_ctl higher register bit assignments.

Table 4-2395 por_mpu_por_mpu_m7_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

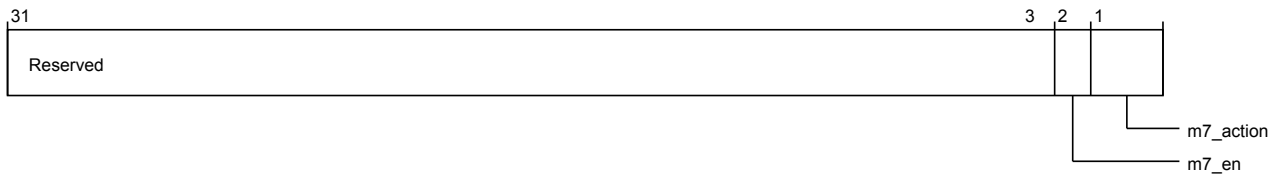


Figure 4-2379 por_mpu_por_mpu_m7_ctl (low)

The following table shows the por_mpu_m7_ctl lower register bit assignments.

Table 4-2396 por_mpu_por_mpu_m7_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	m7_en	MPU master 7 enable.	RW	1'b0
1:0	m7_action	Indicates action HN* should take if no access permission is granted 2'b00: FUSA interrupt 2'b01: Bus error to the originating bus master 2'b10: Both FUSA interrupt and bus error.	RW	2'b10

por_mpu_m7_prbar0

MPU master 0 programmable base address register 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

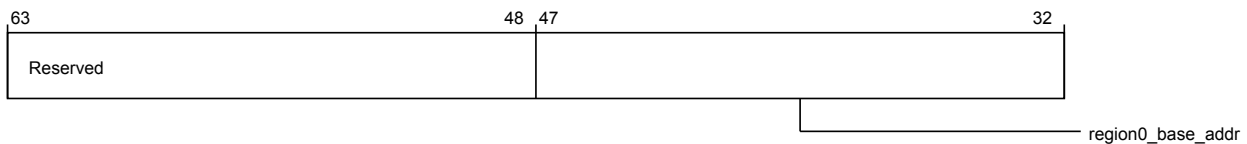


Figure 4-2380 por_mpu_por_mpu_m7_prbar0 (high)

The following table shows the por_mpu_m7_prbar0 higher register bit assignments.

Table 4-2397 por_mpu_por_mpu_m7_prbar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

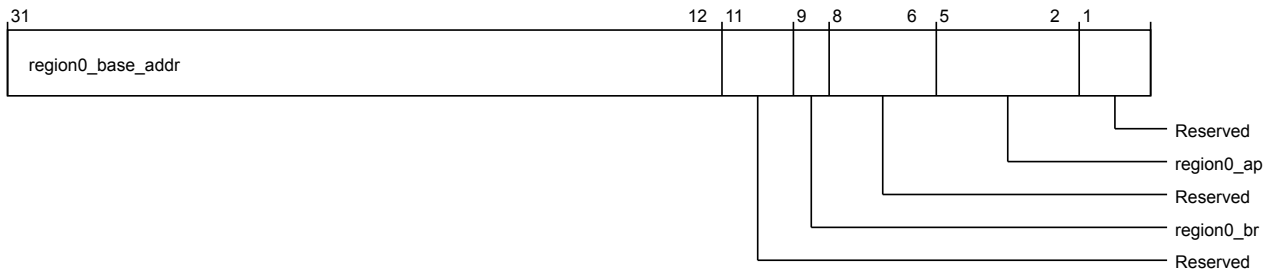


Figure 4-2381 por_mpu_por_mpu_m7_prbar0 (low)

The following table shows the por_mpu_m7_prbar0 lower register bit assignments.

Table 4-2398 por_mpu_por_mpu_m7_prbar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region0_br	Region 0 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region0_ap	Region 0 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar0

MPU master 0 programmable limit address register 0.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2C18
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

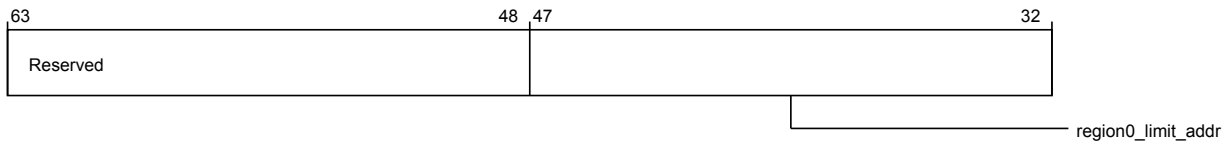


Figure 4-2382 por_mpu_por_mpu_m7_prlar0 (high)

The following table shows the por_mpu_m7_prlar0 higher register bit assignments.

Table 4-2399 por_mpu_por_mpu_m7_prlar0 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region0_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

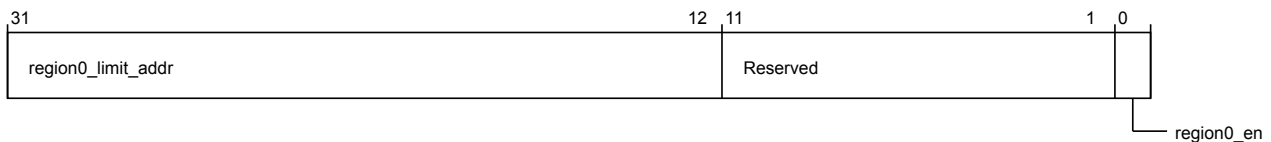


Figure 4-2383 por_mpu_por_mpu_m7_prlar0 (low)

The following table shows the por_mpu_m7_prlar0 lower register bit assignments.

Table 4-2400 por_mpu_por_mpu_m7_prlar0 (low)

Bits	Field name	Description	Type	Reset
31:12	region0_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region0_en	Region 0 enable.	RW	1'b0

por_mpu_m7_prbar1

MPU master 0 programmable base address register 1.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2C20
Register reset	64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

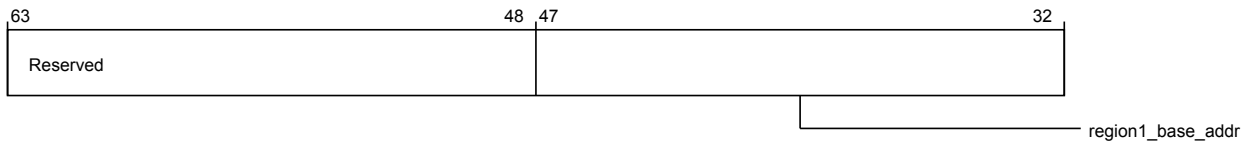


Figure 4-2384 por_mpu_por_mpu_m7_prbar1 (high)

The following table shows the por_mpu_m7_prbar1 higher register bit assignments.

Table 4-2401 por_mpu_por_mpu_m7_prbar1 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region1_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

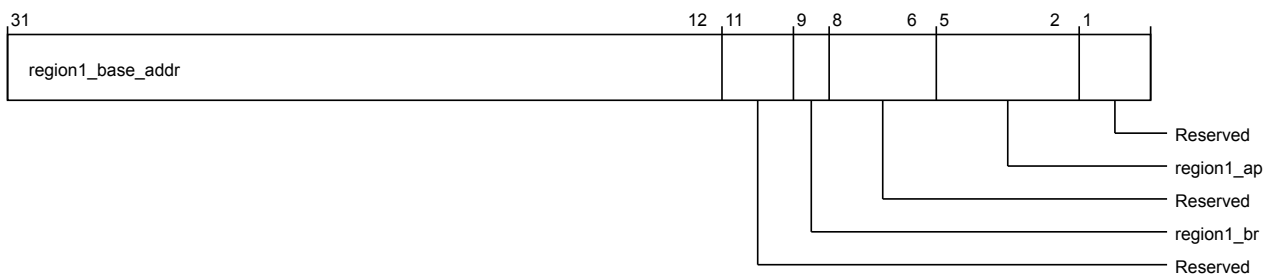


Figure 4-2385 por_mpu_por_mpu_m7_prbar1 (low)

The following table shows the por_mpu_m7_prbar1 lower register bit assignments.

Table 4-2402 por_mpu_por_mpu_m7_prbar1 (low)

Bits	Field name	Description	Type	Reset
31:12	region1_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region1_br	Region 1 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-

Table 4-2402 por_mpu_por_mpu_m7_prbar1 (low) (continued)

Bits	Field name	Description	Type	Reset
5:2	region1_ap	Region 1 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar1

MPU master 0 programmable limit address register 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C28

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

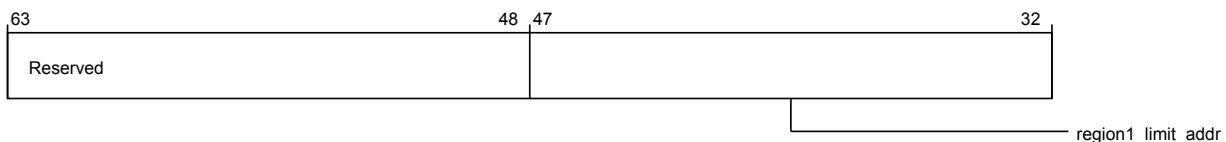


Figure 4-2386 por_mpu_por_mpu_m7_prlar1 (high)

The following table shows the por_mpu_m7_prlar1 higher register bit assignments.

Table 4-2403 por_mpu_por_mpu_m7_prlar1 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region1_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

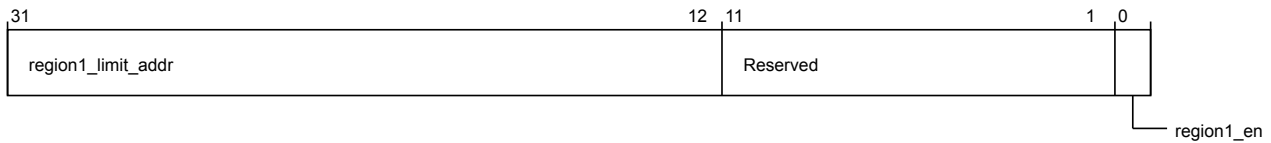


Figure 4-2387 `por_mpu_por_mpu_m7_prlar1` (low)

The following table shows the `por_mpu_m7_prlar1` lower register bit assignments.

Table 4-2404 `por_mpu_por_mpu_m7_prlar1` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region1_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region1_en</code>	Region 1 enable.	RW	1'b0

`por_mpu_m7_prbar2`

MPU master 0 programmable base address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C30

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

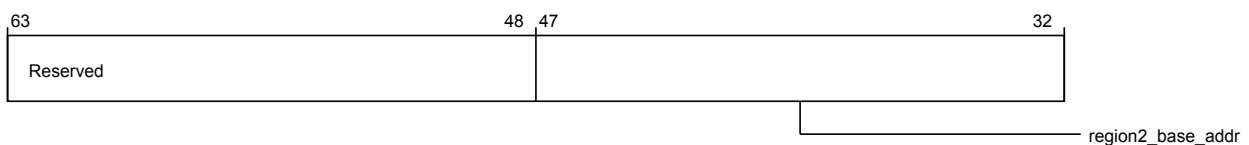


Figure 4-2388 `por_mpu_por_mpu_m7_prbar2` (high)

The following table shows the `por_mpu_m7_prbar2` higher register bit assignments.

Table 4-2405 `por_mpu_por_mpu_m7_prbar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

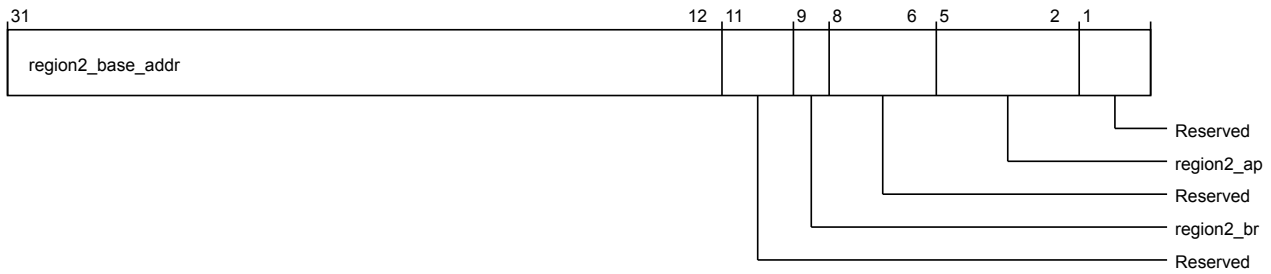


Figure 4-2389 por_mpu_por_mpu_m7_prbar2 (low)

The following table shows the por_mpu_m7_prbar2 lower register bit assignments.

Table 4-2406 por_mpu_por_mpu_m7_prbar2 (low)

Bits	Field name	Description	Type	Reset
31:12	region2_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region2_br	Region 2 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region2_ap	Region 2 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar2

MPU master 0 programmable limit address register 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C38

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

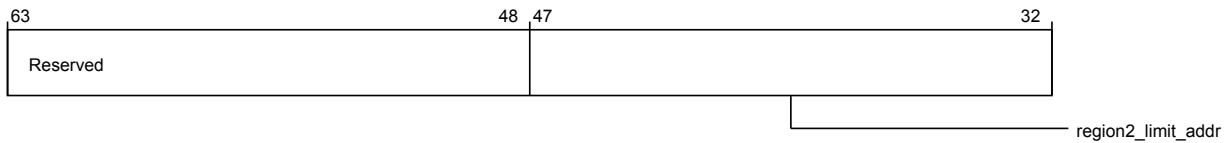


Figure 4-2390 `por_mpu_m7_prlar2` (high)

The following table shows the `por_mpu_m7_prlar2` higher register bit assignments.

Table 4-2407 `por_mpu_m7_prlar2` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region2_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

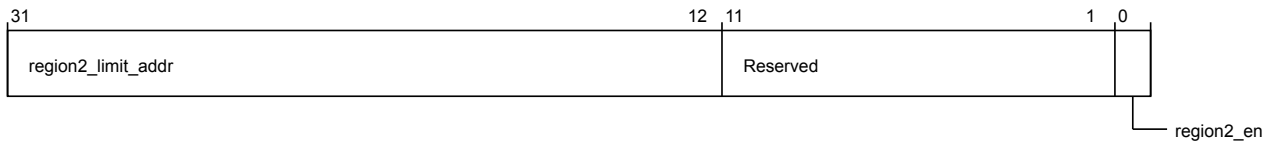


Figure 4-2391 `por_mpu_m7_prlar2` (low)

The following table shows the `por_mpu_m7_prlar2` lower register bit assignments.

Table 4-2408 `por_mpu_m7_prlar2` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region2_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region2_en</code>	Region 2 enable.	RW	1'b0

`por_mpu_m7_prbar3`

MPU master 0 programmable base address register 3.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2C40
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

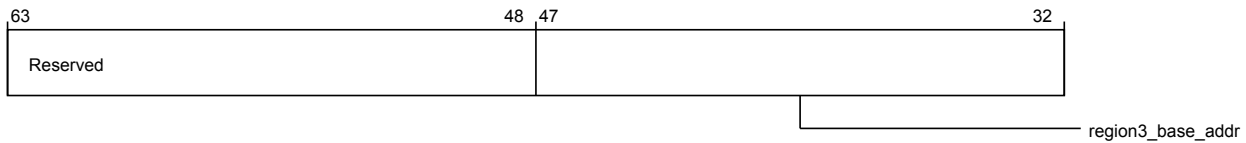


Figure 4-2392 por_mpu_por_mpu_m7_prbar3 (high)

The following table shows the por_mpu_m7_prbar3 higher register bit assignments.

Table 4-2409 por_mpu_por_mpu_m7_prbar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

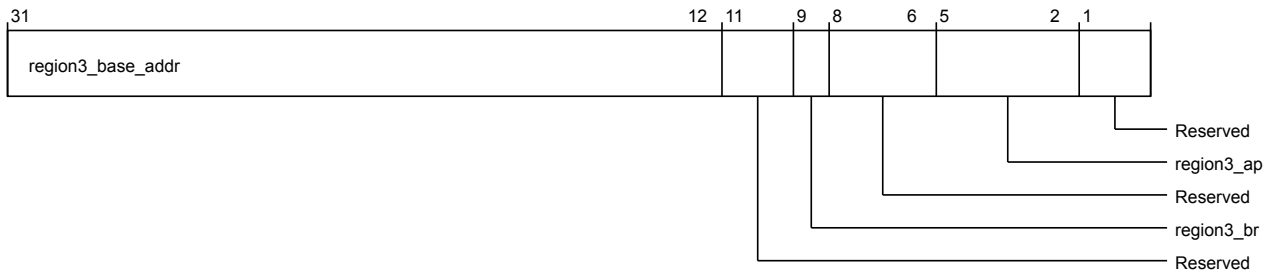


Figure 4-2393 por_mpu_por_mpu_m7_prbar3 (low)

The following table shows the por_mpu_m7_prbar3 lower register bit assignments.

Table 4-2410 por_mpu_por_mpu_m7_prbar3 (low)

Bits	Field name	Description	Type	Reset
31:12	region3_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region3_br	Region 3 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region3_ap	Region 3 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar3

MPU master 0 programmable limit address register 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C48

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

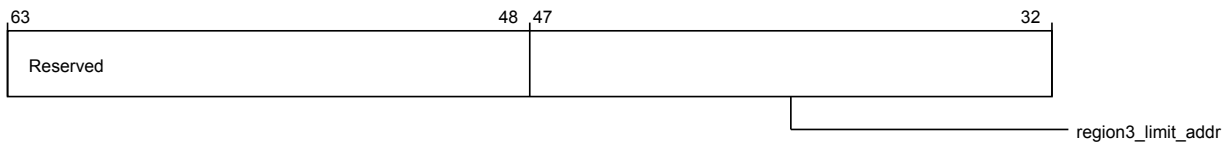


Figure 4-2394 por_mpu_por_mpu_m7_prlar3 (high)

The following table shows the por_mpu_m7_prlar3 higher register bit assignments.

Table 4-2411 por_mpu_por_mpu_m7_prlar3 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region3_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

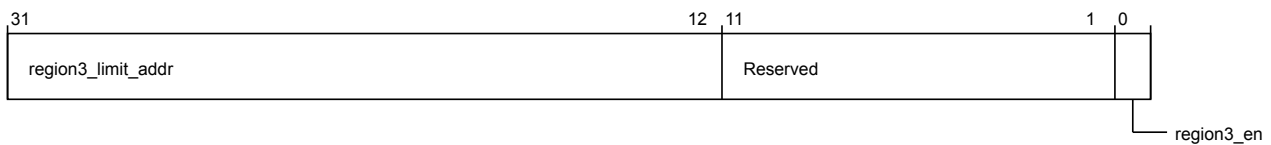


Figure 4-2395 por_mpu_por_mpu_m7_prlar3 (low)

The following table shows the por_mpu_m7_prlar3 lower register bit assignments.

Table 4-2412 por_mpu_por_mpu_m7_prlar3 (low)

Bits	Field name	Description	Type	Reset
31:12	region3_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region3_en	Region 3 enable.	RW	1'b0

por_mpu_m7_prbar4

MPU master 0 programmable base address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C50

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

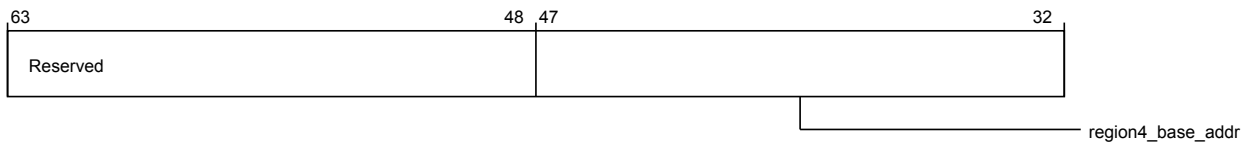


Figure 4-2396 por_mpu_por_mpu_m7_prbar4 (high)

The following table shows the por_mpu_m7_prbar4 higher register bit assignments.

Table 4-2413 por_mpu_por_mpu_m7_prbar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

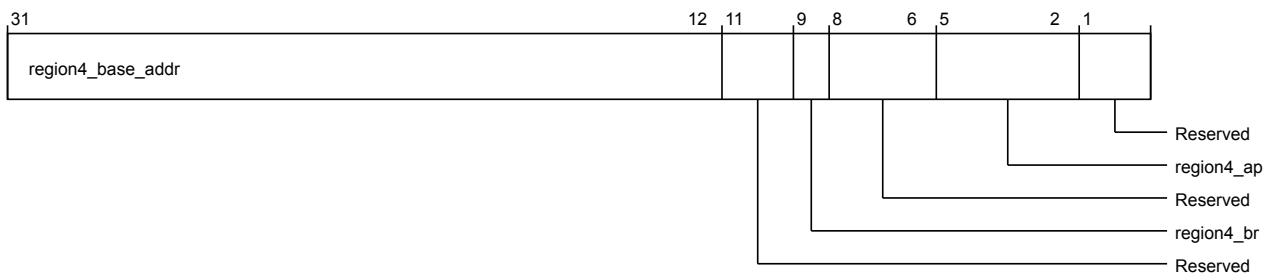


Figure 4-2397 por_mpu_por_mpu_m7_prbar4 (low)

The following table shows the por_mpu_m7_prbar4 lower register bit assignments.

Table 4-2414 por_mpu_por_mpu_m7_prbar4 (low)

Bits	Field name	Description	Type	Reset
31:12	region4_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2414 por_mpu_por_mpu_m7_prbar4 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region4_br	Region 4 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region4_ap	Region 4 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar4

MPU master 0 programmable limit address register 4.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C58

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

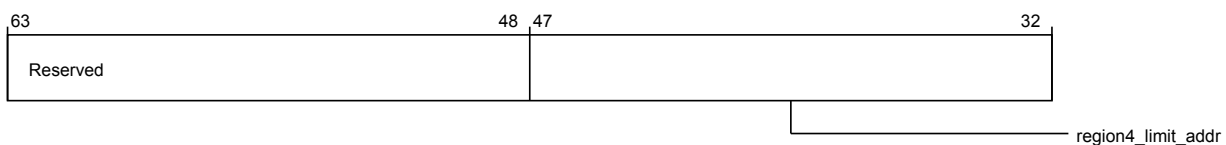


Figure 4-2398 por_mpu_por_mpu_m7_prlar4 (high)

The following table shows the por_mpu_m7_prlar4 higher register bit assignments.

Table 4-2415 por_mpu_por_mpu_m7_prlar4 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region4_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

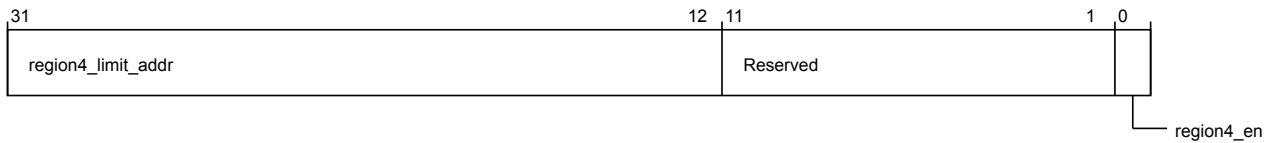


Figure 4-2399 `por_mpu_por_mpu_m7_prlar4` (low)

The following table shows the `por_mpu_m7_prlar4` lower register bit assignments.

Table 4-2416 `por_mpu_por_mpu_m7_prlar4` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region4_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region4_en</code>	Region 4 enable.	RW	1'b0

`por_mpu_m7_prbar5`

MPU master 0 programmable base address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C60

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

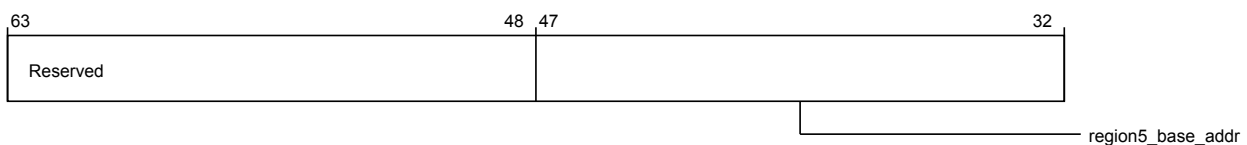


Figure 4-2400 `por_mpu_por_mpu_m7_prbar5` (high)

The following table shows the `por_mpu_m7_prbar5` higher register bit assignments.

Table 4-2417 `por_mpu_por_mpu_m7_prbar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

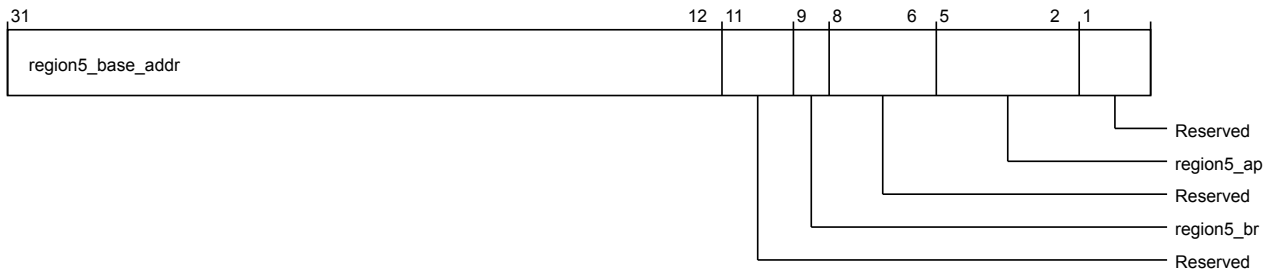


Figure 4-2401 por_mpu_por_mpu_m7_prbar5 (low)

The following table shows the por_mpu_m7_prbar5 lower register bit assignments.

Table 4-2418 por_mpu_por_mpu_m7_prbar5 (low)

Bits	Field name	Description	Type	Reset
31:12	region5_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region5_br	Region 5 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region5_ap	Region 5 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar5

MPU master 0 programmable limit address register 5.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C68

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

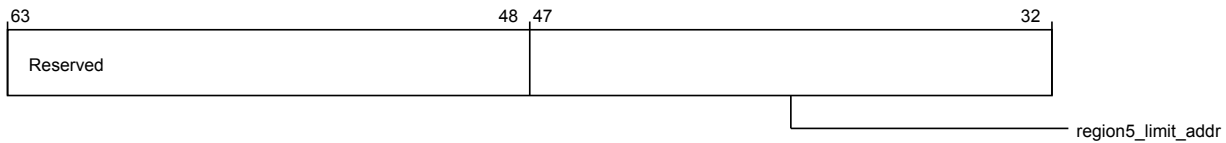


Figure 4-2402 `por_mpu_m7_prlar5` (high)

The following table shows the `por_mpu_m7_prlar5` higher register bit assignments.

Table 4-2419 `por_mpu_m7_prlar5` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region5_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

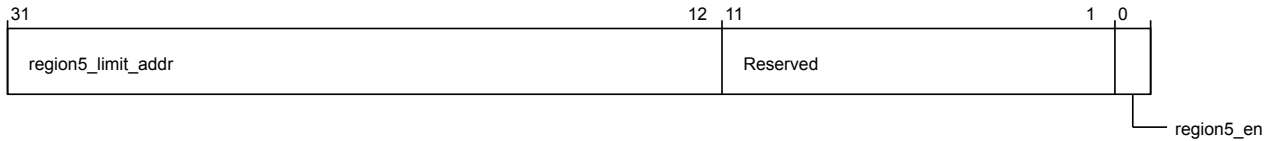


Figure 4-2403 `por_mpu_m7_prlar5` (low)

The following table shows the `por_mpu_m7_prlar5` lower register bit assignments.

Table 4-2420 `por_mpu_m7_prlar5` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region5_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region5_en</code>	Region 5 enable.	RW	1'b0

`por_mpu_m7_prbar6`

MPU master 0 programmable base address register 6.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2C70
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

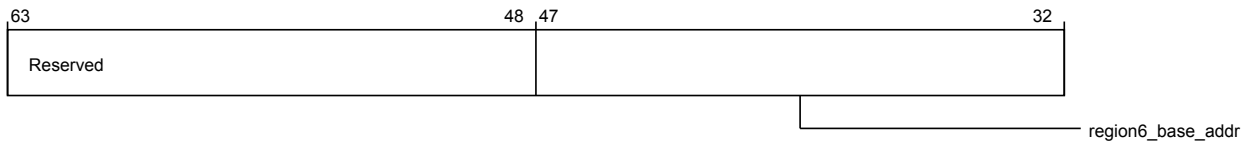


Figure 4-2404 por_mpu_por_mpu_m7_prbar6 (high)

The following table shows the por_mpu_m7_prbar6 higher register bit assignments.

Table 4-2421 por_mpu_por_mpu_m7_prbar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

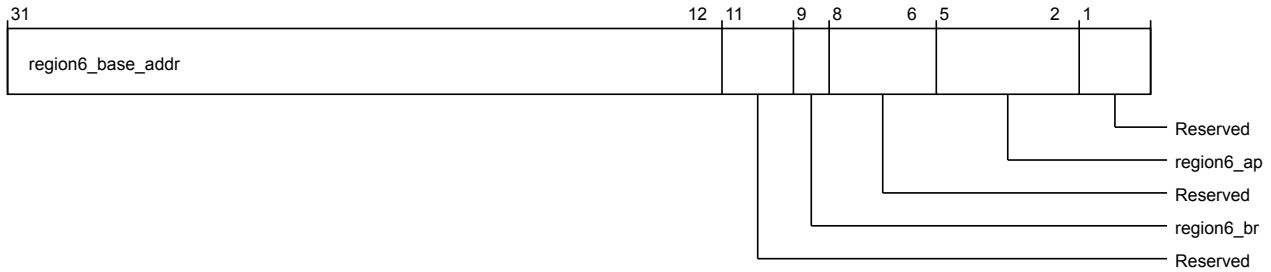


Figure 4-2405 por_mpu_por_mpu_m7_prbar6 (low)

The following table shows the por_mpu_m7_prbar6 lower register bit assignments.

Table 4-2422 por_mpu_por_mpu_m7_prbar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region6_br	Region 6 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region6_ap	Region 6 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar6

MPU master 0 programmable limit address register 6.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C78

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

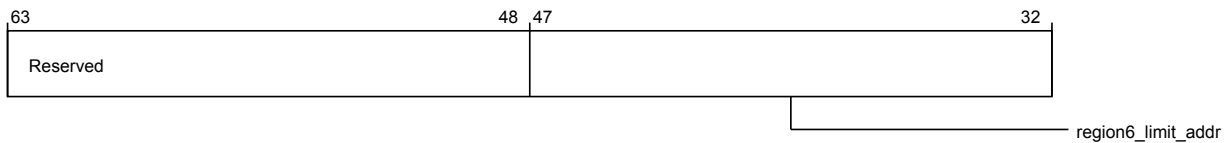


Figure 4-2406 por_mpu_por_mpu_m7_prlar6 (high)

The following table shows the por_mpu_m7_prlar6 higher register bit assignments.

Table 4-2423 por_mpu_por_mpu_m7_prlar6 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region6_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

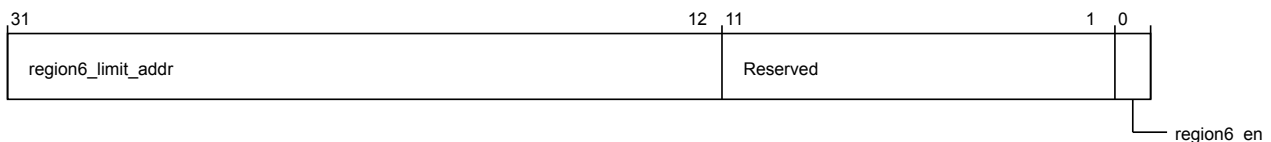


Figure 4-2407 por_mpu_por_mpu_m7_prlar6 (low)

The following table shows the por_mpu_m7_prlar6 lower register bit assignments.

Table 4-2424 por_mpu_por_mpu_m7_prlar6 (low)

Bits	Field name	Description	Type	Reset
31:12	region6_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region6_en	Region 6 enable.	RW	1'b0

por_mpu_m7_prbar7

MPU master 0 programmable base address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

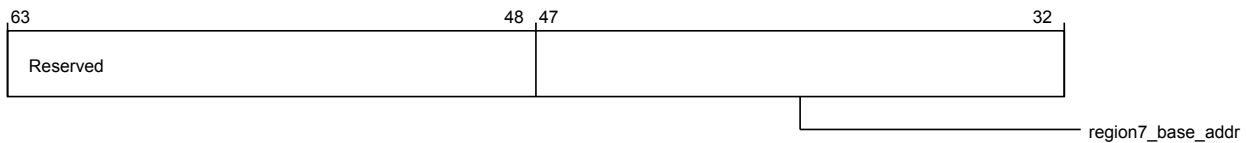


Figure 4-2408 por_mpu_por_mpu_m7_prbar7 (high)

The following table shows the `por_mpu_m7_prbar7` higher register bit assignments.

Table 4-2425 por_mpu_por_mpu_m7_prbar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

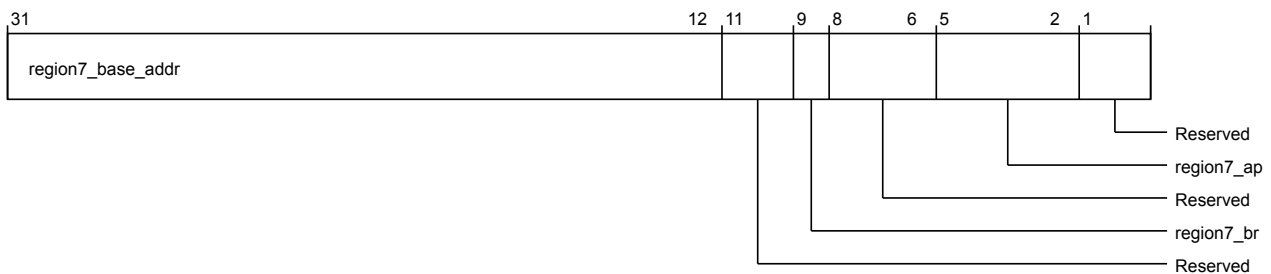


Figure 4-2409 por_mpu_por_mpu_m7_prbar7 (low)

The following table shows the `por_mpu_m7_prbar7` lower register bit assignments.

Table 4-2426 por_mpu_por_mpu_m7_prbar7 (low)

Bits	Field name	Description	Type	Reset
31:12	region7_base_addr	Bits [31:12] of base address of the range.	RW	16'b0
11:10	Reserved	Reserved	RO	-

Table 4-2426 por_mpu_por_mpu_m7_prbar7 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region7_br	Region 7 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region7_ap	Region 7 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar7

MPU master 0 programmable limit address register 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C88

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

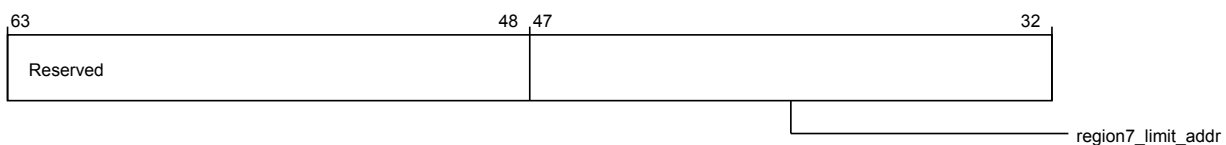


Figure 4-2410 por_mpu_por_mpu_m7_prlar7 (high)

The following table shows the por_mpu_m7_prlar7 higher register bit assignments.

Table 4-2427 por_mpu_por_mpu_m7_prlar7 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region7_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

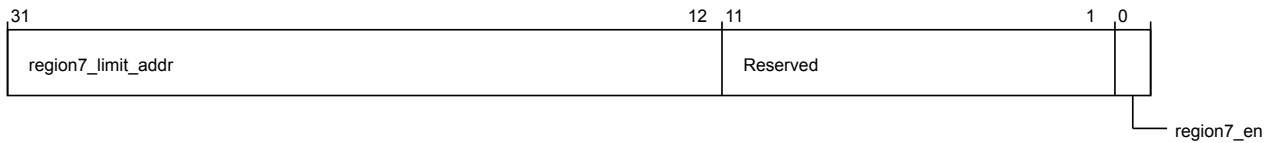


Figure 4-2411 `por_mpu_por_mpu_m7_prlar7` (low)

The following table shows the `por_mpu_m7_prlar7` lower register bit assignments.

Table 4-2428 `por_mpu_por_mpu_m7_prlar7` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region7_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region7_en</code>	Region 7 enable.	RW	1'b0

`por_mpu_m7_prbar8`

MPU master 0 programmable base address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C90

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

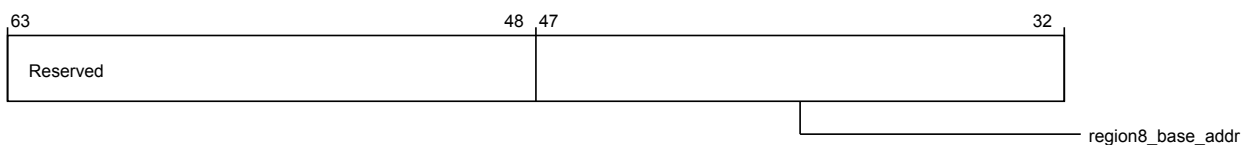


Figure 4-2412 `por_mpu_por_mpu_m7_prbar8` (high)

The following table shows the `por_mpu_m7_prbar8` higher register bit assignments.

Table 4-2429 `por_mpu_por_mpu_m7_prbar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

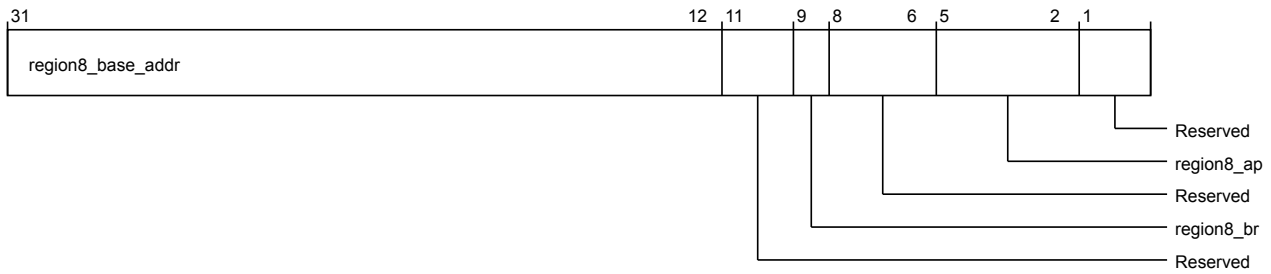


Figure 4-2413 por_mpu_por_mpu_m7_prbar8 (low)

The following table shows the por_mpu_m7_prbar8 lower register bit assignments.

Table 4-2430 por_mpu_por_mpu_m7_prbar8 (low)

Bits	Field name	Description	Type	Reset
31:12	region8_base_addr	Bits [32:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region8_br	Region 8 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region8_ap	Region 8 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar8

MPU master 0 programmable limit address register 8.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2C98

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

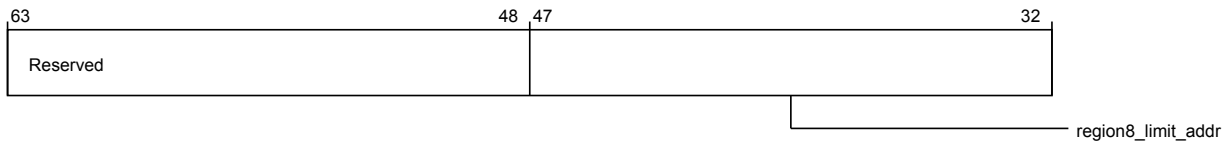


Figure 4-2414 `por_mpu_m7_prlar8` (high)

The following table shows the `por_mpu_m7_prlar8` higher register bit assignments.

Table 4-2431 `por_mpu_m7_prlar8` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region8_limit_addr</code>	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

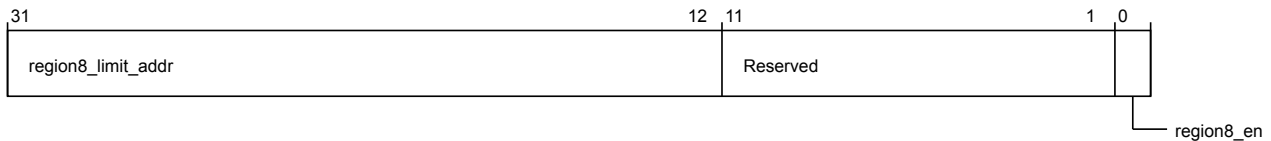


Figure 4-2415 `por_mpu_m7_prlar8` (low)

The following table shows the `por_mpu_m7_prlar8` lower register bit assignments.

Table 4-2432 `por_mpu_m7_prlar8` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region8_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region8_en</code>	Region 8 enable.	RW	1'b0

`por_mpu_m7_prbar9`

MPU master 0 programmable base address register 9.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2CA0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

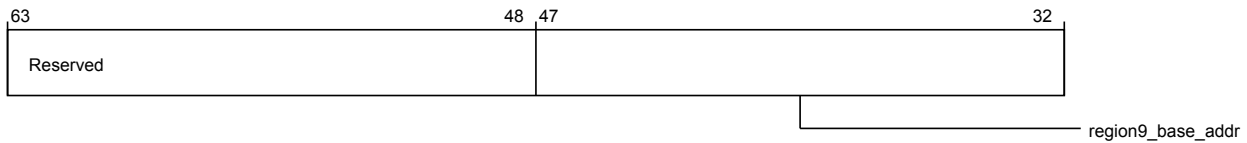


Figure 4-2416 por_mpu_por_mpu_m7_prbar9 (high)

The following table shows the por_mpu_m7_prbar9 higher register bit assignments.

Table 4-2433 por_mpu_por_mpu_m7_prbar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

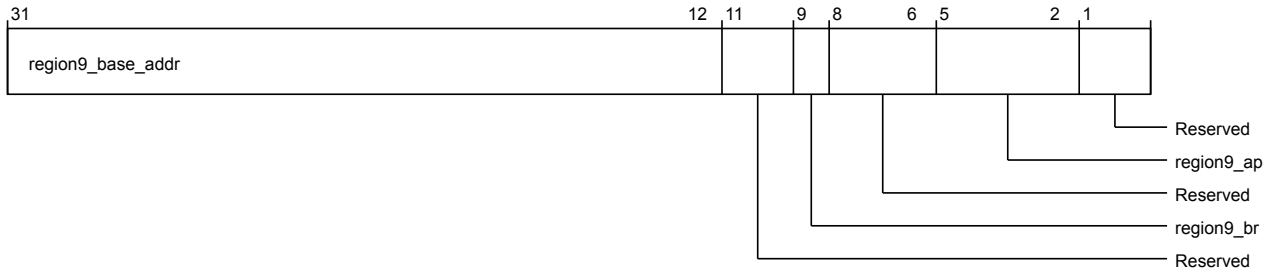


Figure 4-2417 por_mpu_por_mpu_m7_prbar9 (low)

The following table shows the por_mpu_m7_prbar9 lower register bit assignments.

Table 4-2434 por_mpu_por_mpu_m7_prbar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region9_br	Region 9 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region9_ap	Region 9 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar9

MPU master 0 programmable limit address register 9.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2CA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

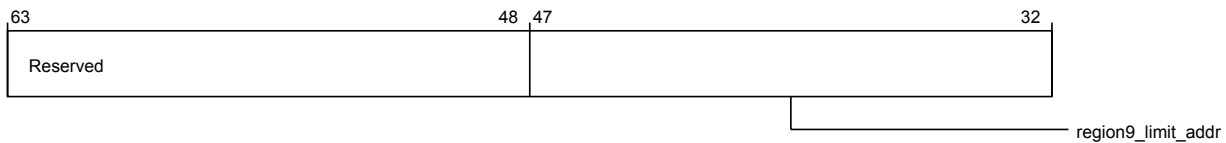


Figure 4-2418 por_mpu_por_mpu_m7_prlar9 (high)

The following table shows the por_mpu_m7_prlar9 higher register bit assignments.

Table 4-2435 por_mpu_por_mpu_m7_prlar9 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region9_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

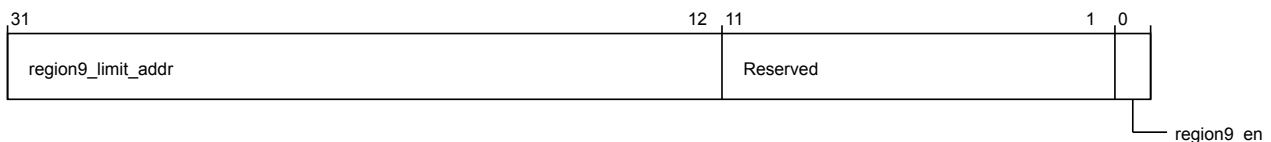


Figure 4-2419 por_mpu_por_mpu_m7_prlar9 (low)

The following table shows the por_mpu_m7_prlar9 lower register bit assignments.

Table 4-2436 por_mpu_por_mpu_m7_prlar9 (low)

Bits	Field name	Description	Type	Reset
31:12	region9_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region9_en	Region 9 enable.	RW	1'b0

por_mpu_m7_prbar10

MPU master 0 programmable base address register 10.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2CB0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

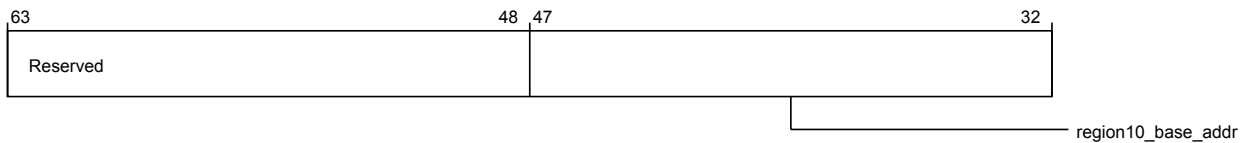


Figure 4-2420 por_mpu_por_mpu_m7_prbar10 (high)

The following table shows the por_mpu_m7_prbar10 higher register bit assignments.

Table 4-2437 por_mpu_por_mpu_m7_prbar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

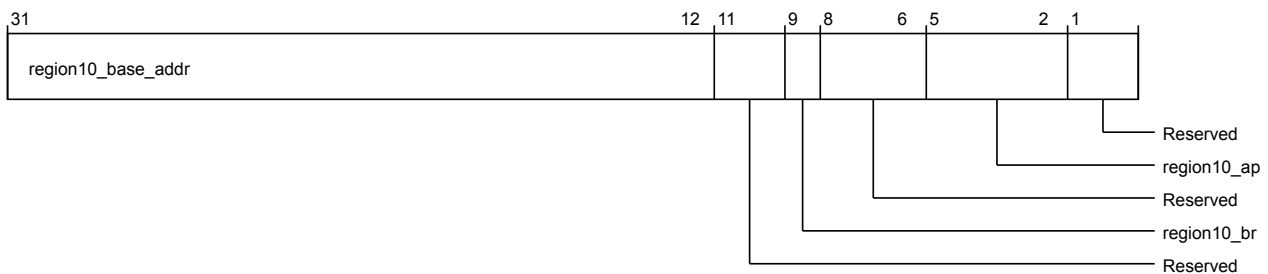


Figure 4-2421 por_mpu_por_mpu_m7_prbar10 (low)

The following table shows the por_mpu_m7_prbar10 lower register bit assignments.

Table 4-2438 por_mpu_por_mpu_m7_prbar10 (low)

Bits	Field name	Description	Type	Reset
31:12	region10_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2438 por_mpu_por_mpu_m7_prbar10 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region10_br	Region 10 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region10_ap	Region 10 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar10

MPU master 0 programmable limit address register 10.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2CB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

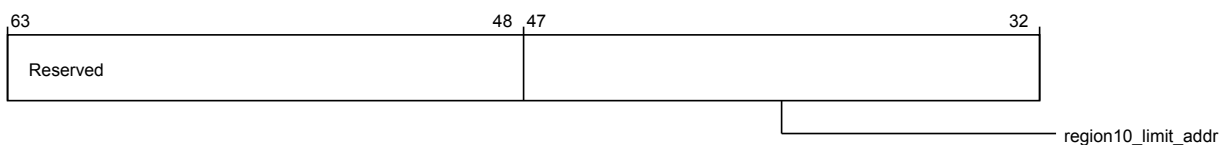


Figure 4-2422 por_mpu_por_mpu_m7_prlar10 (high)

The following table shows the por_mpu_m7_prlar10 higher register bit assignments.

Table 4-2439 por_mpu_por_mpu_m7_prlar10 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region10_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

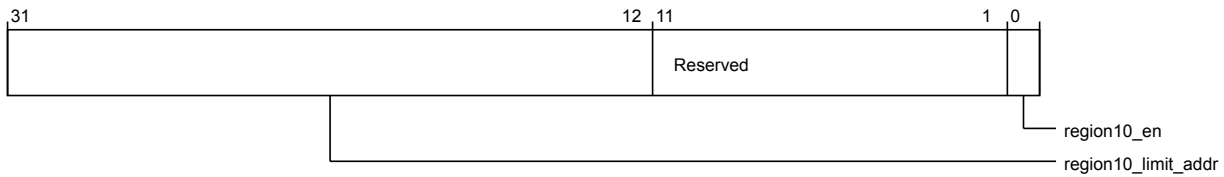


Figure 4-2423 `por_mpu_por_mpu_m7_prlar10` (low)

The following table shows the `por_mpu_m7_prlar10` lower register bit assignments.

Table 4-2440 `por_mpu_por_mpu_m7_prlar10` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region10_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region10_en</code>	Region 10 enable.	RW	1'b0

`por_mpu_m7_prbar11`

MPU master 0 programmable base address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2CC0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

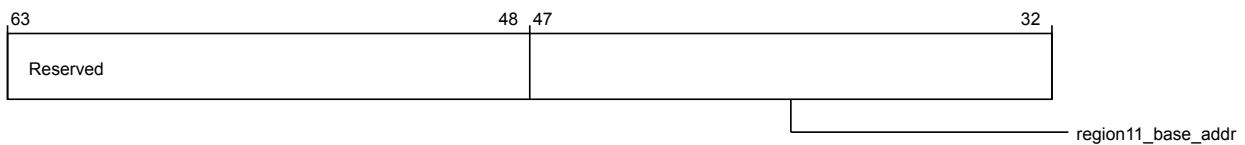


Figure 4-2424 `por_mpu_por_mpu_m7_prbar11` (high)

The following table shows the `por_mpu_m7_prbar11` higher register bit assignments.

Table 4-2441 `por_mpu_por_mpu_m7_prbar11` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region11_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

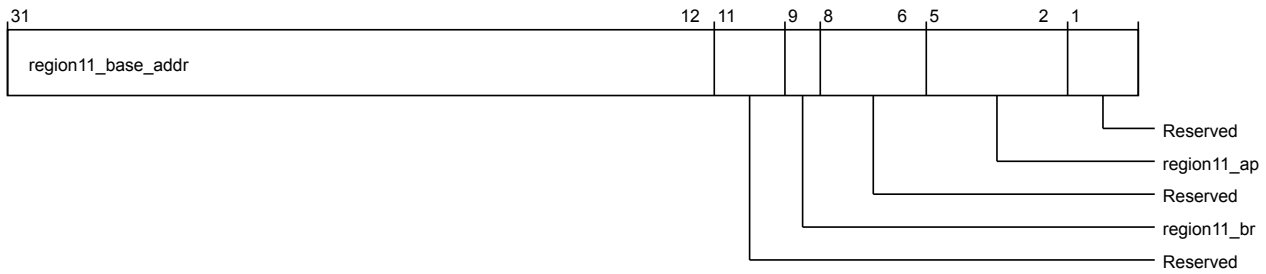


Figure 4-2425 por_mpu_por_mpu_m7_prbar11 (low)

The following table shows the por_mpu_m7_prbar11 lower register bit assignments.

Table 4-2442 por_mpu_por_mpu_m7_prbar11 (low)

Bits	Field name	Description	Type	Reset
31:12	region11_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region11_br	Region 11 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region11_ap	Region 11 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar11

MPU master 0 programmable limit address register 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2CC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

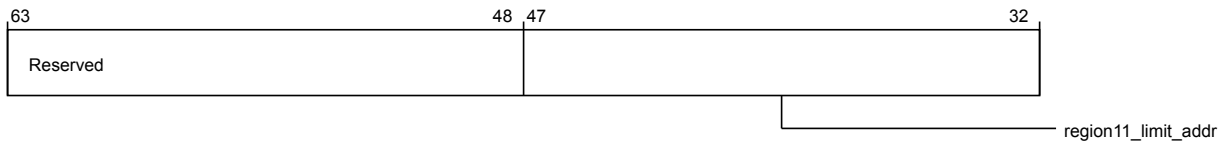


Figure 4-2426 por_mpu_por_mpu_m7_prlar11 (high)

The following table shows the por_mpu_m7_prlar11 higher register bit assignments.

Table 4-2443 por_mpu_por_mpu_m7_prlar11 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region11_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

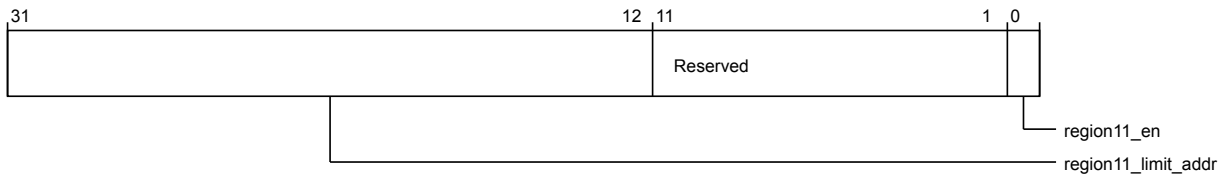


Figure 4-2427 por_mpu_por_mpu_m7_prlar11 (low)

The following table shows the por_mpu_m7_prlar11 lower register bit assignments.

Table 4-2444 por_mpu_por_mpu_m7_prlar11 (low)

Bits	Field name	Description	Type	Reset
31:12	region11_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region11_en	Region 11 enable.	RW	1'b0

por_mpu_m7_prbar12

MPU master 0 programmable base address register 12.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2CD0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

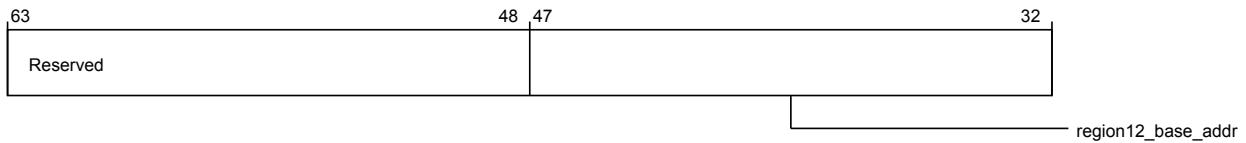


Figure 4-2428 `por_mpu_por_mpu_m7_prbar12` (high)

The following table shows the `por_mpu_m7_prbar12` higher register bit assignments.

Table 4-2445 `por_mpu_por_mpu_m7_prbar12` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region12_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

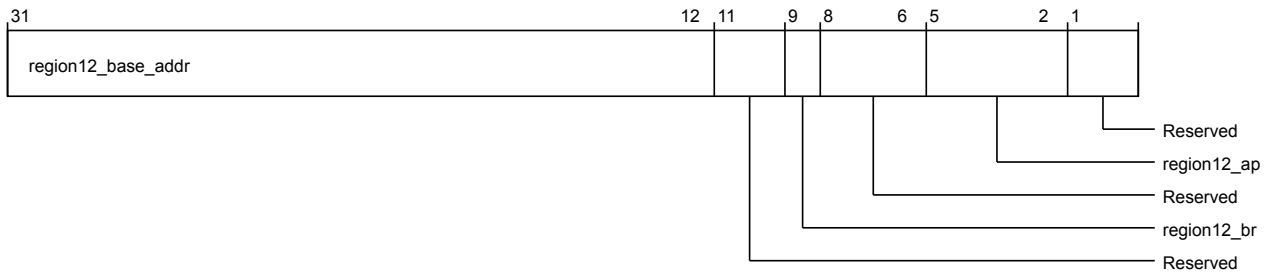


Figure 4-2429 `por_mpu_por_mpu_m7_prbar12` (low)

The following table shows the `por_mpu_m7_prbar12` lower register bit assignments.

Table 4-2446 `por_mpu_por_mpu_m7_prbar12` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region12_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region12_br</code>	Region 12 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region12_ap</code>	Region 12 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar12

MPU master 0 programmable limit address register 12.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2CD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

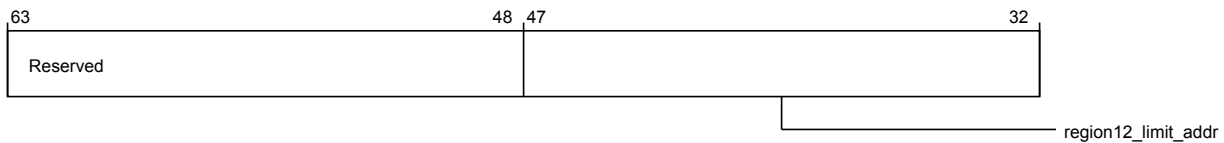


Figure 4-2430 por_mpu_por_mpu_m7_prlar12 (high)

The following table shows the por_mpu_m7_prlar12 higher register bit assignments.

Table 4-2447 por_mpu_por_mpu_m7_prlar12 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region12_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

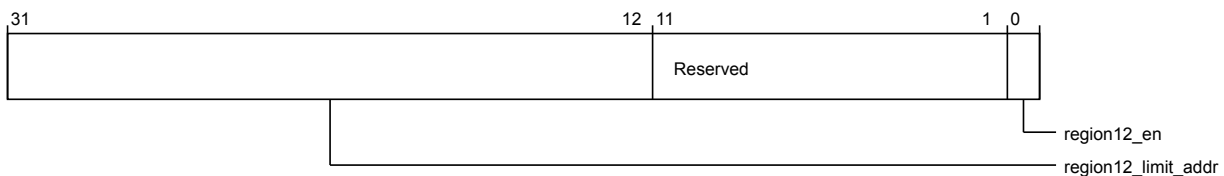


Figure 4-2431 por_mpu_por_mpu_m7_prlar12 (low)

The following table shows the por_mpu_m7_prlar12 lower register bit assignments.

Table 4-2448 por_mpu_por_mpu_m7_prlar12 (low)

Bits	Field name	Description	Type	Reset
31:12	region12_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region12_en	Region 12 enable.	RW	1'b0

por_mpu_m7_prbar13

MPU master 0 programmable base address register 13.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2CE0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

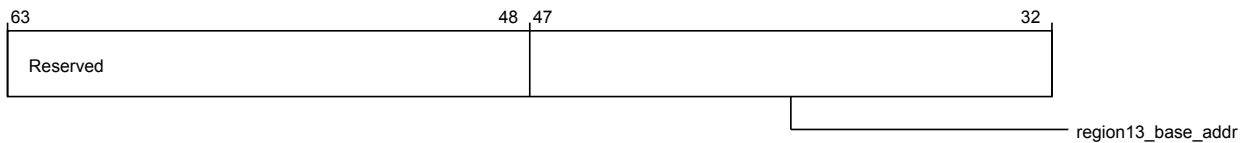


Figure 4-2432 por_mpu_por_mpu_m7_prbar13 (high)

The following table shows the por_mpu_m7_prbar13 higher register bit assignments.

Table 4-2449 por_mpu_por_mpu_m7_prbar13 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

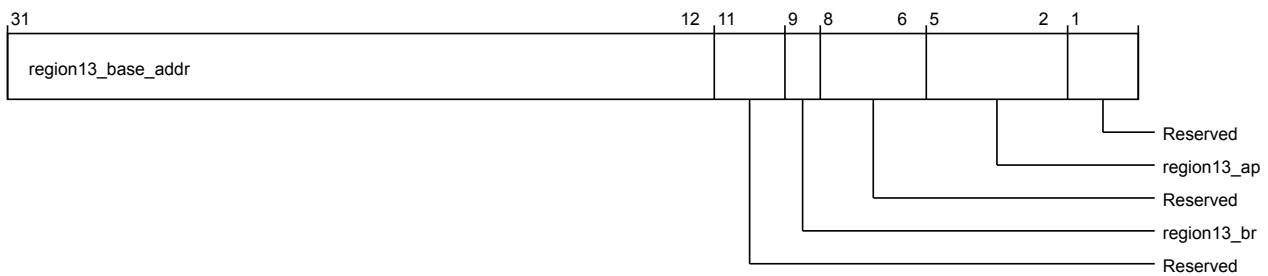


Figure 4-2433 por_mpu_por_mpu_m7_prbar13 (low)

The following table shows the por_mpu_m7_prbar13 lower register bit assignments.

Table 4-2450 por_mpu_por_mpu_m7_prbar13 (low)

Bits	Field name	Description	Type	Reset
31:12	region13_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2450 `por_mpu_por_mpu_m7_prbar13` (low) (continued)

Bits	Field name	Description	Type	Reset
9	region13_br	Region 13 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region13_ap	Region 13 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m7_prlar13`

MPU master 0 programmable limit address register 13.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2CE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

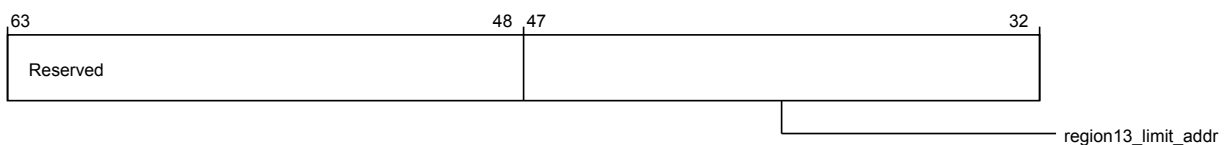


Figure 4-2434 `por_mpu_por_mpu_m7_prlar13` (high)

The following table shows the `por_mpu_m7_prlar13` higher register bit assignments.

Table 4-2451 `por_mpu_por_mpu_m7_prlar13` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region13_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

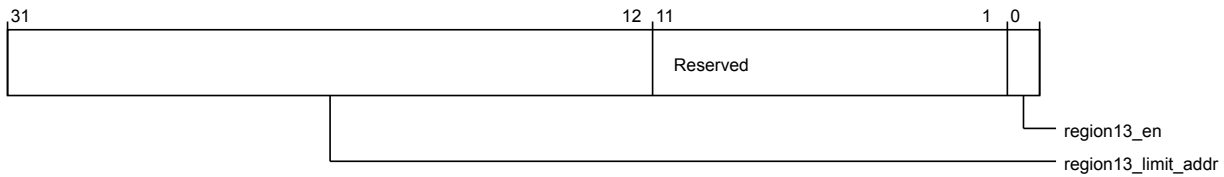


Figure 4-2435 `por_mpu_por_mpu_m7_prlar13` (low)

The following table shows the `por_mpu_m7_prlar13` lower register bit assignments.

Table 4-2452 `por_mpu_por_mpu_m7_prlar13` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region13_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region13_en</code>	Region 13 enable.	RW	1'b0

`por_mpu_m7_prbar14`

MPU master 0 programmable base address register 14.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2CF0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

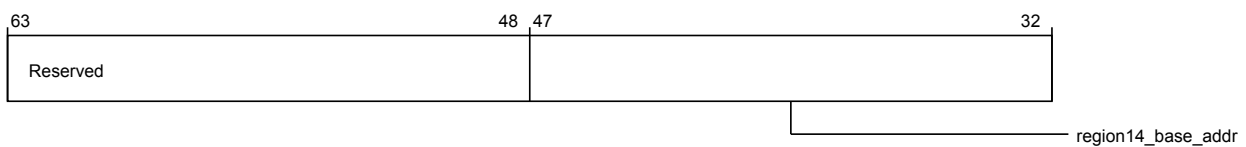


Figure 4-2436 `por_mpu_por_mpu_m7_prbar14` (high)

The following table shows the `por_mpu_m7_prbar14` higher register bit assignments.

Table 4-2453 `por_mpu_por_mpu_m7_prbar14` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region14_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

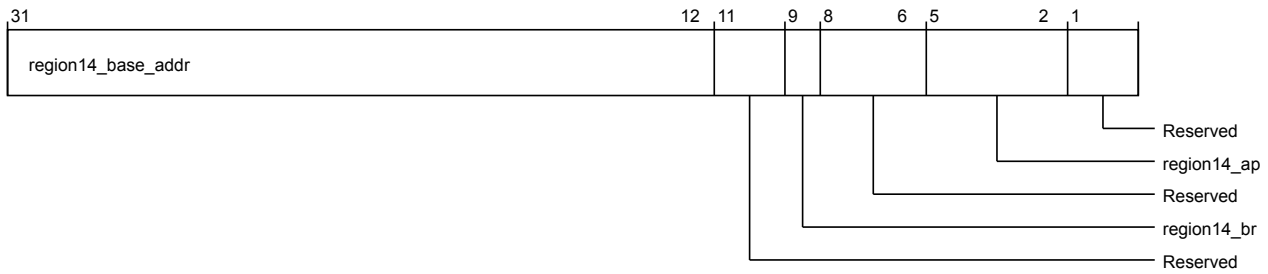


Figure 4-2437 `por_mpu_m7_prbar14` (low)

The following table shows the `por_mpu_m7_prbar14` lower register bit assignments.

Table 4-2454 `por_mpu_m7_prbar14` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region14_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region14_br</code>	Region 14 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region14_ap</code>	Region 14 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m7_prlar14`

MPU master 0 programmable limit address register 14.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2CF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

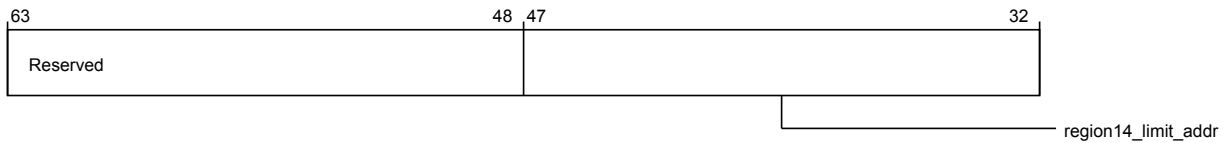


Figure 4-2438 por_mpu_m7_prlar14 (high)

The following table shows the por_mpu_m7_prlar14 higher register bit assignments.

Table 4-2455 por_mpu_m7_prlar14 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region14_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

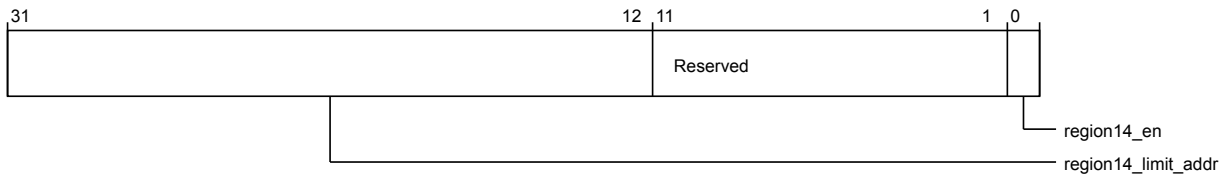


Figure 4-2439 por_mpu_m7_prlar14 (low)

The following table shows the por_mpu_m7_prlar14 lower register bit assignments.

Table 4-2456 por_mpu_m7_prlar14 (low)

Bits	Field name	Description	Type	Reset
31:12	region14_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region14_en	Region 14 enable.	RW	1'b0

por_mpu_m7_prbar15

MPU master 0 programmable base address register 15.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2D00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

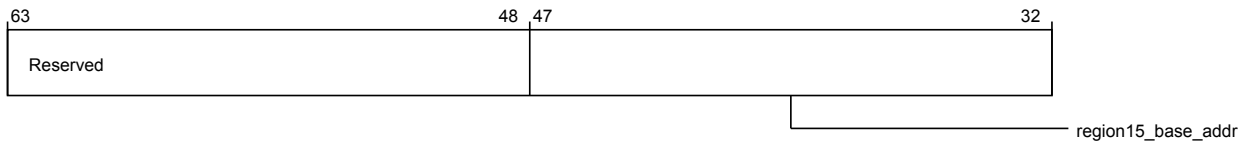


Figure 4-2440 por_mpu_por_mpu_m7_prbar15 (high)

The following table shows the por_mpu_m7_prbar15 higher register bit assignments.

Table 4-2457 por_mpu_por_mpu_m7_prbar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

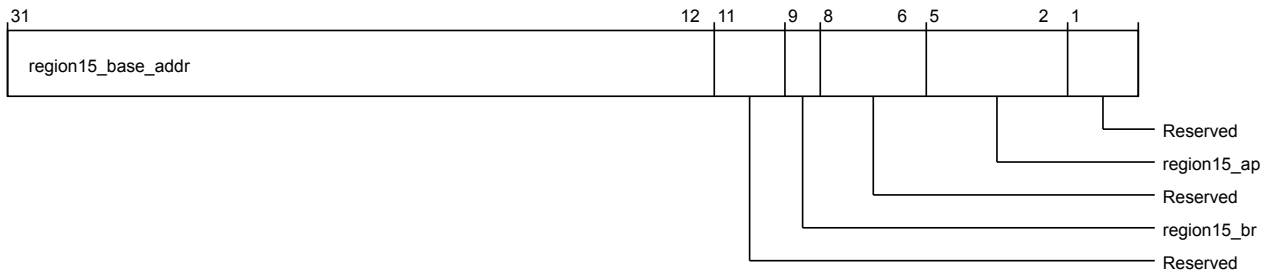


Figure 4-2441 por_mpu_por_mpu_m7_prbar15 (low)

The following table shows the por_mpu_m7_prbar15 lower register bit assignments.

Table 4-2458 por_mpu_por_mpu_m7_prbar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region15_br	Region 15 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region15_ap	Region 15 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar15

MPU master 0 programmable limit address register 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

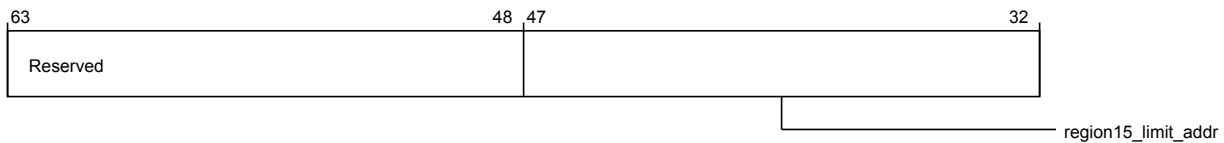


Figure 4-2442 por_mpu_por_mpu_m7_prlar15 (high)

The following table shows the por_mpu_m7_prlar15 higher register bit assignments.

Table 4-2459 por_mpu_por_mpu_m7_prlar15 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region15_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

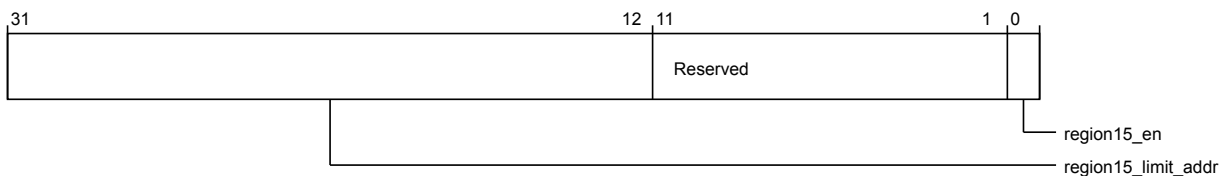


Figure 4-2443 por_mpu_por_mpu_m7_prlar15 (low)

The following table shows the por_mpu_m7_prlar15 lower register bit assignments.

Table 4-2460 por_mpu_por_mpu_m7_prlar15 (low)

Bits	Field name	Description	Type	Reset
31:12	region15_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region15_en	Region 15 enable.	RW	1'b0

por_mpu_m7_prbar16

MPU master 0 programmable base address register 16.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2D10
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

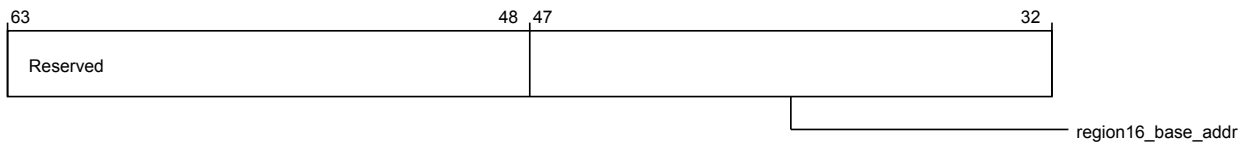


Figure 4-2444 por_mpu_por_mpu_m7_prbar16 (high)

The following table shows the por_mpu_m7_prbar16 higher register bit assignments.

Table 4-2461 por_mpu_por_mpu_m7_prbar16 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

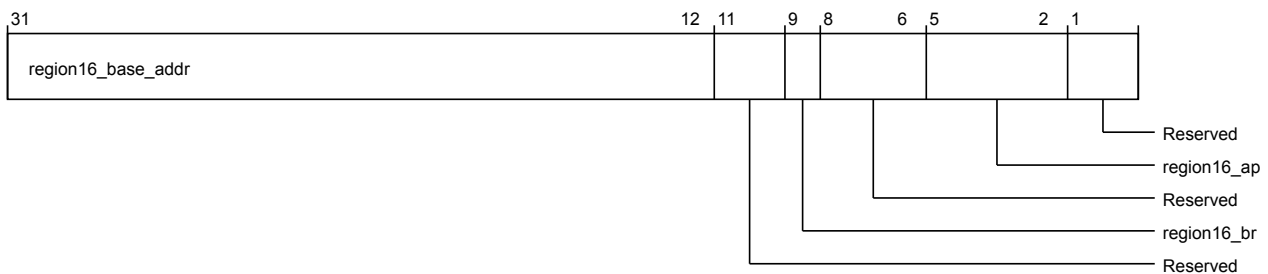


Figure 4-2445 por_mpu_por_mpu_m7_prbar16 (low)

The following table shows the por_mpu_m7_prbar16 lower register bit assignments.

Table 4-2462 por_mpu_por_mpu_m7_prbar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2462 `por_mpu_por_mpu_m7_prbar16` (low) (continued)

Bits	Field name	Description	Type	Reset
9	region16_br	Region 16 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region16_ap	Region 16 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m7_prlar16`

MPU master 0 programmable limit address register 16.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D18

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

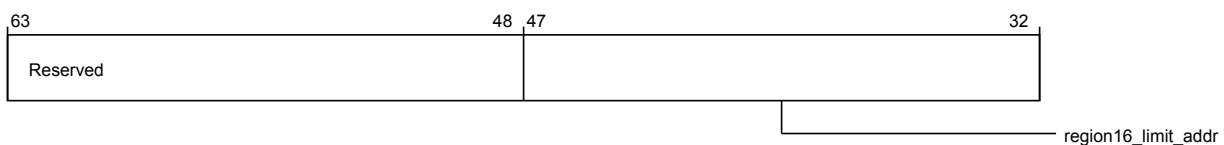


Figure 4-2446 `por_mpu_por_mpu_m7_prlar16` (high)

The following table shows the `por_mpu_m7_prlar16` higher register bit assignments.

Table 4-2463 `por_mpu_por_mpu_m7_prlar16` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region16_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

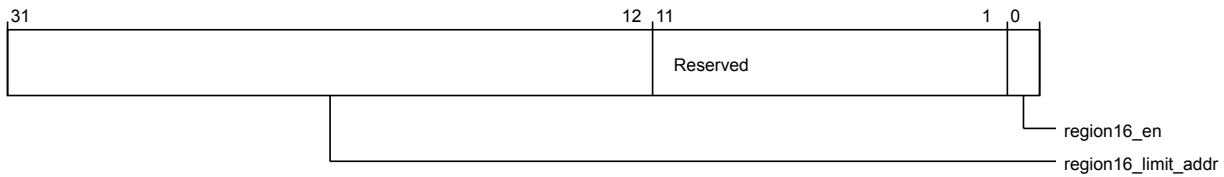


Figure 4-2447 por_mpu_por_mpu_m7_prlar16 (low)

The following table shows the por_mpu_m7_prlar16 lower register bit assignments.

Table 4-2464 por_mpu_por_mpu_m7_prlar16 (low)

Bits	Field name	Description	Type	Reset
31:12	region16_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region16_en	Region 16 enable.	RW	1'b0

por_mpu_m7_prbar17

MPU master 0 programmable base address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D20

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

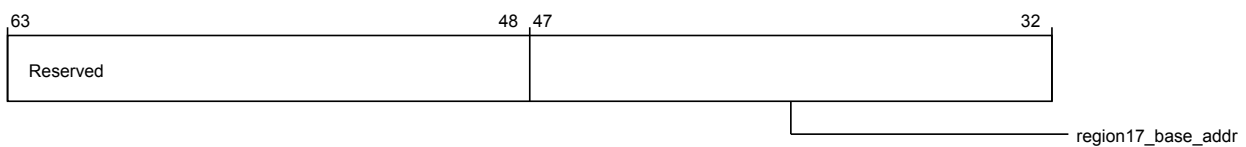


Figure 4-2448 por_mpu_por_mpu_m7_prbar17 (high)

The following table shows the por_mpu_m7_prbar17 higher register bit assignments.

Table 4-2465 por_mpu_por_mpu_m7_prbar17 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

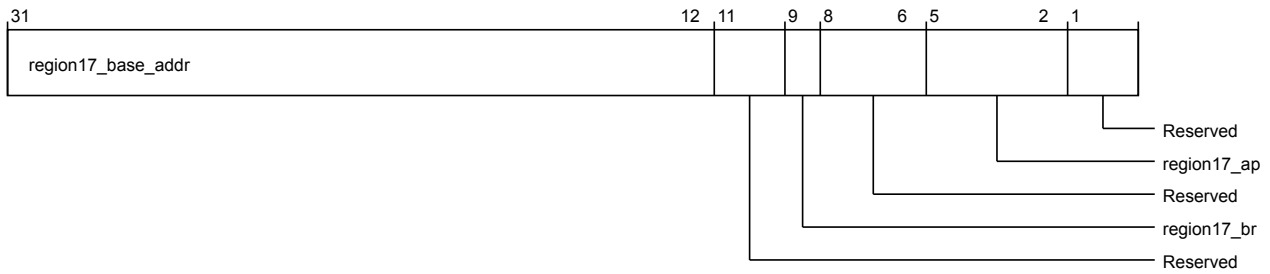


Figure 4-2449 `por_mpu_m7_prbar17` (low)

The following table shows the `por_mpu_m7_prbar17` lower register bit assignments.

Table 4-2466 `por_mpu_m7_prbar17` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region17_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region17_br</code>	Region 17 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region17_ap</code>	Region 17 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m7_prlar17`

MPU master 0 programmable limit address register 17.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D28

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

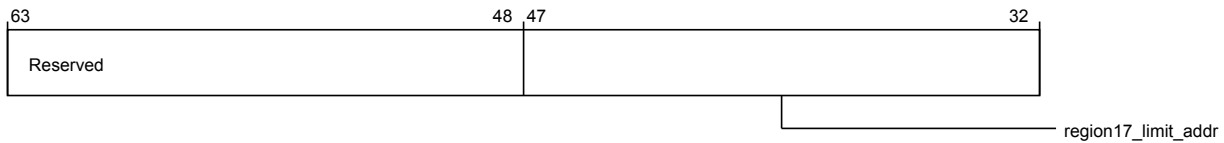


Figure 4-2450 por_mpu_m7_prlar17 (high)

The following table shows the por_mpu_m7_prlar17 higher register bit assignments.

Table 4-2467 por_mpu_m7_prlar17 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region17_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

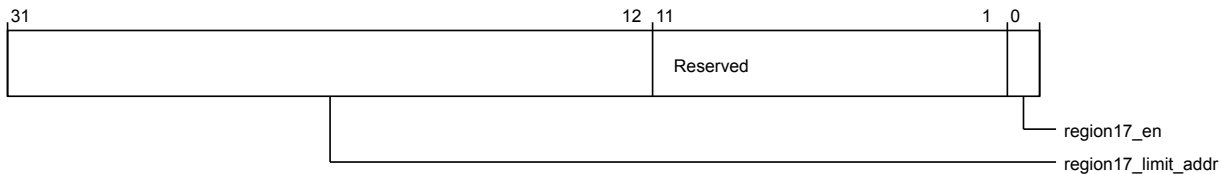


Figure 4-2451 por_mpu_m7_prlar17 (low)

The following table shows the por_mpu_m7_prlar17 lower register bit assignments.

Table 4-2468 por_mpu_m7_prlar17 (low)

Bits	Field name	Description	Type	Reset
31:12	region17_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region17_en	Region 17 enable.	RW	1'b0

por_mpu_m7_prbar18

MPU master 0 programmable base address register 18.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2D30
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

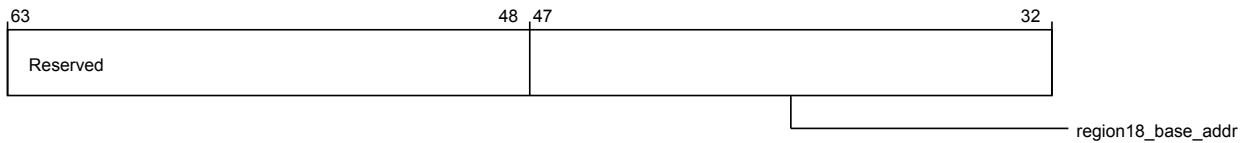


Figure 4-2452 `por_mpu_por_mpu_m7_prbar18` (high)

The following table shows the `por_mpu_m7_prbar18` higher register bit assignments.

Table 4-2469 `por_mpu_por_mpu_m7_prbar18` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

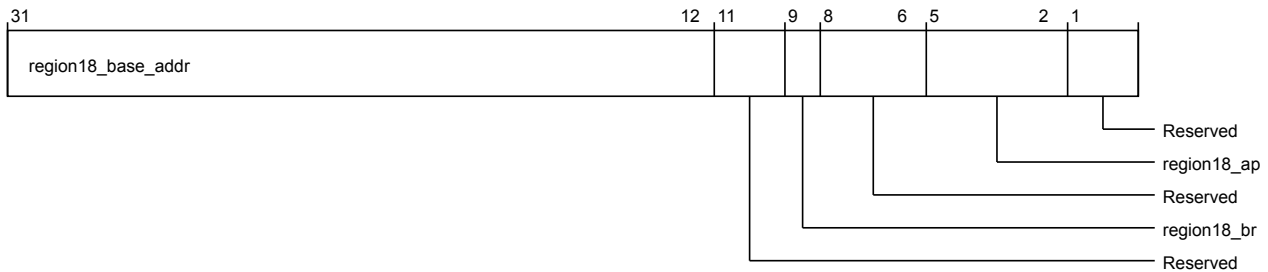


Figure 4-2453 `por_mpu_por_mpu_m7_prbar18` (low)

The following table shows the `por_mpu_m7_prbar18` lower register bit assignments.

Table 4-2470 `por_mpu_por_mpu_m7_prbar18` (low)

Bits	Field name	Description	Type	Reset
31:12	region18_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region18_br	Region 18 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region18_ap	Region 18 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar18

MPU master 0 programmable limit address register 18.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D38

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

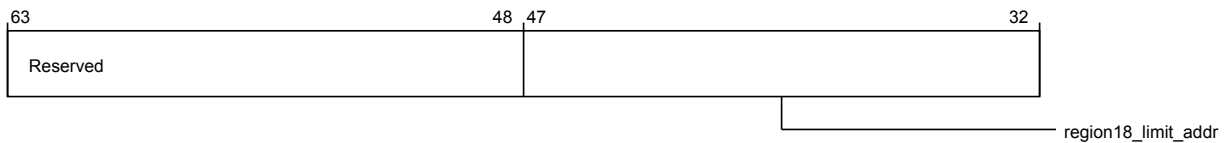


Figure 4-2454 por_mpu_por_mpu_m7_prlar18 (high)

The following table shows the por_mpu_m7_prlar18 higher register bit assignments.

Table 4-2471 por_mpu_por_mpu_m7_prlar18 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region18_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

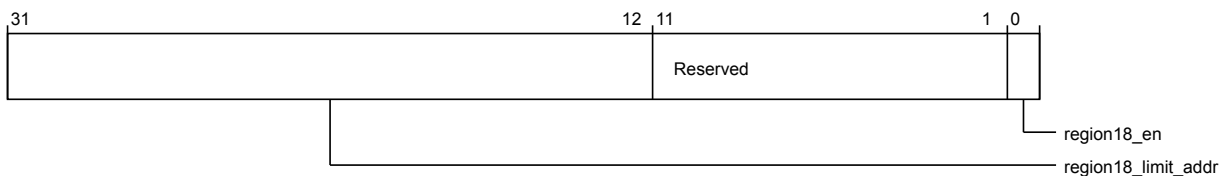


Figure 4-2455 por_mpu_por_mpu_m7_prlar18 (low)

The following table shows the por_mpu_m7_prlar18 lower register bit assignments.

Table 4-2472 por_mpu_por_mpu_m7_prlar18 (low)

Bits	Field name	Description	Type	Reset
31:12	region18_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region18_en	Region 18 enable.	RW	1'b0

por_mpu_m7_prbar19

MPU master 0 programmable base address register 19.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2D40
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

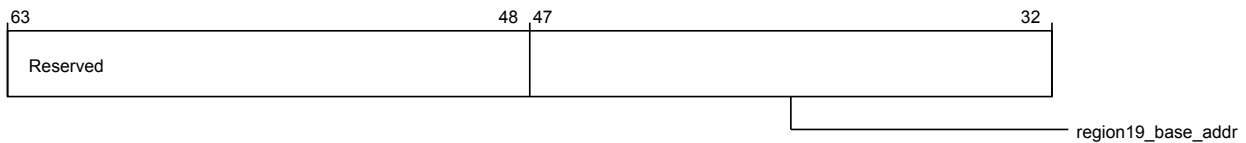


Figure 4-2456 por_mpu_por_mpu_m7_prbar19 (high)

The following table shows the por_mpu_m7_prbar19 higher register bit assignments.

Table 4-2473 por_mpu_por_mpu_m7_prbar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

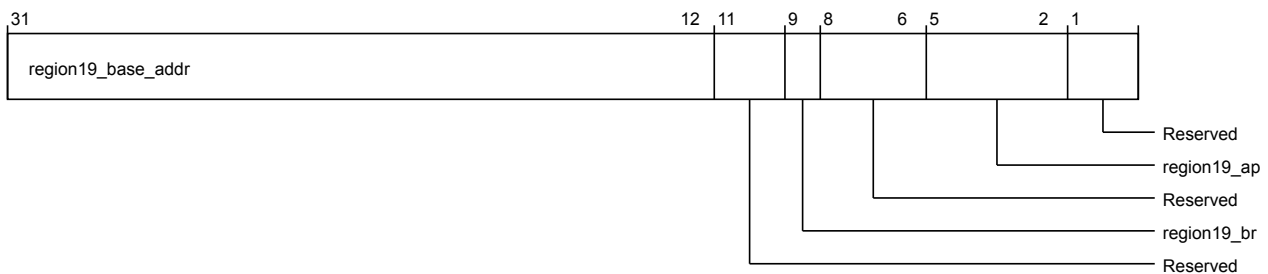


Figure 4-2457 por_mpu_por_mpu_m7_prbar19 (low)

The following table shows the por_mpu_m7_prbar19 lower register bit assignments.

Table 4-2474 por_mpu_por_mpu_m7_prbar19 (low)

Bits	Field name	Description	Type	Reset
31:12	region19_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2474 por_mpu_por_mpu_m7_prbar19 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region19_br	Region 19 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region19_ap	Region 19 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar19

MPU master 0 programmable limit address register 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D48

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

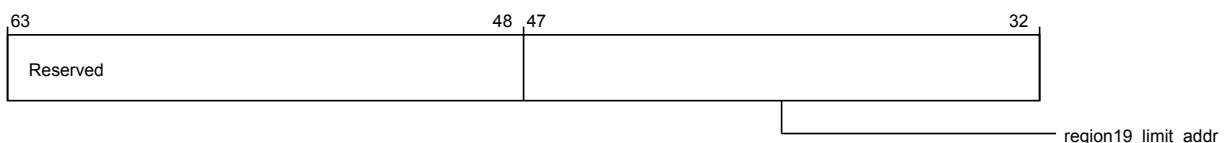


Figure 4-2458 por_mpu_por_mpu_m7_prlar19 (high)

The following table shows the por_mpu_m7_prlar19 higher register bit assignments.

Table 4-2475 por_mpu_por_mpu_m7_prlar19 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region19_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

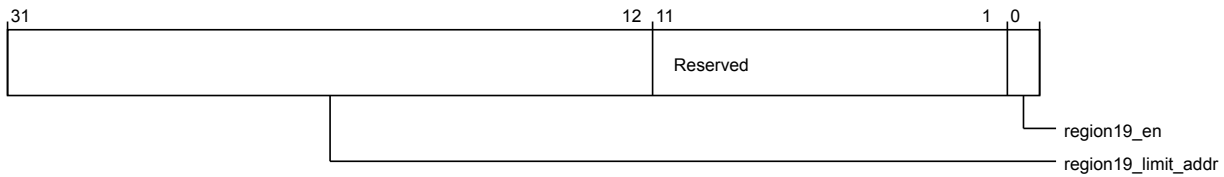


Figure 4-2459 `por_mpu_por_mpu_m7_prlar19` (low)

The following table shows the `por_mpu_m7_prlar19` lower register bit assignments.

Table 4-2476 `por_mpu_por_mpu_m7_prlar19` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region19_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region19_en</code>	Region 19 enable.	RW	1'b0

`por_mpu_m7_prbar20`

MPU master 0 programmable base address register 20.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2D50
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

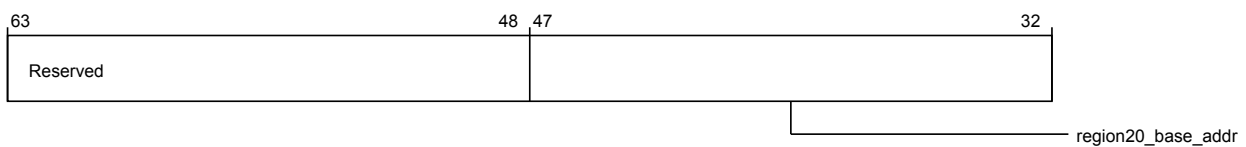


Figure 4-2460 `por_mpu_por_mpu_m7_prbar20` (high)

The following table shows the `por_mpu_m7_prbar20` higher register bit assignments.

Table 4-2477 `por_mpu_por_mpu_m7_prbar20` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region20_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

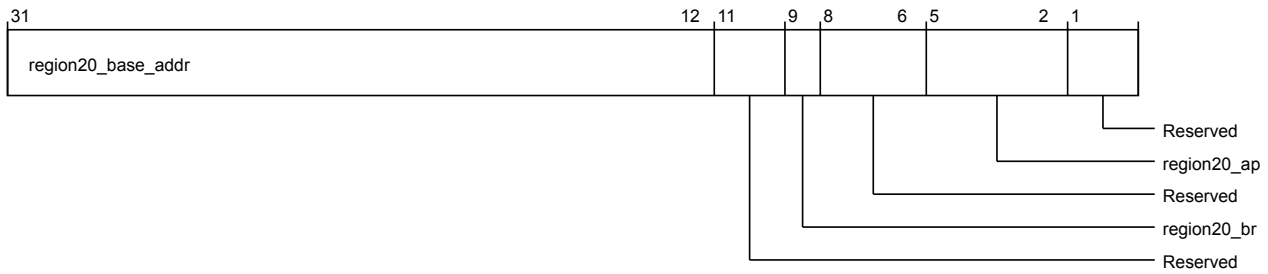


Figure 4-2461 `por_mpu_m7_prbar20` (low)

The following table shows the `por_mpu_m7_prbar20` lower register bit assignments.

Table 4-2478 `por_mpu_m7_prbar20` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region20_base_addr</code>	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	<code>region20_br</code>	Region 20 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	<code>region20_ap</code>	Region 20 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m7_prlar20`

MPU master 0 programmable limit address register 20.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D58

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

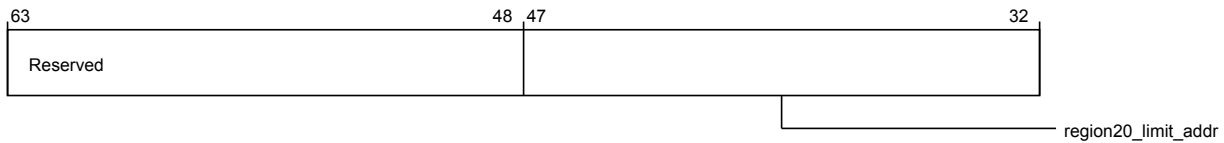


Figure 4-2462 por_mpu_m7_prlar20 (high)

The following table shows the por_mpu_m7_prlar20 higher register bit assignments.

Table 4-2479 por_mpu_m7_prlar20 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region20_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

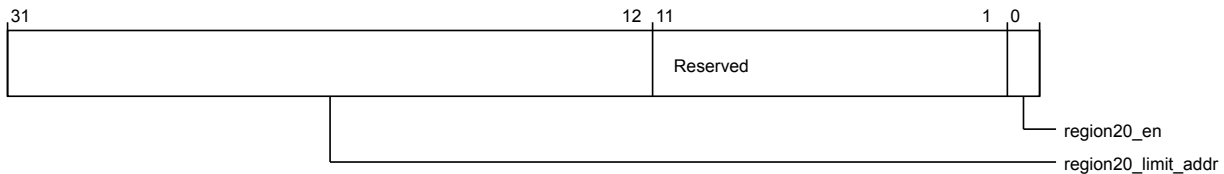


Figure 4-2463 por_mpu_m7_prlar20 (low)

The following table shows the por_mpu_m7_prlar20 lower register bit assignments.

Table 4-2480 por_mpu_m7_prlar20 (low)

Bits	Field name	Description	Type	Reset
31:12	region20_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region20_en	Region 20 enable.	RW	1'b0

por_mpu_m7_prbar21

MPU master 0 programmable base address register 21.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2D60
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

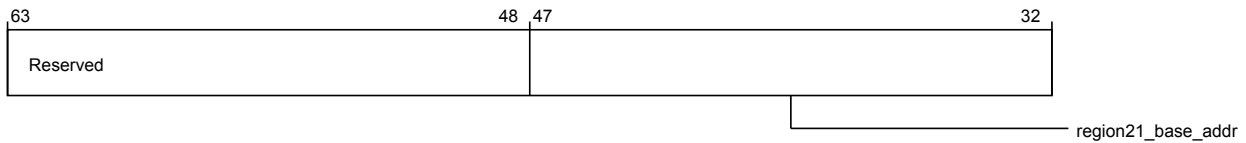


Figure 4-2464 por_mpu_por_mpu_m7_prbar21 (high)

The following table shows the por_mpu_m7_prbar21 higher register bit assignments.

Table 4-2481 por_mpu_por_mpu_m7_prbar21 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

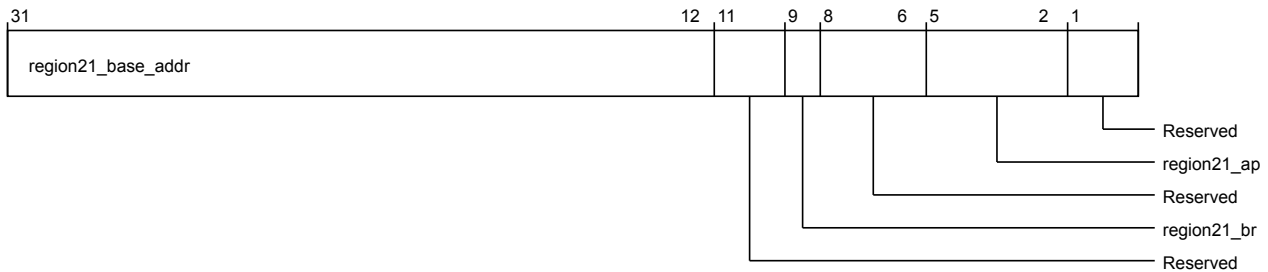


Figure 4-2465 por_mpu_por_mpu_m7_prbar21 (low)

The following table shows the por_mpu_m7_prbar21 lower register bit assignments.

Table 4-2482 por_mpu_por_mpu_m7_prbar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region21_br	Region 21 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region21_ap	Region 21 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar21

MPU master 0 programmable limit address register 21.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2D68
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

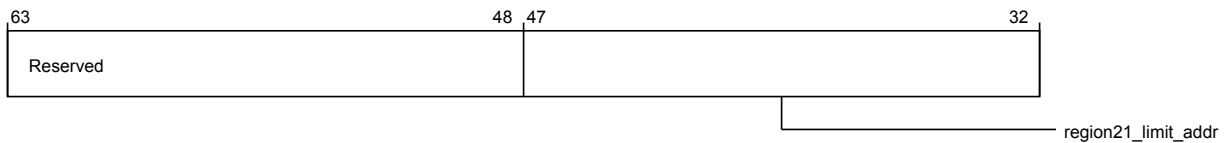


Figure 4-2466 por_mpu_por_mpu_m7_prlar21 (high)

The following table shows the `por_mpu_m7_prlar21` higher register bit assignments.

Table 4-2483 por_mpu_por_mpu_m7_prlar21 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region21_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

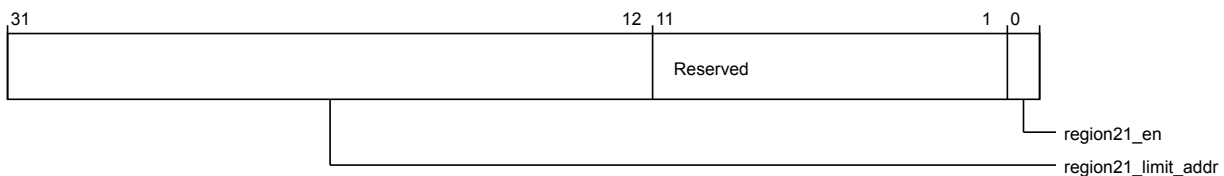


Figure 4-2467 por_mpu_por_mpu_m7_prlar21 (low)

The following table shows the `por_mpu_m7_prlar21` lower register bit assignments.

Table 4-2484 por_mpu_por_mpu_m7_prlar21 (low)

Bits	Field name	Description	Type	Reset
31:12	region21_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region21_en	Region 21 enable.	RW	1'b0

por_mpu_m7_prbar22

MPU master 0 programmable base address register 22.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2D70
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

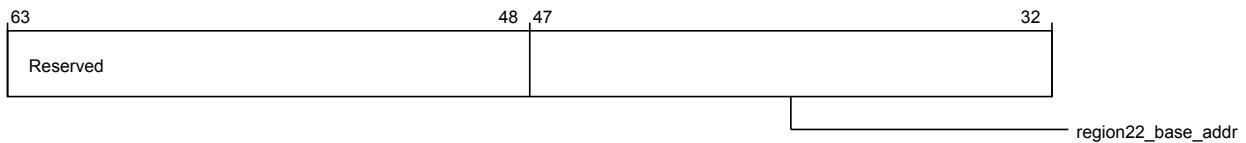


Figure 4-2468 por_mpu_por_mpu_m7_prbar22 (high)

The following table shows the por_mpu_m7_prbar22 higher register bit assignments.

Table 4-2485 por_mpu_por_mpu_m7_prbar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

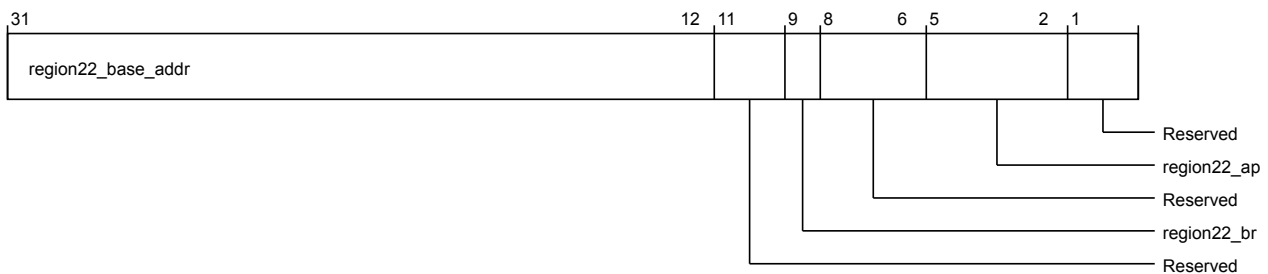


Figure 4-2469 por_mpu_por_mpu_m7_prbar22 (low)

The following table shows the por_mpu_m7_prbar22 lower register bit assignments.

Table 4-2486 por_mpu_por_mpu_m7_prbar22 (low)

Bits	Field name	Description	Type	Reset
31:12	region22_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2486 por_mpu_por_mpu_m7_prbar22 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region22_br	Region 22 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region22_ap	Region 22 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar22

MPU master 0 programmable limit address register 22.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D78

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

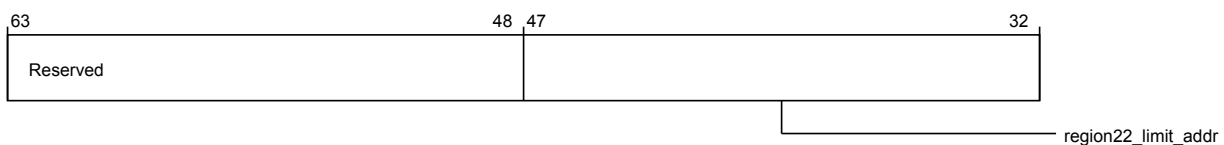


Figure 4-2470 por_mpu_por_mpu_m7_prlar22 (high)

The following table shows the por_mpu_m7_prlar22 higher register bit assignments.

Table 4-2487 por_mpu_por_mpu_m7_prlar22 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region22_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

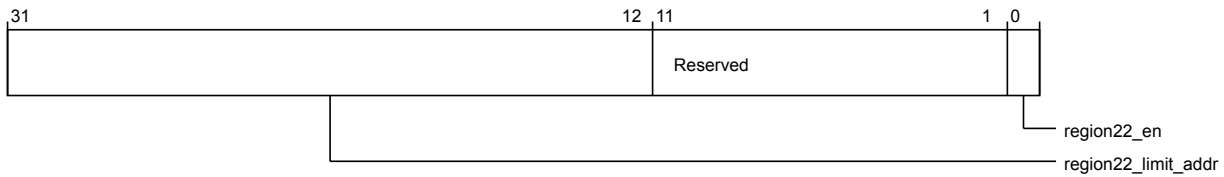


Figure 4-2471 `por_mpu_por_mpu_m7_prlar22` (low)

The following table shows the `por_mpu_m7_prlar22` lower register bit assignments.

Table 4-2488 `por_mpu_por_mpu_m7_prlar22` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region22_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region22_en</code>	Region 22 enable.	RW	1'b0

`por_mpu_m7_prbar23`

MPU master 0 programmable base address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

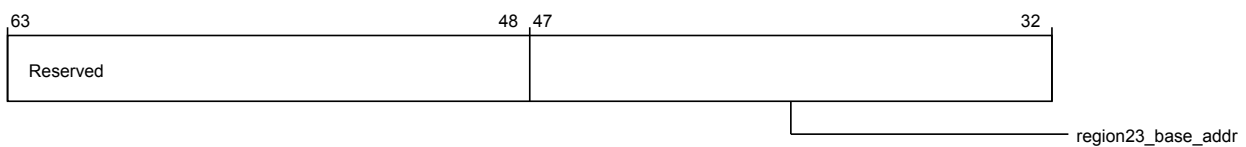


Figure 4-2472 `por_mpu_por_mpu_m7_prbar23` (high)

The following table shows the `por_mpu_m7_prbar23` higher register bit assignments.

Table 4-2489 `por_mpu_por_mpu_m7_prbar23` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region23_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

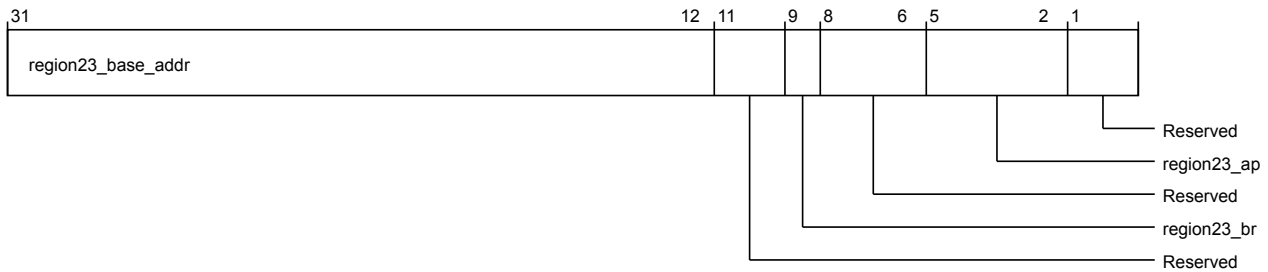


Figure 4-2473 por_mpu_por_mpu_m7_prbar23 (low)

The following table shows the por_mpu_m7_prbar23 lower register bit assignments.

Table 4-2490 por_mpu_por_mpu_m7_prbar23 (low)

Bits	Field name	Description	Type	Reset
31:12	region23_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region23_br	Region 23 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region23_ap	Region 23 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar23

MPU master 0 programmable limit address register 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D88

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

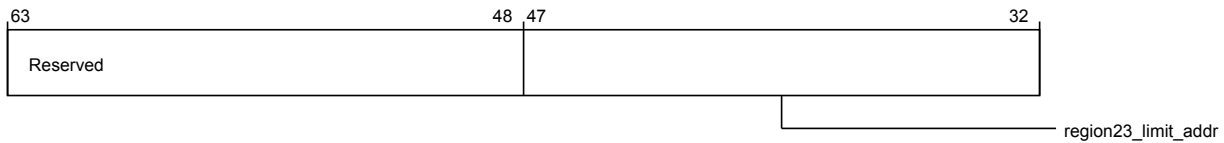


Figure 4-2474 por_mpu_m7_prlar23 (high)

The following table shows the por_mpu_m7_prlar23 higher register bit assignments.

Table 4-2491 por_mpu_m7_prlar23 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region23_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

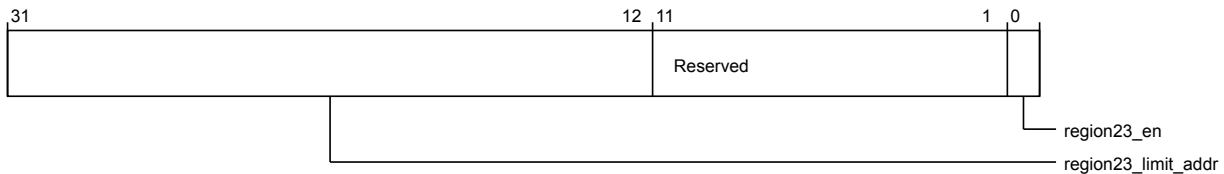


Figure 4-2475 por_mpu_m7_prlar23 (low)

The following table shows the por_mpu_m7_prlar23 lower register bit assignments.

Table 4-2492 por_mpu_m7_prlar23 (low)

Bits	Field name	Description	Type	Reset
31:12	region23_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region23_en	Region 23 enable.	RW	1'b0

por_mpu_m7_prbar24

MPU master 0 programmable base address register 24.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2D90
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

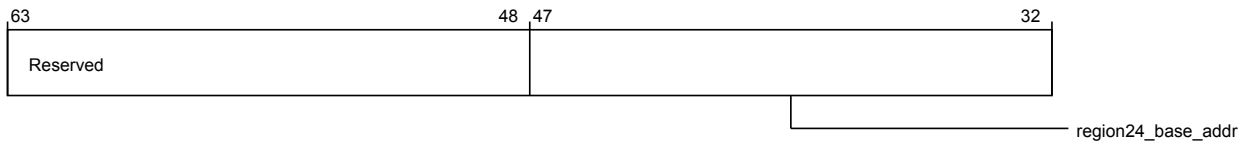


Figure 4-2476 `por_mpu_por_mpu_m7_prbar24` (high)

The following table shows the `por_mpu_m7_prbar24` higher register bit assignments.

Table 4-2493 `por_mpu_por_mpu_m7_prbar24` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

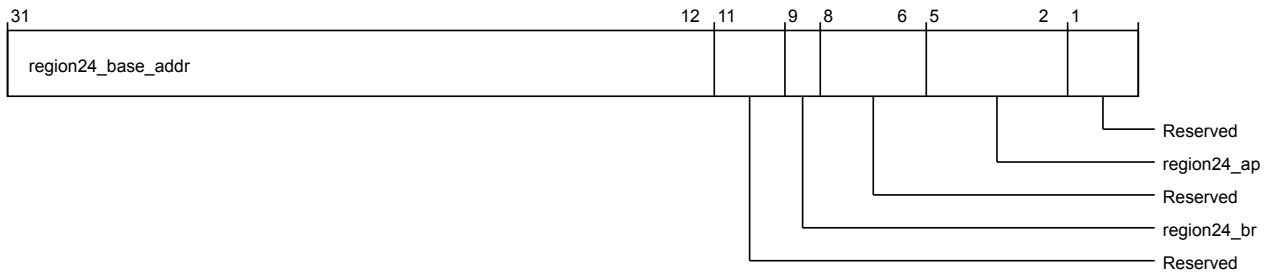


Figure 4-2477 `por_mpu_por_mpu_m7_prbar24` (low)

The following table shows the `por_mpu_m7_prbar24` lower register bit assignments.

Table 4-2494 `por_mpu_por_mpu_m7_prbar24` (low)

Bits	Field name	Description	Type	Reset
31:12	region24_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region24_br	Region 24 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region24_ap	Region 24 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar24

MPU master 0 programmable limit address register 24.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2D98

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

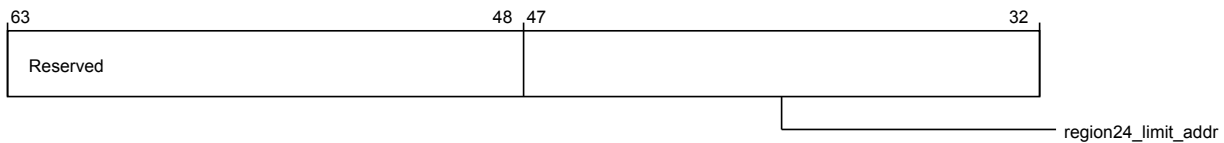


Figure 4-2478 `por_mpu_por_mpu_m7_prlar24` (high)

The following table shows the `por_mpu_m7_prlar24` higher register bit assignments.

Table 4-2495 `por_mpu_por_mpu_m7_prlar24` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region24_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

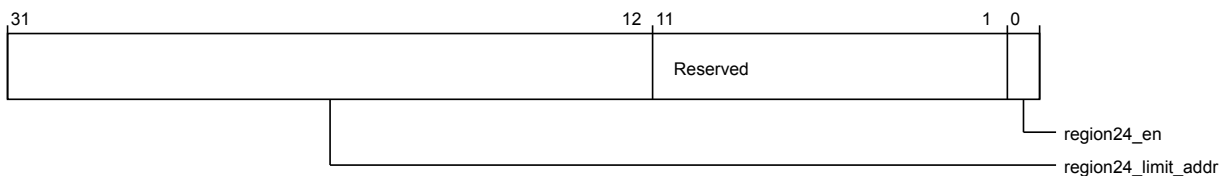


Figure 4-2479 `por_mpu_por_mpu_m7_prlar24` (low)

The following table shows the `por_mpu_m7_prlar24` lower register bit assignments.

Table 4-2496 `por_mpu_por_mpu_m7_prlar24` (low)

Bits	Field name	Description	Type	Reset
31:12	region24_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region24_en	Region 24 enable.	RW	1'b0

por_mpu_m7_prbar25

MPU master 0 programmable base address register 25.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2DA0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

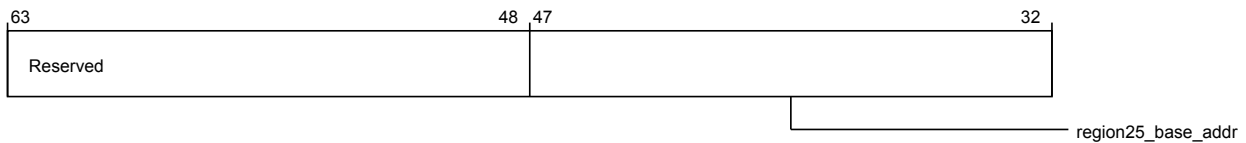


Figure 4-2480 por_mpu_por_mpu_m7_prbar25 (high)

The following table shows the por_mpu_m7_prbar25 higher register bit assignments.

Table 4-2497 por_mpu_por_mpu_m7_prbar25 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

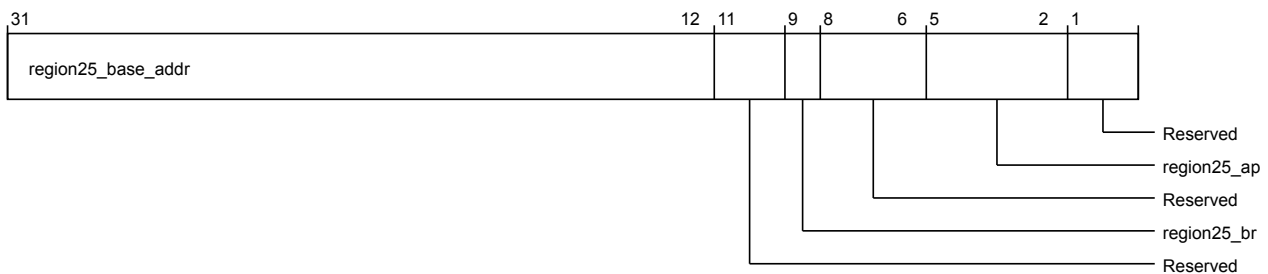


Figure 4-2481 por_mpu_por_mpu_m7_prbar25 (low)

The following table shows the por_mpu_m7_prbar25 lower register bit assignments.

Table 4-2498 por_mpu_por_mpu_m7_prbar25 (low)

Bits	Field name	Description	Type	Reset
31:12	region25_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2498 `por_mpu_por_mpu_m7_prbar25` (low) (continued)

Bits	Field name	Description	Type	Reset
9	region25_br	Region 25 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region25_ap	Region 25 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

`por_mpu_m7_prlar25`

MPU master 0 programmable limit address register 25.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2DA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

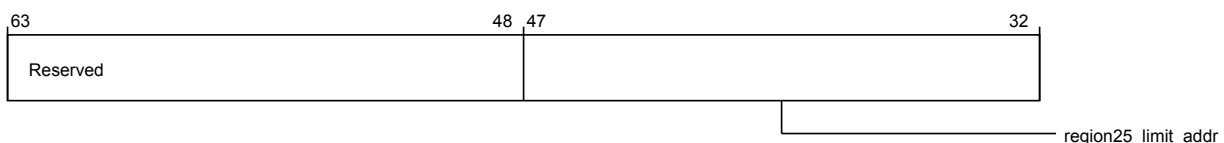


Figure 4-2482 `por_mpu_por_mpu_m7_prlar25` (high)

The following table shows the `por_mpu_m7_prlar25` higher register bit assignments.

Table 4-2499 `por_mpu_por_mpu_m7_prlar25` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region25_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

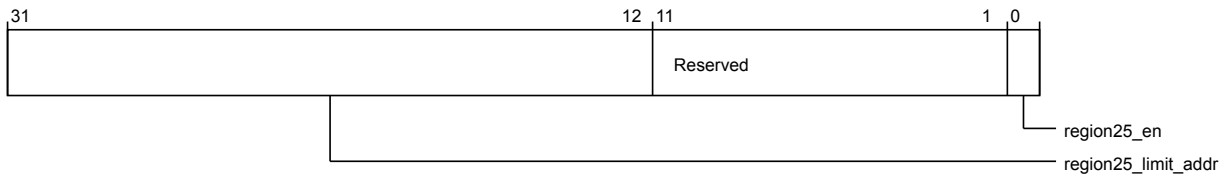


Figure 4-2483 por_mpu_por_mpu_m7_prlar25 (low)

The following table shows the por_mpu_m7_prlar25 lower register bit assignments.

Table 4-2500 por_mpu_por_mpu_m7_prlar25 (low)

Bits	Field name	Description	Type	Reset
31:12	region25_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region25_en	Region 25 enable.	RW	1'b0

por_mpu_m7_prbar26

MPU master 0 programmable base address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2DB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

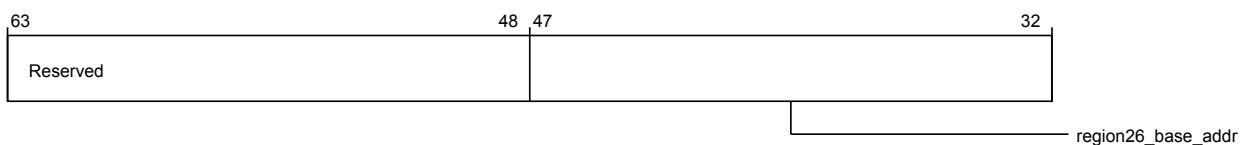


Figure 4-2484 por_mpu_por_mpu_m7_prbar26 (high)

The following table shows the por_mpu_m7_prbar26 higher register bit assignments.

Table 4-2501 por_mpu_por_mpu_m7_prbar26 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region26_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

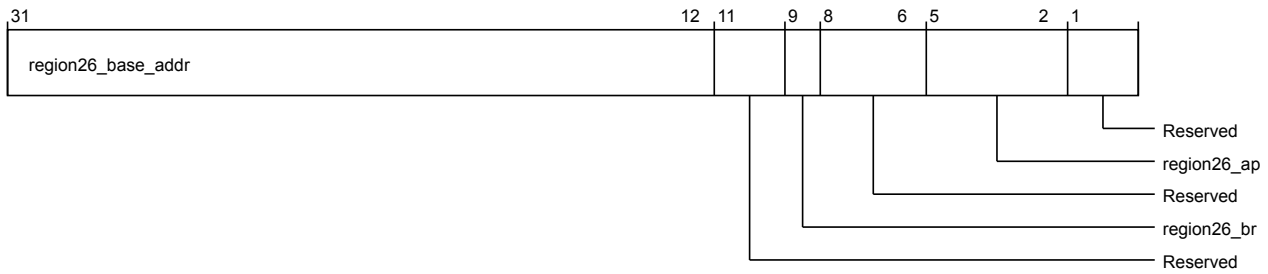


Figure 4-2485 por_mpu_m7_prbar26 (low)

The following table shows the por_mpu_m7_prbar26 lower register bit assignments.

Table 4-2502 por_mpu_m7_prbar26 (low)

Bits	Field name	Description	Type	Reset
31:12	region26_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region26_br	Region 26 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region26_ap	Region 26 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar26

MPU master 0 programmable limit address register 26.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2DB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

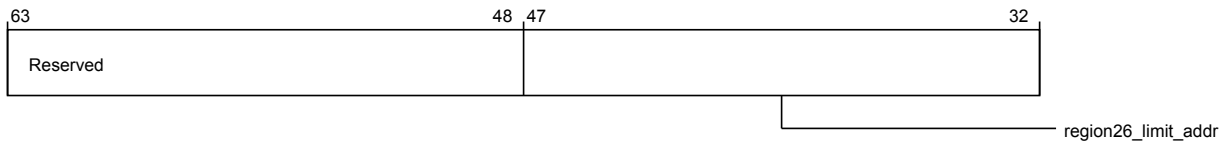


Figure 4-2486 por_mpu_m7_prlar26 (high)

The following table shows the por_mpu_m7_prlar26 higher register bit assignments.

Table 4-2503 por_mpu_m7_prlar26 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region26_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

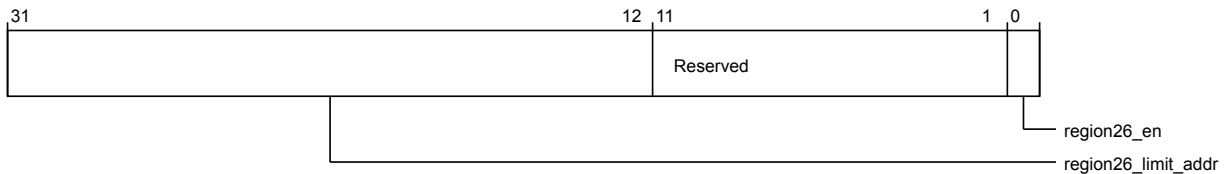


Figure 4-2487 por_mpu_m7_prlar26 (low)

The following table shows the por_mpu_m7_prlar26 lower register bit assignments.

Table 4-2504 por_mpu_m7_prlar26 (low)

Bits	Field name	Description	Type	Reset
31:12	region26_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region26_en	Region 26 enable.	RW	1'b0

por_mpu_m7_prbar27

MPU master 0 programmable base address register 27.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2DC0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

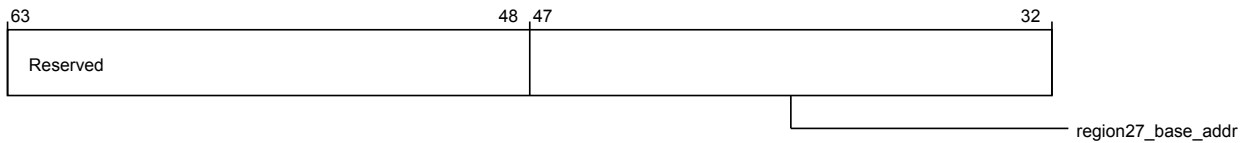


Figure 4-2488 por_mpu_por_mpu_m7_prbar27 (high)

The following table shows the por_mpu_m7_prbar27 higher register bit assignments.

Table 4-2505 por_mpu_por_mpu_m7_prbar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

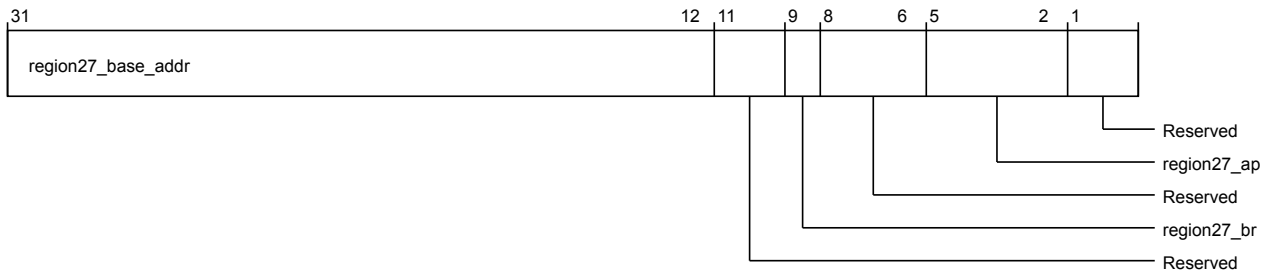


Figure 4-2489 por_mpu_por_mpu_m7_prbar27 (low)

The following table shows the por_mpu_m7_prbar27 lower register bit assignments.

Table 4-2506 por_mpu_por_mpu_m7_prbar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region27_br	Region 27 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region27_ap	Region 27 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar27

MPU master 0 programmable limit address register 27.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2DC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

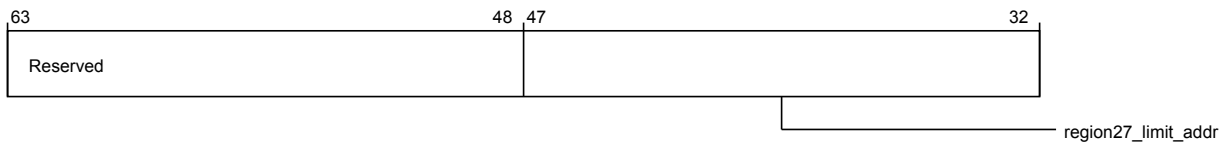


Figure 4-2490 por_mpu_por_mpu_m7_prlar27 (high)

The following table shows the `por_mpu_m7_prlar27` higher register bit assignments.

Table 4-2507 por_mpu_por_mpu_m7_prlar27 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region27_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

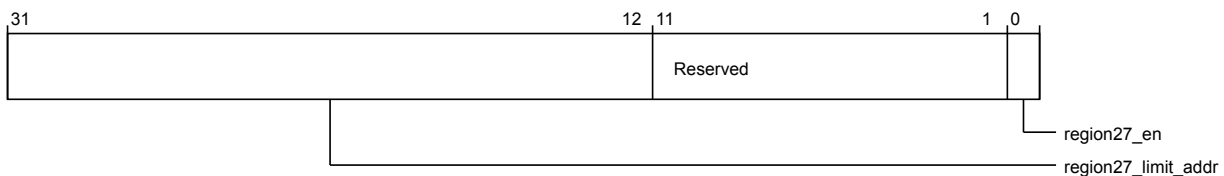


Figure 4-2491 por_mpu_por_mpu_m7_prlar27 (low)

The following table shows the `por_mpu_m7_prlar27` lower register bit assignments.

Table 4-2508 por_mpu_por_mpu_m7_prlar27 (low)

Bits	Field name	Description	Type	Reset
31:12	region27_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region27_en	Region 27 enable.	RW	1'b0

por_mpu_m7_prbar28

MPU master 0 programmable base address register 28.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2DD0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

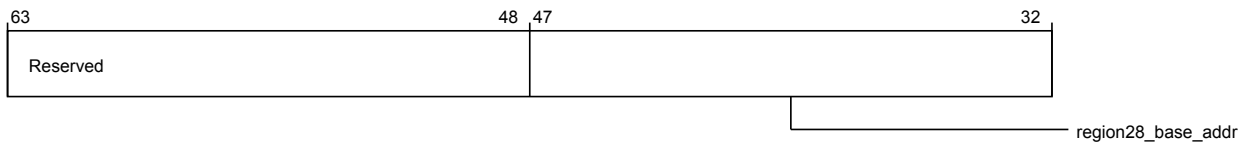


Figure 4-2492 por_mpu_por_mpu_m7_prbar28 (high)

The following table shows the por_mpu_m7_prbar28 higher register bit assignments.

Table 4-2509 por_mpu_por_mpu_m7_prbar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

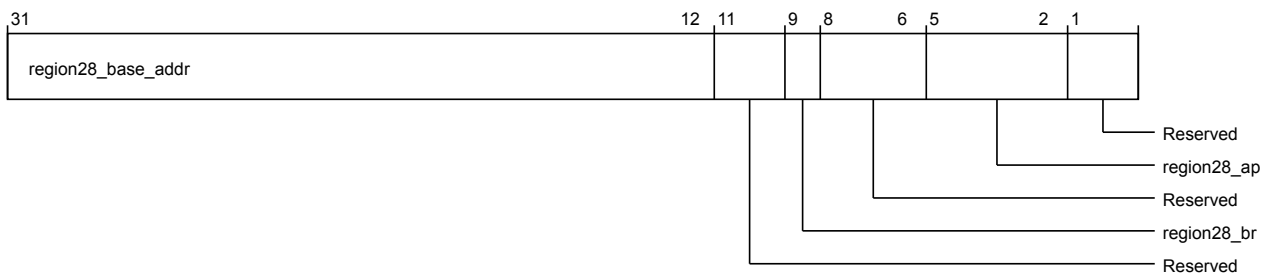


Figure 4-2493 por_mpu_por_mpu_m7_prbar28 (low)

The following table shows the por_mpu_m7_prbar28 lower register bit assignments.

Table 4-2510 por_mpu_por_mpu_m7_prbar28 (low)

Bits	Field name	Description	Type	Reset
31:12	region28_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2510 por_mpu_por_mpu_m7_prbar28 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region28_br	Region 28 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region28_ap	Region 28 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar28

MPU master 0 programmable limit address register 28.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2DD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

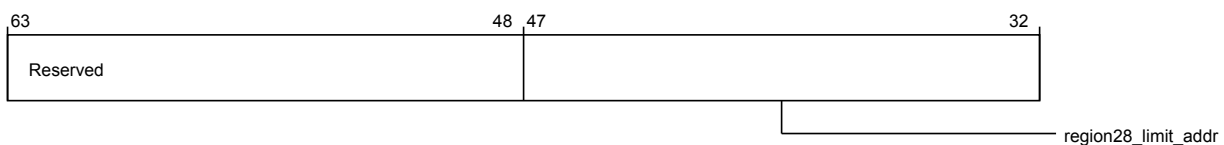


Figure 4-2494 por_mpu_por_mpu_m7_prlar28 (high)

The following table shows the por_mpu_m7_prlar28 higher register bit assignments.

Table 4-2511 por_mpu_por_mpu_m7_prlar28 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region28_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

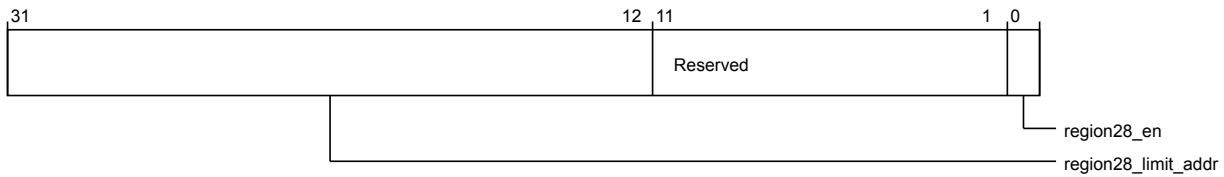


Figure 4-2495 `por_mpu_por_mpu_m7_prlar28` (low)

The following table shows the `por_mpu_m7_prlar28` lower register bit assignments.

Table 4-2512 `por_mpu_por_mpu_m7_prlar28` (low)

Bits	Field name	Description	Type	Reset
31:12	<code>region28_limit_addr</code>	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	<code>region28_en</code>	Region 28 enable.	RW	1'b0

`por_mpu_m7_prbar29`

MPU master 0 programmable base address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2DE0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

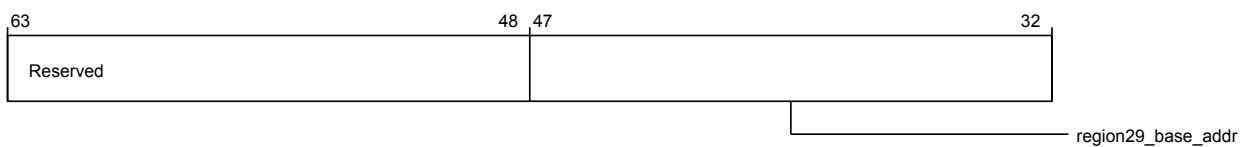


Figure 4-2496 `por_mpu_por_mpu_m7_prbar29` (high)

The following table shows the `por_mpu_m7_prbar29` higher register bit assignments.

Table 4-2513 `por_mpu_por_mpu_m7_prbar29` (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	<code>region29_base_addr</code>	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

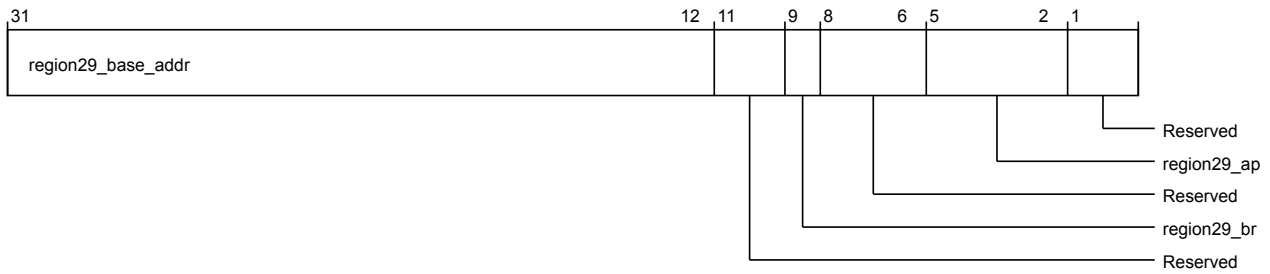


Figure 4-2497 por_mpu_m7_prbar29 (low)

The following table shows the por_mpu_m7_prbar29 lower register bit assignments.

Table 4-2514 por_mpu_m7_prbar29 (low)

Bits	Field name	Description	Type	Reset
31:12	region29_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region29_br	Region 29 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region29_ap	Region 29 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar29

MPU master 0 programmable limit address register 29.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2DE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

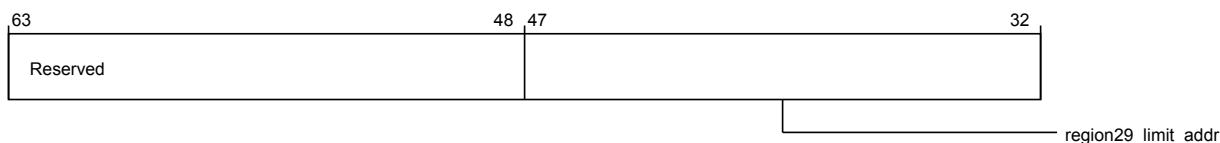


Figure 4-2498 por_mpu_m7_prlar29 (high)

The following table shows the por_mpu_m7_prlar29 higher register bit assignments.

Table 4-2515 por_mpu_m7_prlar29 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region29_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

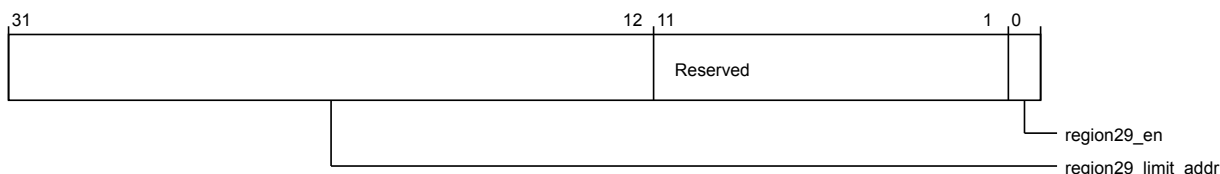


Figure 4-2499 por_mpu_m7_prlar29 (low)

The following table shows the por_mpu_m7_prlar29 lower register bit assignments.

Table 4-2516 por_mpu_m7_prlar29 (low)

Bits	Field name	Description	Type	Reset
31:12	region29_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region29_en	Region 29 enable.	RW	1'b0

por_mpu_m7_prbar30

MPU master 0 programmable base address register 30.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2DF0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

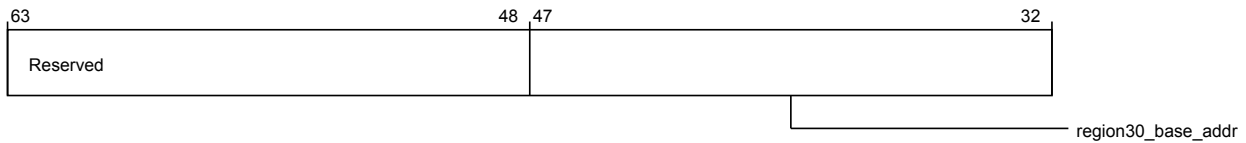


Figure 4-2500 por_mpu_por_mpu_m7_prbar30 (high)

The following table shows the por_mpu_m7_prbar30 higher register bit assignments.

Table 4-2517 por_mpu_por_mpu_m7_prbar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

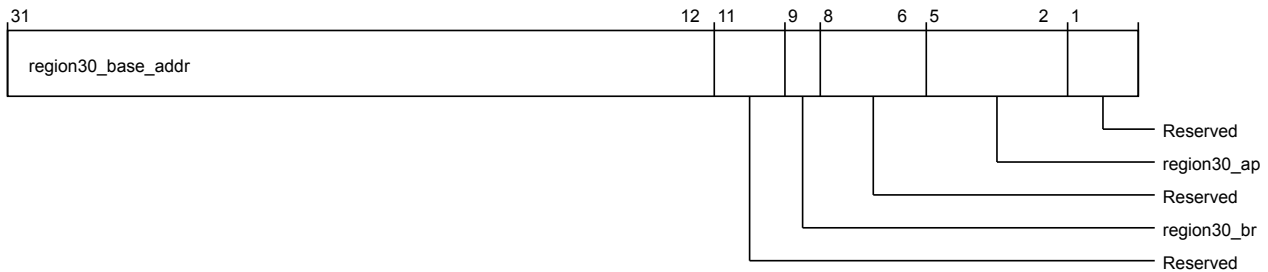


Figure 4-2501 por_mpu_por_mpu_m7_prbar30 (low)

The following table shows the por_mpu_m7_prbar30 lower register bit assignments.

Table 4-2518 por_mpu_por_mpu_m7_prbar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-
9	region30_br	Region 30 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region30_ap	Region 30 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar30

MPU master 0 programmable limit address register 30.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2DF8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

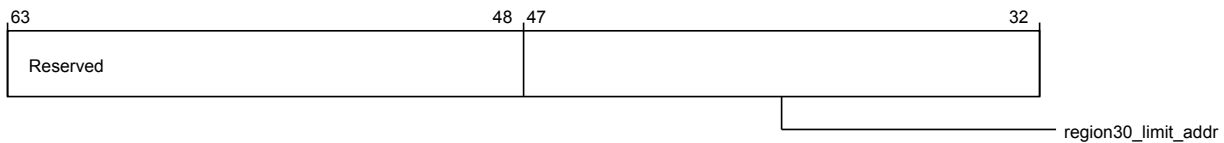


Figure 4-2502 por_mpu_por_mpu_m7_prlar30 (high)

The following table shows the por_mpu_m7_prlar30 higher register bit assignments.

Table 4-2519 por_mpu_por_mpu_m7_prlar30 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region30_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

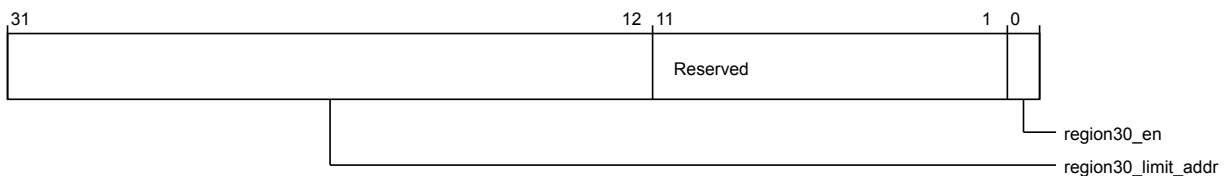


Figure 4-2503 por_mpu_por_mpu_m7_prlar30 (low)

The following table shows the por_mpu_m7_prlar30 lower register bit assignments.

Table 4-2520 por_mpu_por_mpu_m7_prlar30 (low)

Bits	Field name	Description	Type	Reset
31:12	region30_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region30_en	Region 30 enable.	RW	1'b0

por_mpu_m7_prbar31

MPU master 0 programmable base address register 31.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h2E00
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

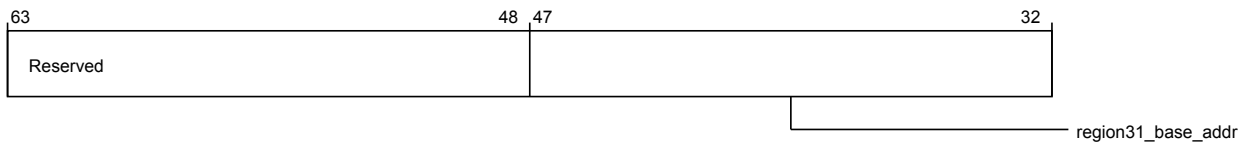


Figure 4-2504 por_mpu_por_mpu_m7_prbar31 (high)

The following table shows the por_mpu_m7_prbar31 higher register bit assignments.

Table 4-2521 por_mpu_por_mpu_m7_prbar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_base_addr	Bits [47:32] of base address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

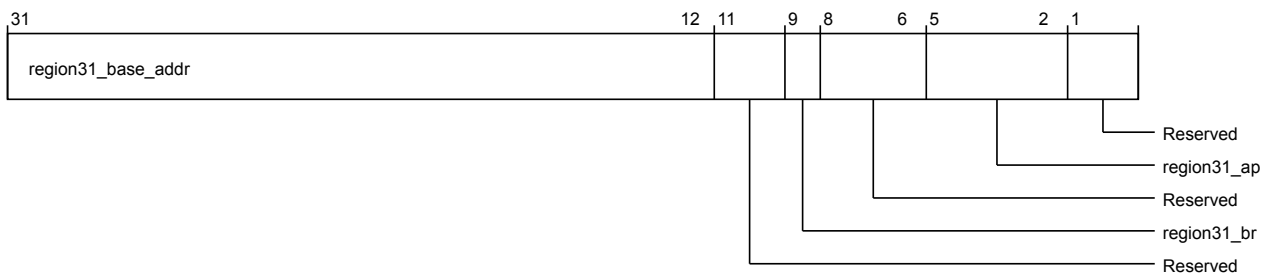


Figure 4-2505 por_mpu_por_mpu_m7_prbar31 (low)

The following table shows the por_mpu_m7_prbar31 lower register bit assignments.

Table 4-2522 por_mpu_por_mpu_m7_prbar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_base_addr	Bits [31:12] of base address of the range.	RW	20'b0
11:10	Reserved	Reserved	RO	-

Table 4-2522 por_mpu_por_mpu_m7_prbar31 (low) (continued)

Bits	Field name	Description	Type	Reset
9	region31_br	Region 31 back ground region indication.	RW	1'b0
8:6	Reserved	Reserved	RO	-
5:2	region31_ap	Region 31 access permission. 0 - not permitted; 1 - permitted. It is illegal to program write to 1, but read to 0. ap[0]: NW non secure write ap[1]: SW secure write ap[2]: NR non secure read ap[3]: SR secure read	RW	4'b0
1:0	Reserved	Reserved	RO	-

por_mpu_m7_prlar31

MPU master 0 programmable limit address register 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2E08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

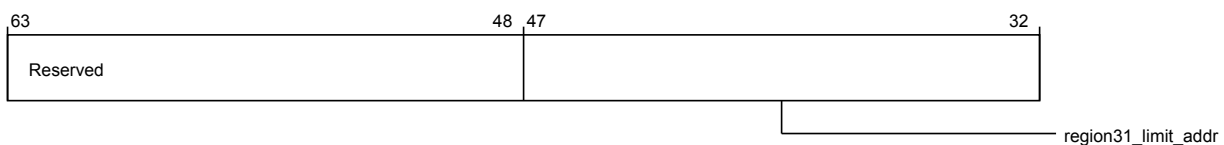


Figure 4-2506 por_mpu_por_mpu_m7_prlar31 (high)

The following table shows the por_mpu_m7_prlar31 higher register bit assignments.

Table 4-2523 por_mpu_por_mpu_m7_prlar31 (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	region31_limit_addr	Bits [47:32] of limit address of the range.	RW	16'b0

The following image shows the lower register bit assignments.

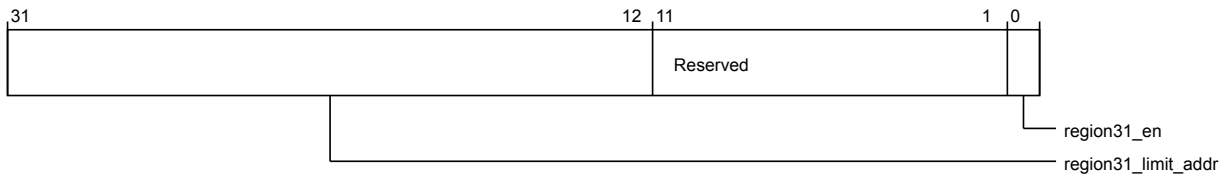


Figure 4-2507 por_mpu_por_mpu_m7_prlar31 (low)

The following table shows the por_mpu_m7_prlar31 lower register bit assignments.

Table 4-2524 por_mpu_por_mpu_m7_prlar31 (low)

Bits	Field name	Description	Type	Reset
31:12	region31_limit_addr	Bits [31:12] of limit address of the range.	RW	20'b0
11:1	Reserved	Reserved	RO	-
0	region31_en	Region 31 enable.	RW	1'b0

4.3.16 FDC configuration registers

This section lists the FDC configuration registers.

por_fdc_node_info

Provides component identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h0
Register reset	Configuration dependent
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

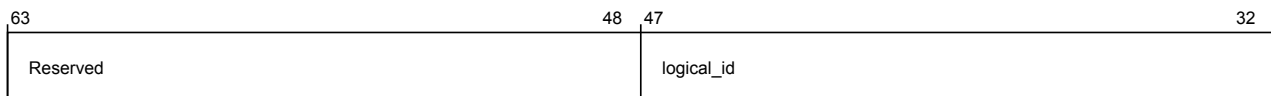


Figure 4-2508 por_fdc_node_info (high)

The following table shows the por_fdc_node_info higher register bit assignments.

Table 4-2525 por_fdc_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

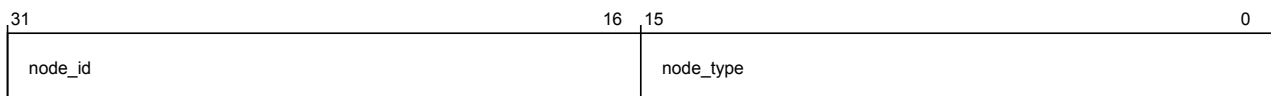


Figure 4-2509 por_fdc_node_info (low)

The following table shows the por_fdc_node_info lower register bit assignments.

Table 4-2526 por_fdc_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600AE node type identifier	RO	16'h0201

por_fdc_child_info

Provides component child identification information.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h80
Register reset	64'b0
Usage constraints	There are no usage constraints.

The following image shows the higher register bit assignments.

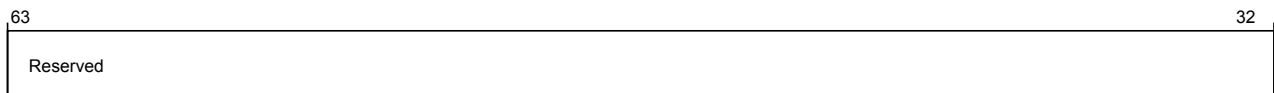


Figure 4-2510 por_fdc_por_fdc_child_info (high)

The following table shows the por_fdc_child_info higher register bit assignments.

Table 4-2527 por_fdc_por_fdc_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

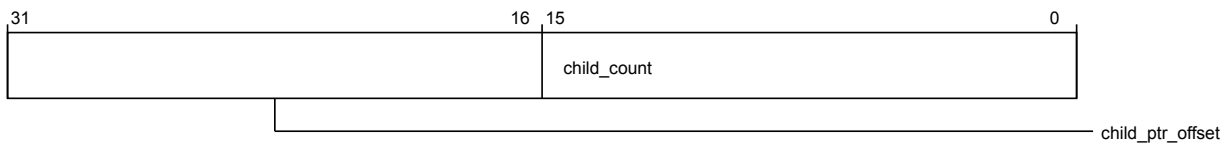


Figure 4-2511 por_fdc_por_fdc_child_info (low)

The following table shows the por_fdc_child_info lower register bit assignments.

Table 4-2528 por_fdc_por_fdc_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_errinject

Error injection control

Its characteristics are:

Type	WO
Register width (Bits)	64

Address offset 14'h3300
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-2512 `por_fdc_por_errinject (high)`

The following table shows the `por_errinject` higher register bit assignments.

Table 4-2529 `por_fdc_por_errinject (high)`

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

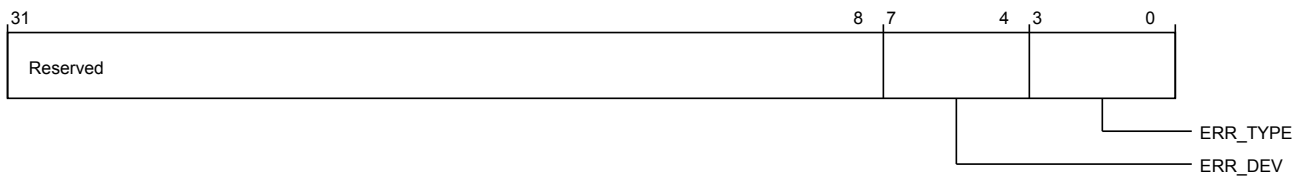


Figure 4-2513 `por_fdc_por_errinject (low)`

The following table shows the `por_errinject` lower register bit assignments.

Table 4-2530 por_fdc_por_errinject (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:4	ERR_DEV	The device where error is injected: 4'b0000: P0_D0 4'b0001: P0_D1 4'b0010: P0_D2 4'b0011: P0_D3 4'b0100: P1_D0 4'b0101: P1_D1 4'b0110: P1_D2 4'b0111: P1_D3 4'b1000: XP	WO	4'b0
3:0	ERR_TYPE	The type of error injected: 4'h0: clk error 4'h1: reset error 4'h2: lsc error 4'h3: ioc error 4'h4: async error 4'h5: hang error 4'h6: mpu error 4'h7: ecc ue error 4'h8: ecc ce error	WO	4'b0

por_fdc_key

FDC write key

Its characteristics are:

Type WO

Register width (Bits) 64

Address offset 14'h3308

Register reset 64'b10111110

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

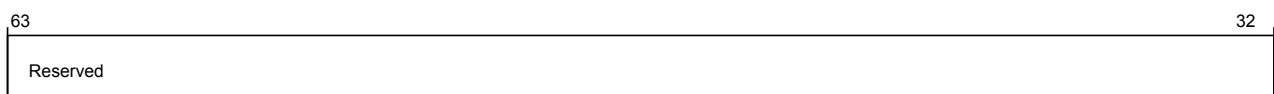


Figure 4-2514 por_fdc_por_fdc_key (high)

The following table shows the por_fdc_key higher register bit assignments.

Table 4-2531 por_fdc_por_fdc_key (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

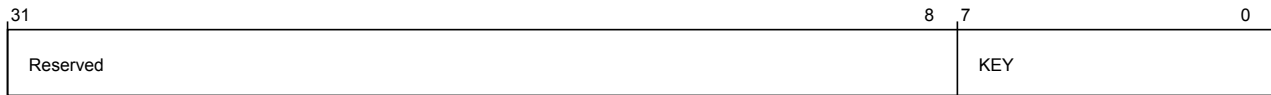


Figure 4-2515 por_fdc_por_fdc_key (low)

The following table shows the por_fdc_key lower register bit assignments.

Table 4-2532 por_fdc_por_fdc_key (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	KEY	The write protection key. Only writing of correct value will enable subsequent write to other FDC registers.	WO	8'hBE

por_errfr_mxp

Functions as the error feature register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3000

Register reset 64'b101001

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

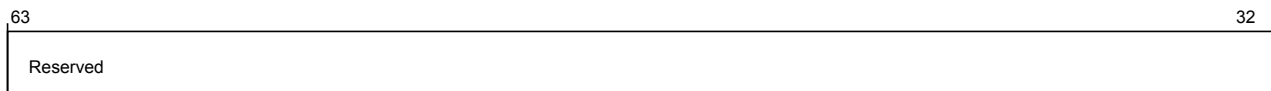


Figure 4-2516 por_fdc_por_errfr_mxp (high)

The following table shows the por_errfr_mxp higher register bit assignments.

Table 4-2533 por_fdc_por_errfr_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

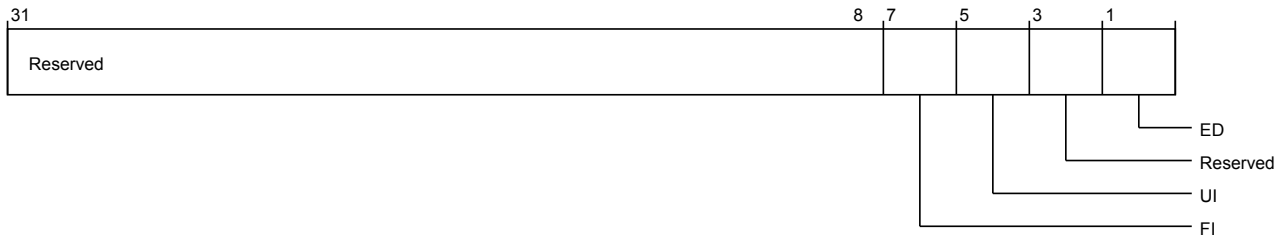


Figure 4-2517 por_fdc_por_errfr_mxp (low)

The following table shows the por_errfr_mxp lower register bit assignments.

Table 4-2534 por_fdc_por_errfr_mxp (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	FI	enable error propagation to FHI interrupt	RO	2'b10
5:4	UI	enable error propagation to ERI interrupt	RO	2'b10
3:2	Reserved	Reserved	RO	-
1:0	ED	FUSA Error Detection	RO	2'b01

por_errctlr_mxp

Functions as the error control register. Controls whether specific error-reporting and fault-handling interrupts are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3008
Register reset	64'b0111
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

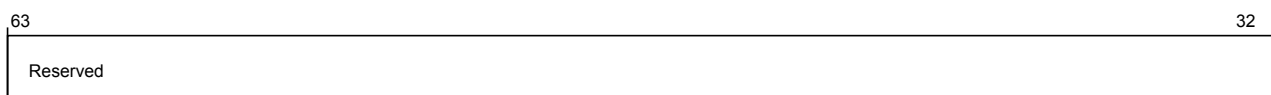


Figure 4-2518 por_fdc_por_errctlr_mxp (high)

The following table shows the por_errctlr_mxp higher register bit assignments.

Table 4-2535 por_fdc_por_errctlr_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

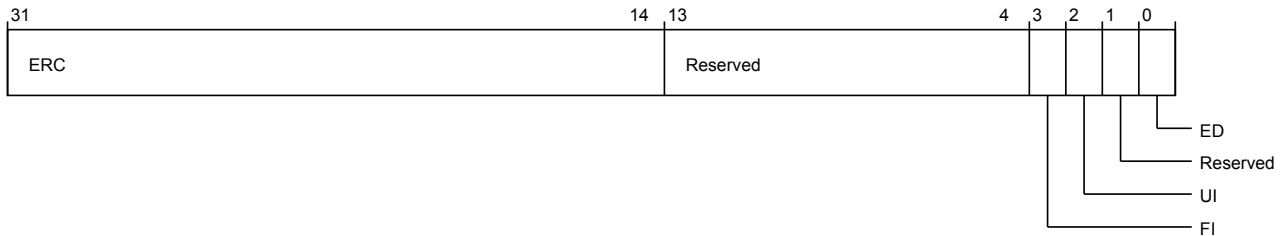


Figure 4-2519 por_fdc_por_errctlr_mxp (low)

The following table shows the por_errctlr_mxp lower register bit assignments.

Table 4-2536 por_fdc_por_errctlr_mxp (low)

Bits	Field name	Description	Type	Reset
31:14	ERC	Error report control, two bits per error type 2'b00: report as critical error (ERI) 2'b01: report as non-critical error (FHI) 2'b10: do not report 2'b11: reserved ERC[1:0]: clk error ERC[3:2]: reset error ERC[5:4]: lsc error ERC[7:6]: ioc error ERC[9:8]: async error ERC[11:10]: hang error ERC[13:12]: mpu error ERC[15:14]: ecc ue error ERC[17:16]: ecc ce error	RW	18'b0
13:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt as specified in por_errfr_mxp.FI	RW	1'b1
2	UI	Enables error reporting interrupt as specified in por_errfr_mxp.UI	RW	1'b1

Table 4-2536 por_fdc_por_errctlr_mxp (low) (continued)

Bits	Field name	Description	Type	Reset
1	Reserved	Reserved	RO	-
0	ED	Enables error detection as specified in por_errfr_mxp.ED	RW	1'b1

por_errstatus_mxp

Functions as the error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3010
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

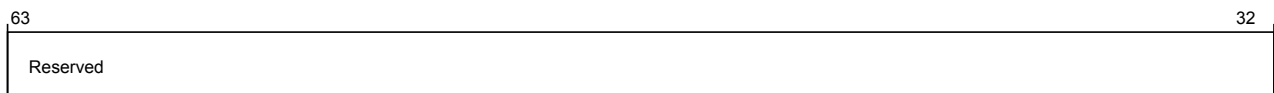


Figure 4-2520 por_fdc_por_errstatus_mxp (high)

The following table shows the por_errstatus_mxp higher register bit assignments.

Table 4-2537 por_fdc_por_errstatus_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

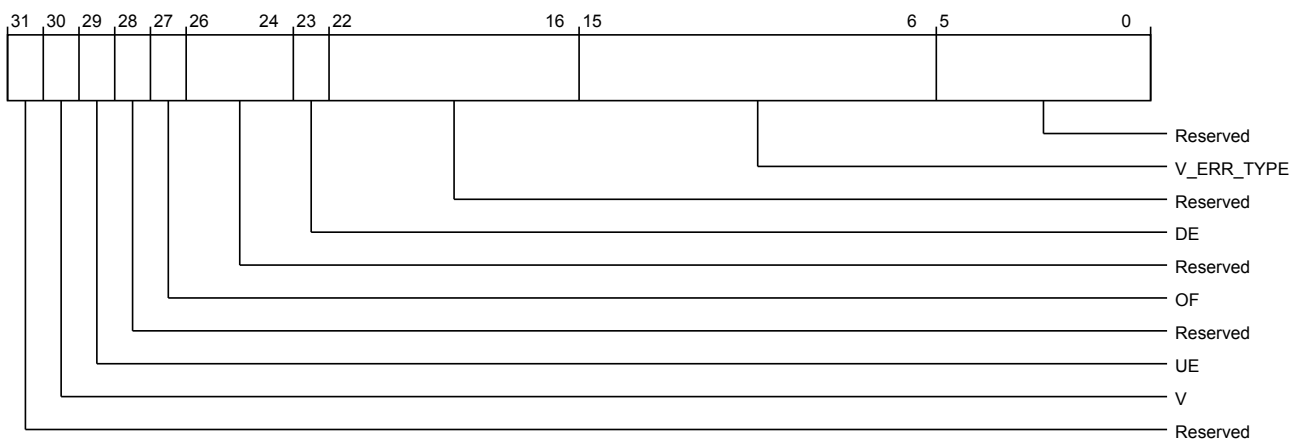


Figure 4-2521 por_fdc_por_errstatus_mxp (low)

The following table shows the por_errstatus_mxp lower register bit assignments.

Table 4-2538 por_fdc_por_errstatus_mxp (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30	V	Register valid; writes to this bit are ignored if any of the UE or DE bit is set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one critical error detected 1'b0: No critical errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors for the same error type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the same type detected as described	W1C	1'b0
26:24	Reserved	Reserved	RO	-
23	DE	Non-critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one non-critical error detected 1'b0: No non-critical errors detected	W1C	1'b0
22:16	Reserved	Reserved	RO	-
15:6	V_ERR_TYPE	Error valid for the type of errors: writes to the bits are ignored if the V bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear V_ERR_TYPE[0]: clk error V_ERR_TYPE[1]: reset error V_ERR_TYPE[2]: lsc error V_ERR_TYPE[3]: ioc error V_ERR_TYPE[4]: async error V_ERR_TYPE[5]: hang error V_ERR_TYPE[6]: mpu error V_ERR_TYPE[7]: ecc ue error V_ERR_TYPE[8]: ecc ce error V_ERR_TYPE[9]: multiple errors	W1C	10'b0
5:0	Reserved	Reserved	RO	-

por_fdc_aux_ctl_mxp

Functions as the aux control register. Controls specific error features.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3018
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

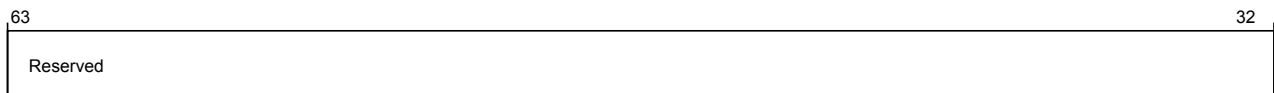


Figure 4-2522 por_fdc_por_fdc_aux_ctl_mxp (high)

The following table shows the por_fdc_aux_ctl_mxp higher register bit assignments.

Table 4-2539 por_fdc_por_fdc_aux_ctl_mxp (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

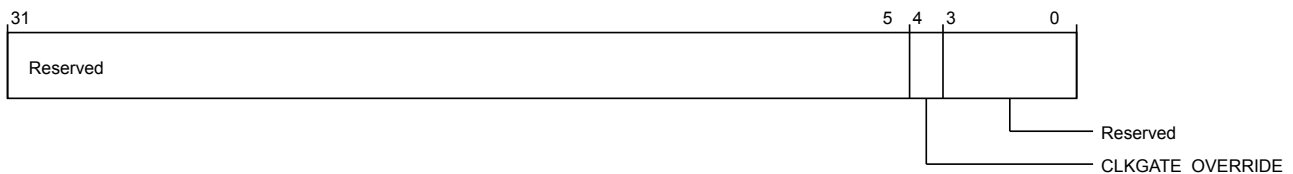


Figure 4-2523 por_fdc_por_fdc_aux_ctl_mxp (low)

The following table shows the por_fdc_aux_ctl_mxp lower register bit assignments.

Table 4-2540 por_fdc_por_fdc_aux_ctl_mxp (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	CLKGATE_OVERRIDE	FUSA checker clock gate disable in XP.	RW	1'b0
3:0	Reserved	Reserved	RO	-

por_errfr_p0_d0

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3040
Register reset	64'b101001
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

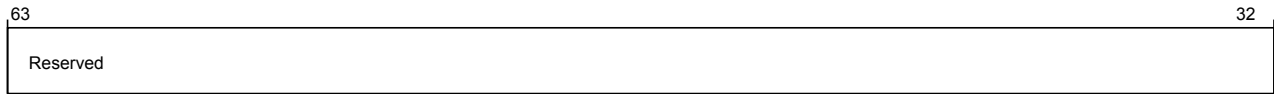


Figure 4-2524 por_fdc_por_errfr_p0_d0 (high)

The following table shows the por_errfr_p0_d0 higher register bit assignments.

Table 4-2541 por_fdc_por_errfr_p0_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

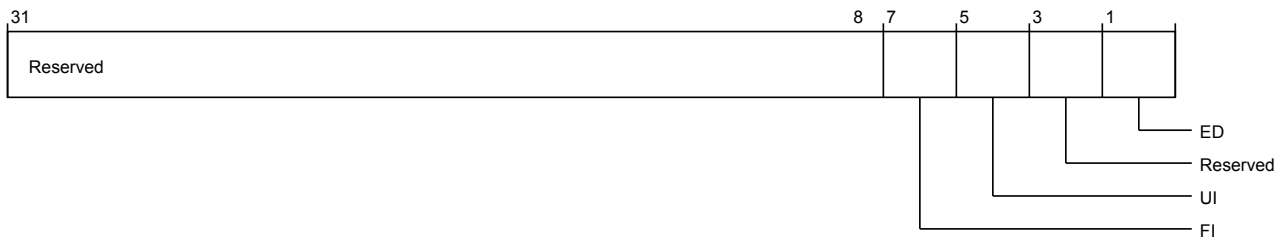


Figure 4-2525 por_fdc_por_errfr_p0_d0 (low)

The following table shows the por_errfr_p0_d0 lower register bit assignments.

Table 4-2542 por_fdc_por_errfr_p0_d0 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	FI	enable error propagation to FHI interrupt	RO	2'b10
5:4	UI	enable error propagation to ERI interrupt	RO	2'b10
3:2	Reserved	Reserved	RO	-
1:0	ED	FUSA Error Detection	RO	2'b01

por_errctlr_p0_d0

Functions as the error control register. Controls whether specific error-reporting and fault-handling interrupts are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3048
Register reset	64'b0111
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-2526 por_fdc_por_errctlr_p0_d0 (high)

The following table shows the por_errctlr_p0_d0 higher register bit assignments.

Table 4-2543 por_fdc_por_errctlr_p0_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

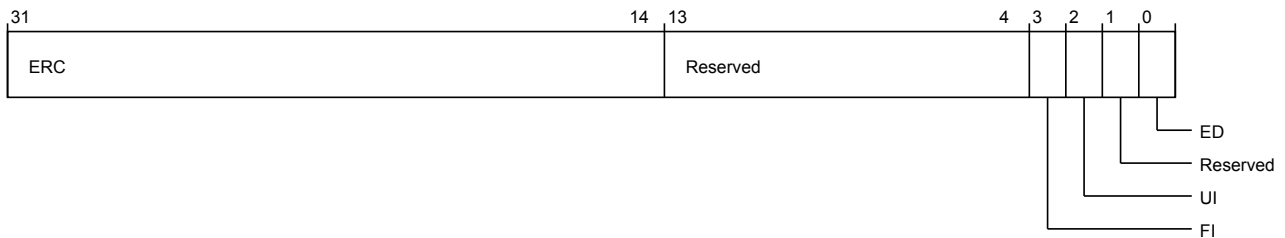


Figure 4-2527 por_fdc_por_errctlr_p0_d0 (low)

The following table shows the por_errctlr_p0_d0 lower register bit assignments.

Table 4-2544 por_fdc_por_errctlr_p0_d0 (low)

Bits	Field name	Description	Type	Reset
31:14	ERC	Error report control, two bits per error type 2'b00: report as critical error (ERI) 2'b01: report as non-critical error (FHI) 2'b10: do not report 2'b11: reserved ERC[1:0]: clk error ERC[3:2]: reset error ERC[5:4]: lsc error ERC[7:6]: ioc error ERC[9:8]: async error ERC[11:10]: hang error ERC[13:12]: mpu error ERC[15:14]: ecc ue error ERC[17:16]: ecc ce error	RW	18'b0
13:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt as specified in por_errfr_p0_d0.FI	RW	1'b1
2	UI	Enables error reporting interrupt as specified in por_errfr_p0_d0.UI	RW	1'b1
1	Reserved	Reserved	RO	-
0	ED	Enables error detection as specified in por_errfr_p0_d0.ED	RW	1'b1

por_errstatus_p0_d0

Functions as the error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3050
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

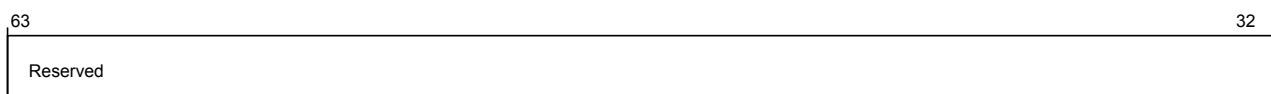


Figure 4-2528 por_fdc_por_errstatus_p0_d0 (high)

The following table shows the por_errstatus_p0_d0 higher register bit assignments.

Table 4-2545 `por_fdc_por_errstatus_p0_d0` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

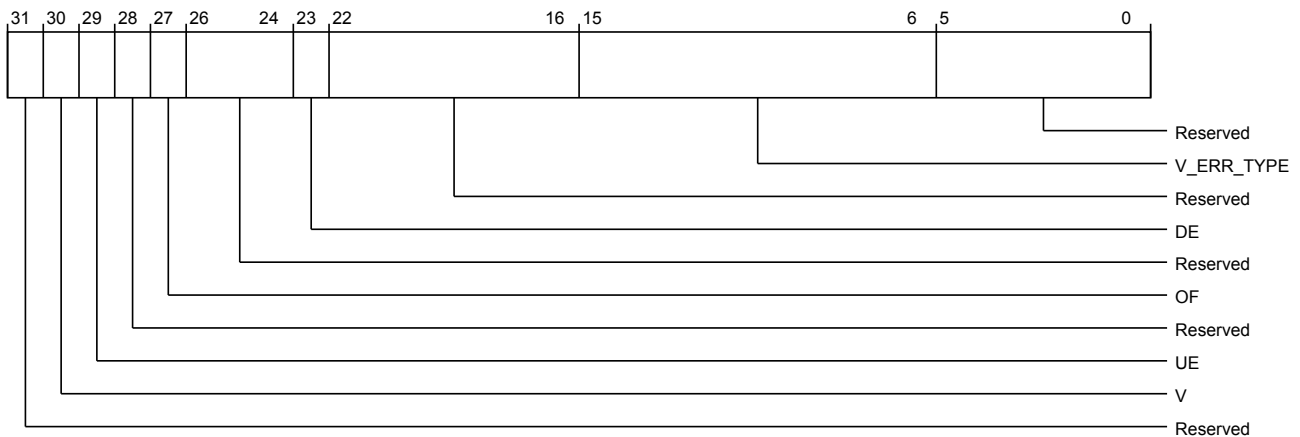


Figure 4-2529 `por_fdc_por_errstatus_p0_d0` (low)

The following table shows the `por_errstatus_p0_d0` lower register bit assignments.

Table 4-2546 `por_fdc_por_errstatus_p0_d0` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30	V	Register valid; writes to this bit are ignored if any of the UE or DE bit is set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one critical error detected 1'b0: No critical errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors for the same error type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the same type detected as described	W1C	1'b0
26:24	Reserved	Reserved	RO	-

Table 4-2546 por_fdc_por_errstatus_p0_d0 (low) (continued)

Bits	Field name	Description	Type	Reset
23	DE	Non-critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one non-critical error detected 1'b0: No non-critical errors detected	W1C	1'b0
22:16	Reserved	Reserved	RO	-
15:6	V_ERR_TYPE	Error valid for the type of errors: writes to the bits are ignored if the V bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear V_ERR_TYPE[0]: clk error V_ERR_TYPE[1]: reset error V_ERR_TYPE[2]: lsc error V_ERR_TYPE[3]: ioc error V_ERR_TYPE[4]: async error V_ERR_TYPE[5]: hang error V_ERR_TYPE[6]: mpu error V_ERR_TYPE[7]: ecc ue error V_ERR_TYPE[8]: ecc ce error V_ERR_TYPE[9]: multiple errors	W1C	10'b0
5:0	Reserved	Reserved	RO	-

por_fdc_aux_ctl_p0_d0

Functions as the aux control register. Controls specific error features.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3058

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

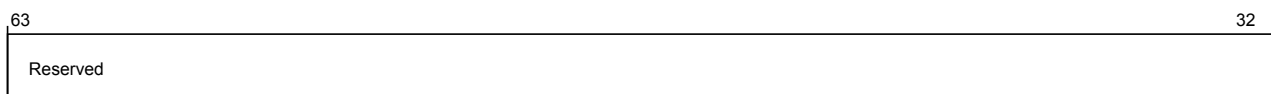


Figure 4-2530 por_fdc_por_fdc_aux_ctl_p0_d0 (high)

The following table shows the por_fdc_aux_ctl_p0_d0 higher register bit assignments.

Table 4-2547 `por_fdc_por_fdc_aux_ctl_p0_d0` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

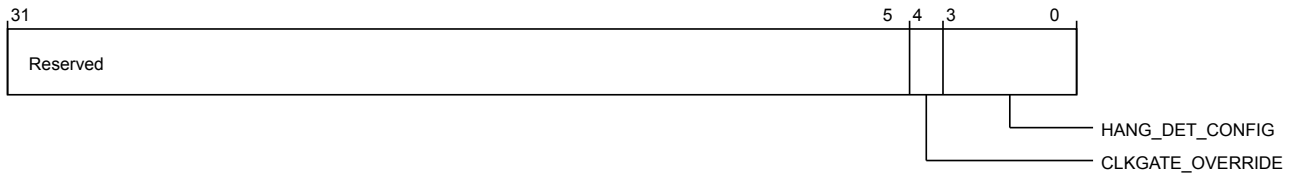


Figure 4-2531 `por_fdc_por_fdc_aux_ctl_p0_d0` (low)

The following table shows the `por_fdc_aux_ctl_p0_d0` lower register bit assignments.

Table 4-2548 `por_fdc_por_fdc_aux_ctl_p0_d0` (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	CLKGATE_OVERRIDE	FUSA checker clock gate disable in device connected to p0_d0 port.	RW	1'b0
3:0	HANG_DET_CONFIG	<p>timeout setting for hang detection in device connected to p0_d0 port.</p> <p>4'hx: timeout range in clock cycles (min - max), timeout range in duration @ 2Ghz (min - max)</p> <p>4'h0: 3x2²⁴ - 4x2²⁴, 25ms - 34ms</p> <p>4'h1: 3x2²³ - 4x2²³, 12.5ms - 17ms</p> <p>4'h2: 3x2²² - 4x2²², 6.29ms - 8.4ms</p> <p>4'h3: 3x2²¹ - 4x2²¹, 3.14ms - 4.2ms</p> <p>4'h4: 3x2²⁰ - 4x2²⁰, 1.57ms - 2.1ms</p> <p>4'h5: 3x2¹⁹ - 4x2¹⁹, 0.786ms - 1.05ms</p> <p>4'h6: 3x2¹⁸ - 4x2¹⁸, 393us - 525us</p> <p>4'h7: 3x2¹⁷ - 4x2¹⁷, 196us - 263us</p> <p>4'h8: 3x2¹⁶ - 4x2¹⁶, 98us - 132us</p> <p>4'h9: 3x2¹⁵ - 4x2¹⁵, 49us - 66us</p> <p>4'hA: 3x2¹⁴ - 4x2¹⁴, 24us - 33us</p> <p>4'hB: 3x2¹³ - 4x2¹³, 12us - 17us</p> <p>4'hC: 3x2¹² - 4x2¹², 6us - 8.2us</p> <p>4'hD: 3x2¹¹ - 4x2¹¹, 3us - 4.1us</p> <p>4'hE: 3x2¹⁰ - 4x2¹⁰, 1.5us - 2.1us</p> <p>4'hF: 3x2⁹ - 4x2⁹, 0.75us - 1.1us</p>	RW	4'b0

por_errfr_p0_d1

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3080
Register reset	64'b101001
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-2532 por_fdc_por_errfr_p0_d1 (high)

The following table shows the por_errfr_p0_d1 higher register bit assignments.

Table 4-2549 por_fdc_por_errfr_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

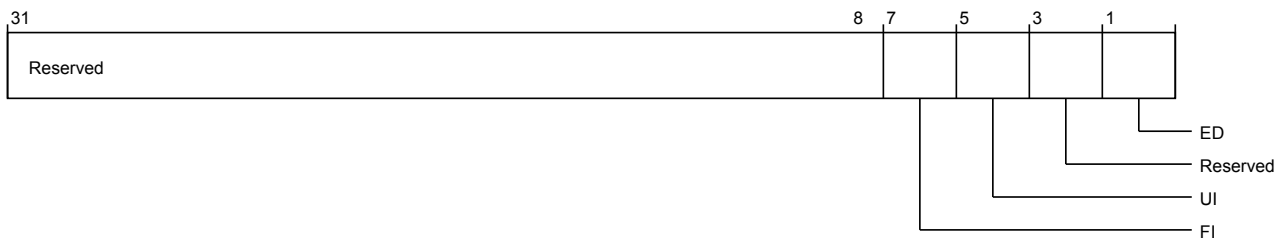


Figure 4-2533 por_fdc_por_errfr_p0_d1 (low)

The following table shows the por_errfr_p0_d1 lower register bit assignments.

Table 4-2550 por_fdc_por_errfr_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	FI	enable error propagation to FHI interrupt	RO	2'b10
5:4	UI	enable error propagation to ERI interrupt	RO	2'b10

Table 4-2550 por_fdc_por_errfr_p0_d1 (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	Reserved	Reserved	RO	-
1:0	ED	FUSA Error Detection	RO	2'b01

por_errctlr_p0_d1

Functions as the error control register. Controls whether specific error-reporting and fault-handling interrupts are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3088
Register reset	64'b0111
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

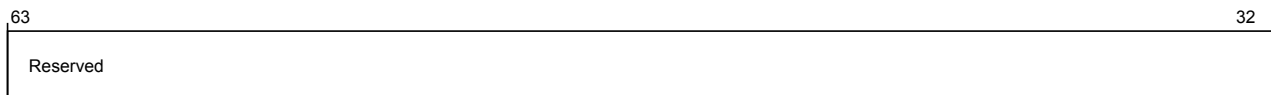


Figure 4-2534 por_fdc_por_errctlr_p0_d1 (high)

The following table shows the por_errctlr_p0_d1 higher register bit assignments.

Table 4-2551 por_fdc_por_errctlr_p0_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

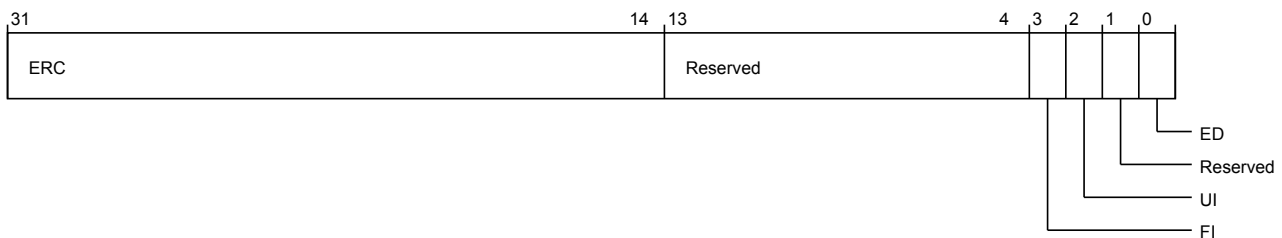


Figure 4-2535 por_fdc_por_errctlr_p0_d1 (low)

The following table shows the por_errctlr_p0_d1 lower register bit assignments.

Table 4-2552 por_fdc_por_errctlr_p0_d1 (low)

Bits	Field name	Description	Type	Reset
31:14	ERC	Error report control, two bits per error type 2'b00: report as critical error (ERI) 2'b01: report as non-critical error (FHI) 2'b10: do not report 2'b11: reserved ERC[1:0]: clk error ERC[3:2]: reset error ERC[5:4]: lsc error ERC[7:6]: ioc error ERC[9:8]: async error ERC[11:10]: hang error ERC[13:12]: mpu error ERC[15:14]: ecc ue error ERC[17:16]: ecc ce error	RW	18'b0
13:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt as specified in por_errfr_p0_d1.FI	RW	1'b1
2	UI	Enables error reporting interrupt as specified in por_errfr_p0_d1.UI	RW	1'b1
1	Reserved	Reserved	RO	-
0	ED	Enables error detection as specified in por_errfr_p0_d1.ED	RW	1'b1

por_errstatus_p0_d1

Functions as the error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3090
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

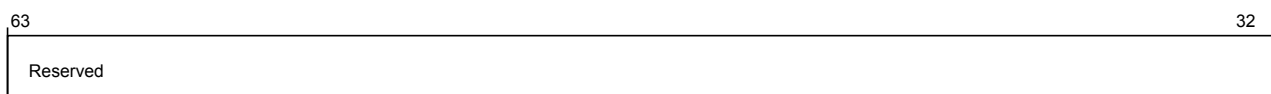


Figure 4-2536 por_fdc_por_errstatus_p0_d1 (high)

The following table shows the por_errstatus_p0_d1 higher register bit assignments.

Table 4-2553 `por_fdc_por_errstatus_p0_d1` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

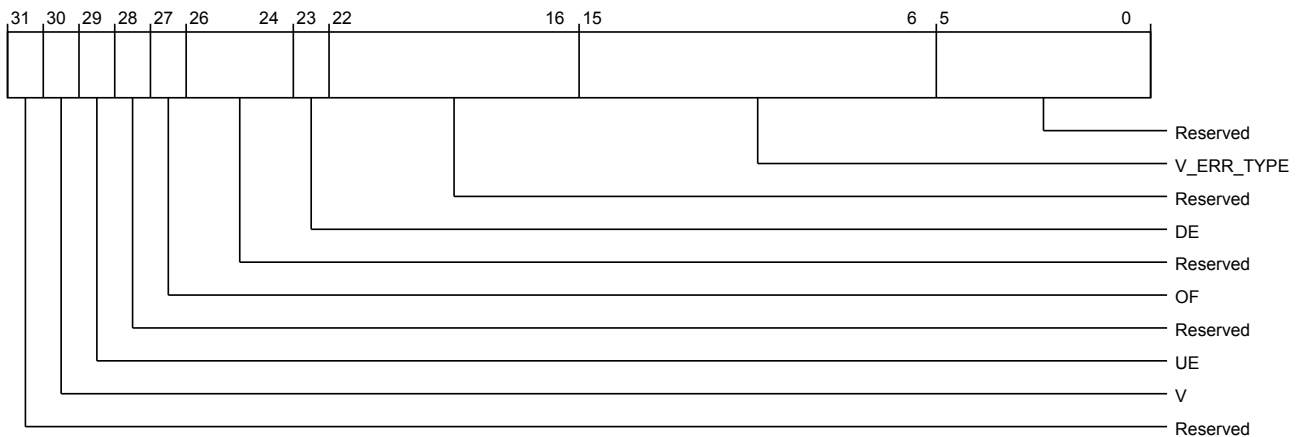


Figure 4-2537 `por_fdc_por_errstatus_p0_d1` (low)

The following table shows the `por_errstatus_p0_d1` lower register bit assignments.

Table 4-2554 `por_fdc_por_errstatus_p0_d1` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30	V	Register valid; writes to this bit are ignored if any of the UE or DE bit is set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one critical error detected 1'b0: No critical errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors for the same error type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the same type detected as described	W1C	1'b0
26:24	Reserved	Reserved	RO	-

Table 4-2554 por_fdc_por_errstatus_p0_d1 (low) (continued)

Bits	Field name	Description	Type	Reset
23	DE	Non-critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one non-critical error detected 1'b0: No non-critical errors detected	W1C	1'b0
22:16	Reserved	Reserved	RO	-
15:6	V_ERR_TYPE	Error valid for the type of errors: writes to the bits are ignored if the V bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear V_ERR_TYPE[0]: clk error V_ERR_TYPE[1]: reset error V_ERR_TYPE[2]: lsc error V_ERR_TYPE[3]: ioc error V_ERR_TYPE[4]: async error V_ERR_TYPE[5]: hang error V_ERR_TYPE[6]: mpu error V_ERR_TYPE[7]: ecc ue error V_ERR_TYPE[8]: ecc ce error V_ERR_TYPE[9]: multiple errors	W1C	10'b0
5:0	Reserved	Reserved	RO	-

por_fdc_aux_ctl_p0_d1

Functions as the aux control register. Controls specific error features.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3098
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

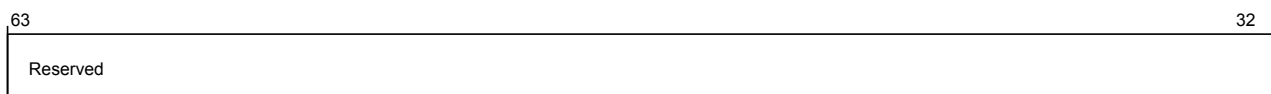


Figure 4-2538 por_fdc_por_fdc_aux_ctl_p0_d1 (high)

The following table shows the por_fdc_aux_ctl_p0_d1 higher register bit assignments.

Table 4-2555 `por_fdc_por_fdc_aux_ctl_p0_d1` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

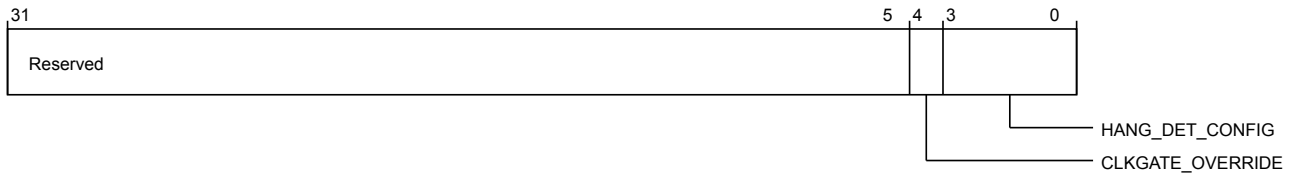


Figure 4-2539 `por_fdc_por_fdc_aux_ctl_p0_d1` (low)

The following table shows the `por_fdc_aux_ctl_p0_d1` lower register bit assignments.

Table 4-2556 `por_fdc_por_fdc_aux_ctl_p0_d1` (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	CLKGATE_OVERRIDE	FUSA checker clock gate disable in device connected to p0_d1 port.	RW	1'b0
3:0	HANG_DET_CONFIG	<p>timeout setting for hang detection in device connected to p0_d1 port.</p> <p>4'hx: timeout range in clock cycles (min - max), timeout range in duration @ 2Ghz (min - max)</p> <p>4'h0: 3x2²⁴ - 4x2²⁴, 25ms - 34ms</p> <p>4'h1: 3x2²³ - 4x2²³, 12.5ms - 17ms</p> <p>4'h2: 3x2²² - 4x2²², 6.29ms - 8.4ms</p> <p>4'h3: 3x2²¹ - 4x2²¹, 3.14ms - 4.2ms</p> <p>4'h4: 3x2²⁰ - 4x2²⁰, 1.57ms - 2.1ms</p> <p>4'h5: 3x2¹⁹ - 4x2¹⁹, 0.786ms - 1.05ms</p> <p>4'h6: 3x2¹⁸ - 4x2¹⁸, 393us - 525us</p> <p>4'h7: 3x2¹⁷ - 4x2¹⁷, 196us - 263us</p> <p>4'h8: 3x2¹⁶ - 4x2¹⁶, 98us - 132us</p> <p>4'h9: 3x2¹⁵ - 4x2¹⁵, 49us - 66us</p> <p>4'hA: 3x2¹⁴ - 4x2¹⁴, 24us - 33us</p> <p>4'hB: 3x2¹³ - 4x2¹³, 12us - 17us</p> <p>4'hC: 3x2¹² - 4x2¹², 6us - 8.2us</p> <p>4'hD: 3x2¹¹ - 4x2¹¹, 3us - 4.1us</p> <p>4'hE: 3x2¹⁰ - 4x2¹⁰, 1.5us - 2.1us</p> <p>4'hF: 3x2⁹ - 4x2⁹, 0.75us - 1.1us</p>	RW	4'b0

por_errfr_p0_d2

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h30C0
Register reset	64'b101001
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

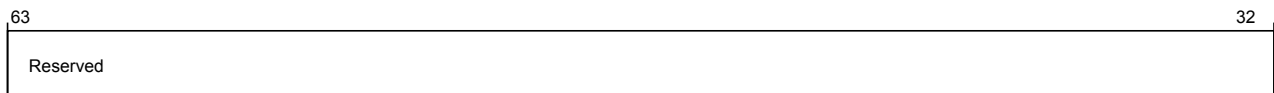


Figure 4-2540 por_fdc_por_errfr_p0_d2 (high)

The following table shows the por_errfr_p0_d2 higher register bit assignments.

Table 4-2557 por_fdc_por_errfr_p0_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

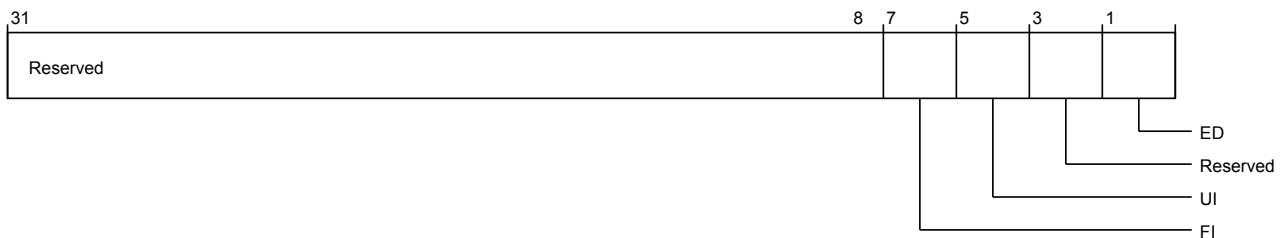


Figure 4-2541 por_fdc_por_errfr_p0_d2 (low)

The following table shows the por_errfr_p0_d2 lower register bit assignments.

Table 4-2558 por_fdc_por_errfr_p0_d2 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	FI	enable error propagation to FHI interrupt	RO	2'b10
5:4	UI	enable error propagation to ERI interrupt	RO	2'b10

Table 4-2558 por_fdc_por_errfr_p0_d2 (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	Reserved	Reserved	RO	-
1:0	ED	FUSA Error Detection	RO	2'b01

por_errctlr_p0_d2

Functions as the error control register. Controls whether specific error-reporting and fault-handling interrupts are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h30C8
Register reset	64'b0111
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

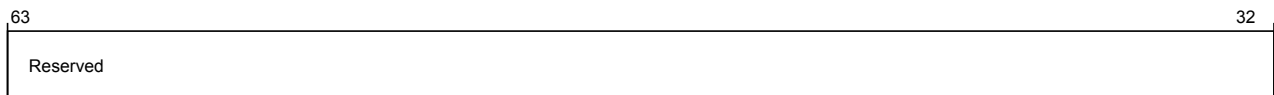


Figure 4-2542 por_fdc_por_errctlr_p0_d2 (high)

The following table shows the por_errctlr_p0_d2 higher register bit assignments.

Table 4-2559 por_fdc_por_errctlr_p0_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

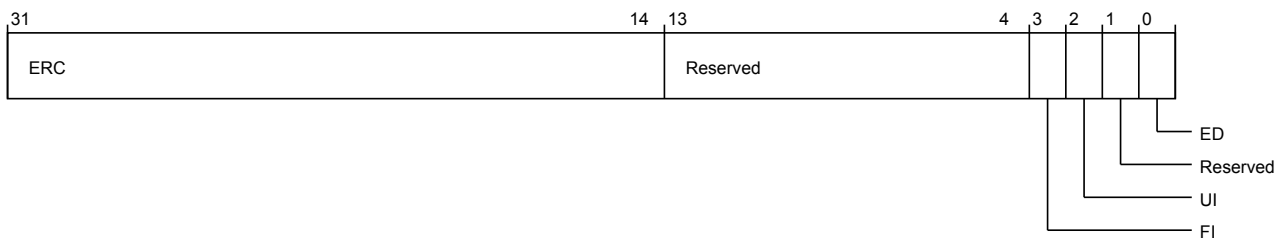


Figure 4-2543 por_fdc_por_errctlr_p0_d2 (low)

The following table shows the por_errctlr_p0_d2 lower register bit assignments.

Table 4-2560 por_fdc_por_errctlr_p0_d2 (low)

Bits	Field name	Description	Type	Reset
31:14	ERC	Error report control, two bits per error type 2'b00: report as critical error (ERI) 2'b01: report as non-critical error (FHI) 2'b10: do not report 2'b11: reserved ERC[1:0]: clk error ERC[3:2]: reset error ERC[5:4]: lsc error ERC[7:6]: ioc error ERC[9:8]: async error ERC[11:10]: hang error ERC[13:12]: mpu error ERC[15:14]: ecc ue error ERC[17:16]: ecc ce error	RW	18'b0
13:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt as specified in por_errfr_p0_d2.FI	RW	1'b1
2	UI	Enables error reporting interrupt as specified in por_errfr_p0_d2.UI	RW	1'b1
1	Reserved	Reserved	RO	-
0	ED	Enables error detection as specified in por_errfr_p0_d2.ED	RW	1'b1

por_errstatus_p0_d2

Functions as the error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h30D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

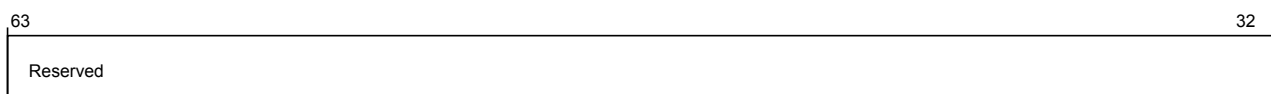


Figure 4-2544 por_fdc_por_errstatus_p0_d2 (high)

The following table shows the por_errstatus_p0_d2 higher register bit assignments.

Table 4-2561 `por_fdc_por_errstatus_p0_d2` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

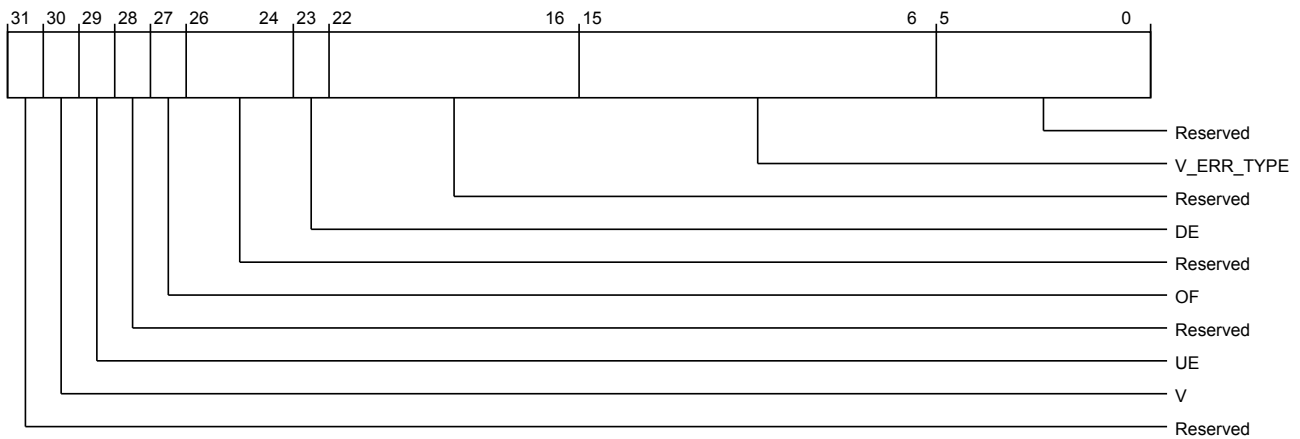


Figure 4-2545 `por_fdc_por_errstatus_p0_d2` (low)

The following table shows the `por_errstatus_p0_d2` lower register bit assignments.

Table 4-2562 `por_fdc_por_errstatus_p0_d2` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30	V	Register valid; writes to this bit are ignored if any of the UE or DE bit is set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one critical error detected 1'b0: No critical errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors for the same error type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the same type detected as described	W1C	1'b0
26:24	Reserved	Reserved	RO	-

Table 4-2562 `por_fdc_por_errstatus_p0_d2` (low) (continued)

Bits	Field name	Description	Type	Reset
23	DE	Non-critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one non-critical error detected 1'b0: No non-critical errors detected	W1C	1'b0
22:16	Reserved	Reserved	RO	-
15:6	V_ERR_TYPE	Error valid for the type of errors: writes to the bits are ignored if the V bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear V_ERR_TYPE[0]: clk error V_ERR_TYPE[1]: reset error V_ERR_TYPE[2]: lsc error V_ERR_TYPE[3]: ioc error V_ERR_TYPE[4]: async error V_ERR_TYPE[5]: hang error V_ERR_TYPE[6]: mpu error V_ERR_TYPE[7]: ecc ue error V_ERR_TYPE[8]: ecc ce error V_ERR_TYPE[9]: multiple errors	W1C	10'b0
5:0	Reserved	Reserved	RO	-

`por_fdc_aux_ctl_p0_d2`

Functions as the aux control register. Controls specific error features.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h30D8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

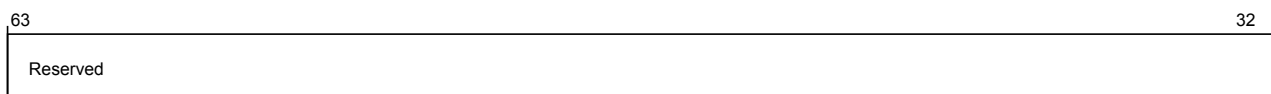


Figure 4-2546 `por_fdc_por_fdc_aux_ctl_p0_d2` (high)

The following table shows the `por_fdc_aux_ctl_p0_d2` higher register bit assignments.

Table 4-2563 `por_fdc_por_fdc_aux_ctl_p0_d2` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

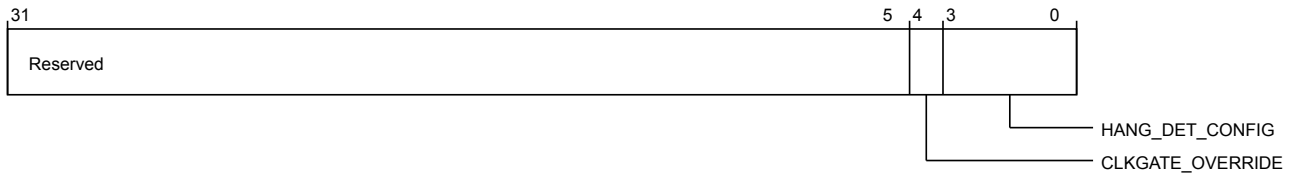


Figure 4-2547 `por_fdc_por_fdc_aux_ctl_p0_d2` (low)

The following table shows the `por_fdc_aux_ctl_p0_d2` lower register bit assignments.

Table 4-2564 `por_fdc_por_fdc_aux_ctl_p0_d2` (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	CLKGATE_OVERRIDE	FUSA checker clock gate disable in device connected to p0_d2 port.	RW	1'b0
3:0	HANG_DET_CONFIG	<p>timeout setting for hang detection in device connected to p0_d2 port.</p> <p>4'hx: timeout range in clock cycles (min - max), timeout range in duration @ 2Ghz (min - max)</p> <p>4'h0: 3x2²⁴ - 4x2²⁴, 25ms - 34ms</p> <p>4'h1: 3x2²³ - 4x2²³, 12.5ms - 17ms</p> <p>4'h2: 3x2²² - 4x2²², 6.29ms - 8.4ms</p> <p>4'h3: 3x2²¹ - 4x2²¹, 3.14ms - 4.2ms</p> <p>4'h4: 3x2²⁰ - 4x2²⁰, 1.57ms - 2.1ms</p> <p>4'h5: 3x2¹⁹ - 4x2¹⁹, 0.786ms - 1.05ms</p> <p>4'h6: 3x2¹⁸ - 4x2¹⁸, 393us - 525us</p> <p>4'h7: 3x2¹⁷ - 4x2¹⁷, 196us - 263us</p> <p>4'h8: 3x2¹⁶ - 4x2¹⁶, 98us - 132us</p> <p>4'h9: 3x2¹⁵ - 4x2¹⁵, 49us - 66us</p> <p>4'hA: 3x2¹⁴ - 4x2¹⁴, 24us - 33us</p> <p>4'hB: 3x2¹³ - 4x2¹³, 12us - 17us</p> <p>4'hC: 3x2¹² - 4x2¹², 6us - 8.2us</p> <p>4'hD: 3x2¹¹ - 4x2¹¹, 3us - 4.1us</p> <p>4'hE: 3x2¹⁰ - 4x2¹⁰, 1.5us - 2.1us</p> <p>4'hF: 3x2⁹ - 4x2⁹, 0.75us - 1.1us</p>	RW	4'b0

por_errfr_p0_d3

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3100
Register reset	64'b101001
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

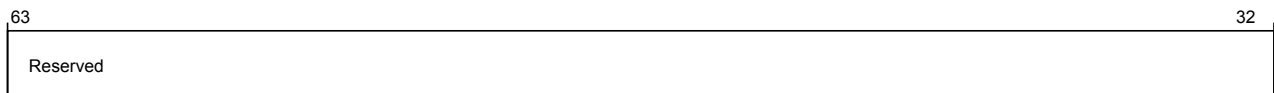


Figure 4-2548 por_fdc_por_errfr_p0_d3 (high)

The following table shows the por_errfr_p0_d3 higher register bit assignments.

Table 4-2565 por_fdc_por_errfr_p0_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

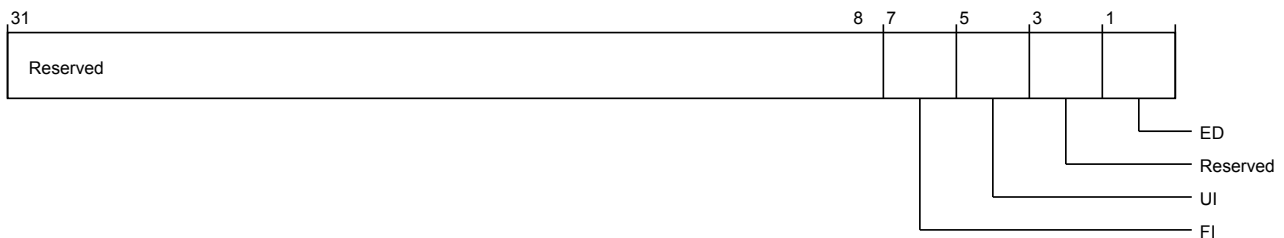


Figure 4-2549 por_fdc_por_errfr_p0_d3 (low)

The following table shows the por_errfr_p0_d3 lower register bit assignments.

Table 4-2566 por_fdc_por_errfr_p0_d3 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	FI	enable error propagation to FHI interrupt	RO	2'b10
5:4	UI	enable error propagation to ERI interrupt	RO	2'b10

Table 4-2566 por_fdc_por_errfr_p0_d3 (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	Reserved	Reserved	RO	-
1:0	ED	FUSA Error Detection	RO	2'b01

por_errctlr_p0_d3

Functions as the error control register. Controls whether specific error-reporting and fault-handling interrupts are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3108
Register reset	64'b0111
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-2550 por_fdc_por_errctlr_p0_d3 (high)

The following table shows the por_errctlr_p0_d3 higher register bit assignments.

Table 4-2567 por_fdc_por_errctlr_p0_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

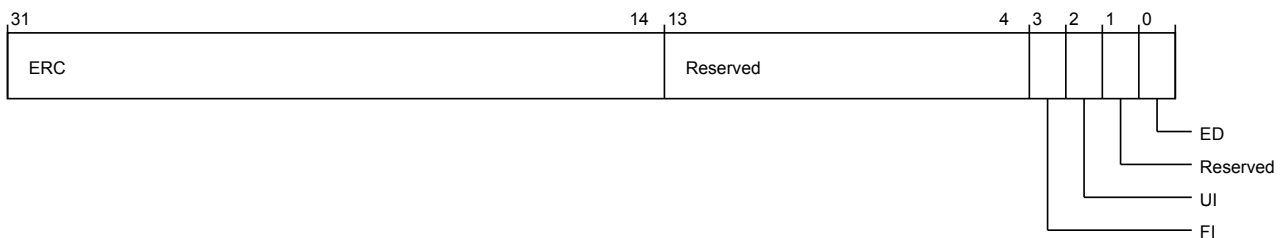


Figure 4-2551 por_fdc_por_errctlr_p0_d3 (low)

The following table shows the por_errctlr_p0_d3 lower register bit assignments.

Table 4-2568 por_fdc_por_errctlr_p0_d3 (low)

Bits	Field name	Description	Type	Reset
31:14	ERC	Error report control, two bits per error type 2'b00: report as critical error (ERI) 2'b01: report as non-critical error (FHI) 2'b10: do not report 2'b11: reserved ERC[1:0]: clk error ERC[3:2]: reset error ERC[5:4]: lsc error ERC[7:6]: ioc error ERC[9:8]: async error ERC[11:10]: hang error ERC[13:12]: mpu error ERC[15:14]: ecc ue error ERC[17:16]: ecc ce error	RW	18'b0
13:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt as specified in por_errfr_p0_d3.FI	RW	1'b1
2	UI	Enables error reporting interrupt as specified in por_errfr_p0_d3.UI	RW	1'b1
1	Reserved	Reserved	RO	-
0	ED	Enables error detection as specified in por_errfr_p0_d3.ED	RW	1'b1

por_errstatus_p0_d3

Functions as the error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3110
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

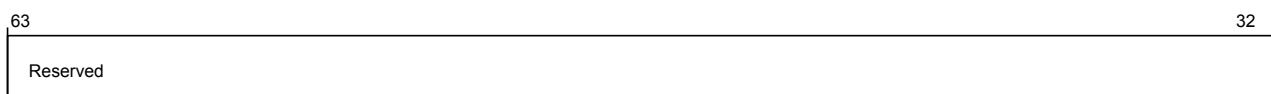


Figure 4-2552 por_fdc_por_errstatus_p0_d3 (high)

The following table shows the por_errstatus_p0_d3 higher register bit assignments.

Table 4-2569 `por_fdc_por_errstatus_p0_d3` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

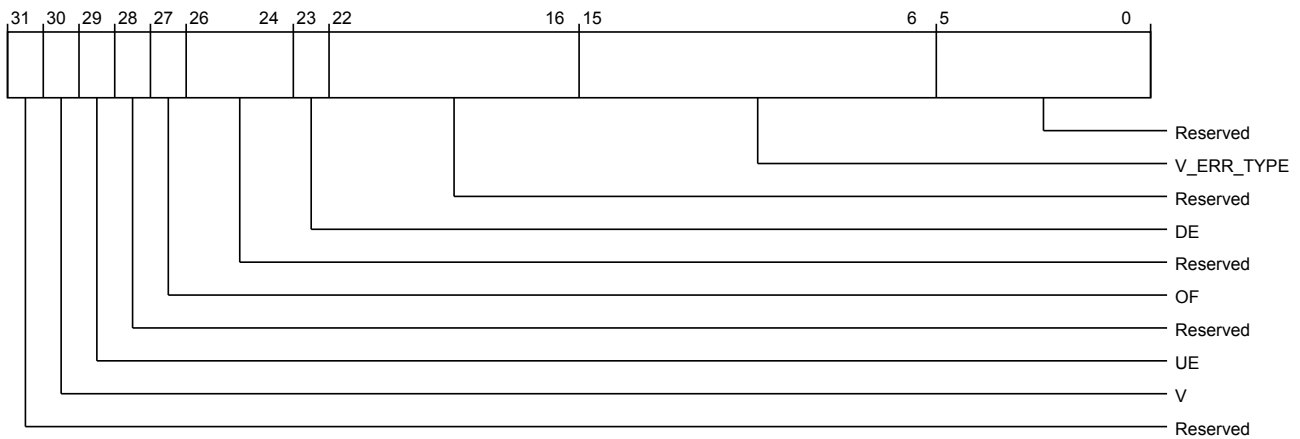


Figure 4-2553 `por_fdc_por_errstatus_p0_d3` (low)

The following table shows the `por_errstatus_p0_d3` lower register bit assignments.

Table 4-2570 `por_fdc_por_errstatus_p0_d3` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30	V	Register valid; writes to this bit are ignored if any of the UE or DE bit is set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one critical error detected 1'b0: No critical errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors for the same error type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the same type detected as described	W1C	1'b0
26:24	Reserved	Reserved	RO	-

Table 4-2570 `por_fdc_por_errstatus_p0_d3` (low) (continued)

Bits	Field name	Description	Type	Reset
23	DE	Non-critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one non-critical error detected 1'b0: No non-critical errors detected	W1C	1'b0
22:16	Reserved	Reserved	RO	-
15:6	V_ERR_TYPE	Error valid for the type of errors: writes to the bits are ignored if the V bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear V_ERR_TYPE[0]: clk error V_ERR_TYPE[1]: reset error V_ERR_TYPE[2]: lsc error V_ERR_TYPE[3]: ioc error V_ERR_TYPE[4]: async error V_ERR_TYPE[5]: hang error V_ERR_TYPE[6]: mpu error V_ERR_TYPE[7]: ecc ue error V_ERR_TYPE[8]: ecc ce error V_ERR_TYPE[9]: multiple errors	W1C	10'b0
5:0	Reserved	Reserved	RO	-

`por_fdc_aux_ctl_p0_d3`

Functions as the aux control register. Controls specific error features.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3118

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

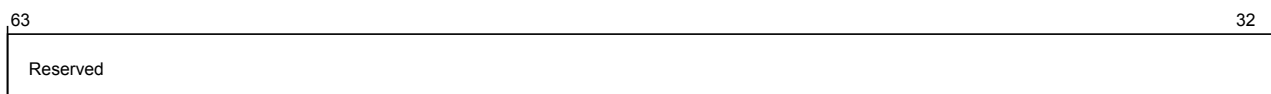


Figure 4-2554 `por_fdc_por_fdc_aux_ctl_p0_d3` (high)

The following table shows the `por_fdc_aux_ctl_p0_d3` higher register bit assignments.

Table 4-2571 `por_fdc_por_fdc_aux_ctl_p0_d3` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

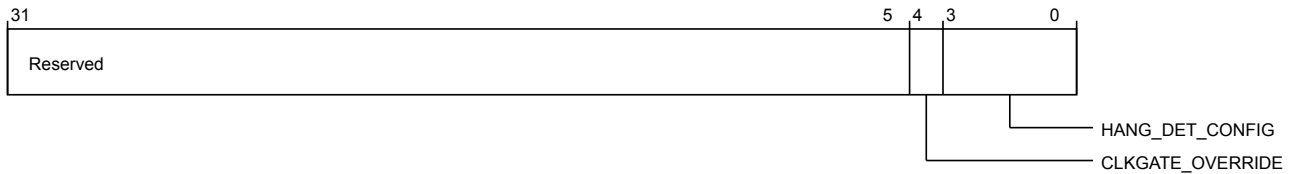


Figure 4-2555 `por_fdc_por_fdc_aux_ctl_p0_d3` (low)

The following table shows the `por_fdc_aux_ctl_p0_d3` lower register bit assignments.

Table 4-2572 `por_fdc_por_fdc_aux_ctl_p0_d3` (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	CLKGATE_OVERRIDE	FUSA checker clock gate disable in device connected to p0_d3 port.	RW	1'b0
3:0	HANG_DET_CONFIG	<p>timeout setting for hang detection in device connected to p0_d3 port.</p> <p>4'hx: timeout range in clock cycles (min - max), timeout range in duration @ 2Ghz (min - max)</p> <p>4'h0: 3x2²⁴ - 4x2²⁴, 25ms - 34ms</p> <p>4'h1: 3x2²³ - 4x2²³, 12.5ms - 17ms</p> <p>4'h2: 3x2²² - 4x2²², 6.29ms - 8.4ms</p> <p>4'h3: 3x2²¹ - 4x2²¹, 3.14ms - 4.2ms</p> <p>4'h4: 3x2²⁰ - 4x2²⁰, 1.57ms - 2.1ms</p> <p>4'h5: 3x2¹⁹ - 4x2¹⁹, 0.786ms - 1.05ms</p> <p>4'h6: 3x2¹⁸ - 4x2¹⁸, 393us - 525us</p> <p>4'h7: 3x2¹⁷ - 4x2¹⁷, 196us - 263us</p> <p>4'h8: 3x2¹⁶ - 4x2¹⁶, 98us - 132us</p> <p>4'h9: 3x2¹⁵ - 4x2¹⁵, 49us - 66us</p> <p>4'hA: 3x2¹⁴ - 4x2¹⁴, 24us - 33us</p> <p>4'hB: 3x2¹³ - 4x2¹³, 12us - 17us</p> <p>4'hC: 3x2¹² - 4x2¹², 6us - 8.2us</p> <p>4'hD: 3x2¹¹ - 4x2¹¹, 3us - 4.1us</p> <p>4'hE: 3x2¹⁰ - 4x2¹⁰, 1.5us - 2.1us</p> <p>4'hF: 3x2⁹ - 4x2⁹, 0.75us - 1.1us</p>	RW	4'b0

por_errfr_p1_d0

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3140
Register reset	64'b101001
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-2556 por_fdc_por_errfr_p1_d0 (high)

The following table shows the por_errfr_p1_d0 higher register bit assignments.

Table 4-2573 por_fdc_por_errfr_p1_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

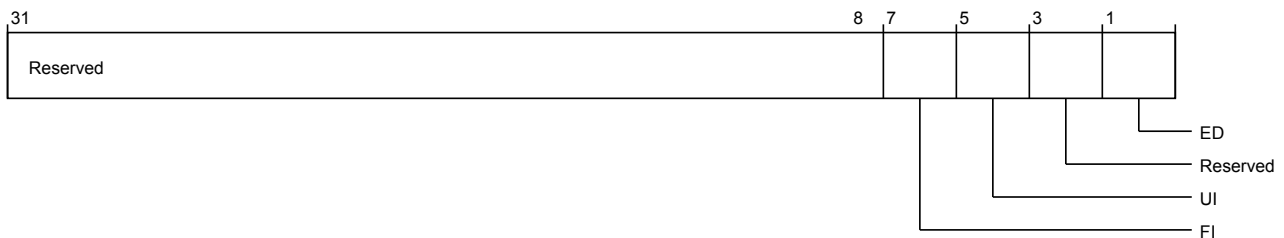


Figure 4-2557 por_fdc_por_errfr_p1_d0 (low)

The following table shows the por_errfr_p1_d0 lower register bit assignments.

Table 4-2574 por_fdc_por_errfr_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	FI	enable error propagation to FHI interrupt	RO	2'b10
5:4	UI	enable error propagation to ERI interrupt	RO	2'b10

Table 4-2574 `por_fdc_por_errfr_p1_d0` (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	Reserved	Reserved	RO	-
1:0	ED	FUSA Error Detection	RO	2'b01

`por_errctlr_p1_d0`

Functions as the error control register. Controls whether specific error-reporting and fault-handling interrupts are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3148
Register reset	64'b0111
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-2558 `por_fdc_por_errctlr_p1_d0` (high)

The following table shows the `por_errctlr_p1_d0` higher register bit assignments.

Table 4-2575 `por_fdc_por_errctlr_p1_d0` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

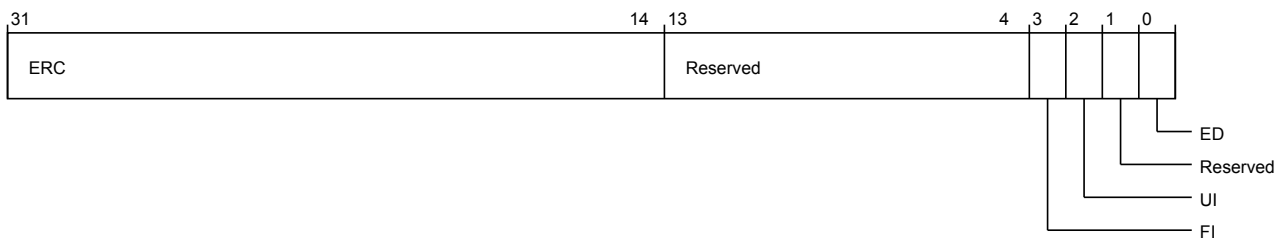


Figure 4-2559 `por_fdc_por_errctlr_p1_d0` (low)

The following table shows the `por_errctlr_p1_d0` lower register bit assignments.

Table 4-2576 por_fdc_por_errctlr_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:14	ERC	Error report control, two bits per error type 2'b00: report as critical error (ERI) 2'b01: report as non-critical error (FHI) 2'b10: do not report 2'b11: reserved ERC[1:0]: clk error ERC[3:2]: reset error ERC[5:4]: lsc error ERC[7:6]: ioc error ERC[9:8]: async error ERC[11:10]: hang error ERC[13:12]: mpu error ERC[15:14]: ecc ue error ERC[17:16]: ecc ce error	RW	18'b0
13:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt as specified in por_errfr_p1_d0.FI	RW	1'b1
2	UI	Enables error reporting interrupt as specified in por_errfr_p1_d0.UI	RW	1'b1
1	Reserved	Reserved	RO	-
0	ED	Enables error detection as specified in por_errfr_p1_d0.ED	RW	1'b1

por_errstatus_p1_d0

Functions as the error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3150
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

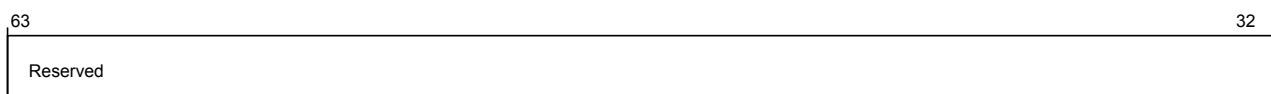


Figure 4-2560 por_fdc_por_errstatus_p1_d0 (high)

The following table shows the por_errstatus_p1_d0 higher register bit assignments.

Table 4-2577 `por_fdc_por_errstatus_p1_d0` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

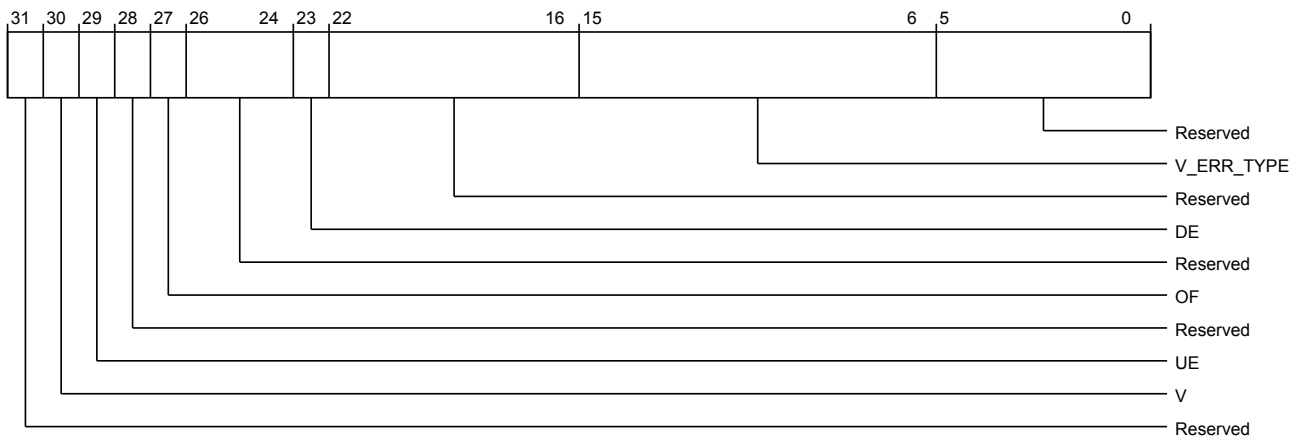


Figure 4-2561 `por_fdc_por_errstatus_p1_d0` (low)

The following table shows the `por_errstatus_p1_d0` lower register bit assignments.

Table 4-2578 `por_fdc_por_errstatus_p1_d0` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30	V	Register valid; writes to this bit are ignored if any of the UE or DE bit is set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one critical error detected 1'b0: No critical errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors for the same error type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the same type detected as described	W1C	1'b0
26:24	Reserved	Reserved	RO	-

Table 4-2578 por_fdc_por_errstatus_p1_d0 (low) (continued)

Bits	Field name	Description	Type	Reset
23	DE	Non-critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one non-critical error detected 1'b0: No non-critical errors detected	W1C	1'b0
22:16	Reserved	Reserved	RO	-
15:6	V_ERR_TYPE	Error valid for the type of errors: writes to the bits are ignored if the V bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear V_ERR_TYPE[0]: clk error V_ERR_TYPE[1]: reset error V_ERR_TYPE[2]: lsc error V_ERR_TYPE[3]: ioc error V_ERR_TYPE[4]: async error V_ERR_TYPE[5]: hang error V_ERR_TYPE[6]: mpu error V_ERR_TYPE[7]: ecc ue error V_ERR_TYPE[8]: ecc ce error V_ERR_TYPE[9]: multiple errors	W1C	10'b0
5:0	Reserved	Reserved	RO	-

por_fdc_aux_ctl_p1_d0

Functions as the aux control register. Controls specific error features.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3158

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

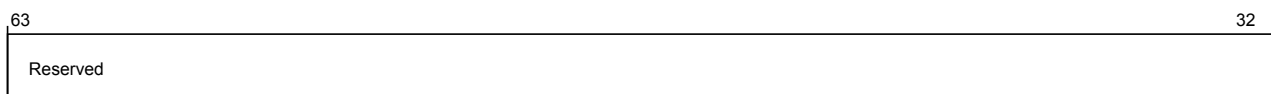


Figure 4-2562 por_fdc_por_fdc_aux_ctl_p1_d0 (high)

The following table shows the por_fdc_aux_ctl_p1_d0 higher register bit assignments.

Table 4-2579 por_fdc_por_fdc_aux_ctl_p1_d0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

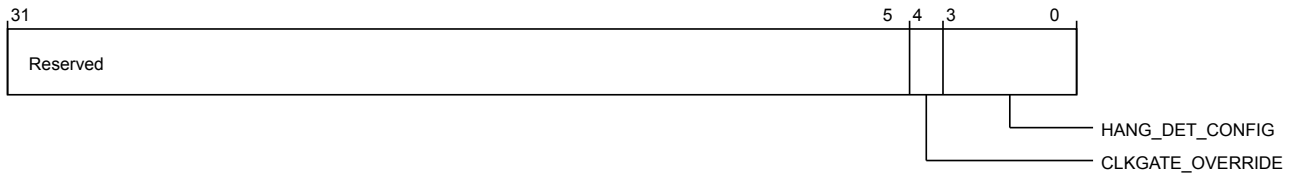


Figure 4-2563 por_fdc_por_fdc_aux_ctl_p1_d0 (low)

The following table shows the por_fdc_aux_ctl_p1_d0 lower register bit assignments.

Table 4-2580 por_fdc_por_fdc_aux_ctl_p1_d0 (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	CLKGATE_OVERRIDE	FUSA checker clock gate disable in device connected to p1_d0 port.	RW	1'b0
3:0	HANG_DET_CONFIG	<p>timeout setting for hang detection in device connected to p1_d0 port.</p> <p>4'hx: timeout range in clock cycles (min - max), timeout range in duration @ 2Ghz (min - max)</p> <p>4'h0: 3x2²⁴ - 4x2²⁴, 25ms - 34ms</p> <p>4'h1: 3x2²³ - 4x2²³, 12.5ms - 17ms</p> <p>4'h2: 3x2²² - 4x2²², 6.29ms - 8.4ms</p> <p>4'h3: 3x2²¹ - 4x2²¹, 3.14ms - 4.2ms</p> <p>4'h4: 3x2²⁰ - 4x2²⁰, 1.57ms - 2.1ms</p> <p>4'h5: 3x2¹⁹ - 4x2¹⁹, 0.786ms - 1.05ms</p> <p>4'h6: 3x2¹⁸ - 4x2¹⁸, 393us - 525us</p> <p>4'h7: 3x2¹⁷ - 4x2¹⁷, 196us - 263us</p> <p>4'h8: 3x2¹⁶ - 4x2¹⁶, 98us - 132us</p> <p>4'h9: 3x2¹⁵ - 4x2¹⁵, 49us - 66us</p> <p>4'hA: 3x2¹⁴ - 4x2¹⁴, 24us - 33us</p> <p>4'hB: 3x2¹³ - 4x2¹³, 12us - 17us</p> <p>4'hC: 3x2¹² - 4x2¹², 6us - 8.2us</p> <p>4'hD: 3x2¹¹ - 4x2¹¹, 3us - 4.1us</p> <p>4'hE: 3x2¹⁰ - 4x2¹⁰, 1.5us - 2.1us</p> <p>4'hF: 3x2⁹ - 4x2⁹, 0.75us - 1.1us</p>	RW	4'b0

por_errfr_p1_d1

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3180
Register reset	64'b101001
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-2564 por_fdc_por_errfr_p1_d1 (high)

The following table shows the por_errfr_p1_d1 higher register bit assignments.

Table 4-2581 por_fdc_por_errfr_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

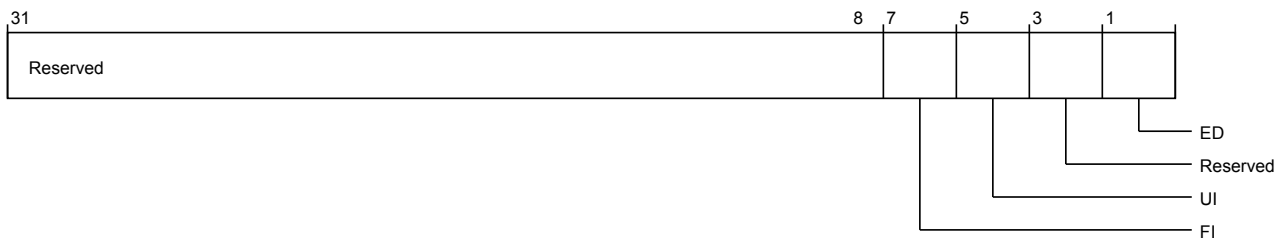


Figure 4-2565 por_fdc_por_errfr_p1_d1 (low)

The following table shows the por_errfr_p1_d1 lower register bit assignments.

Table 4-2582 por_fdc_por_errfr_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	FI	enable error propagation to FHI interrupt	RO	2'b10
5:4	UI	enable error propagation to ERI interrupt	RO	2'b10

Table 4-2582 por_fdc_por_errfr_p1_d1 (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	Reserved	Reserved	RO	-
1:0	ED	FUSA Error Detection	RO	2'b01

por_errctlr_p1_d1

Functions as the error control register. Controls whether specific error-reporting and fault-handling interrupts are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3188
Register reset	64'b0111
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

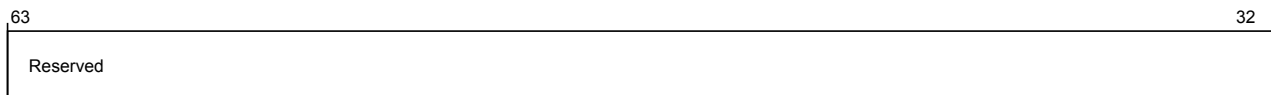


Figure 4-2566 por_fdc_por_errctlr_p1_d1 (high)

The following table shows the por_errctlr_p1_d1 higher register bit assignments.

Table 4-2583 por_fdc_por_errctlr_p1_d1 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

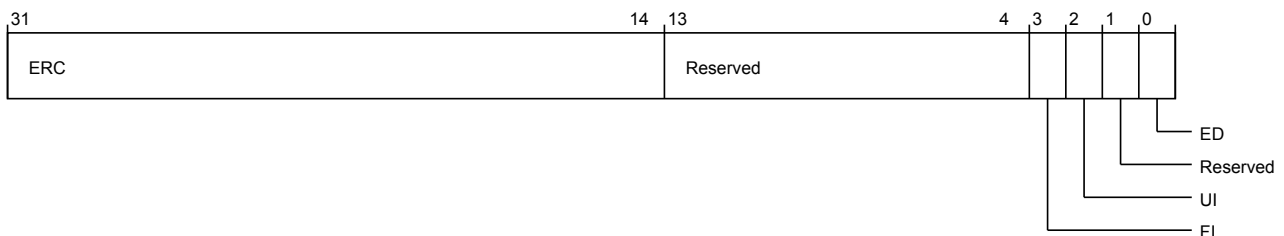


Figure 4-2567 por_fdc_por_errctlr_p1_d1 (low)

The following table shows the por_errctlr_p1_d1 lower register bit assignments.

Table 4-2584 por_fdc_por_errctlr_p1_d1 (low)

Bits	Field name	Description	Type	Reset
31:14	ERC	Error report control, two bits per error type 2'b00: report as critical error (ERI) 2'b01: report as non-critical error (FHI) 2'b10: do not report 2'b11: reserved ERC[1:0]: clk error ERC[3:2]: reset error ERC[5:4]: lsc error ERC[7:6]: ioc error ERC[9:8]: async error ERC[11:10]: hang error ERC[13:12]: mpu error ERC[15:14]: ecc ue error ERC[17:16]: ecc ce error	RW	18'b0
13:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt as specified in por_errfr_p1_d1.FI	RW	1'b1
2	UI	Enables error reporting interrupt as specified in por_errfr_p1_d1.UI	RW	1'b1
1	Reserved	Reserved	RO	-
0	ED	Enables error detection as specified in por_errfr_p1_d1.ED	RW	1'b1

por_errstatus_p1_d1

Functions as the error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3190
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

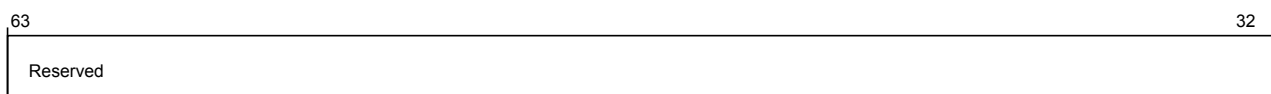


Figure 4-2568 por_fdc_por_errstatus_p1_d1 (high)

The following table shows the por_errstatus_p1_d1 higher register bit assignments.

Table 4-2585 `por_fdc_por_errstatus_p1_d1` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

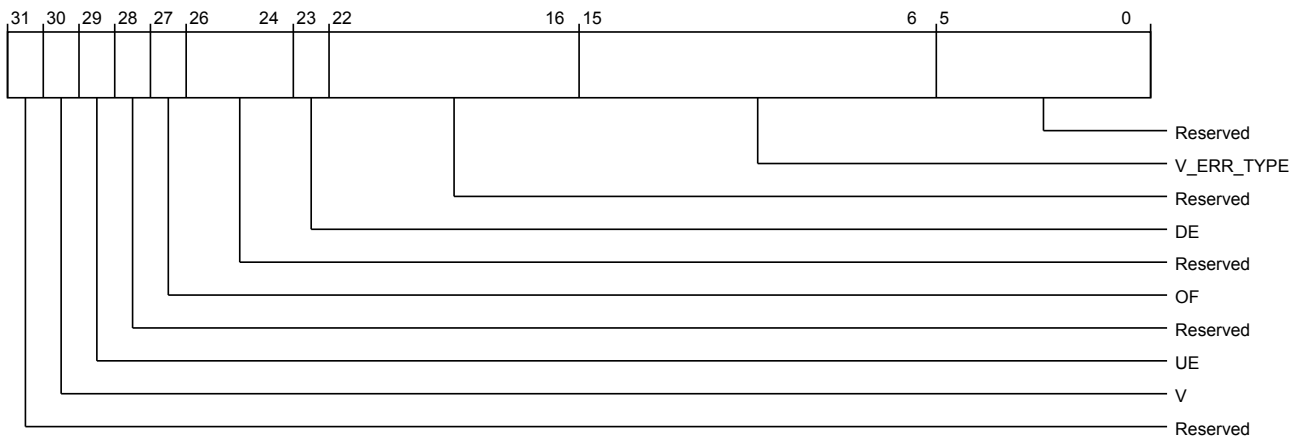


Figure 4-2569 `por_fdc_por_errstatus_p1_d1` (low)

The following table shows the `por_errstatus_p1_d1` lower register bit assignments.

Table 4-2586 `por_fdc_por_errstatus_p1_d1` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30	V	Register valid; writes to this bit are ignored if any of the UE or DE bit is set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one critical error detected 1'b0: No critical errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors for the same error type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the same type detected as described	W1C	1'b0
26:24	Reserved	Reserved	RO	-

Table 4-2586 `por_fdc_por_errstatus_p1_d1` (low) (continued)

Bits	Field name	Description	Type	Reset
23	DE	Non-critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one non-critical error detected 1'b0: No non-critical errors detected	W1C	1'b0
22:16	Reserved	Reserved	RO	-
15:6	V_ERR_TYPE	Error valid for the type of errors: writes to the bits are ignored if the V bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear V_ERR_TYPE[0]: clk error V_ERR_TYPE[1]: reset error V_ERR_TYPE[2]: lsc error V_ERR_TYPE[3]: ioc error V_ERR_TYPE[4]: async error V_ERR_TYPE[5]: hang error V_ERR_TYPE[6]: mpu error V_ERR_TYPE[7]: ecc ue error V_ERR_TYPE[8]: ecc ce error V_ERR_TYPE[9]: multiple errors	W1C	10'b0
5:0	Reserved	Reserved	RO	-

`por_fdc_aux_ctl_p1_d1`

Functions as the aux control register. Controls specific error features.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3198

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

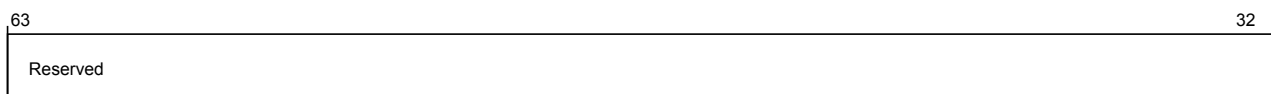


Figure 4-2570 `por_fdc_por_fdc_aux_ctl_p1_d1` (high)

The following table shows the `por_fdc_aux_ctl_p1_d1` higher register bit assignments.

Table 4-2587 `por_fdc_por_fdc_aux_ctl_p1_d1` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

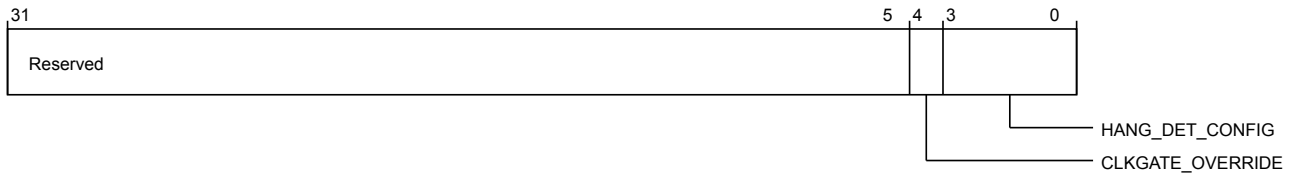


Figure 4-2571 `por_fdc_por_fdc_aux_ctl_p1_d1` (low)

The following table shows the `por_fdc_aux_ctl_p1_d1` lower register bit assignments.

Table 4-2588 `por_fdc_por_fdc_aux_ctl_p1_d1` (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	CLKGATE_OVERRIDE	FUSA checker clock gate disable in device connected to p1_d1 port.	RW	1'b0
3:0	HANG_DET_CONFIG	<p>timeout setting for hang detection in device connected to p1_d1 port.</p> <p>4'hx: timeout range in clock cycles (min - max), timeout range in duration @ 2Ghz (min - max)</p> <p>4'h0: 3x2²⁴ - 4x2²⁴, 25ms - 34ms</p> <p>4'h1: 3x2²³ - 4x2²³, 12.5ms - 17ms</p> <p>4'h2: 3x2²² - 4x2²², 6.29ms - 8.4ms</p> <p>4'h3: 3x2²¹ - 4x2²¹, 3.14ms - 4.2ms</p> <p>4'h4: 3x2²⁰ - 4x2²⁰, 1.57ms - 2.1ms</p> <p>4'h5: 3x2¹⁹ - 4x2¹⁹, 0.786ms - 1.05ms</p> <p>4'h6: 3x2¹⁸ - 4x2¹⁸, 393us - 525us</p> <p>4'h7: 3x2¹⁷ - 4x2¹⁷, 196us - 263us</p> <p>4'h8: 3x2¹⁶ - 4x2¹⁶, 98us - 132us</p> <p>4'h9: 3x2¹⁵ - 4x2¹⁵, 49us - 66us</p> <p>4'hA: 3x2¹⁴ - 4x2¹⁴, 24us - 33us</p> <p>4'hB: 3x2¹³ - 4x2¹³, 12us - 17us</p> <p>4'hC: 3x2¹² - 4x2¹², 6us - 8.2us</p> <p>4'hD: 3x2¹¹ - 4x2¹¹, 3us - 4.1us</p> <p>4'hE: 3x2¹⁰ - 4x2¹⁰, 1.5us - 2.1us</p> <p>4'hF: 3x2⁹ - 4x2⁹, 0.75us - 1.1us</p>	RW	4'b0

por_errfr_p1_d2

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h31C0
Register reset	64'b101001
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

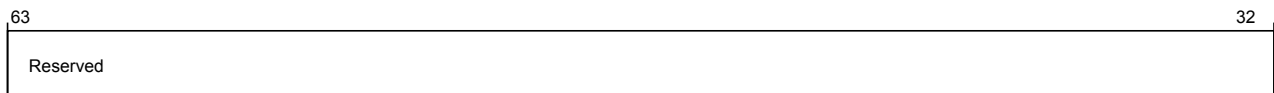


Figure 4-2572 por_fdc_por_errfr_p1_d2 (high)

The following table shows the por_errfr_p1_d2 higher register bit assignments.

Table 4-2589 por_fdc_por_errfr_p1_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

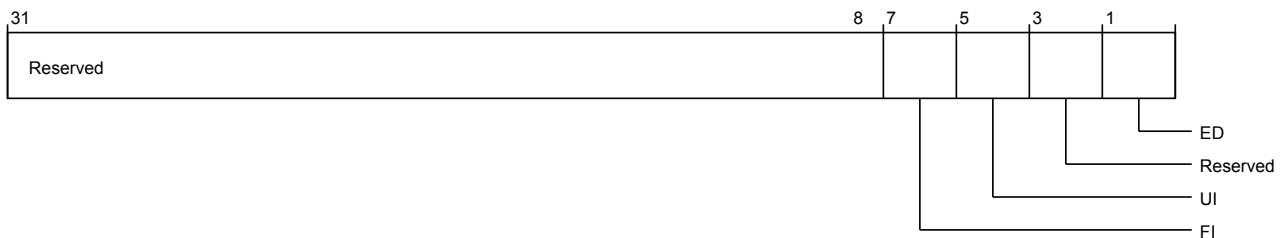


Figure 4-2573 por_fdc_por_errfr_p1_d2 (low)

The following table shows the por_errfr_p1_d2 lower register bit assignments.

Table 4-2590 por_fdc_por_errfr_p1_d2 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	FI	enable error propagation to FHI interrupt	RO	2'b10
5:4	UI	enable error propagation to ERI interrupt	RO	2'b10

Table 4-2590 por_fdc_por_errfr_p1_d2 (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	Reserved	Reserved	RO	-
1:0	ED	FUSA Error Detection	RO	2'b01

por_errctlr_p1_d2

Functions as the error control register. Controls whether specific error-reporting and fault-handling interrupts are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h31C8
Register reset	64'b0111
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-2574 por_fdc_por_errctlr_p1_d2 (high)

The following table shows the por_errctlr_p1_d2 higher register bit assignments.

Table 4-2591 por_fdc_por_errctlr_p1_d2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

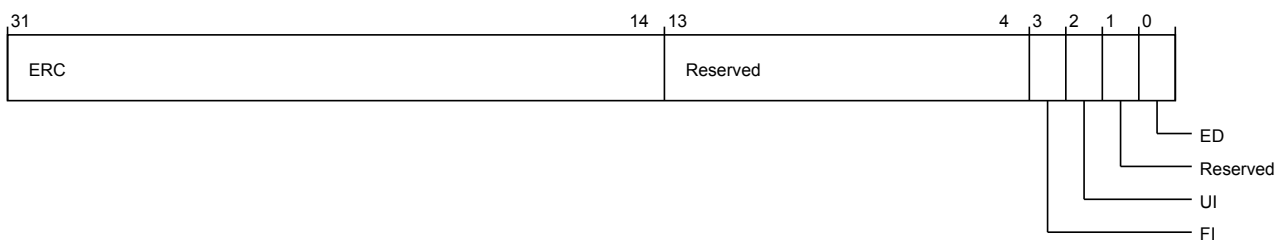


Figure 4-2575 por_fdc_por_errctlr_p1_d2 (low)

The following table shows the por_errctlr_p1_d2 lower register bit assignments.

Table 4-2592 por_fdc_por_errctlr_p1_d2 (low)

Bits	Field name	Description	Type	Reset
31:14	ERC	Error report control, two bits per error type 2'b00: report as critical error (ERI) 2'b01: report as non-critical error (FHI) 2'b10: do not report 2'b11: reserved ERC[1:0]: clk error ERC[3:2]: reset error ERC[5:4]: lsc error ERC[7:6]: ioc error ERC[9:8]: async error ERC[11:10]: hang error ERC[13:12]: mpu error ERC[15:14]: ecc ue error ERC[17:16]: ecc ce error	RW	18'b0
13:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt as specified in por_errfr_p1_d2.FI	RW	1'b1
2	UI	Enables error reporting interrupt as specified in por_errfr_p1_d2.UI	RW	1'b1
1	Reserved	Reserved	RO	-
0	ED	Enables error detection as specified in por_errfr_p1_d2.ED	RW	1'b1

por_errstatus_p1_d2

Functions as the error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h31D0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

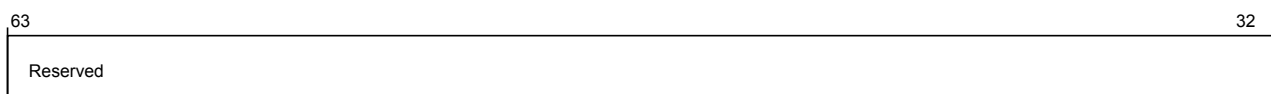


Figure 4-2576 por_fdc_por_errstatus_p1_d2 (high)

The following table shows the por_errstatus_p1_d2 higher register bit assignments.

Table 4-2593 `por_fdc_por_errstatus_p1_d2` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

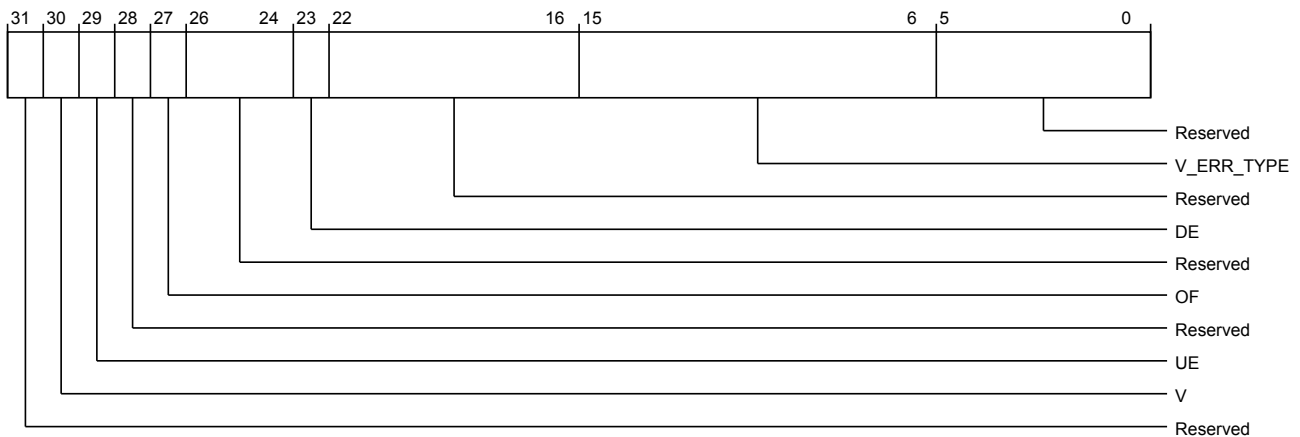


Figure 4-2577 `por_fdc_por_errstatus_p1_d2` (low)

The following table shows the `por_errstatus_p1_d2` lower register bit assignments.

Table 4-2594 `por_fdc_por_errstatus_p1_d2` (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30	V	Register valid; writes to this bit are ignored if any of the UE or DE bit is set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one critical error detected 1'b0: No critical errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors for the same error type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the same type detected as described	W1C	1'b0
26:24	Reserved	Reserved	RO	-

Table 4-2594 `por_fdc_por_errstatus_p1_d2` (low) (continued)

Bits	Field name	Description	Type	Reset
23	DE	Non-critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one non-critical error detected 1'b0: No non-critical errors detected	W1C	1'b0
22:16	Reserved	Reserved	RO	-
15:6	V_ERR_TYPE	Error valid for the type of errors: writes to the bits are ignored if the V bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear V_ERR_TYPE[0]: clk error V_ERR_TYPE[1]: reset error V_ERR_TYPE[2]: lsc error V_ERR_TYPE[3]: ioc error V_ERR_TYPE[4]: async error V_ERR_TYPE[5]: hang error V_ERR_TYPE[6]: mpu error V_ERR_TYPE[7]: ecc ue error V_ERR_TYPE[8]: ecc ce error V_ERR_TYPE[9]: multiple errors	W1C	10'b0
5:0	Reserved	Reserved	RO	-

`por_fdc_aux_ctl_p1_d2`

Functions as the aux control register. Controls specific error features.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h31D8
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

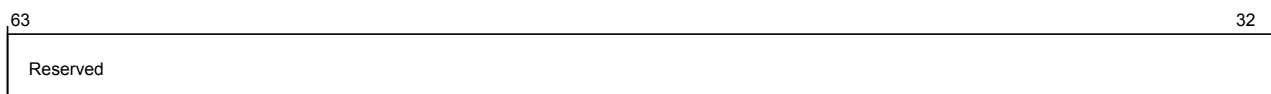


Figure 4-2578 `por_fdc_por_fdc_aux_ctl_p1_d2` (high)

The following table shows the `por_fdc_aux_ctl_p1_d2` higher register bit assignments.

Table 4-2595 `por_fdc_por_fdc_aux_ctl_p1_d2` (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

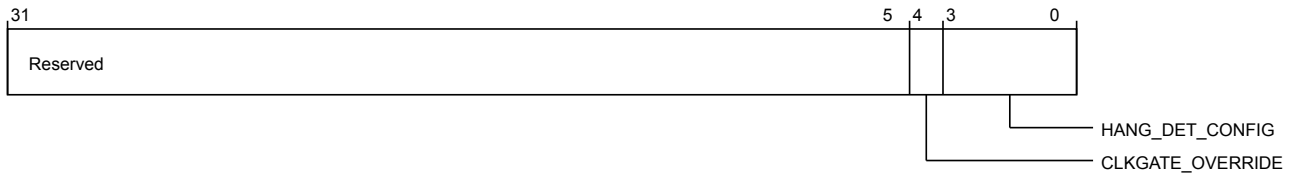


Figure 4-2579 `por_fdc_por_fdc_aux_ctl_p1_d2` (low)

The following table shows the `por_fdc_aux_ctl_p1_d2` lower register bit assignments.

Table 4-2596 `por_fdc_por_fdc_aux_ctl_p1_d2` (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	CLKGATE_OVERRIDE	FUSA checker clock gate disable in device connected to p1_d2 port.	RW	1'b0
3:0	HANG_DET_CONFIG	<p>timeout setting for hang detection in device connected to p1_d2 port.</p> <p>4'hx: timeout range in clock cycles (min - max), timeout range in duration @ 2Ghz (min - max)</p> <p>4'h0: 3x2²⁴ - 4x2²⁴, 25ms - 34ms</p> <p>4'h1: 3x2²³ - 4x2²³, 12.5ms - 17ms</p> <p>4'h2: 3x2²² - 4x2²², 6.29ms - 8.4ms</p> <p>4'h3: 3x2²¹ - 4x2²¹, 3.14ms - 4.2ms</p> <p>4'h4: 3x2²⁰ - 4x2²⁰, 1.57ms - 2.1ms</p> <p>4'h5: 3x2¹⁹ - 4x2¹⁹, 0.786ms - 1.05ms</p> <p>4'h6: 3x2¹⁸ - 4x2¹⁸, 393us - 525us</p> <p>4'h7: 3x2¹⁷ - 4x2¹⁷, 196us - 263us</p> <p>4'h8: 3x2¹⁶ - 4x2¹⁶, 98us - 132us</p> <p>4'h9: 3x2¹⁵ - 4x2¹⁵, 49us - 66us</p> <p>4'hA: 3x2¹⁴ - 4x2¹⁴, 24us - 33us</p> <p>4'hB: 3x2¹³ - 4x2¹³, 12us - 17us</p> <p>4'hC: 3x2¹² - 4x2¹², 6us - 8.2us</p> <p>4'hD: 3x2¹¹ - 4x2¹¹, 3us - 4.1us</p> <p>4'hE: 3x2¹⁰ - 4x2¹⁰, 1.5us - 2.1us</p> <p>4'hF: 3x2⁹ - 4x2⁹, 0.75us - 1.1us</p>	RW	4'b0

por_errfr_p1_d3

Functions as the error feature register.

Its characteristics are:

Type	RO
Register width (Bits)	64
Address offset	14'h3200
Register reset	64'b101001
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

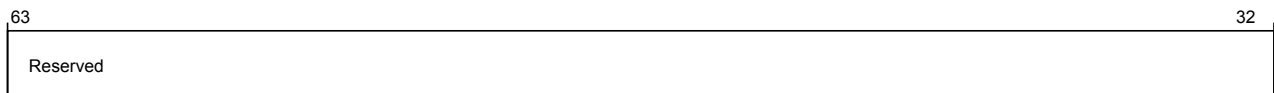


Figure 4-2580 por_fdc_por_errfr_p1_d3 (high)

The following table shows the por_errfr_p1_d3 higher register bit assignments.

Table 4-2597 por_fdc_por_errfr_p1_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

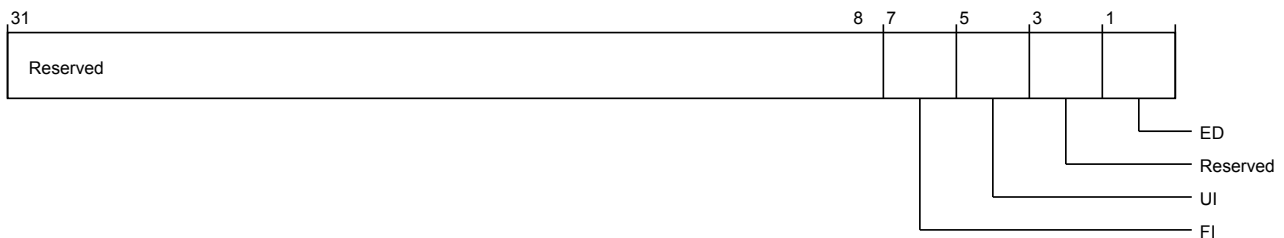


Figure 4-2581 por_fdc_por_errfr_p1_d3 (low)

The following table shows the por_errfr_p1_d3 lower register bit assignments.

Table 4-2598 por_fdc_por_errfr_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	FI	enable error propagation to FHI interrupt	RO	2'b10
5:4	UI	enable error propagation to ERI interrupt	RO	2'b10

Table 4-2598 por_fdc_por_errfr_p1_d3 (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	Reserved	Reserved	RO	-
1:0	ED	FUSA Error Detection	RO	2'b01

por_errctlr_p1_d3

Functions as the error control register. Controls whether specific error-reporting and fault-handling interrupts are enabled.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3208
Register reset	64'b0111
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.



Figure 4-2582 por_fdc_por_errctlr_p1_d3 (high)

The following table shows the por_errctlr_p1_d3 higher register bit assignments.

Table 4-2599 por_fdc_por_errctlr_p1_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

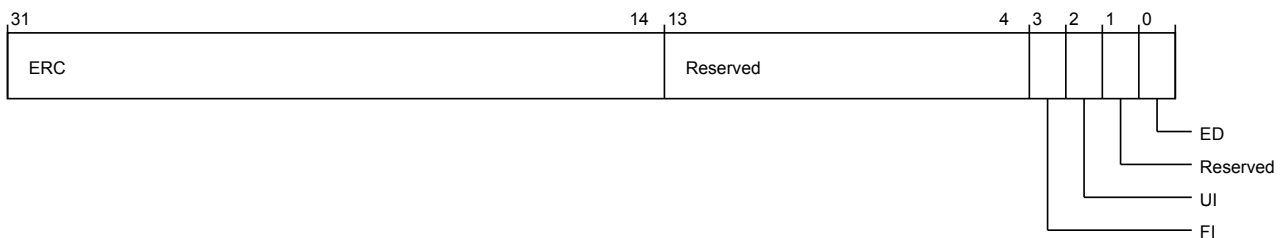


Figure 4-2583 por_fdc_por_errctlr_p1_d3 (low)

The following table shows the por_errctlr_p1_d3 lower register bit assignments.

Table 4-2600 por_fdc_por_errctlr_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31:14	ERC	Error report control, two bits per error type 2'b00: report as critical error (ERI) 2'b01: report as non-critical error (FHI) 2'b10: do not report 2'b11: reserved ERC[1:0]: clk error ERC[3:2]: reset error ERC[5:4]: lsc error ERC[7:6]: ioc error ERC[9:8]: async error ERC[11:10]: hang error ERC[13:12]: mpu error ERC[15:14]: ecc ue error ERC[17:16]: ecc ce error	RW	18'b0
13:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt as specified in por_errfr_p1_d3.FI	RW	1'b1
2	UI	Enables error reporting interrupt as specified in por_errfr_p1_d3.UI	RW	1'b1
1	Reserved	Reserved	RO	-
0	ED	Enables error detection as specified in por_errfr_p1_d3.ED	RW	1'b1

por_errstatus_p1_d3

Functions as the error status register.

Its characteristics are:

Type	W1C
Register width (Bits)	64
Address offset	14'h3210
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

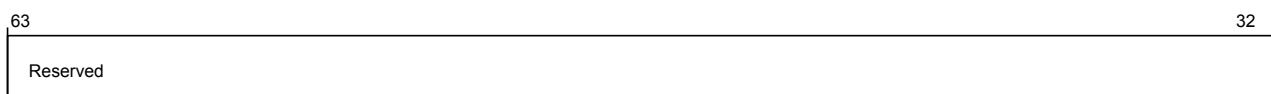


Figure 4-2584 por_fdc_por_errstatus_p1_d3 (high)

The following table shows the por_errstatus_p1_d3 higher register bit assignments.

Table 4-2601 por_fdc_por_errstatus_p1_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

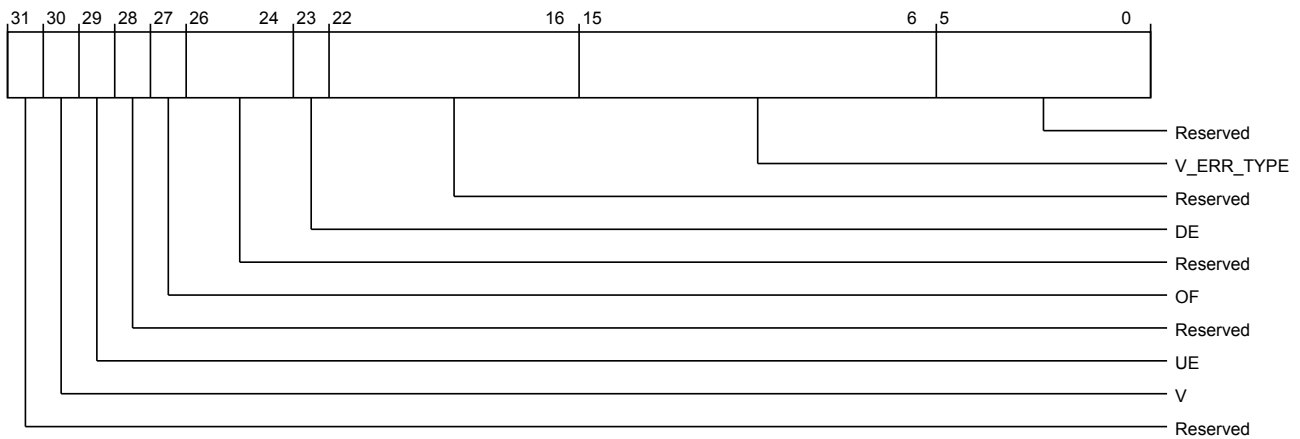


Figure 4-2585 por_fdc_por_errstatus_p1_d3 (low)

The following table shows the por_errstatus_p1_d3 lower register bit assignments.

Table 4-2602 por_fdc_por_errstatus_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30	V	Register valid; writes to this bit are ignored if any of the UE or DE bit is set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one critical error detected 1'b0: No critical errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors for the same error type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the same type detected as described	W1C	1'b0
26:24	Reserved	Reserved	RO	-

Table 4-2602 `por_fdc_por_errstatus_p1_d3` (low) (continued)

Bits	Field name	Description	Type	Reset
23	DE	Non-critical errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one non-critical error detected 1'b0: No non-critical errors detected	W1C	1'b0
22:16	Reserved	Reserved	RO	-
15:6	V_ERR_TYPE	Error valid for the type of errors: writes to the bits are ignored if the V bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear V_ERR_TYPE[0]: clk error V_ERR_TYPE[1]: reset error V_ERR_TYPE[2]: lsc error V_ERR_TYPE[3]: ioc error V_ERR_TYPE[4]: async error V_ERR_TYPE[5]: hang error V_ERR_TYPE[6]: mpu error V_ERR_TYPE[7]: ecc ue error V_ERR_TYPE[8]: ecc ce error V_ERR_TYPE[9]: multiple errors	W1C	10'b0
5:0	Reserved	Reserved	RO	-

`por_fdc_aux_ctl_p1_d3`

Functions as the aux control register. Controls specific error features.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3218

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

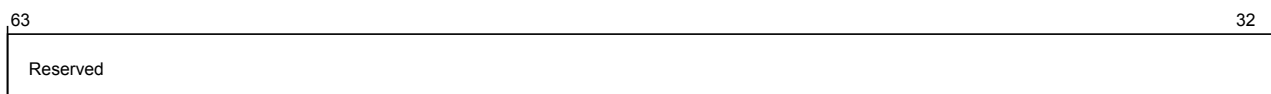


Figure 4-2586 `por_fdc_por_fdc_aux_ctl_p1_d3` (high)

The following table shows the `por_fdc_aux_ctl_p1_d3` higher register bit assignments.

Table 4-2603 por_fdc_por_fdc_aux_ctl_p1_d3 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

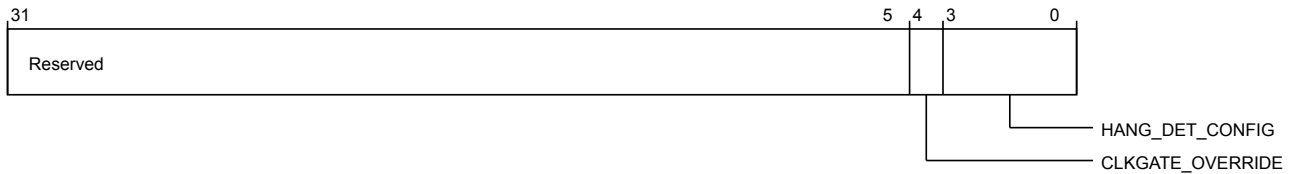


Figure 4-2587 por_fdc_por_fdc_aux_ctl_p1_d3 (low)

The following table shows the por_fdc_aux_ctl_p1_d3 lower register bit assignments.

Table 4-2604 por_fdc_por_fdc_aux_ctl_p1_d3 (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	CLKGATE_OVERRIDE	FUSA checker clock gate disable in device connected to p1_d3 port.	RW	1'b0
3:0	HANG_DET_CONFIG	<p>timeout setting for hang detection in device connected to p1_d3 port.</p> <p>4'hx: timeout range in clock cycles (min - max), timeout range in duration @ 2Ghz (min - max)</p> <p>4'h0: 3x2²⁴ - 4x2²⁴, 25ms - 34ms</p> <p>4'h1: 3x2²³ - 4x2²³, 12.5ms - 17ms</p> <p>4'h2: 3x2²² - 4x2²², 6.29ms - 8.4ms</p> <p>4'h3: 3x2²¹ - 4x2²¹, 3.14ms - 4.2ms</p> <p>4'h4: 3x2²⁰ - 4x2²⁰, 1.57ms - 2.1ms</p> <p>4'h5: 3x2¹⁹ - 4x2¹⁹, 0.786ms - 1.05ms</p> <p>4'h6: 3x2¹⁸ - 4x2¹⁸, 393us - 525us</p> <p>4'h7: 3x2¹⁷ - 4x2¹⁷, 196us - 263us</p> <p>4'h8: 3x2¹⁶ - 4x2¹⁶, 98us - 132us</p> <p>4'h9: 3x2¹⁵ - 4x2¹⁵, 49us - 66us</p> <p>4'hA: 3x2¹⁴ - 4x2¹⁴, 24us - 33us</p> <p>4'hB: 3x2¹³ - 4x2¹³, 12us - 17us</p> <p>4'hC: 3x2¹² - 4x2¹², 6us - 8.2us</p> <p>4'hD: 3x2¹¹ - 4x2¹¹, 3us - 4.1us</p> <p>4'hE: 3x2¹⁰ - 4x2¹⁰, 1.5us - 2.1us</p> <p>4'hF: 3x2⁹ - 4x2⁹, 0.75us - 1.1us</p>	RW	4'b0

4.4 CMN-600AE programming

This section contains CMN-600AE programming information.

This section contains the following subsections:

- [4.4.1 Boot-time programming sequence on page 4-1832.](#)
- [4.4.2 Runtime programming requirements on page 4-1832.](#)

4.4.1 Boot-time programming sequence

A specific boot-time programming sequence must be used to set up CMN-600AE correctly. An example sequence is provided, which uses a *System Control Processor* (SCP) to perform the initial boot configuration.

After reset, the following configuration steps must happen before broad access to CMN-600AE components is available:

1. CMN-600AE uses a default configuration to access boot flash through the HN-D ACE-Lite master interface and also the configuration registers.
2. An RN-F, or a master that is connected to an RN-I, must then access the configuration registers to configure CMN-600AE. This boot-time configuration must happen before there is broader access to components such as HN-F or SN.

The following example provides more information on the boot process. It assumes an SCP is performing the CMN-600AE configuration.

1. The SCP boots, either from local memory or through CMN-600AE memory accesses targeting memory behind the HN-D:
 - All other masters are either held in reset or issue no requests to CMN-600AE until the boot programming is complete.
 - The HN-D is identified through straps on the RN SAM.
2. If necessary, the SCP discovers the system.
3. The SCP determines the wanted address map and corresponding SAM register values.
4. If necessary, the SCP remaps the configuration register space by completing the following steps:
 - a. It drains all requests in flight by waiting for their responses.
 - b. It issues a single 64-bit store to a PERIPBASE register behind the HN-D. This register would be in logic that is external to CMN-600AE and an update would cause the signal values on the CFGM_PERIPBASE input to change.
 - c. It waits for the response for that store.
5. If necessary, the SCP writes to the CMN-600AE configuration registers to program the SAM for all HN-Fs.
6. The SCP writes to the CMN-600AE configuration registers to program the SAM for all RNs including the one being used by the SCP.

————— **Note** —————

RN-F ESAM types cannot block transactions, therefore an external mechanism must block transactions.

After programming the SAM for all RNs, the SCP sets a bit that enables use of the programmed address map instead of the default address map. This bit indicates that the SAM setup is complete.

Once the preceding steps are complete, the SCP can make general accesses anywhere in the address space and other masters can begin issuing requests.

4.4.2 Runtime programming requirements

This section describes the requirements for programming during runtime.

The hardware for handling RN membership in the coherence domain or DVM domain has been shifted to the XP to which the RN is attached. A low-level four-phase handshake mechanism, **SYSCOREQ/SYSCOACK**, is added to allow quick and local entry to and exit from snoop and DVM domains. No

communication with central hardware resources is required. When a block is removed from the coherence or DVM domain, the XP acts as a protocol agent to give a generic response to any snoop or DVM messages.

For legacy devices that do not support the **SYSREQ/SYSACK** mechanism, direct configuration writes to the XP by software can trigger the same mechanism. For more information, see [2.27 RN entry to and exit from Snoop and DVM domains](#) on page 2-151.

4.5 CML programming

The system must be programmed to enable correct operation with CML.

This section contains the following subsections:

- [4.5.1 CML-related programmable registers on page 4-1834.](#)
- [4.5.2 Bring up a CML system on page 4-1835.](#)
- [4.5.3 Program CML system to enable CCIX communication on page 4-1837.](#)
- [4.5.4 Program CMN-600AE CML system at runtime on page 4-1842.](#)
- [4.5.5 Establish protocol link up between CXG and remote CCIX link on page 4-1842.](#)
- [4.5.6 Prerequisites to link down a CCIX protocol link between CXG and remote CCIX link on page 4-1843.](#)
- [4.5.7 CCIX entry and exit protocol links from coherency domains and DVM domains on page 4-1844.](#)

4.5.1 CML-related programmable registers

This section contains a list of CML programmable registers.

CXRA

- RA SAM address region registers (por_cxg_ra_sam_addr_region_reg<X>)
- LDID to RAID LUT registers:
 - por_cxg_ra_rnf_ldid_to RAID_reg<X>
 - por_cxg_ra_rnd_ldid_to RAID_reg<X>
 - por_cxg_ra_rni_ldid_to RAID_reg<X>
 - por_cxg_ra_rnf_ldid_to RAID_val
 - por_cxg_ra_rni_ldid_to RAID_val
 - por_cxg_ra_rnd_ldid_to RAID_val
- RAID or HAID to LinkID LUT registers:
 - por_cxg_ra_agentid_to linkid_reg<X>
 - por_cxg_ra_agentid_to linkid_val
- CCIX Protocol Link Control and Status registers:
 - por_cxg_ra_exptcl_link<X>_ctl
 - por_cxg_ra_exptcl_link<X>_status

CXHA

- HAID register (por_cxg_ha_id)
- RAID to LDID LUT registers:
 - por_cxg_ha_rnf RAID_to_ldid_reg<X>
 - por_cxg_ha_rnf RAID_to_ldid_val
- RAID or HAID to LinkID LUT registers:
 - por_cxg_ha_agentid_to linkid_reg<X>
 - por_cxg_ha_agentid_to linkid_val
- CCIX Protocol Link Control and Status registers:
 - por_cxg_ha_exptcl_link<X>_ctl
 - por_cxg_ha_exptcl_link<X>_status
- RN SAM

CXLA

- CCIX capabilities (por_cxla_ccix_prop_capabilities). This register is RO.
- CCIX Configured Properties (por_cxla_ccix_prop_configured)
- CXS Interface Properties Registers. These registers are RO:
 - por_cxla_tx_cxs_attr_capabilities
 - por_cxla_rx_cxs_attr_capabilities
- RAID or HAID to LinkID LUT registers:

- `por_cxla_agentid_to_linkid_reg<X>`
- `por_cxla_agentid_to_linkid_val`
- LinkID to PCIe Bus Number LUT register (`por_cxla_linkid_to_pcie_bus_num`)

HN-F

- LDID to CHI NodeID registers (`por_hnf_rn_phys_id<X>`)
- CCIX Port Aggregation Mask register (`por_hnf_cml_port_aggr_grp0_add_mask`)
- CCIX Port Aggregation Control register (`por_hnf_cml_port_aggr_grp0_reg`)

RN-F/RN-I/RN-D

- RN SAM
- CCIX Port Aggregation Mode Enable and Control registers:
 - `cml_port_aggr_grp0_reg`
 - `cml_port_aggr_mode_ctrl_reg`
- CCIX Port Aggregation Mask register (`cml_port_aggr_grp0_add_mask`)

4.5.2 Bring up a CML system

Use the following sequence to bring up a CML system.

Procedure

1. Discover and bring up the local CMN-600AE system.
For more information, see [Discover and bring up a local CMN-600AE system on page 4-1835](#).
2. Discover CCIX devices and CCIX systems.
For more information, see [Discover CCIX devices in CCIX system on page 4-1836](#).
3. Enumerate and configure CCIX devices.
For more information, see [Enumerate and configure CCIX devices on page 4-1836](#).

Next Steps

For information about the programming requirements that are necessary for communication between CCIX components, see [4.5.3 Program CML system to enable CCIX communication on page 4-1837](#).

Discover and bring up a local CMN-600AE system

Use this process to bring up a local CMN-600AE system during a full bring up of a CML system.

This procedure is the first step in the sequence to bring up a CMN-600AE CML system. For the full sequence, see [4.5.2 Bring up a CML system on page 4-1835](#).

Procedure

1. Complete the CMN-600AE discovery mechanism to discover node types, their corresponding locations (node IDs), and their logical IDs.
[2.4 Node ID mapping on page 2-51](#) and [2.5 Discovery on page 2-53](#) define the discovery mechanism. Node types that are relevant to CML-specific programming are RN-Fs, RN-Is, RN-Ds, HN-Fs, and CCIX gateway blocks (CXRA, CXHA, and CXLA).
2. Bring up the local system to allow normal local operations. To bring up all local non-CCIX components (HN-F, HN-D, HN-I, RN-I, SN-F, and XP):
 - a. Complete CMN-600AE boot time programming.
For more information, see [4.4.1 Boot-time programming sequence on page 4-1832](#).
 - b. Program RN SAM with the local address map.
For more information, see [2.20.1 Program the SAM on page 2-111](#).

Next Steps

For information about how to discover the CCIX devices in your CML configuration, see [Discover CCIX devices in CCIX system on page 4-1836](#).

Discover CCIX devices in CCIX system

CCIX system discovery involves going through the PCIe link activation and device enumeration mechanism. Use this process to discover CCIX devices in your CCIX system.

This procedure is the second step in the sequence to bring up a CMN-600AE CML system. For the full sequence, see [4.5.2 Bring up a CML system on page 4-1835](#).

Prerequisites

You must first discover and bring up your local CMN-600AE system. For more information, see [Discover and bring up a local CMN-600AE system on page 4-1835](#).

Procedure

- Follow the standard PCIe device enumeration steps to detect CCIX capable devices.
For more information, see *Cache Coherent Interconnect for Accelerators CCIX Base Specification Revision 1.0 Version 0.9*.

Next Steps

If one or more CCIX-capable devices are detected during PCIe device enumeration, then complete the following steps:

- See [Enumerate and configure CCIX devices on page 4-1836](#), which shows how to enumerate CCIX devices.
- Program the PCIe-RC to enable multiple *Virtual Channels* (VCs).

Enumerate and configure CCIX devices

Use this procedure to enumerate CCIX devices in your CML system and configure their CCIX properties during bring up.

This procedure is the last step in the sequence to bring up a CMN-600AE CML system. For the full sequence, see [4.5.2 Bring up a CML system on page 4-1835](#).

Prerequisites

Before enumerating CCIX devices, you must first complete the following steps:

- Discover and bring up your local CMN-600AE system. For more information, see [Discover and bring up a local CMN-600AE system on page 4-1835](#).
- Discover CCIX devices in your CCIX system. For more information, see [Discover CCIX devices in CCIX system on page 4-1836](#).

Procedure

- Discover all CCIX agents (RA and HA) at each CCIX device.
These agents must be uniquely identifiable. If any CCIX device contains CMN-600AE, follow the CMN-600AE discovery mechanism to discover node types, their corresponding locations (node IDs), and their logical IDs. The discovery mechanism is described in [2.4 Node ID mapping on page 2-51](#) and [2.5 Discovery on page 2-53](#).
- Discover the address map requirements of each CCIX device.
- Read the CCIX capabilities of each CCIX device.
 - Read the `por_cxla_ccix_prop_capabilities` register, which is present in each CXLA, to determine the CCIX capabilities of CMN-600AE.
- Determine the common properties and capabilities that all CCIX devices support and configure them in each CCIX device.
- Program the properties that are determined in the preceding step in the `por_cxla_ccix_prop_configured` register, which is present in each CMN-600AE CXLA.

Next Steps

To enable CCIX communication, follow the programming procedures that are described in [4.5.3 Program CML system to enable CCIX communication on page 4-1837](#).

4.5.3 Program CML system to enable CCIX communication

Use this procedure to enable CCIX communication between different CCIX entities. The steps can be completed in any order.

The terms *link*, *CCIX link*, and *CCIX protocol link* that are used in subsequent sections refer to CCIX logical link.

The CCIX logical link is defined in the *Cache Coherent Interconnect for Accelerators CCIX Base Specification Revision 1.0 Version 0.9*.

Prerequisites

Before enabling CCIX communication, you must first complete the bring up process. For more information, see [4.5.2 Bring up a CML system on page 4-1835](#).

Procedure

- Program IDs for local CXRAs and CXHAs. For more information, see [Assign IDs for local CXRAs and CXHAs on page 4-1837](#).
- Program remote CCIX agents:
 - Assign LinkIDs to remote CCIX protocol links. For more information, see [Assign LinkIDs to remote CCIX protocol links on page 4-1838](#).
 - Assign PCIe bus numbers for LinkIDs. For more information, see [Assign PCIe bus numbers for LinkIDs on page 4-1838](#).
 - Assign LDIDs to remote caching agents. For more information, see [Assign LDIDs to remote caching agents on page 4-1839](#).
 - Program RA SAMs. For more information, see [Program RA SAM on page 4-1839](#).
 - Program RN SAM in CXHAs. For more information, see [Program RN SAM in CXHA on page 4-1839](#).
 - Program CCIX protocol link control registers. For more information, see [Program CCIX protocol link control registers on page 4-1839](#).
 - Program CPA functionality in RN SAM, if using CPAGs. For more information, see [Program CPA functionality in RN SAM on page 4-1840](#).
 - Program CPA functionality in HN-F SAM, if using CPAGs. For more information, see [Program CPA functionality in HN-F SAM on page 4-1841](#).

Assign IDs for local CXRAs and CXHAs

Use this procedure to assign CCIX identifiers for local CXRAs and CXHAs and configure them in the relevant registers.

This task is part of the requirements to enable communication between local and remote CCIX agents. For the full list of requirements, see [4.5.3 Program CML system to enable CCIX communication on page 4-1837](#).

Procedure

- Assign *Requesting Agent IDs* (RAIDs) for local CXRAs.
 1. Program all the local RAIDs in the following registers for all CXRAs:
 - `por_cxg_ra_rnf_ldid_to_raid_reg<X>`
 - `por_cxg_ra_rni_ldid_to_raid_reg<X>`
 - `por_cxg_ra_rnd_ldid_to_raid_reg<X>`

This programming sets up the LDID to RAID LUT.

2. Set the corresponding valid bit in the following registers that are present in each CXRA:

- `por_cxg_ra_rnf_ldid_to_raid_val`
- `por_cxg_ra_rni_ldid_to_raid_val`
- `por_cxg_ra_rnd_ldid_to_raid_val`
- Program *Home Agent IDs* (HAIDs) for all local CXHAs into the `por_cxg_ha_id` registers that are present in each CXHA.

Because all CXHAs can communicate with all local HNs (HN-F, HN-I, and HN-D, they can have the same HAID. However, if uniqueness is between HAIDs is required for routing purposes, HAIDs do not have to be the same.

For compliance with the CCIX specification, a CXHA and CXRA with the same ID must reside behind the same CCIX protocol link. For more information, see *Cache Coherent Interconnect for Accelerators CCIX Base Specification Revision 1.0 Version 0.9*.

Assign LinkIDs to remote CCIX protocol links

Use this procedure to assign a unique LinkID to each remote CCIX protocol link with which a CXG can communicate.

This task is part of the requirements to enable communication between local and remote CCIX agents. For the full list of requirements, see [4.5.3 Program CML system to enable CCIX communication on page 4-1837](#).

Each CMN-600AE CXG contains a CXRA, CXHA, and CXLA node. Each CXG can communicate with up to three remote CCIX protocol links. These links are marked sequentially as links 0, 1, and 2. Remote links are identified using LinkIDs.

Remote CCIX agents (RAs or HAs) are identified using their RAID or HAID. Each remote RA or HA that a CXG can communicate with must be behind only one link.

It is only necessary for LinkIDs to be unique within a CXG. Each CXG has a respective LinkID space. Each remote link has its own CCIX protocol link control and status registers.

Procedure

1. Determine the LinkID of each remote agent, in other words the targets, of the CXG.
2. Program these LinkIDs in the following registers, which are present in the CXRA, CXHA, and CXLA:
 - `por_cxg_ra_agentid_to_linkid_reg<X>`
 - `por_cxg_ha_agentid_to_linkid_reg<X>`
 - `por_cxla_agentid_to_linkid_reg<X>`

This step sets up the AgentID (RAID or HAID) to LinkID LUT.

3. Set the respective valid bits in the following registers:
 - `por_cxg_ra_agentid_to_linkid_val`
 - `por_cxg_ha_agentid_to_linkid_val`
 - `por_cxla_agentid_to_linkid_val`

Assign PCIe bus numbers for LinkIDs

Use this procedure to set up the LinkID to PCIe bus number LUT in the CXLA. This programming is only required if the PCIe header is used to route a CCIX TLP.

This task is part of the requirements to enable communication between local and remote CCIX agents. For the full list of requirements, see [4.5.3 Program CML system to enable CCIX communication on page 4-1837](#).

Procedure

- Program the PCIe bus number for each remote link in the `por_cxla_linkid_to_pcie_bus_num` register, which is present in each CXLA.

Assign LDIDs to remote caching agents

Use this procedure to assign a unique LDID for each remote caching agent (RN-F) that can send requests to HNs (HN-F, HN-I, and HN-D).

This task is part of the requirements to enable communication between local and remote CCIX agents. For the full list of requirements, see [4.5.3 Program CML system to enable CCIX communication on page 4-1837](#).

HN-Fs use the LDID of remote caching agents for SF tracking. LDID assignment is not required for non-caching RAs, which are not required to be snooped.

Procedure

1. Program unique LDIDs for each remote caching agent in the `por_cxg_ha_rnf RAID_to_ldid_reg<X>` register that is present in each CXHA.
The LDID values for remote RN-Fs must be greater than those values that are used by the local RN-F nodes.
2. Set the `ldid<X>_rnf` bit to mark the remote agent as a caching agent.
3. Set the respective valid bit in the `por_cxg_ha_rnf RAID_to_ldid_val` register.
4. Program the NodeID of each CXHA in the `por_hnf_rn_phys_id<X>` register in the HN-F. Program each remote RN-F (caching agent) that is proxied through that CXHA.

Program RA SAM

Use this procedure to program the RA SAM, which generates the target ID for CCIX requests.

This task is part of the requirements to enable communication between local and remote CCIX agents. For the full list of requirements, see [4.5.3 Program CML system to enable CCIX communication on page 4-1837](#).

Procedure

- Program the following properties for each remote HA into the `por_cxg_ra_sam_addr_region_reg<X>` register that is present in each CXRA, and set the corresponding valid bit.
 - The base address of the address region and the corresponding size of the address region
 - The HAID that requests for the address range are mapped to

Program RN SAM in CXHA

Use this procedure to program the RN SAM in each CXHA.

You can program CXHA RN SAM as part of local system bring up.

Procedure

- Program the RN SAM present in each CXHA with the address and memory map of the local HNs.
For more information on RN SAM programming, see .

Program CCIX protocol link control registers

Use this procedure to set up CCIX protocol links for a CXG and configure the distribution of credits that the CXG uses.

There is a CCIX protocol link control register for each CCIX protocol link that a given CCIX gateway block (CXRA, CXHA, and CXLA) can communicate with.

Procedure

1. Program the `por_cxg_ra_cxprtcl_link<X>_ctl` and `por_cxg_ha_cxprtcl_link<X>_ctl` registers that are present in each CXRA and CXHA.
2. Set the `lnk<X>_link_en` bit for each CCIX protocol link that can be used in the future.
If this bit is not set, credits are not set aside for this link.
3. Program the `lnk<X>_num_{snpcrds, reqcrds, datcrds}` fields with the percentage of protocol credits that must be assigned or granted for a given link.

This step is optional. Default credits are equally assigned or granted to each enabled link as determined by the link enable bit (`lnk<X>_link_en`). For more information about credit distribution and the permitted configurations, see [CCIX protocol link credit distribution on page 4-1840](#).

You must ensure that the total percentage of credits that are allocated to all links does not exceed 100.

CCIX protocol link credit distribution

When setting up CCIX protocol links, you can specify the CCIX protocol link credit distribution. The distribution can be configured when programming the CCIX protocol link control registers.

The link enable bits (`lnk<X>_link_en`) of the `por_cxg_ra_cxprtcl_link<X>_ctl` and `por_cxg_ha_cxprtcl_link<X>_ctl` registers determine how many links are active for a CXG. By default, credits are equally assigned or granted to each enabled link. However, you can program these registers to configure the distribution of credits across multiple links.

The following table shows the number of links and allowed credit distribution percentages for that number of links.

Table 4-2605 Number of links and allowed credit distribution percentage

Number of links	Allowed credit distribution
1	100%
2	50% : 50%
	25% : 75%
3	50% : 25% : 25%
	33% : 33% : 33%

After distributing credits based on the programmed percentage across all the links available, any remaining credits are allocated to link0. For example, link0 is allocated 44 credits while link1 and link2 are allocated 42 credits each for the 128 credit, 33% credit distribution configuration.

For more information about programming the CCIX protocol link control registers, see [Program CCIX protocol link control registers on page 4-1839](#).

Program CPA functionality in RN SAM

There is a specific sequence of programming steps that must be followed to set up the RN SAM to distribute requests to CPAGs.

This task is part of the requirements to enable communication between local and remote CCIX agents. For the full list of requirements, see [4.5.3 Program CML system to enable CCIX communication on page 4-1837](#).

To enable CPA, you must program registers in both the RN SAM and HN-F SAM. For the programming sequence for the HN-F SAM registers, see [Program CPA functionality in HN-F SAM on page 4-1841](#).

There are certain rules and restrictions that apply to how CPA can be enabled in a CMN-600AE system. For more information, see [2.20.4 Support for CCIX Port Aggregation on page 2-117](#).

Note

The CPA group ID control bits for non-hashed region 7 are aligned differently from other regions. For more information, see the index of the region7_pag_grpid field in [cml_port_aggr_mode_ctrl_reg on page 4-846](#).

In a two-chip system with CPA enabled, the RN SAM CPA mask of Chip 0 and HN-F SAM CPA mask of Chip 1 must be programmed to match. Similarly, the RN SAM CPA mask of Chip 1 must match the HN-F SAM CPA mask of Chip 0.

Procedure

1. Set the region<n>_pag_en field of the cml_port_aggr_mode_ctrl_reg register to 1 for each non-hashed memory region that belongs to a remote chip and is required to use CPA.
This programming enables CPA mode for the non-hashed memory region and specifies the CPAG that requests must be hashed across.
2. Set each bit that must be used to hash requests across CXGs to 1 in the addr_mask field of the cml_port_aggr_grp<n>_addr_mask register. Set each bit that must be masked from the hash function to 0.

If CPA mode is enabled, RN SAM hashes PA bits [47:6] to distribute traffic between CXGs. The PA is compared against the addr_mask field of the cml_port_aggr_grp<n>_addr_mask register. Any PA bit that corresponds to a bit with a 0 value in the mask register is masked from hashing.

3. Program the characteristics of the CXGs for each CPAG by completing the following steps:
 - a. Program the number of CXGs in each CPAG by setting the num_cxg_pag0 field in the cml_port_aggr_grp<m> register.
 - b. Program the CHI node ID of each CXG by setting the pag_tgtid<n> fields in cml_port_aggr_grp_reg0 and cml_port_aggr_grp_reg1.

This programming is used by all regions that have CPA enabled.

4. Repeat the preceding steps for all RN SAMs in the chip.

Program CPA functionality in HN-F SAM

There is a specific sequence of programming steps that must be followed to set up the HN-F SAM to distribute snoop traffic to CPAGs.

This task is part of the requirements to enable communication between local and remote CCIX agents. For the full list of requirements, see [4.5.3 Program CML system to enable CCIX communication on page 4-1837](#).

To enable CPA, you must program registers in both the RN SAM and HN-F SAM. For the programming sequence for the RN SAM registers, see [Program CPA functionality in RN SAM on page 4-1840](#).

There are certain rules and restrictions that apply to how CPA can be enabled in a CMN-600AE system. For more information, see [2.20.4 Support for CCIX Port Aggregation on page 2-117](#).

In a two-chip system with CPA enabled, the RN SAM CPA mask of Chip 0 and HN-F SAM CPA mask of Chip 1 must be programmed to match. Similarly, the RN SAM CPA mask of Chip 1 must match the HN-F SAM CPA mask of Chip 0.

Procedure

1. Set the following fields in the por_hnf_rn_phys_id<n> registers for each valid LDID in the system:

nodeid_ra<ldid>

When using CPA, set this value to match the pag0_tgtid field of the por_hnf_cml_port_aggr_grp_reg<m> field of the corresponding CPAG.

remote_ra<ldid>

Set this value to 1 if the RN-F is a remote requestor.

cpa_en_ra<ldid>

Set this value to 1 if CPA is enabled for a remote RN-F.

Local RN-F LDIDs must have the remote_ra<ldid> and cpa_en_ra<ldid> bits set to 0 and the corresponding CPA group ID set to 0.

2. Set each bit that must be used to hash snoop traffic across CXGs to 1 in the addr_mask field of the por_hnf_cml_port_aggr_grp<m>_addr_mask register. Set each bit that must be masked from the hash function to 0.

If CPA mode is enabled, HN-F SAM hashes PA bits [47:6] to distribute snoop traffic between CXGs. The PA is compared against the addr_mask field of the cml_port_aggr_grp<m>_addr_mask register. Any PA bit that corresponds to a bit with a 0 value in the mask register is masked from hashing.

3. Program the characteristics of the CXGs for each CPAG by completing the following steps:
 - a. Program the number of CXGs in each CPAG by setting the num_cxg_pag0 field in the por_hnf_cml_port_aggr_grp<m>_reg register.
 - b. Program the CHI node ID of each CXG into the pag<k>_tgtid field of the same register.

This programming is used by all regions that have CPA enabled.

4. Repeat the preceding steps for all HN-F SAMs in the chip.

4.5.4 Program CMN-600AE CML system at runtime

Use this procedure to program a CMN-600AE CML system at runtime.

Procedure

1. Bring up CCIX protocol link.
For more information, see [4.5.5 Establish protocol link up between CXG and remote CCIX link on page 4-1842](#).
2. Add a CCIX protocol link in system coherency and DVM domains.
For more information, see [4.5.7 CCIX entry and exit protocol links from coherency domains and DVM domains on page 4-1844](#).
3. Program the remote address range and corresponding CXRA node ID for each remote memory region in RN SAM present in CMN-600AE RN-F, RN-I, and RN-D.

————— Note —————

If the software can guarantee that there is no traffic to the remote address range until CCIX-related initial programming is complete and CCIX protocol links are up, then this programming should be done when programming RN SAMs with local address map.

4.5.5 Establish protocol link up between CXG and remote CCIX link

Use the following procedure to link up a CXG with a remote CCIX link that the CXG can communicate with.

A CCIX protocol link can be established between each CXG in CMN-600AE and a corresponding remote CCIX link that the CXG can communicate with. The term *link* is used here to refer to a CCIX protocol link. Multiple CCIX links can be set up simultaneously by extending this sequence for each link.

CMN-600AE CXGs contain CXRA, CXHA, and CXLA nodes.

Procedure

1. Poll the lnk<X>_link_en bit in both por_cxg_ra_cxprtcl_link<X>_ctl and por_cxg_ha_cxprtcl_link<X>_ctl to ensure that the link is enabled.

If the link is enabled, then communication on the link can be established.

2. Ensure that the link is down and can accept a new link up request by polling the following bits:

- a. Poll the `lnk<X>_link_up` bits in the `por_cxg_ra_cxprtcl_link<X>_ctl` and `por_cxg_ha_cxprtcl_link<X>_ctl` registers to ensure that they are clear.
- b. Poll the `lnk<X>_link_down` bits in the `por_cxg_ra_cxprtcl_link<X>_status` and `por_cxg_ha_cxprtcl_link<X>_status` registers to ensure that they are set.
- c. Poll the `lnk<X>_link_ack` bits in the `por_cxg_ra_cxprtcl_link<X>_status` and `por_cxg_ha_cxprtcl_link<X>_status` registers to ensure that they are clear.

3. Set the `lnk<X>_link_req` bits in the `por_cxg_ra_cxprtcl_link<X>_ctl` and `por_cxg_ha_cxprtcl_link<X>_ctl` registers.

Setting this bit generates a request to link up, which in turn brings up the link.

4. Poll the following bits in the `por_cxg_ra_cxprtcl_link<X>_status` and `por_cxg_ha_cxprtcl_link<X>_status` registers to ensure that the link up request is accepted:

- `lnk<X>_link_ack`
- `lnk<X>_link_down`

The hardware acknowledges a link up request by setting the `lnk<X>_link_ack` bits and then clearing `lnk<X>_link_down` bits in `CXRA` and `CXHA`.

Results: Hardware acknowledgment of link up means that both sides are ready to receive and grant CCIX protocol credits.

5. Set the `lnk<X>_link_up` bit in the `por_cxg_ra_cxprtcl_link<X>_ctl` and `por_cxg_ha_cxprtcl_link<X>_ctl` registers to instruct both sides to start granting credits.

`Link<X>` is now up. Both sides can now exchange CCIX protocol credits and protocol messages.

4.5.6 Prerequisites to link down a CCIX protocol link between CXG and remote CCIX link

This section describes the prerequisites to deactivate a CCIX protocol link between a CMN-600AE CXG and a remote CCIX link.

You must follow a specific process to bring down a CCIX protocol link between each CMN-600AE CXG and the corresponding remote CCIX link that the CXG can communicate with. The term *link* is used here to refer to a CCIX protocol link. Multiple CCIX protocol links can be brought down at the same time by extending this sequence for each link.

CMN-600AE CXGs contain `CXRA`, `CXHA`, and `CXLA` nodes.

Prerequisites

Software must ensure that the following conditions are met before initiating a link down sequence:

- There are no outstanding transactions that require CCIX message transfers across the link for their completion. This condition includes GIC-D in SMP mode.
- The protocol agents on both sides of the link are configured to not initiate new transactions across the link. For CMN-600AE:
 1. To make sure the `lnk<X>_ot_cbkwr` bit in the `por_cxg_ra_cxprtcl_link<X>_status` register is clear, poll the `lnk<X>_ot_cbkwr` bit. This step ensures that there are no outstanding CopyBack requests targeting the link.
 2. Take the link out of system coherency and DVM domains. For more information, see [4.5.7 CCIX entry and exit protocol links from coherency domains and DVM domains on page 4-1844](#).

Procedure

1. To ensure the link is up and can accept a new link down request, poll these bits in the `por_cxg_ra_cxprtcl_link<X>_ctl` and `por_cxg_ha_cxprtcl_link<X>_ctl` registers:

- `lnk<X>_link_up`
- `lnk<X>_link_req`

These bits must be set before the link can accept a new link down request.

2. Clear the `lnk<X>_link_req` bits in the `por_cxg_ra_cxprtcl_link<X>_ctl` and `por_cxg_ha_cxprtcl_link<X>_ctl` registers to make a link down request.
3. Poll the `lnk<X>_link_ack` bit in the `por_cxg_ra_cxprtcl_link<X>_status` and `por_cxg_ha_cxprtcl_link<X>_status` registers to ensure that it is cleared.

The hardware acknowledges a link down request by clearing the `lnk<X>_link_ack`. After a link down request is accepted, each side must stop granting local CCIX protocol credits and start returning remote CCIX protocol credits.

4. Poll the `lnk<X>_link_down` bits in the `por_cxg_ra_cxprtcl_link<X>_status` and `por_cxg_ha_cxprtcl_link<X>_status` registers to ensure that each side has received all its protocol credits and is ready to go down.

The hardware sets the `lnk<X>_link_down` bits to convey that it is ready for the link to go down.

5. Clear the `lnk<X>_link_up` bits in the `por_cxg_ra_cxprtcl_link<X>_ctl` and `por_cxg_ha_cxprtcl_link<X>_ctl` registers to instruct both sides to deactivate the link.

Link<X> is now down. No protocol message or credit transfers must occur across the link.

4.5.7 CCIX entry and exit protocol links from coherency domains and DVM domains

CMN-600AE CXG blocks, which contain CXRA, CXHA, and CXLA nodes, can establish a CCIX protocol link with a remote CCIX link. Each CXG has software-programmable bits to allow the CCIX protocol links to enter and exit the system coherency domains and DVM domains.

The CXHA has 2 bits which facilitate snoop coherency domain entry and exit requests and acknowledgment:

- The `lnk<X>_snoopdomain_req` bit of the `por_cxg_ha_cxprtcl_link<X>_ctl` in each CXHA, controls snoop coherency domain requests for the link.
- The `lnk<X>_snoopdomain_ack` bit of the `por_cxg_ha_cxprtcl_link<X>_status` register, provides acknowledgment and status of the snoop coherency domain requests for the link.

The CXRA has 2 bits which facilitate DVM domain entry and exit requests and acknowledgment:

- The `lnk<X>_dvmdomain_req` bit in the `por_cxg_ra_cxprtcl_link<X>_ctl` register in each CXRA, controls DVM domain requests for the link.
- The `lnk<X>_dvmdomain_ack` bit in the `por_cxg_ra_cxprtcl_link<X>_status` register, provides acknowledgment and status of the DVM domain requests for the link.

For more information, see [2.27 RN entry to and exit from Snoop and DVM domains on page 2-151](#).

4.6 Support for RN-Fs compliant with CHI Issue A specification

Although CMN-600AE natively supports devices compliant with CHI Issue B specification, it also provides support for connecting RN-Fs based on CHI Issue A specification with some feature restrictions and the corresponding CMN-600AE programming requirements.

This section describes these feature restrictions.

This section contains the following subsections:

- [4.6.1 CHI Issue A device node ID mapping on page 4-1845.](#)
- [4.6.2 Stashing on page 4-1845.](#)
- [4.6.3 Direct Cache Transfer on page 4-1845.](#)
- [4.6.4 Data poison on page 4-1845.](#)
- [4.6.5 RN SAM programming on page 4-1846.](#)
- [4.6.6 System coherency entry and exit on page 4-1846.](#)

4.6.1 CHI Issue A device node ID mapping

In a CMN-600AE system, all devices are assigned a unique CHI Issue B node ID such as B_NID [n:0], where n = 6, 8, or 10 based on the system node ID width.

CHI Issue A devices, however, have a fixed 7-bit wide node ID such as A_NID[6:0]. For such devices, the A_NID is derived from the CHI Issue B node ID by shifting the LSBs and padding the MSBs with zeros as necessary as shown in the following tables.

Table 4-2606 Mapping CHI Issue A device node ID into CMN-600AE device node ID

Node ID width	CMN-600AE device node ID	Comments
7 bits	B_NID [6:0] = (A_NID[4:0], 2'b00)	A_NID[6:5] must be zero
9 bits	B_NID [8:0] = (A_NID[6:0], 2'b00)	-
11 bits	B_NID [10:0] = (2'b00, A_NID[6:0], 2'b00)	2 MSBs of B_NID are padded with zeros

Table 4-2607 Mapping CMN-600AE device node ID into CHI Issue A device node ID

Node ID width	CHI Issue A device node ID	Comments
7 bits	A_NID [6:0] = (2'b00, B_NID[6:2])	B_NID[1:0] are zeros and are discarded
9 bits	A_NID [6:0] = B_NID[8:2]	B_NID[1:0] bits are zeros and are discarded
11 bits	A_NID [6:0] = B_NID[8:2]	B_NID[10:9] and B_NID[1:0] bits are zeros and are discarded

4.6.2 Stashing

CHI Issue A RN-Fs do not support stashing.

All HN-F instances are configured to not send snoop stash requests to the CHI Issue A RN-F.

4.6.3 Direct Cache Transfer

CHI Issue A RN-Fs do not support *Direct Cache Transfer* (DCT).

All HN-F instances are configured to disable DCT in snoop requests to the CHI Issue A RN-F.

4.6.4 Data poison

CHI Issue A RN-Fs do not support data poisoning.

All HN-F instances are configured to report and log data poison errors detected on SLC data sent to the CHI Issue A RN-F.

Likewise, DMC must be configured to report and log data poison errors detected on read data.

4.6.5 RN SAM programming

CHI Issue A RN-Fs can be configured as ESAM.

When CHI Issue A RN-F is configured as ESAM, then the SAM in CMN-600AE must be programmed following the steps that [2.17 RN SAM on page 2-98](#) describes.

4.6.6 System coherency entry and exit

For system coherency entry or exit, either the hardware or software interface must be enabled.

[2.27 RN entry to and exit from Snoop and DVM domains on page 2-151](#) describes how the hardware or software interface must be enabled for system coherency entry or exit.

Chapter 5

SLC memory system

This chapter describes the SLC memory system.

It contains the following sections:

- [5.1 About the SLC memory system on page 5-1848.](#)
- [5.2 HN-F configurable options on page 5-1850.](#)
- [5.3 Basic operation on page 5-1851.](#)
- [5.4 Cache maintenance operations on page 5-1852.](#)
- [5.5 Cacheable and Non-cacheable exclusives on page 5-1853.](#)
- [5.6 TrustZone technology support on page 5-1854.](#)
- [5.7 Snoop connectivity and control on page 5-1855.](#)
- [5.8 QoS features on page 5-1856.](#)
- [5.9 Hardware-based cache flush engine on page 5-1858.](#)
- [5.10 DataSource handling on page 5-1860.](#)
- [5.11 Software configurable memory region locking on page 5-1861.](#)
- [5.12 Software-configurable On-Chip Memory on page 5-1863.](#)
- [5.13 Source-based SLC cache partitioning on page 5-1864.](#)
- [5.14 Way-based SLC cache partitioning on page 5-1865.](#)
- [5.15 Error reporting and software-configured error injection on page 5-1867.](#)

5.1 About the SLC memory system

The SLC memory system consists of the HN-F protocol nodes in CMN-600AE.

There is a configurable number of instances (1-64) of the HN-F. Each HN-F node or slice has the following features:

- 0KB, 128KB, 256KB, 512KB, 1MB, 2MB, 3MB, or 4MB of SLC Data RAM and Tag RAM.
- Combined *Point-of-Coherency* (PoC) and *Point-of-Serialization* (PoS).
- SF size of 512KB, 1MB, 2MB, 4MB, or 8MB.

Each HN-F in CMN-600AE is configured to manage a specific portion of the total address space. For each portion of the address, each HN-F:

- Can cache data in SLC
- Manages PoC and PoS functionality for ordering and coherency
- Tracks RN-F caching in the SF

Each HN-F in CMN-600AE is configured to do in-line ECC check and correct in the SLC and SF RAM access pipeline.

The SLC memory system has the following features:

- *Physically Indexed and Physically Tagged* (PIPT)
- Coherency granule is a fixed length of 64B. SLC line size is a fixed length of 64B.
- Both SLC and SF are 16-way set-associative. 12-way for 3MB SLC configurations.
- By default the SLC and SF use a pseudo-random victim selection policy. If there is an invalid way, it is not necessary to select a victim.
- Optionally, CMN-600AE supports an *enhanced LRU* (eLRU) cache replacement policy that can be enabled by setting a bit in the configuration register. eLRU is Dynamic Biased Replacement Policy. 2 bits per set/way are used to track and predict how soon a cache line is expected to be used again. This information is dynamically adjusted based on a few reference sets.
- SLC and SF arrays:
 - Supports one-cycle, two-cycle, or three-cycle non-pipelined tag array
 - Supports two-cycle or three-cycle non-pipelined data array
 - SLC Tag, SF Tag, and SLC Data arrays are single-ported, supporting one read or write access with no concurrency available
 - SLC Tag, SF Tag, and SLC Data arrays are ECC SECDED protected, with inline ECC checking and correction
- 32 or 64-entry address and data buffer, which is known as the *PoC Queue* (POCQ), to service:
 - All transactions from the CHI interface
 - SLC evictions to the memory controller
 - SF evictions and associated WriteBacks to the memory controller
- CMO propagation to SN-F or SBSX:
 - Conditional CMO propagation to the memory controller to support external DRAM caches
 - HN-F must be explicitly programmed using the `por_hnf_sam_sn_properties` register of the HN-F SAM to allow such propagation to each SN-F
- Supports QoS-based protocol flow control:
 - POCQ resources are allocated or rejected for protocol retry according to the QoS class
 - POCQ resources are watermarked for different QoS classes with user-configurable options
 - Starvation prevention for lower-priority QoS classes
 - QoS-based static grantee selection for CHI architecture credit return
- QoS priority-based request selection to the memory controller
- Supports allocation in the SLC from Snoop intervention. This feature enables data sharing through the SLC for multiple sharers.
- SLC state includes a caching LDID to detect dynamic read sharing
- Configurable 34b, 44b, or 48b *Physical Address* (PA) support
- PoC and PoS for all Snooperable and Non-snooperable, and Cacheable and Non-cacheable address space
- Supports ECC scrubbing for single-bit ECC errors on SF and SLC Tag RAMs

- Software-controlled error injection support to enable testing of software error handler routine
- Power management states to support:
 - Full powerdown of the SLC and SF. HN-F only mode when both SLC and SF are powered down
 - Half the SLC ways powered down
 - Retention for SLC and SF
 - SLC full powerdown with SF on, when in SF only mode
- Arm TrustZone® technology support in SLC and SF
- Software-configurable (one, two, four, eight, or 12 ways) Memory Region locking support in the SLC
- Software-configurable (one, two, four, eight, or 12 ways) OCM support in the SLC
 - OCM memory does not require any physical memory backing
- Supports CHI enhancements for:
 - *Direct Cache Transfer* (DCT)
 - *Direct Memory Transfer* (DMT). DMT not supported with 128b SBSX configurations.
 - Cache Stashing
 - Atomics support
 - Data Poison
 - Data Parity (Data Check)
 - Trace Tag
- Invisible SLC support:
 - CMN-600AE HN-F implements an invisible cache. All accesses (cacheable, non-cacheable, and Device types) are checked against the SLC and SF. The SLC cannot be cleaned and invalidated (flushed) by software using Arm architecture set/way operations. Software specific to CMN-600AE would instead be required to flush the SLC, as described in this TRM. Invisible SLC support eliminates the requirement to perform SLC flushes for software context switches from cacheable to non-cacheable.
- Supports up to two memory-region-based SN targets and one, three, or six SN-F address hashing

5.2 HN-F configurable options

The HN-F can be configured in several ways.

The HN-F has the following configurable parameters:

- SLC size of 0KB, 128KB, 256KB, 512KB, 1MB, 2MB, 3MB, or 4MB
- SF size of 512KB, 1MB, 2MB, 4MB, or 8MB
- 32, or 64 POCQ entries
- One-cycle, two-cycle, or three-cycle Tag RAM arrays. For a given configuration, both SLC Tag and SF Tag have the same latency.
- Two-cycle or three-cycle Data RAMs, data, and SF array RAMs. All Data RAMs have the same latency.

The HN-F has the following fixed parameters:

- HN-F CHI interface data-VC (DAT) width of 256 bits

5.3 Basic operation

CMN-600AE system level cache is a distributed, mostly exclusive last-level cache.

The SLC is optimized to eliminate redundancy for private data lines from the RN-F, and enables redundancy, or pseudo-inclusion, when a sharing pattern is detected between RN-F clusters.

CMN-600AE SLC also acts as DRAM cache for I/O coherent agents, that is, RN-Is, by enabling RN-Is to allocate or not allocate, based on the usage model.

The SF works with the SLC to track coherent lines that are present in the RN-F caches. The SF is fully inclusive of all the lines present in the RN-F caches. SF eviction invalidates the lines from RN-F caches to maintain this inclusion.

Normally, a particular coherent cache line is present only in the system level cache or SF except when the line is shared between RN-F clusters. In the shared case, the line can be present in both the SLC and the SF.

5.4 Cache maintenance operations

CMN-600AE uses several CHI *Cache Maintenance Operations* (CMOs).

The following operations are supported:

- CleanInvalid.
- CleanShared.
- MakeInvalid.
- CleanSharedPersist.

These operations always look up the SLC and the SF, and take the following actions:

- Clean and invalidate the line if present in the SLC.
- If the CMO is Snoopable, the HN-F sends a snoop to the RN-F post SF lookup if necessary.
- If the cache line is modified in the SLC or in the cache of the RN-Fs, the HN-F initiates a memory controller WriteBack if necessary.

Note

If the CMO is MakeInvalid, there is no WriteBack to the memory controller.

The SF does not track RN-F coherence while the HN-F is in NOSFSLC state. Therefore, the RN-F caches must be flushed before transitioning from NOSFSLC to SFONLY, HAM, or FAM states.

CMN-600AE supports propagation of CMO and PCMO requests for a given cache line to the memory controller. This feature ensures that the cache line has been written to the memory controller and any copies in the CMN-600AE system have been removed. Conditional CMO and PCMO propagation to the memory controller also supports external DRAM caches. This feature can be enabled or disabled in each HN-F's `por_hnf_sam_sn_properties` register bits corresponding to each SN-F.

5.5 Cacheable and Non-cacheable exclusives

The HN-F supports PoC monitor functionality for Cacheable and Snoopable exclusive operations from the RN-Fs.

The Cacheable and Snoopable exclusive transactions are:

- ReadShared.
- ReadClean.
- CleanUnique.
- ReadNotSharedDirty.

The HN-F also supports system monitor functionality for Non-cacheable exclusive support. For more information about exclusives, see the *Arm® AMBA® 5 CHI Architecture Specification*.

Note

Each HN-F in CMN-600AE can support tracking of up to 64 logical processors for exclusive operations. The system programmer must ensure that there are no more than 64 logical processors capable of concurrently sending exclusive operations.

5.6 TrustZone technology support

The HN-F supports TrustZone technology by treating the Non-secure bit from a request as part of the address.

TrustZone enables the HN-F to treat Secure and Non-secure as two different areas of the memory space:

- The NS bit is stored in the SLC and SF tags.
- Snoops also propagate the NS bit as part of the message.
- Any request to the memory controller also propagates the NS bit.

5.7 Snoop connectivity and control

Each HN-F can send three types of snoop.

The available types of snoop request are:

- Directed, to one RN-F.
- Multicast, to more than one but not all.
- Broadcast, to all RN-Fs.

5.8 QoS features

The HN-F protocol queue (POCQ) is a key shared system resource that communicates with the memory controller for external memory access.

The HN-F provides QoS capabilities in support of the following traffic classes:

- Real-time or pseudo-real-time traffic that requires a maximum bounded latency at potentially fixed bandwidth.
- Latency-sensitive traffic, traditionally from a processor device.

CMN-600AE uses QoS values to designate these traffic classes. Every request to the HN-F has a 4-bit QoS value that is associated with it, with a higher number indicating a higher priority. The four QoS classes are:

- Highest priority (known as HighHigh).
- High priority.
- Medium priority.
- Low priority.

This section contains the following subsections:

- [5.8.1 QoS decoding on page 5-1856](#).
- [5.8.2 QoS class and POCQ resource availability on page 5-1856](#).

5.8.1 QoS decoding

QoS decoding takes place inside the HN-F.

The QoS decoding is as follows:

- The CHI interface supports a 4-bit QoS value.
- The 4-bit QoS has 16 possible values. For the QoS ranges and class values in HN-F, refer to [Table 2-10 QoS classes in HN-F on page 2-71](#).
- QoS mapping is fixed, and is shown in the qos_band register.

The POCQ is logically partitioned to service different QoS class traffic. The HN-F also uses the priorities in the table to arbitrate for the following:

- Memory controller request selection in the POCQ control block.
- Data return selection logic, that is, a CompData to a requester.
- Protocol credits that are sent to an RN-F or RN-I following a protocol-layer retry.

5.8.2 QoS class and POCQ resource availability

The POCQ buffers are shared resources for all QoS classes.

The higher the QoS class, the higher the occupancy availability. For example, the *HighHigh* (HH) QoS class can use all the POCQ entries except for the dedicated SF pool.

The following figure shows the availability of POCQ resources for various QoS levels, using a particular QoS pool that is shared between multiple QoS classes.

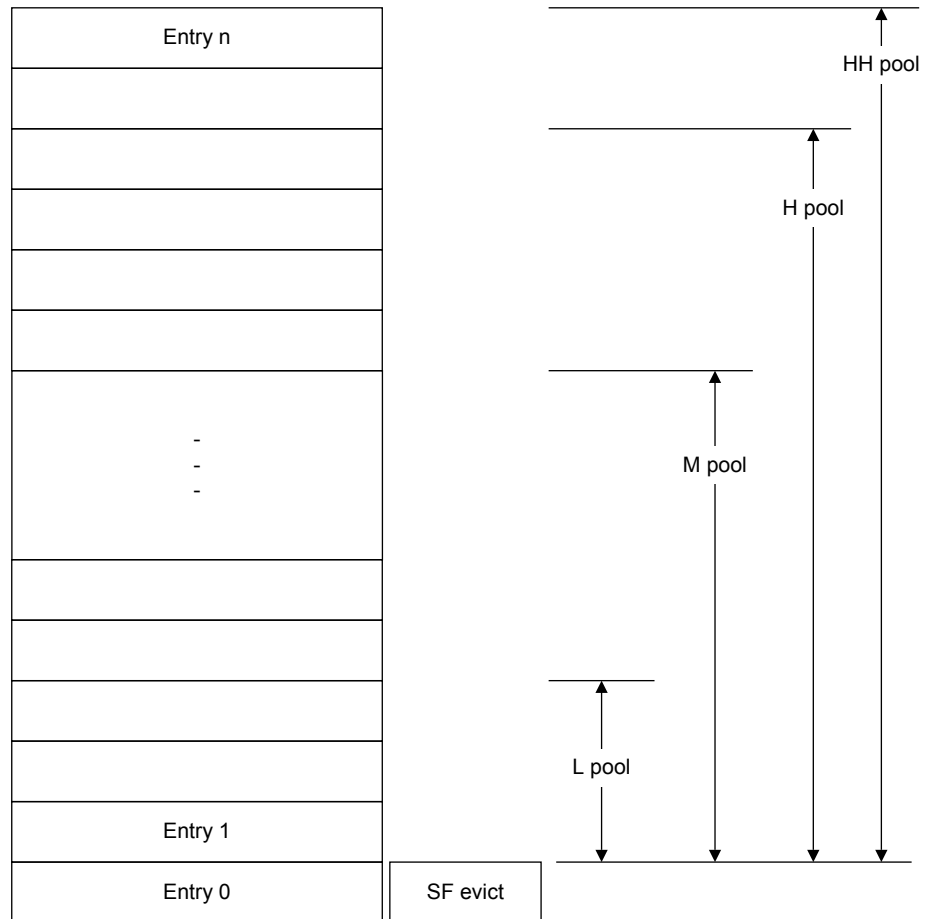


Figure 5-1 POCQ availability and QoS classes

The QoS pools are:

hh_pool	Available for HH class.
h_pool	Available for H class and HH class.
m_pool	Available for M class, H class, and HH class.
l_pool	Available for all classes.
seq	SF evictions only.

This scheme enables a higher-priority QoS class to have more POCQ resources for transaction processing, and prevents a lower-priority QoS from using all the POCQ. The level of POCQ availability decreases for the lower QoS classes.

QoS pool distribution of the POCQ is software-configurable using the qos_reservation register.

5.9 Hardware-based cache flush engine

The HN-F supports a hardware-based cache flush engine mechanism to flush the SF and SLC. The flush engine ensures that all cache lines in the lower and upper range are flushed from the CMN-600AE SF and SLC.

Various *Address Based Flush* (ABF) configuration registers per HN-F instance support the cache flush engine:

por_hnf_abf_lo_addr ABF lower range address.

por_hnf_abf_hi_addr ABF upper range address.

por_hnf_abf_pr ABF Policy Register. Triggers flush start, indicates flush operation type.

por_hnf_abf_sr ABF Status Register. Indicates flush completion and other status information.

The flush engine ensures that all cache lines in the lower and upper range are flushed from the CMN-600AE SF and SLC. When all cache lines within this range are flushed, a bit in the `por_hnf_abf_sr` register is set indicating that the flush engine has completed. If enabled, an interrupt (**INTREQPPU**) is then sent.

Note

Interrupt indication and complete bit in the `por_hnf_abf_sr` registers are set regardless of normal completion or abort condition. To determine if a flush request completed normally or aborted, check the error bits in the `por_hnf_abf_sr` register.

To complete the flush sequence, the HN-F carries out the following steps:

1. Flush CMN-600AE SFs. This operation flushes the lines in the lower-level caches. Lower-level write-backs go to memory and are not allocated to the CMN-600AE SLC.
2. Flush the CMN-600AE SLC.
3. On completion of the flush:
 - a. The HN-F sets the status bit in the `por_hnf_abf_sr` register when the flush is complete for that HN-F. If there are error conditions, they are also set in the `por_hnf_abf_sr` register. This register is cleared when next ABF request starts.
 - b. The HN-F sends a completion message to the global Power/Clock/Reset unit, and an optional **INTREQPPU** is asserted when all HN-F instances have completed the flush.

ABF requests are processed in parallel to other ongoing requests from RNs. If an ABF request and another ongoing request target the same address, then no ordering or coherency guarantee is provided. Power management transition requests have higher precedence than ABF requests. An ABF request is only supported when:

- The Power management state is in FAM, HAM, or SFONLY mode.
- The retention state is IDLE or RETENTION (not transitional).

While ABF is in progress, any update to the *Power Policy Register* (PWPR) causes the ABF state machine to abort and the Power management request proceeds.

By default, the flush engine writes back any modified data to memory before invalidating the cache line from internal caches. Two more configuration modes are provided for user flexibility. Therefore, the flush engine has the following three modes of operation:

CleanInvalid Write back and invalidate (default).

MakeInvalid In this mode, modified data is not written back to memory.

CleanShare In this mode, modified data is written back to memory but clean data remain in internal caches.

If *On Chip Memory* (OCM) is enabled and the address range overlaps with the ABF range, OCM behavior supersedes ABF. For SLC, this condition means that for CleanInvalid and CleanShare modes,

no action is taken. For MakeInvalid, there is no difference in behavior regardless of whether the address is in the OCM range or not. For SF flush, the behavior is the same between an OCM address match and not.

The following tables show a summary for SF and SLC caches for all three modes.

Table 5-1 SF cache operation

SF state	Hit		Miss	
ABF mode	SNP type to RN-F	Change SF state?	SNP to RN-F	Change SF state?
CleanInvalid	CleanInvalid	Yes	N/A	No
MakeInvalid	MakeInvalid	Yes	N/A	No
CleanShared	CleanShared	Yes	N/A	No

Table 5-2 SLC cache operation

SLC state		Modified		Exclusive or Shared		Invalid	
ABF mode	OCM match?	Evict line?	Change L3 state? (Final state)	Evict line?	Change L3 state? (Final state)	Evict line?	Change L3 state (Final state)
CleanInvalid	No	Yes	Yes (I)	No	Yes (I)	No	No (I)
	Yes	No	No (M)	No	No (ES)	No	No (I)
MakeInvalid	No	No	Yes (I)	No	Yes (I)	No	No (I)
	Yes	No	Yes (I)	No	Yes (I)	No	No (I)
CleanShared	No	Yes	Yes (E)	No	No (ES)	No	No (I)
	Yes	No	No (M)	No	No (ES)	No	No (I)

Note

The following assumptions are made:

- To ensure coherency and ordering is maintained, RNs should not access a cache line within the flush range while ABF is in progress.
- Address ranges and trigger must be programmed for each HN-F in the SCG.
- Do not change ABF-related configuration register bits when the abf_enable bit of the por_hnf_abf_pr register is set, until the abf_complete bit of the por_hnf_abf_sr register indicates flush is done.
- HN-F must be in one of the three operational modes (FAM, HAM, SFONLY). When flush starts, any update to the PWPR causes ABF to abort.
- SF must be enabled for the flush engine to operate. If SF is disabled, the flush engine aborts and indicates an error status in the por_hnf_abf_sr register.
- When ABF completes, check the por_hnf_abf_sr to ensure ABF completed without any errors. If ABF aborted for any reasons, then the por_hnf_abf_sr indicates that the flush was aborted.

5.10 DataSource handling

CMN-600AE populates the DataSource field of a CompData response to specify the source of the data.

DataSource information can be used:

- To determine the usefulness of a PrefetchTgt (Memory controller prefetch) transaction.
- To profile and debug software to evaluate and optimize data sharing patterns.

Table 5-3 DataSource encodings

Source of data	Message	Encoding
HN-I	Default (Non-memory source)	0b0000
RN-F	Peer processor cache within local cluster	0b0001
RN-F	Local cluster cache	0b0010
HN-F	<i>System Level Cache</i> (SLC)	0b0011
RN-F	Peer cluster cache	0b0100
Remote chip	Remote chip caches	0b0101
SN-F or SBSX	PrefetchTgt was useful.	0b0110
SN-F or SBSX	PrefetchTgt was not useful.	0b0111

CMN-600AE drives the DataSource value only when the source of the data is either HN-F or HN-I. For other data sources, CMN-600AE acts as a conduit.

The encoding that is used by CMN-600AE to indicate a data source is the same as the suggested value in the *Arm® AMBA® 5 CHI Architecture Specification*. Any deviation from the specified encodings might result in unexpected behavior.

5.11 Software configurable memory region locking

The HN-F supports variable size memory regions that can be locked in the system level cache with way reservation.

These variable size memory regions ensure that locked lines are not evicted from the SLC. Any access to those lines is guaranteed to hit in the SLC. The variable memory region is calculated as a factor of the total SLC size and number of ways that are locked. For example, consider an SLC that is built with 16 ways. In this case, way locking of 1, 2, 4, 8 or 12 yields 1/16, 2/16, 4/16, 8/16 or 12/16 of the SLC size respectively.

Software uses the following mechanism to program the HN-F configuration registers to enable region locking:

- The `hnf_slc_lock_ways` register specifies the total number of locked HN-F system level cache ways. This register can have a value of 1, 2, 4, 8, or 12.
- The following region base registers specify the base address of the region that is using locked ways:
 - `hnf_slc_lock_base0` register
 - `hnf_slc_lock_base1` register
 - `hnf_slc_lock_base2` register
 - `hnf_slc_lock_base3` register
- A combination of the total SLC size, `hnf_slc_lock_ways` register, and the `hnf_slc_lock_base0` register to `hnf_slc_lock_base3` register defines the following:
 - The total amount of cache that is locked, calculated as follows:

$$\frac{\text{Total SLC size} \times \text{Number of locked ways}}{16}$$

Figure 5-2 Total cache locked equation

- Ways are locked beginning with way 0 and then in ascending order
- The number of valid regions and exactly which regions are valid and included in the HN-F way allocation. This definition therefore indicates which of the `hnf_slc_lock_base0` to `hnf_slc_lock_base3` registers are valid and included in the HN-F way allocation.
- The exact location, size, and alignment requirement of each region
- The region alignment is identical to the region size, for example:
 - A 0.5MB region is aligned to any 0.5MB boundary
 - A 4MB region is aligned to any 4MB boundary
- The size and alignment requirement is enforced in hardware, to prevent any errors in software
- Regions can be disjointed or contiguous, to create a larger single region
- All valid regions use all locked ways. There is no application-level way segregation.
- The HN-F must be in the FAM power state. Memory Region Locking is not supported in other CMN-600AE power states

Note

The locked regions do not comprehend Secure as opposed to Non-secure memory regions, so if aliasing is performed between Secure and Non-secure regions, overlocking can occur.

The following tables specify various combinations of region size and the number of locked ways that software must program. Software can program these values using the `hnf_slc_lock_ways` register and the `hnf_slc_lock_base0` register to `hnf_slc_lock_base3` register.

Table 5-4 SLC Region Lock sizes

SLC size	Number of locked ways	Total locked region size	Locked ways	Number of ways per region	Region 0	Region 1	Region 2	Region 3
8MB	1	0.5MB	0	1	0.5MB	-	-	-
8MB	2	1MB	0-1	1, 1	0.5MB	0.5MB	-	-
8MB	4	2MB	0-3	1, 1, 1, 1	0.5MB	0.5MB	0.5MB	0.5MB
8MB	8	4MB	0-7	2, 2, 2, 2	1MB	1MB	1MB	1MB
8MB	12	6MB	0-11	2, 2, 4, 4	1MB	1MB	2MB	2MB

Table 5-5 Settings for hnf_slc_lock_baseX

Region size	Valid bits
0.5MB	[PA_WIDTH-1:19]
1MB	[PA_WIDTH-1:20]
2MB	[PA_WIDTH-1:21]
4MB	[PA_WIDTH-1:22]
8MB	[PA_WIDTH-1:23]

5.12 Software-configurable On-Chip Memory

The CMN-600AE HN-F supports software configurable *On-Chip Memory* (OCM) which allows for the creation of systems without physical DDR memory. It also allows a system to use SLC as scratchpad memory.

In OCM mode, the HN-F does not send requests to the SN-F. To enable OCM, the following requirements must be met:

- The HN-F must be in the FAM power state. Other CMN-600AE power states are not supported in OCM mode.
- All OCM ways must be same across all HN-Fs in a system cache group.
- OCM mode must be enabled before any non-config accesses are sent to HN-F.

In OCM mode, the following CMOs terminate in the SLC:

- CleanInvalid and CleanShared CMOs terminate in the SLC without invalidation or performing a WriteBack to the SN-F.
- MakeInvalid invalidates the cache line in SLC, and can be used to invalidate the OCM region.

OCM mode can be enabled by programming the `hnf_ocm_en` bit in the `por_hnf_cfg_ctl` register. If the `hnf_ocm_allways_en` bit is set to 1, then all transactions targeting the HN-Fs have OCM behavior. The OCM region must be contiguous and aligned to the total SLC size of the configuration when the `hnf_ocm_allways_en` is set to 1. If the `hnf_ocm_allways_en` bit is 0, region locking registers define the OCM regions. For more information about these region locking registers, see [5.11 Software configurable memory region locking on page 5-1861](#).

Note

Region locking registers do not explicitly control Secure and Non-secure memory regions. Therefore combined Secure and Non-secure memory regions should not exceed the total SLC size that is locked for OCM.

5.13 Source-based SLC cache partitioning

HN-F supports a feature to lock SLC ways for requesting nodes RN-F, RN-I, and RN-D.

This feature is an extension of the address-based way locking but the locked ways are based on the requestors instead of the programmed address. CMN-600AE supports programming of the number of ways that can be locked, RN devices for which these ways are locked and allocation policies in each HN-F. With this feature enabled, the locked SLC ways are only available to the programmed RNs for any new cache line allocations.

Source-based way locking feature can be enabled by programming the `por_hnf_rn_region_lock.rn_region_lock_en` bit to 1 in each HN-F instance. The requesting nodes, for which these ways are to be locked must also be explicitly enabled in the `por_hnf_rn*region_vec` registers. The requesting nodes are individually identified using the logical IDs. CMN-600AE has three RN types: RN-F, RN-I, and RN-D. Each requesting node type has different registers and is uniquely identified in a CMN-600AE system using logical IDs. The number of ways that are locked are programmed in the `por_hnf_slc_lock_ways.ways` field.

The region locking feature has two allocation modes:

- Allocating new cache lines for matching RNs only in the locked ways. By doing so, the matching RNs are restricted to allocate to the locked partition only. This mode can be enabled by setting `por_hnf_rn_region_lock.rn_pick_locked_ways_only` bit to 1.
- Allocating new cache lines for matching RNs to one of the locked or unlocked ways. This mode is the default behavior. In this mode, the locked ways are restricted only to the matching RNs but the unlocked ways are accessible by all the RNs.

Source-based SLC cache partitioning is supported only when *Enhanced LRU* (eLRU) mode is used.

Note

The HN-F must be in the FAM power state. Source-based cache partitioning is not supported in other CMN-600AE power states.

5.14 Way-based SLC cache partitioning

Each SLC cache instance can be partitioned into different regions. This partitioning allows each requesting node (RN-F, RN-I, RN-D) to allocate in one or more regions, each consisting of four consecutive ways.

Each region group has configuration registers that indicate which of the logical RN-F/RN-I/RN-D masters can allocate to the corresponding group of SLC ways. By default, all RNs can allocate all 16 ways, as the following tables show.

Table 5-6 Logical RN-F ID requesting node

Register	Address offset	Ways reserved	Default	Logical RN-F ID								
				63	62	61	60	----	3	2	1	0
por_hnf_slcway_partition0_rnf_vec	0xC48	[3:0]	{64' {1'b1}}									
por_hnf_slcway_partition1_rnf_vec	0xC50	[7:4]	{64' {1'b1}}									
por_hnf_slcway_partition2_rnf_vec	0xC58	[11:8]	{64' {1'b1}}									
por_hnf_slcway_partition3_rnf_vec	0xC60	[15:12]	{64' {1'b1}}									

Table 5-7 Logical RN-I ID requesting node

Register	Address offset	Ways reserved	Default	Logical RN-I ID								
				31	30	29	28	----	3	2	1	0
por_hnf_slcway_partition0_rni_vec	0xC68	[3:0]	{32' {1'b1}}									
por_hnf_slcway_partition1_rni_vec	0xC70	[7:4]	{32' {1'b1}}									
por_hnf_slcway_partition2_rni_vec	0xC78	[11:8]	{32' {1'b1}}									
por_hnf_slcway_partition3_rni_vec	0xC80	[15:12]	{32' {1'b1}}									

Table 5-8 Logical RN-D ID requesting node

Register	Address offset	Ways reserved	Default	Logical RN-D ID								
				31	30	29	28	----	3	2	1	0
por_hnf_slcway_partition0_rnd_vec	0xC88	[3:0]	{32' {1'b1}}									
por_hnf_slcway_partition1_rnd_vec	0xC90	[7:4]	{32' {1'b1}}									
por_hnf_slcway_partition2_rnd_vec	0xC98	[11:8]	{32' {1'b1}}									
por_hnf_slcway_partition3_rnd_vec	0xCA0	[15:12]	{32' {1'b1}}									

The registers in these tables are used to mask the ways that are available for an RN to allocate to at all times. A value of:

0b1 Indicates that the corresponding Logical RN ID can allocate in this region.

0b0 Indicates that the corresponding Logical RN ID cannot allocate to this region.

To enable the way reservation only to a subset of RNs, the mask in the preceding registers must be programmed as the following example shows:

Example 5-1 Reserve ways 0-3 for RN-F {0-3}

1. Write 64'h000000000000000F to `por_hnf_slcway_partition0_rnf_vec`. This operation enables logical RN-F IDs 0, 1, 2, and 3 to allocate to ways 0-3. All other RN-F IDs (4-63) cannot allocate to these ways.
2. Write 32'h0 to `por_hnf_slcway_partition0_rni_vec`. This operation disables all 32 RN-Is from allocating to ways 0-3.
3. Write 32'h0 to `por_hnf_slcway_partition0_rnd_vec`. This operation disables all 32 RN-Ds from allocating to ways 0-3.

Note

The following conditions apply to this example:

- This feature cannot be used if region-based locking, source-based locking, or OCM is enabled.
- The region registers can be changed at runtime.
- When the way partitioning scheme is not being used, the preceding registers must be returned to the default values.
- Each RN should be configured to allocate to at least one partition. Setting the bit for a given RN to 0 in all partition registers defaults it to allocating in any partition.

Way-based SLC cache partitioning is supported only when *Enhanced LRU* (eLRU) mode is used.

Note

The HN-F must be in the FAM power state. Cache partitioning is not supported in other CMN-600AE power states.

5.15 Error reporting and software-configured error injection

HN-F detects and reports several types of errors to the error block.

HN-F supports the following types of errors:

Correctable Errors

For example, single-bit ECC error detection and correction in the SLC Tag RAM, SF Tag RAM, and SLC Data RAM

Deferred Errors

For example, double-bit ECC error detection in SLC Tag RAM and double-bit ECC error detection in SLC Data RAM

Uncorrectable Errors

For example, double-bit ECC errors in the SLC Tag RAMs

Request MPU violations

If an HN-F receives a request that violates MPU permissions, it is logged in the HN-F RAS registers as an Uncorrectable Error with the request attributes (Source ID, opcode type, address).

For logging and reporting all error types, HN-F follows the procedures described in [2.14 Reliability, Availability, and Serviceability on page 2-80](#).

For information regarding the error source, see the ERRSRC field of [por_hnf_errmisc on page 4-409](#).

5.15.1 Software-configurable error injection

The HN-F supports software-configurable error injection and reporting. This feature enables testing of the software error handler routine for SLC double-bit ECC data errors.

The HN-F configuration register for a particular logical thread enables configurable error injection and reporting.

Any Cacheable read for which the HN-F is the source of the data is defined as a system cache hit. If error injection and reporting are enabled, any system cache hit drives the slave error from the system cache pipe and a fault interrupt through the RAS control block for that read. This functionality emulates a double-bit ECC error in the SLC data RAM but does not pollute the SLC data RAM through the fill path.

Note

This mechanism is designed to mimic SLC data ECC errors for SLC hits. SLC misses do not drive any errors or error interrupts. If enabled, this mechanism causes only an error to be logged and optionally an interrupt to be generated. Error injection on SLC hits does not alter the Resp*, Poison, or Data fields in the DAT flit that is returned to the RN.

For more information about configuring error injection, see [por_hnf_err_inj on page 4-411](#).

5.15.2 Software-configurable parity error injection

The HN-F supports software-configurable parity error injection.

This feature enables testing of the software error handler routine for parity error. For more information about enabling this feature, see [por_hnf_byte_par_err_inj on page 4-412](#). This register specifies the byte lane from 0-31 in which a parity error is introduced. The memory data is uncorrupted with such injection, but the Data Check field of the DAT flit that is returned to an RN is altered.

Chapter 6

Debug Trace and PMU

This chapter describes the *Debug Trace* (DT) and *Performance Monitoring Unit* (PMU) features.

It contains the following sections:

- [6.1 Debug trace system overview](#) on page 6-1869.
- [6.2 DT programming](#) on page 6-1882.
- [6.3 DT usage examples](#) on page 6-1884.
- [6.4 PMU system overview](#) on page 6-1889.
- [6.5 PMU system programming](#) on page 6-1890.
- [6.6 Secure debug support](#) on page 6-1892.

6.1 Debug trace system overview

CMN-600AE provides at-speed self-hosted *Debug Trace* (DT) capabilities.

The CMN-600AE DT capabilities include:

- Watchpoint-initiated and trace-tag-initiated transaction tracing
- Globally synchronized cycle counters for precise tracing
- CHI trace tag generation
- CoreSight™ ATB trace streaming
- Access to trace data through configuration registers
- Cross trigger support
- Secure debug support
- Event-based interrupts

The CMN-600AE DT system consists of a set of *Debug Trace Controllers* (DTCs) and *Debug Trace Monitors* (DTMs) distributed across the interconnect. DTCs are located inside HN-Ds and HN-Ts while DTMs are located inside XPs.

All DTCs, including the master DTC, have an ATB interface and the following signals:

- **DBGWATCHTRIGREQ**
- **DBGWATCHTRIGACK**
- **INTREQPMU**

The following signals are only present in the master DTC:

- **NIDEN**
- **SPNIDEN**
- **PMUSNAPSHOTREQ**
- **PMUSNAPSHOTACK**

Note

NIDEN and **SPNIDEN** are propagated from the master DTC to all DTMs. When asserted, they must remain asserted for at least 72 clock cycles. Likewise, when deasserted, they must remain deasserted for at least 72 clock cycles. This requirement ensures that all internal CMN-600AE components transit into their debug and trace states correctly.

The following figure shows an example DT system with two DTC domains.

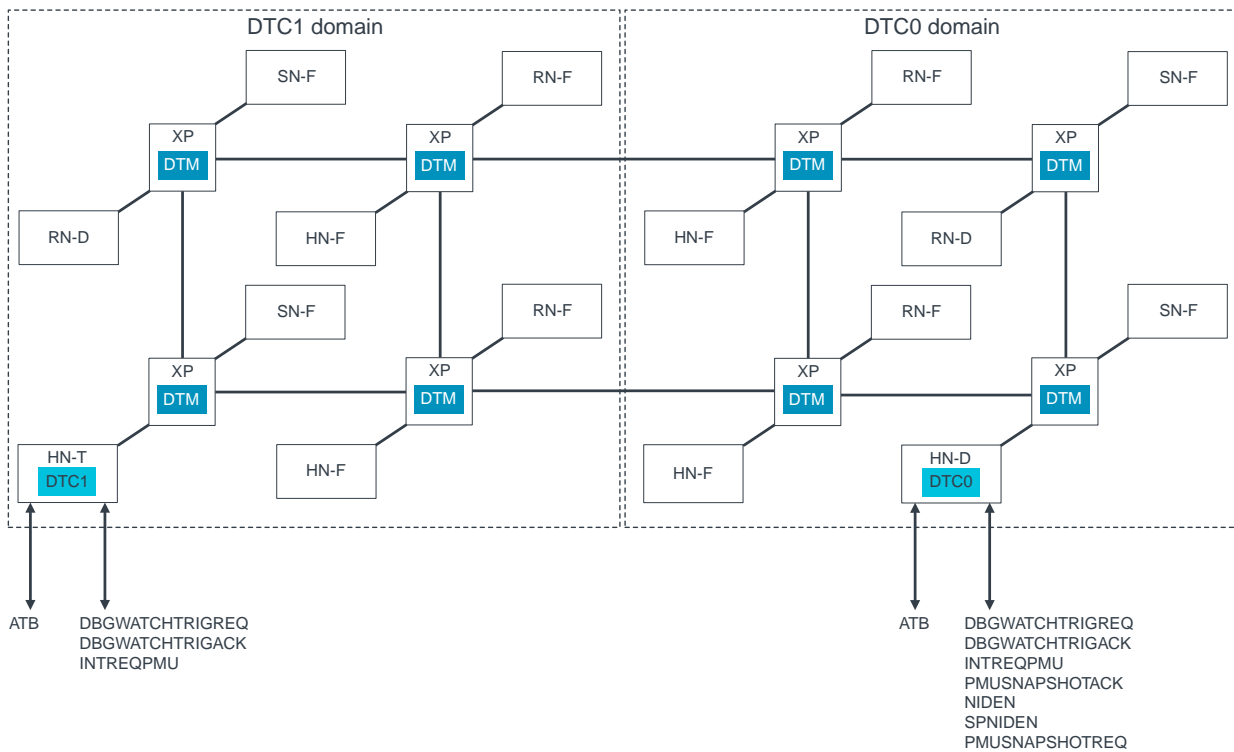


Figure 6-1 Example DT system with two DTC domains

Each DTC is associated with a set of DTMs to form an exclusive DTC domain. When enabled, DTMs within a DTC domain collect trace data and transmit it to the associated DTC. The number of HN-T nodes in the mesh determines the number of DTC domains.

In a DT system comprising multiple DTCs, the DTC that is located inside the HN-D is designated as the master DTC or DTC0. You assign DTMs to DTCs by configuring XP parameters in Socrates IP Tooling platform.

Each DTC must have a contiguous XP for that domain.

The DT system implements the following functions:

- Monitoring of CHI flits at XP device ports using four sets of *WatchPoints* (WPs) in each DTM
- Flit trace generation and storage at each DTM with control register access to trace packets
- Trace tag generation
- Debug trigger signaling and trace packet streaming over the ATB at each DTC
- Internal event-based cross trigger generation and broadcast to all DTMs
- Globally synchronized cycle counters

Note

The DT system must not be active in mission critical mode.

This section contains the following subsections:

- [6.1.1 DTM watchpoint on page 6-1870.](#)
- [6.1.2 DTM FIFO buffer on page 6-1874.](#)
- [6.1.3 Read mode on page 6-1877.](#)
- [6.1.4 DTC on page 6-1878.](#)
- [6.1.5 ATB packets on page 6-1878.](#)

6.1.1 DTM watchpoint

A DTM has four WPs that monitor flit uploads and downloads at XP device ports.

WPs monitor flits by matching on a subset of flit fields that you specify using a pair of val and mask registers. The following figure shows the WP comparator and the registers that control this functionality.

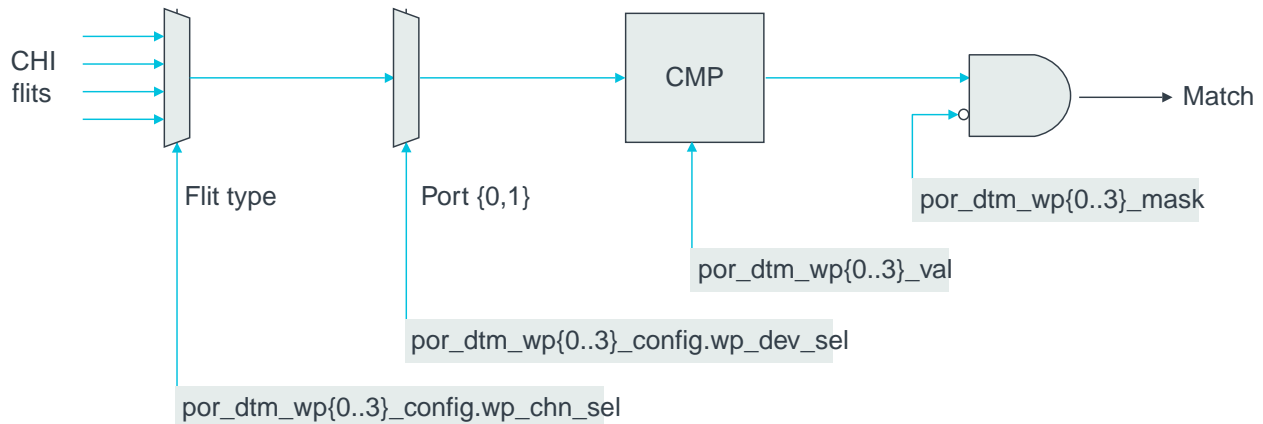


Figure 6-2 DTM WP comparator

A WP can be configured to monitor flits from one of two XP device ports and one of four CHI channels:

- REQ
- RSP
- SNP
- DAT

In addition, you can configure the WP to perform one or more of the following tasks on detecting a flit match:

- Set trace tag bit on the flit
- Generate flit trace
- Generate cross trigger to DTC
- Generate debug trigger to DTC
- Increment PMU counters

Note

You can combine two WPs within a group for complex matching. For example, you can combine WP0 and WP1, just as you can combine WP2 and WP3.

The four DTM WPs are assigned to flit uploads and downloads according to the following groups:

- WP0 and WP1 are assigned to flit uploads
- WP2 and WP3 are assigned to flit downloads

WP match value and mask register

The WP flit matching criterion is specified using a 64-bit match value register `dtm_wpN_val` and a 64-bit mask register `dtm_wpN_mask`, where $N=0, 1, 2, \text{ or } 3$. These registers permit matching up to 64 bits of the flit.

The value to be matched is written in the `dtm_wpN_val` register. Bits that must be masked off in the match comparison are specified in the `dtm_wpN_mask` register by writing a 1'b1 in the corresponding bit positions.

The CHI flits fields are divided into two match groups: a primary match group, and a secondary match group. The following tables specify the flit fields that belong to each of the groups for the different CHI channels. The RSP and DAT channels have only a primary match group while REQ and SNP channels have both primary and secondary match groups.

Flit matching from two different match groups requires two WPs to be combined. For example, if both the Opcode and Address fields of flits uploaded on the REQ channel are to be matched, then WP0 and WP1 must be combined with the Opcode match specified in WP0 and the Address match specified in WP1, or conversely. Furthermore, if both Opcode and Address fields of flits downloaded on the REQ channel must match, then WP2 and WP3 must be combined in a similar manner.

The following table contains the REQ channel width and bit ranges for the primary match group.

Table 6-1 REQ channel: primary match group

Field	Width	Bit range
SRCID and TGTID	11	[10:0]
STASHNID and RETURNNID	11	[21:11]
STASHNIDVALID/ENDIAN	1	[22]
RETURNTXNID/{3'b0, STASHLPIDVALID, STASHLPID[3:0]}	8	[30:23]
OPCODE	6	[36:31]
SIZE	3	[39:37]
NS	1	[40]
ALLOWRETRY	1	[41]
ORDER	2	[43:42]
PCRDTYPE	4	[47:44]
LPID	5	[52:48]
EXPCOMPACT	1	[53]
TRACETAG	1	[54]
RSVDC	8	[62:55]

The following table contains the REQ channel width and bit ranges for the secondary match group.

Table 6-2 REQ channel: secondary match group

Field	Width	Bit range
QOS	4	[3:0]
ADDR	48	[51:4]
LIKELYSHARED	1	[52]
MEMATTR	4	[56:53]
SNPATR	1	[57]
EXCL and SNOOPME	1	[58]
TRACETAG	1	[59]

The following table contains the RSP channel width and bit ranges for the primary match group.

Table 6-3 RSP channel: primary match group

Field	Width	Bit range
QOS	4	[3:0]
SRCID and TGTID	11	[14:4]
OPCODE	4	[18:15]

Table 6-3 RSP channel: primary match group (continued)

Field	Width	Bit range
RESPERR	2	[20:19]
RESP	3	[23:21]
FWDSTATE and STASH	3	[26:24]
DBID	8	[34:27]
PCRDTYPE	4	[38:35]
TRACETAG	1	[39]
DEVEVENT	2	[41:40]

The following table contains the SNP channel width and bit ranges for the primary match group.

Table 6-4 SNP channel: primary match group

Field	Width	Bit range
SRCID	11	[10:0]
FWDTXNID / {3'b0, STASHLPIDVALID, STASHLPID[3:0]} and VMIDEXT	8	[18:11]
OPCODE	5	[23:19]
NS	1	[24]
DONOTGOTOSD	1	[25]
RETTOSRC	1	[26]
TRACETAG	1	[27]
ADDR[35:0]	36	[63:28]

The following table contains the SNP channel width and bit ranges for the secondary match group.

Table 6-5 SNP channel: secondary match group

Field	Width	Bit range
SRCID	11	[10:0]
FWDTXNID {3'b0, STASHLPIDVALID, STASHLPID[3:0]} and VMIDEXT	8	[18:11]
OPCODE	5	[23:19]
NS	1	[24]
DONOTGOTOSD	1	[25]
RETTOSRC	1	[26]
TRACETAG	1	[27]
QOS	4	[31:28]
ADDR[44:13]	32	[63:32]

The following table contains the DAT channel width and bit ranges for the primary match group.

Table 6-6 DAT channel: primary match group

Field	Width	Bit range
QOS	4	[3:0]
SRC and TGTID	11	[14:4]
HOMENID	11	[25:15]
OPCODE	3	[28:26]
RESPERR	2	[30:29]
RESP	3	[33:31]
FWDSTATE and STASH	3	[36:34]
DBID	8	[44:37]
CCID	2	[46:45]
DATAID	2	[48:47]
TRACETAG	1	[49]
POISON	1	[50]
CHUNKV	2	[52:51]
DEVEVENT	2	[54:53]
RSVDC	8	[62:55]

Note

chunkv[1:0] denotes whether the upper or lower 128 bits of data are valid.

6.1.2 DTM FIFO buffer

Traces captured by the DTM are stored in a four-entry DTM FIFO buffer. Each entry is 144-bits wide.

Entries are allocated to all enabled WPs as required. Trace data from WPs are packed based on the trace data format and stored within each entry to efficiently use the limited buffer storage. Therefore, an entry might contain trace data from multiple flits captured at different times.

As each FIFO entry is filled, trace data from that entry is sent to the DTC for streaming out through the ATB interface.

Trace data format

CMN-600AE supports several trace data formats.

The 3-bit packet type encoding in the DTM WP configuration register, `por_dtm_wp{0..3}_config.wp_pkt_type`, specifies the trace data format. The following table provides the supported trace data formats and their packet type encodings.

Table 6-7 Trace data formats

Packet type	Trace data format	Size	Max traces per FIFO entry
000	TXNID[7:0]	8-bit	18
001	{2'b00, OPCODE[5:0], TXNID[7:0]}	16-bit	9
010	{TGTID[10:0], SRCID[10:0], OPCODE[5:0], TXNID[7:0]}	36-bit	4

Table 6-7 Trace data formats (continued)

Packet type	Trace data format	Size	Max traces per FIFO entry
011	Reserved	-	-
100	Control Flit (see the following tables for field descriptions)	REQ 141-bit RSP 61-bit SNP 96-bit DAT 83-bit	1
101	DATA[127:0]	128-bit	1
110	DATA[255:128]	128-bit	1
111	Reserved	-	-

Trace data is packed into a DTM FIFO buffer entry which means the higher-order bytes contain older trace data. For example, if the trace data format is set to TXNID (type 0) and three TXNIDs (trace data) are received in the order 0x01, followed by 0x02, followed by 0x03, then the trace FIFO entry is set to:

- 0000_0000_0000_0000_0000_0000_0001_0203

Note

Only use packet types 101 and 110 for trace data capture on the DAT channel. If these formats are used with other CHI channels, the trace data is set to zeros.

The following tables describe the control flit formats for various flit channels beginning with REQ control flit information.

Table 6-8 REQ control flit

Field	Width	Bit range
QOS	4	3:0
TGTID	11	14:4
SRCID	11	25:15
TXNID	8	33:26
STASHNID and RETURNNID	11	44:34
STASHNIDVALID and ENDIAN	1	45:45
RETURNCTXNID / {3'b0, STASHLPIDVALID, STASHLPID[3:0]}	8	53:46
OPCODE	6	59:54
SIZE	3	62:60
NS	1	63:63
LIKELYSHARED	1	64:64
ALLOWRETRY	1	65:65
ORDER	2	67:66
PCRDTYPE	4	71:68
MEMATTR	4	75:72
SNPATTR	1	76:76
LPID	5	81:77

Table 6-8 REQ control flit (continued)

Field	Width	Bit range
EXCL and SNOOPME	1	82:82
EXPCOMPACT	1	83:83
TRACETAG	1	84:84
ADDR	48	132:85
RSVDC	8	140:133
Total	141	-

The following table contains RSP control flit information.

Table 6-9 RSP control flit

Field	Width	Bit range
QOS	4	3:0
TGTID	11	14:4
SRCID	11	25:15
TXNID	8	33:26
OPCODE	4	37:34
RESPERR	2	39:38
RESP	3	42:40
FWDSTATE and STASH	3	45:43
DBID	8	53:46
PCRDTYPE	4	57:54
TRACETAG	1	58:58
DEVEVENT	2	60:59
Total	61	-

The following table contains SNP control flit information. See also [7.10 DEVEVENT](#) on page 7-1919 for more DEVEVENT information.

Table 6-10 SNP control flit

Field	Width	Bit range
QOS	4	3:0
SRCID	11	14:4
TXNID	8	22:15
FWDNID	11	33:23
FWDTXNID / {3'b0, STASHLPIDVALID, STASHLPID[3:0]} / VMIDEXT	8	41:34
OPCODE	5	46:42
NS	1	47:47
DONOTGOTOSD	1	48:48
RETTOSRC	1	49:49

Table 6-10 SNP control flit (continued)

Field	Width	Bit range
TRACETAG	1	50:50
ADDR	45	95:51
Total	96	-

The following table contains DAT control flit information.

Table 6-11 DAT control flit

Field	Width	Bit range
QOS	4	3:0
TGTID	11	14:4
SRCID	11	25:15
TXNID	8	33:26
HOMENID	11	44:34
OPCODE	3	47:45
RESPERR	2	49:48
RESP	3	52:50
FWDSTATE and STASH	3	55:53
DBID	8	63:56
CCID	2	65:64
DATAID	2	67:66
TRACETAG	1	68:68
POISON	4	72:69
CHUNKV	2	74:73
DEVEVENT	2	76:75
RSVDC	8	84:77
Total	85	-

See also [7.10 DEVEVENT](#) on page 7-1919 for more DEVEVENT information.

Note

chunkv[1:0] denotes whether the upper or lower 128 bits of data are valid.

6.1.3 Read mode

Read mode provides an alternate way to access trace data that is stored in the DTM trace FIFO buffer, through configuration register access.

Each entry in the FIFO buffer is mapped to three 64-bit configuration registers, `dtm_fifo_entry{0..3}_X`, where X = 0, 1, or 2.

To enable read mode, set the `trace_no_atb` bit in the `por_dtm_control` register. Setting this bit clears all FIFO entries and resets the `por_dtm_fifo_entry_ready` register.

In this mode, each FIFO entry is allocated to the corresponding WP. For example, `por_dtm_fifo_entry0_{0..2}` is allocated to WP0 and `por_dtm_fifo_entry1_{0..2}` is allocated to WP1.

The availability of WP trace data for each FIFO entry is reflected in the corresponding bit in the `por_dtm_fifo_entry_ready` register. When a FIFO entry is full, the corresponding status bit is set, indicating that the trace data is ready to be read. Subsequent writes into that FIFO entry are disabled until the status bit is cleared. A write of 1 clears the status bit and enables the corresponding FIFO entry to capture subsequent trace data.

6.1.4 DTC

DTCs control DTMs.

The main features of the DTC are:

- Trace packing, generation, and streaming through ATB interface
- Time stamping of traces
- Global synchronized cycle counters in all units (16-bit)
- ATB flush of DTM and DTC
- Watchpoint trigger event-based interrupt
- Eight sets of performance counters (32-bit) with shadow registers, which are paired with one or more DTM local counters
- PMU snapshot of DTM and DTC.
- PMU overflow interrupt.

6.1.5 ATB packets

Each DTC has an ATB interface and generates ATB packets to send downstream through this interface. There are different varieties of ATB packets which are used for different functions.

Each DTC aggregates flit trace data from the DTMs into the DTC trace FIFO, packetizes them, and sends them out on its ATB interface. The DTCs also send other control and debug packets through this interface. There are various packet formats that are used on the ATB interface, which are described in the following sections:

- [Trace data packet format on page 6-1878](#)
- [Alignment sync packet format on page 6-1879](#)
- [Time stamp packet format on page 6-1879](#)
- [Cycle counting packet format on page 6-1879](#)
- [Trace stream example on page 6-1880](#)

Trace data packet format

Trace data packet contains a 4B header and a payload of variable size.

The following figure shows the packet header.

VC		DEV	WP#		Type			Byte 3
Size					node ID[10:8]			
node ID[7:0]								
0	1		CC				lossy	Byte 0

Figure 6-3 Trace data packet header

The packet header contains the following fields:

VC	CHI channel		
	00	REQ	
	01	RSP	
	10	SNP	
	11	DAT	

DEV	Device port number (0 or 1)
WP#	Watchpoint number that captured the trace (0-3)
Type	Packet format type
Size	Payload size, which is specified as (number of bytes – 1)
NodeID	CHI node ID, shifted right by 3 bits reflecting the (X,Y) coordinates of the XP where the trace was captured
CC	Cycle counter. When set, this field indicates that the packet after the payload includes a 2B cycle count.

The following key points must be observed:

- For packet type 100, 101, and 110 the leading zeros in upper-order bytes of the trace data payload are compressed and not transmitted. The payload Size field in the trace packet header is adjusted accordingly. For example, trace data = 0000_0000_0000_0000_0000_0000_0001_0203 is sent as 01_0203, with Size = 2 (indicating 3B transferred).
- The WP field selection for match might be different from the type of payload that is generated from the matching. When WPs are combined, the lower watchpoint number is specified as the WP# in the trace packet header.
- Trace data is of variable length. The expected number of bytes, not including the header, is (Size + 1). With the cycle counter, another 2B are included at the end of the trace data.
- Whenever the previous packets cannot be transmitted in full, a lossy bit is asserted for the immediate next packet. A separate lossy bit is maintained for each of the watchpoints.

Alignment sync packet format

The alignment sync delimits trace start.

The alignment sync packet is 16B long and comprises 9B of zeros followed by 0x80.

The alignment sync packet is the first packet that is sent after tracing is enabled. Also, you can configure the DTC to send the alignment sync packet periodically by programming the por_dt_trace_control register.

Time stamp packet format

The time stamp packet carries the SoC timer information. The time stamp is used to align the sequence of trace events across the SoC.

The time stamp packet is sent opportunistically under the following circumstances when the DTC FIFO has enough space to accommodate the time stamp packet:

- After each alignment sync packet is sent
- When flush is complete
- Periodically based on the setting of the timestamp_period field of the por_dt_trace_control register and only when trace packets have been sent after the last time stamp packet

The following figure shows the time stamp packet format.



Figure 6-4 Time stamp packet

The time stamp packet contains the following fields:

- TS#** 3-bit encoding of the size of time stamp that is specified as (number of bytes – 1)
- CC** When set, indicates that a 2B cycle count is included in the packet after the payload

Cycle counting packet format

Trace packets include an OPTIONAL attached cycle counter.

Each watchpoint includes a configuration bit. The logical operator AND is used on the configuration bit and global cycle count enable. The following figure shows a typical cycle counting scenario.

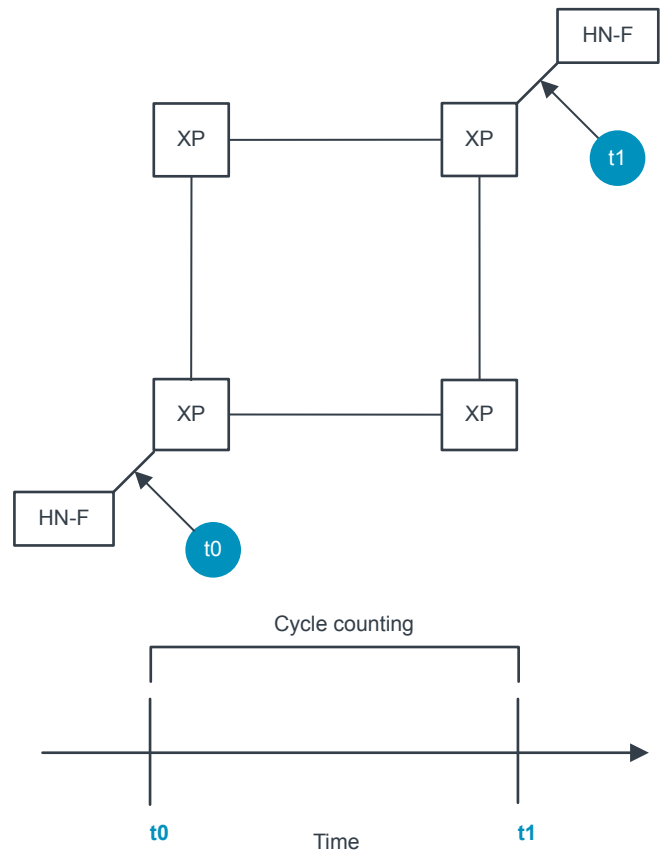


Figure 6-5 Cycle counting

The cycle counter payload is 2B and the CC bit in the trace packet header indicates the cycle counter payload. Cycle counters across the interconnect are turned on and off synchronously. This feature ensures that all of them have the same time stamp value.

Trace stream example

DTCs send out trace data on the ATB bus as a trace stream.

The following figure shows an example trace stream. It consists of:

- 4B trace packet header
- $\langle M \rangle$ B trace data
- 2B cycle count
- 1B time stamp header
- $\langle N \rangle$ B time stamp
- 2B cycle count

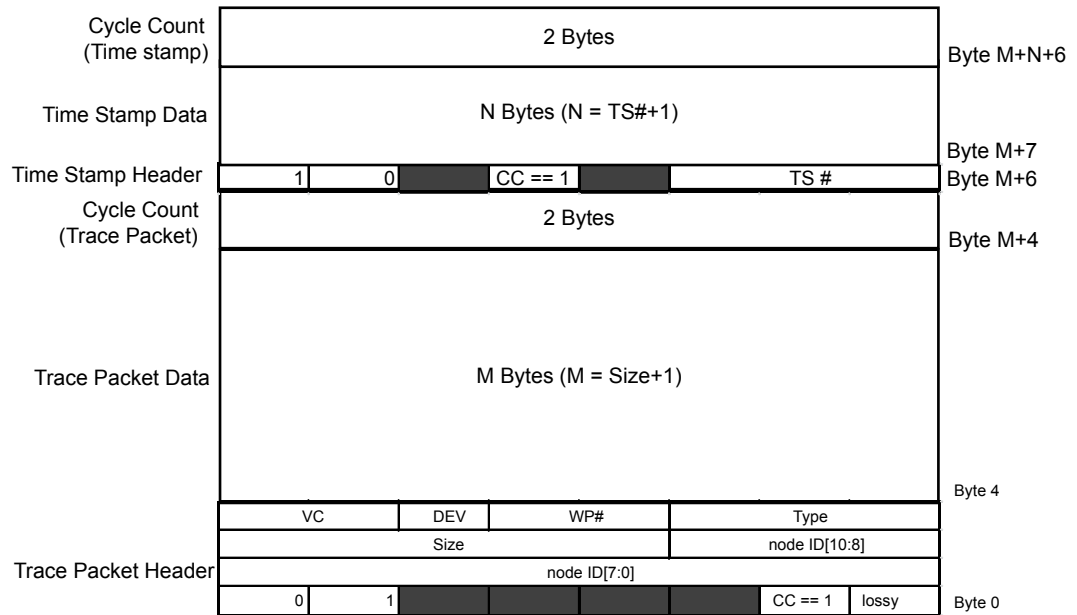


Figure 6-6 Trace stream

6.2 DT programming

You must follow several programming sequences to set up DTM watchpoints and DTC correctly.

This section contains the following subsections:

- [6.2.1 Program DTM watchpoint on page 6-1882.](#)
- [6.2.2 Program DTC on page 6-1882.](#)

6.2.1 Program DTM watchpoint

Use this procedure to program watchpoint N, where N=0..3.

Procedure

1. Program the intended watchpoint matching fields by writing the appropriate values into the `por_dtm_wpN_val` and `por_dtm_wpN_mask` registers.
For example, source ID, target ID and opcode are possible matching fields.
2. Program the WP settings in the following register fields to select the device port and flit CHI channel:
 - `wp_dev_sel` field of the `por_dtm_wpN_config` register
 - `wp_chn_sel` field of the `por_dtm_wpN_config` register
3. Program the `wp_grp` field of the `por_dtm_wpN_config` register to select primary or secondary watchpoint group.
4. Write 1 to the `wp_combine` field of the `por_dtm_wpN_config` register if two watchpoints must be combined.

————— Note —————

The `wp_combine` field is present in WP0 and WP2 only.

5. Program the following register fields if trace packets are to be generated from this watchpoint:
 - a. Program the `wp_pkt_type` field of the `por_dtm_wpN_config` register.
 - b. Write 1 to the `wp_pkt_gen` field of the `por_dtm_wpN_config` register.
6. Write 1 to the `wp_ctrig_en` field of the `por_dtm_wpN_config` register if a cross trigger must be set up from this watchpoint.
7. Program the `wp_dbgtrig_en` field of the `por_dtm_wpN_config` register if a debug watchpoint trigger must be set up from this watchpoint.
8. Set the `wp_cc_en` field of the `por_dtm_wpN_config` = 1 if a cycle count is required in the trace packet.
9. Write 1 to the `trace_tag_enable` field of the `por_dtm_control` register if a debug watchpoint trace tag must be generated.
10. Write 1 to the `dtm_enable` field of the `por_dtm_control` register to enable the WP.

6.2.2 Program DTC

Use this procedure to set up the CMN-600AE debug trace control functionality.

The **NIDEN** input signal must be asserted for any trace and PMU operations. Before trace and PMU operations can occur, you must first program and enable watchpoint functions in the DTMs.

The following registers and register bits are present only in the main DTC (DTC0):

- `por_dt_secure_access` register
- `dt_en` field of the `por_dt_dtc_ctl` register
- `wait_for_trigger` field of the `por_dt_dtc_ctl` register
- `cc_start` field of the `por_dt_dtc_ctl` register
- `pmu_en` field of the `por_dt_pmcr` register
- `por_dt_pmsrr` register

- ss_cfg_active field of the por_dt_pmssr register
- ss_pin_active field of the por_dt_pmssr register

Procedure

1. Write 1 to the dbgtrigger_en field of the por_dt_dtc_ctl register if DBGWATCHTRIG must be generated for DTM debug watchpoint trigger.
2. Write 1 to the atbtrigger_en field of the por_dt_dtc_ctl register if ATB trigger must be generated for DTM debug watchpoint trigger.
3. Write 1 to the cc_enable field of the por_dt_trace_control register to enable cycle count.
4. Write 0 to the dt_wait_for_trigger field of the por_dt_dtc_ctl register if no cross trigger is required.
5. Write 1 to the dt_en field of the por_dt_dtc_ctl register.

6.3 DT usage examples

To help you use the CMN-600AE DT features, we describe some example use cases of the DT system and example programming for those use cases.

For more information, see the following sections:

- [6.3.1 Flit tracing on page 6-1884](#)
- [6.3.2 Trace tag on page 6-1885](#)
- [6.3.3 Debug watch trigger events on page 6-1886](#)
- [6.3.4 Cross trigger on page 6-1887](#)

This section contains the following subsections:

- [6.3.1 Flit tracing on page 6-1884](#).
- [6.3.2 Trace tag on page 6-1885](#).
- [6.3.3 Debug watch trigger events on page 6-1886](#).
- [6.3.4 Cross trigger on page 6-1887](#).

6.3.1 Flit tracing

CMN-600AE can trace individual flits at device interfaces at each XP.

You can program DTM WPs to monitor flit uploads and downloads at each of the two XP device ports on any of the four CHI channels:

- REQ
- RSP
- SNP
- DAT

You can use a set of value and mask registers to define a subset of flit fields that are then used for matching at the WP.

On a match, WPs capture and store flit fields into trace buffers so that they can be used for debug. The generated trace can then be streamed out on the ATB interface or accessed using a control register interface.

For more information about the format of the value and mask registers, and the format of trace packets, see [WP match value and mask register on page 6-1871](#) and [Trace data format on page 6-1874](#).

Flit tracing example

CMN-600AE can trace individual flits at device interfaces at each XP.

For more information, refer to [6.2.1 Program DTM watchpoint on page 6-1882](#).

This section shows an example of setting up a simple trace of REQ flits. The example corresponds to a ReadShared transaction to address=X initiated by RNF2 and sending out the trace packets on the ATB bus.

To monitor REQ flits uploaded from RNF2, set up watchpoints (WPs) inside XP connected to RNF2. The Opcode and Address fields are mapped to the primary and secondary match registers respectively. Therefore, you must set up two WPs, one to monitor the Opcode and the other to monitor the Address.

To set up these WPs:

1. Program WP0 (upload WP) to monitor REQ.Opcode:
 - a. Set dtm_wp0_val/mask registers to match on Opcode=ReadShared
 - b. Set dtm_wp0_config to:
 - a. Select upload device port, wp_dev_sel=RNF2_port
 - b. Select flit channel, wp_chn_sel=REQ
 - c. Match format group to primary for Opcode match wp_grp= 0

- d. Set combined mode to gang-up WP0 and WP1, `wp_combine = 1`
 - e. Enable REQ flit trace packet generation, set `wp_pkt_type` and `wp_pkt_gen = 1`
2. Program WP1, upload WP, to monitor REQ.Address as follows:
 - a. Set `dtm_wp1_val/mask` registers to match on Address = X
 - b. Set `dtm_wp1_config` to:
 - a. Select upload device port, `wp_dev_sel = RNF2_port`
 - b. Select Flit channel, `wp_chn_sel = REQ`
 - c. Match format group to secondary for Address match, `wp_grp = 1`

Note

In combined mode, use WP0 config settings to enable trace generation.

3. To enable trace generation in the WP, set `dtm_control.trace_tag_enable = 1`
4. Set `dtm_control.dtm_enable = 1`
5. Program `por_dt_traceid.traceid` according to the *Arm® CoreSight™ Architecture Specification*. The supported range of values is 0x01-0x6F
6. Program `por_dt_dtc_ctl` to enable tracing, `dt_en = 1`

6.3.2 Trace tag

CMN-600AE can generate trace tags at the device interfaces and propagate them to destination devices.

This feature enables a set of flits corresponding to a specific transaction or set of transactions that match a specific criterion to be tagged for tracing.

For example, using the trace tag mechanism, flits from all four CHI channels can be monitored:

- REQ
- RSP
- SNP
- DAT

An example of a monitored transaction is a memory read transaction to a specific address, which is then tagged for tracing.

Trace tag generation

A trace tag is generated either internally by an XP or externally by an RN-F or SN-F device. The generated trace tag is reflected in the TRACETAG field of the uploaded flit.

Inside the XP, DTM WPs generate the trace tag by matching on flits uploaded at the corresponding XP device port. The DTM WPs can be programmed to match on a flit on any of the four CHI channels: REQ, RSP, DAT, and SNP.

The WP generates a trace tag when there is a match and the `trace_tag_enable` field of the `por_dtm_control` register is set to 1.

You can program DTM WPs to match on a flit on any CHI channel and on any device port. However, for debug, it is most useful to program WPs to match on REQ flits uploaded at the RN and HN-F device ports. We recommend this programming because REQ flits are the starting flits that originate new transactions. When tagged, subsequent RSP, SNP, and DAT flits that relate to the same transaction carry the trace tag.

If the following conditions are all true, the XP does not generate the trace tag:

- Flit transfer takes place from one device port to the other device port, within the same XP.
- The flit destination device is not an HN.
- The flit transfer to its destination occurs one cycle after the XP receives it.

Trace tag propagation

All CMN-600AE devices forward on the trace tag, when asserted, from a received flit corresponding to a transaction to all subsequent flits associated with that transaction.

The HN-F also propagates the trace tag from the source transaction to spawned transactions such as SLC evictions and SF back invalidations.

Using the logical operator OR, the trace tag that is generated inside the XP is combined with the TRACETAG field of the received flit. The resultant value is then sent in the TRACETAG field of the flit transmitted to the destination device.

Trace tag example programming

This example programming outlines a trace tag scenario-based trace generation with synchronized cycle counts.

For more information about watchpoint programming, see [6.2.1 Program DTM watchpoint on page 6-1882](#).

This example programming sets up a simple trace of REQ flits. The example corresponds to a ReadShared transaction to address = X. RN-F 2 initiates the transaction in the mesh and the WP sends trace packets out on the ATB bus.

To monitor REQ flits uploaded from RN-F 2, set up WPs inside the XP that RN-F 2 is connected to. For REQ flits, the Opcode and Address fields are mapped to the primary and secondary match registers respectively. Therefore, you must set up two WPs, one to monitor the Opcode and the other to monitor the Address.

To set up these WPs:

1. Program WP0, upload WP to monitor REQ.Opcodex:
 - a. Set `por_dtm_wp0_val` and `por_dtm_wp0_mask` registers to match on Opcode = ReadShared
 - b. Set `por_dtm_wp0_config` to:
 - a. Select upload device port, `wp_dev_sel` = RN-F 2 port
 - b. Select flit channel, `wp_chn_sel` = REQ
 - c. Match format group to primary for Opcode match, `wp_grp` = 0
 - d. Set combined mode to gang-up WP0 and WP1, `wp_combine` = 1
 - e. Enable REQ flit trace packet generation, set `wp_pkt_type` and `wp_pkt_gen` = 1
2. Program WP1, upload WP, to monitor REQ.Address:
 - a. Set `por_dtm_wp1_val` and `por_dtm_wp1_mask` registers to match on Address = X
 - b. Set `por_dtm_wp1_config` to:
 - a. Select upload device port, `wp_dev_sel` = RN-F 2 port
 - b. Select flit channel, `wp_chn_sel` = REQ
 - c. Match format group to secondary for Address match, `wp_grp` = 1

————— Note —————

In combined mode, use WP0 config settings to enable trace generation.

3. To enable trace tag generation in the WP, set `dtm_control.trace_tag_enable` = 1
4. Set `dtm_control.dtm_enable` = 1
5. Program `por_dt_traceid.traceid` according to the *Arm® CoreSight™ Architecture Specification*. The supported range of values is 0x01-0x6F.
6. Program `por_dt_dtc_ctl` to enable tracing, `dt_en` = 1

6.3.3 Debug watch trigger events

DTM WPs can be programmed to match on specific flits and generate a debug watch trigger event to the DTC.

You can program the DTC to signal the debug watch trigger event in one or both of the following ways:

- Signal a debug watch trigger interrupt on the **DBGWATCHTRIGREQ/DBGWATCHTRIGACK** interface

Note

This interface is based on a four-phase handshake protocol.

- Signal an ATB trace trigger with ATID 0x7D on the ATB interface

In a system with multiple DTCs, each DTC has its own ATB interface on which it signals ATB trace triggers from DTMs within its DTC domain. Multiple DTCs also have their own

DBGWATCHTRIGREQ / DBGWATCHTRIGACK interfaces on which they signal debug watch trace interrupts.

6.3.4 Cross trigger

CMN-600AE can trigger DTMs based on specific events occurring elsewhere in the system.

By default, DTMs start monitoring and tracing flits without waiting for another event. The cross trigger feature allows flit monitoring and tracing to be delayed until after the events of interest are observed in the system.

The cross trigger event is set up in two steps:

1. Set up DTM WPs to monitor flits and generate traces
2. Other DTM WPs (in the same XP or different XPs) are set up to generate a cross trigger on specific events to the DTC. The DTC is programmed to trigger the DTMs in step 1.

Cross trigger example programming

CMN-600AE can trigger DTMs based on specific events occurring elsewhere in the system.

For more information, refer to [6.2.1 Program DTM watchpoint on page 6-1882](#).

This example uses trace DAT flits corresponding to a ReadShared transaction to address-X that originated at RN-F 2. There have also been 10 WriteNoSnoops uploaded to the HN-D.

1. Set WP at RN-F 2 upload port to monitor REQ flits (refer to step 1 in [6.3.4 Cross trigger on page 6-1887](#)).
2. Set WP or WPs at all DAT download ports to generate DAT flit traces (refer to step 2 in [6.3.4 Cross trigger on page 6-1887](#)).
3. Set up WP at HN-D upload port to monitor WriteNoSnoop flits.
 - a. Program WP0 (upload WP) to monitor and enable cross trigger REQ.Opcode:
 - a. Set `por_dtm_wp0_val` and `por_dtm_wp0_mask` registers to match on Opcode = WriteNoSnoop.
 - b. Set `por_dtm_wp0_config` to:
 - a. Select upload device port (`wp_dev_sel` = HN-D port).
 - b. Flit channel (`wp_chn_sel` = REQ).
 - c. Match format group to primary for Opcode match (`wp_grp` = 0).
 - d. Enable cross trigger (`wp_ctrig_en` = 1).
 - b. Enable WP.
 - Set the `dtm_enable` field of the `por_dtm_control` register = 1.
4. Set up counter in DTC to count ten trigger events from step 3.
 - Program `por_dt_dtc_ctl` as follows:
 1. Set cross trigger count (`cross_trigger_count` = 9).
 2. Enable waiting for HN-D WP trigger event (`dt_wait_for_trigger` = 1).
 3. Enable DTC (`dt_en` = 1).

Sample profile

CMN-600AE supports the Armv8.2 sample extension.

WPs can be programmed to monitor channel, opcode, and related PM items. The sampling interval counter register, `por_dtm_pmsicr`, counts down with each match. When the counter reaches zero, the trace tag of the next matched transaction is asserted. At the same time, the counter is reloaded with the

programmed value from the sampling interval reload register, `por_dtm_pmsirr`, and the next count down cycle begins.

There is only one set of `por_dtm_pmsicr` and `por_dtm_pmsirr` registers per XP, as only one outstanding transaction is expected. `Por_dtm_pmsicr` is 24 bits, and the lower 8 bits of `por_dtm_pmsirr` are zero.

In general, Secure transactions are allowed to be tagged and traced with the `secure_debug_disable` field of the `por_dt_secure_access` register. When this bit is set, Secure transactions are not traced.

6.4 PMU system overview

CMN-600AE includes *Performance Monitoring Unit* (PMU) capabilities.

The PMU offers the following features:

- Local and global performance counters with shadow registers
- PMU snapshot across all internal CMN-600AE devices

The PMU consists of local performance counters in the DTMs and global performance counters in the DTCs. The following figure shows this structure of local and global performance counters.

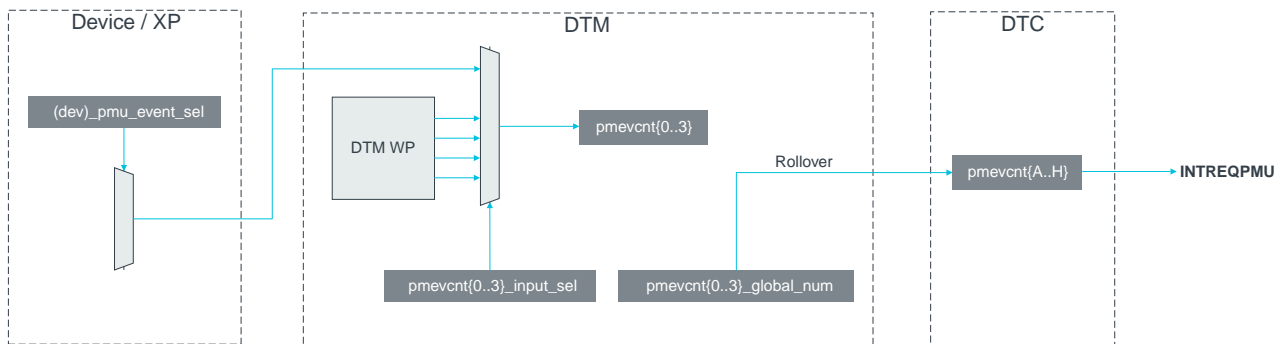


Figure 6-7 PMU local and global performance counters

The PMU system performs the following tasks:

- Selects PMU event from XP, the local watchpoint, and the devices on XP device ports
- Operates four local PMU counters ($4 \times 16b$)
- Operates eight global PMU counters ($8 \times 32b$) associated with the local counters
- Snapshot
- Overflow interrupt from global PMU counters

The PMU counter value can be copied over into the shadow registers when there is either:

- A request of snapshot through input pin **PMUSNAPSHOTREQ**
- A write into the `ss_req` field of the `por_dt_pmsrr` register within the DTC

On receiving a snapshot request, a DTC sends a snapshot request to all DTMs. Multiple snapshot requests are collapsed into a single request. On receiving PMU snapshot packets from all DTMs, rollover information is updated at the global counters, and the counter value is copied to the shadow registers.

6.5 PMU system programming

You must follow specific programming sequences to set up the PMU, PMU snapshot, and PMU interrupt functionality correctly.

This section contains the following subsections:

- [6.5.1 Set up PMU counters on page 6-1890.](#)
- [6.5.2 Program PMU snapshot on page 6-1890.](#)
- [6.5.3 Program PMU counter overflow interrupt on page 6-1891.](#)

6.5.1 Set up PMU counters

Use this procedure to set up the PMU counters correctly.

Procedure

1. Ensure that the **NIDEN** input is asserted for any trace and PMU operations.
2. Program (dev)_pmu_event_sel register in the devices or XP.
3. Program the pmevnt{0..3}_input_sel fields of the por_dtm_pmu_config register to select PMU event counter inputs.
The input can be from one of the following:
 - A watchpoint.
 - Selected events from the devices or XP, depending on step 2.
4. Program the following por_dtm_pmu_config register fields to select the paired top global PMU counters:
 - pmevnt_paired
 - pmevnt{0..3}_global_num
5. Program the pmevnt{01, 23}_combined fields of the por_dtm_pmu_config for any combined local PMU counters.
6. Write 1 to the pmu_en field of the por_dtm_pmu_config register.

————— **Note** —————

To activate CXLA PMU function, program the en_cxla_pmucmd_prop field of the associated por_cxg_ra_cfg_ctl register to 1.

7. Write 1 to the dtm_enable field of the por_dtm_control register.
8. Program the cntcfg field of the por_dt_pmcr register to pair the 32-bit global counters to make a 64-bit counter.
9. Write 1 to the dt_en field of the por_dt_dtc_ctl register.
10. Write 1 to the ovfl_intr_en field of the por_dt_pmcr register to enable interrupts on **INTREQPMU** on any global counter overflow.
11. Write 1 to the pmu_en field of the por_dt_pmcr register to start PMU operation.

6.5.2 Program PMU snapshot

Use this procedure to set up the PMU snapshot functionality.

For a system with multiple DTCs, the sub-DTC maintains snapshot status for the DTM within its own domain.

Prerequisites

The NIDEN input must be asserted for any trace and PMU operation.

Procedure

1. Program PMU counters as described in [6.5.1 Set up PMU counters on page 6-1890.](#)

2. Write 1 to the `ss_req` field of the `por_dt_pmsrr` register.
This action causes the DTC to send a PMU snapshot instruction. On receiving this instruction, the DTM sends PMU snapshot packets to the DTC.

The DTC updates the `ss_status` field of the `por_dt_pmsrr` register after receiving PMU snapshot packets. Software can poll this register field to check if the snapshot process is complete.

6.5.3 Program PMU counter overflow interrupt

Use this procedure to set up the PMU counter overflow interrupt.

Prerequisites

The NIDEN input must be asserted for any trace and PMU operation.

Procedure

1. Program PMU counters as described in [6.5.1 Set up PMU counters on page 6-1890](#).
2. Write 1 to the `ovfl_intr_en` field of the `por_dt_pmcr` register.
Results: Overflow of any PMU counter causes **INTREQPMU** to assert.
3. Write 1 to the `ovfl_intr_en` field in the all other `por_dt_pmcr` registers if your system has multiple DTCs.
4. Poll the `pmovsr[7:0]` field of the `por_dt_pmovsr` register when **INTREQPMU** is asserted to see which global counter causes the interrupt.
For multiple DTCs, all `por_dt_pmovsr` registers must be polled.
5. Write 1 to the corresponding bit in the `pmovsr_clr[7:0]` field of the `por_dt_pmovsr_clr` register to clear **INTREQPMU**.

6.6 Secure debug support

The **SPNIDEN** input and the value of the `secure_debug_disable` field of the `por_dt_secure_access` register control the Secure debug state.

Secure debug is enabled when **SPNIDEN** is asserted, or when the `secure_debug_disable` bit of the `por_dt_secure_access` register is set to 0. The default value of this bit is 0.

When Secure debug is enabled, all events can be counted and all flits can be traced.

When Secure debug is disabled, all events with `UNKNOWN` Secure state are not counted and all flits with `UNKNOWN` Secure state are not traced.

Chapter 7

Performance optimization and monitoring

This chapter describes performance optimization techniques for use by system integrators, and the *Performance Monitoring Unit (PMU)*.

It contains the following sections:

- [7.1 Performance optimization guidelines](#) on page 7-1894.
- [7.2 About the Performance Monitoring Unit](#) on page 7-1895.
- [7.3 HN-F performance events](#) on page 7-1899.
- [7.4 RN-I performance events](#) on page 7-1904.
- [7.5 SBSX performance events](#) on page 7-1908.
- [7.6 HN-I performance events](#) on page 7-1912.
- [7.7 DN performance events](#) on page 7-1916.
- [7.8 XP PMU event summary](#) on page 7-1917.
- [7.9 Occupancy and lifetime measurement using PMU events](#) on page 7-1918.
- [7.10 DEVEVENT](#) on page 7-1919.

7.1 Performance optimization guidelines

There are some restrictions when optimizing CMN-600AE.

To obtain maximum performance from CMN-600AE, the system integrator must be aware of the following information:

RN-I

When request ordering is not required, transaction requests must be dispatched with non-overlapping IDs to ensure optimal bandwidth operation. Large Burst transactions, which are transactions larger than 64B, must be split into 64B or smaller Burst transactions. In addition, set **AxSIZE** to the AXI bus width of the RN-I to fully utilize the available bandwidth.

For example, if the AXI bus width is:

128b Set **AxSIZE** = 4 (16B)

256b Set **AxSIZE** = 5 (32B)

Read or write requests to different parts of the same cache line must be combined into a single cache line request. For example, multiple (partial) WriteUnique transactions must be combined into a single WriteUnique or a single WriteLineUnique transaction. In the resultant transaction, all bytes in the cache line must be written.

Based on the transaction attributes, RN-I can enforce more ordering on transactions, targeting device memory downstream of HN-I, affecting the overall achievable bandwidth.

HN-F

High temporal locality of address usage in transactions can cause same-address dependencies to occur for transactions with addresses to overlapping cache lines. This condition results in higher latency because of serialization delays between these transactions. CMN-600AE is microarchitected to avoid hot spotting in the HN-F partitions or in the memory controllers. However, this condition is unavoidable in cases of temporally local same-address usage.

HN-I

Stream of interleaved reads and writes targeting the same peripheral downstream of HN-I results in higher latencies on these transactions. It also could result in serialization delays between these reads and writes. Arm recommends that read and write transactions are not interleaved when targeting the same peripheral.

7.2 About the Performance Monitoring Unit

CMN-600AE provides access to various performance events. Some of these events are unique to and originate in a specific CMN-600AE component. Some events are available by using watchpoints in the *Debug Watchpoint Module (DWM)* in the XP where the component is located.

This chapter describes the performance events and the relevant use cases for most of those events. See [Chapter 6 Debug Trace and PMU on page 6-1868](#) for information about the infrastructure and logic that enable general utility of the performance monitor events.

The following table shows the PMU events.

Table 7-1 PMU events

Component	NS ^a	Event	Description
HN-D		Refer to 7.7 DN performance events on page 7-1916 for event summary details.	
HN-I	No	PMU_HNI_TXDATFLITV	Transmitted data flits. Available through the DWM.
	No	PMU_HNI_RXDATFLITV	Received data flits. Available through the DWM.
	Yes	PMU_HNI_RXREQFLITV	Received requests. Available through the DWM.
	Yes	PMU_HNI_RXREQ_REQORDER	Received ReqOrder requests. Available through the DWM.
SBSX	No	PMU_SBSX_TXDATFLITV	Transmitted data flits. Available through the DWM.
	No	PMU_SBSX_RXDATFLITV	Received data flits. Available through the DWM.
	Yes	PMU_SBSX_RXREQFLITV	Received requests. Available through the DWM.
HN-F	Yes	PMU_HN_CACHE_MISS	Total cache misses
	Yes	PMU_HNL3_SF_CACHE_ACCESS	Total number of cache accesses
	Yes	PMU_HN_CACHE_FILL	Total allocations in HN SLC cache
	Yes	PMU_HN_POCQ_RETRY	Total number of requests that have been retried
	Yes	PMU_HN_POCQ_REQS_RECVD	Total number of requests that the HN received
	Yes	PMU_HN_SF_HIT	Total number of SF hits
	Yes	PMU_HN_SF_EVICTIONS	Total number of SF evictions
	Yes	PMU_HN_L3_EVICTION	Number of SLC evictions
	Yes	PMU_HN_L3_FILL_INVALID_WAY	Number of SLC fills to an invalid way
	Yes	PMU_HN_MC_RETRIES	Number of requests receiving retry response from the memory controller
	Yes	PMU_HN_MC_REQS	Total number of requests that are sent to the memory controller
	Yes	PMU_HN_QOS_HH_RETRY	Number of times HN-F protocol retried a QoS 15 (highest) class request

^a Can the event be determined to be Secure or Non-secure? If No, the event is considered to be Secure, irrespective of Secure or Non-secure attributes associated with the event.

Table 7-1 PMU events (continued)

Component	NS ^a	Event	Description
RN-I, RN-D	No	PMU_RNI_RDATEBEATS_P0	S0 RDataBeats
	No	PMU_RNI_RDATEBEATS_P1	S1 RDataBeats
	No	PMU_RNI_RDATEBEATS_P2	S2 RDataBeats
	Yes	PMU_RNI_RXDATFLITV	RXDAT flits received
	Yes	PMU_RNI_TXDATFLITV	TXDAT flits sent
	Yes	PMU_RNI_TXREQFLITV	Total TXREQ flits sent
	Yes	PMU_RNI_TXREQFLITV_RETRIED	Retried TXREQ flits sent
	No	PMU_RNI_RRTFULL	Read request tracker full
	No	PMU_RNI_WRTFULL	Write request tracker
	Yes	PMU_RNI_TXREQFLITV_REPLAYED	Replayed TXREQ flits
CXHA	Yes	HA_REQ_TRK_OCC	Request tracker occupancy
	Yes	HA_RD_DAT_BUFF_OCC ^b	Read data buffer occupancy
	Yes	HA_RSP_DATA_BYPASS_BUF_OCC	CCIX response data bypass buffer occupancy
	Yes	HA_WR_DAT_BUFF_OCC ^b	Write data buffer occupancy
	Yes	HA_SNP_TRK_BUF_OCC	Snoop tracker occupancy
	Yes	HA_SNP_DAT_SINK_BUF_OCC	Snoop data sink buffer occupancy
	Yes	HA_SNP_HZD_BUF_OCC	Snoop hazard buffer occupancy
	Yes	HA_RD_DAT_BYPASS	Read data bypass taken
	Yes	HA_SNP_PCRD_STALLS_LNK0 ^b	Snoop request available but no SNP Pcrd to send over CCIX per LinkEnd for Link 0
	Yes	HA_SNP_PCRD_STALLS_LNK1 ^b	Snoop request available but no SNP Pcrd to send over CCIX per LinkEnd for Link 1
	Yes	HA_SNP_PCRD_STALLS_LNK2 ^b	Snoop request available but no SNP Pcrd to send over CCIX per LinkEnd for Link 2
	Yes	HA_CHI_RSP_UPLOAD_STALLS	Local HA upload stalls to CHI because of contention with RA
	Yes	HA_CHI_DAT_UPLOAD_STALLS	Local HA upload stalls to CHI because of contention with RA

^a Can the event be determined to be Secure or Non-secure? If No, the event is considered to be Secure, irrespective of Secure or Non-secure attributes associated with the event.

^b If applications use only Non-secure transactions, then NS counting is correct. If a mix of Secure and Non-secure is used, then use Secure Debug such as assert **SPNIDEN**.

Table 7-1 PMU events (continued)

Component	NS ^a	Event	Description
CXLA	No	LA_RX_TLP_LINK0	RX TLPs on Link 0
	No	LA_RX_TLP_LINK1	RX TLPs on Link 1
	No	LA_RX_TLP_LINK2	RX TLPs on Link 2
	No	LA_TX_TLP_LINK0	TX TLPs on Link 0
	No	LA_TX_TLP_LINK1	TX TLPs on Link 1
	No	LA_TX_TLP_LINK2	TX TLPs on Link 2
	No	LA_RX_CXS_LINK0	RX CXS on Link 0
	No	LA_RX_CXS_LINK1	RX CXS on Link 1
	No	LA_RX_CXS_LINK2	RX CXS on Link 2
	No	LA_TX_CXS_LINK0	TX CXS on Link 0
	No	LA_TX_CXS_LINK1	TX CXS on Link 1
	No	LA_TX_CXS_LINK2	TX CXS on Link 2
	No	LA_RX_TLP_AVG_SIZE	Average RX TLP size in DWs
	No	LA_TX_TLP_AVG_SIZE	Average TX TLP size in DWs
	No	LA_RX_TLP_AVG_CCIX_MSGS	Average RX TLP size in CCIX messages
	No	LA_TX_TLP_AVG_CCIX_MSGS	Average TX TLP size in CCIX messages
	No	LA_RX_CXS_AVG_SIZE	Average size of RX CXS in DWs within a beat
	No	LA_TX_CXS_AVG_SIZE	Average size of TX CXS in DWs within a beat
	No	LA_TX_CXS_LCRD_BACKPRESSURE	TX CXS link credit backpressure from PHY
	No	LA_RX_TLPBUF_FULL_STALL	RX TLP buffer full and backpressured
	No	LA_TX_TLPBUF_FULL_STALL	TX TLP buffer full and backpressured
	No	LA_RX_AVG_TLP_LAT	Average latency to process an RX TLP
	No	LA_TX_AVG_TLP_LAT	Average latency to form a TX TLP

^a Can the event be determined to be Secure or Non-secure? If No, the event is considered to be Secure, irrespective of Secure or Non-secure attributes associated with the event.

Table 7-1 PMU events (continued)

Component	NS ^a	Event	Description
CXRA	Yes	RA_REQ_TRK_OCC	Request tracker occupancy
	Yes	RA_SNP_TRK_OCC	Snoop tracker occupancy
	Yes	RA_RD_DAT_BUF_OCC	Read data buffer occupancy ^b
	Yes	RA_WR_DAT_BUF_OCC	Write data buffer occupancy ^b
	Yes	RA_SNP_SINK_BUF_OCC	Snoop sink buffer occupancy ^b
	Yes	RA_SNP_BCASTS	Snoop broadcasts
	Yes	RA_REQ_CHAINS	Number of request chains formed larger than one
	Yes	RA_REQ_CHAIN_AVG_LEN	Average size of request chains, only for chain sizes larger than one
	Yes	RA_CHI_RSP_UPLOAD_STALLS	Local RA upload stalls to CHI because of contention with HA ^b
	Yes	RA_CHI_DAT_UPLOAD_STALLS	Local RA upload stalls to CHI because of contention with HA
	Yes	RA_DAT_PCRD_STALLS_LNK0	Memory Data Request available, but no DAT Pcrd to send over CCIX per LinkEnd 0 ^b
	Yes	RA_DAT_PCRD_STALLS_LNK1	Memory Data Request available, but no DAT Pcrd to send over CCIX per LinkEnd 1 ^b
	Yes	RA_DAT_PCRD_STALLS_LNK2	Memory Data Request available, but no DAT Pcrd to send over CCIX per LinkEnd 2 ^b
	Yes	RA_REQ_PCRD_STALLS_LNK0	Memory Data Request available but no Req Pcrd to send over CCIX per LinkEnd 0 ^b
	Yes	RA_REQ_PCRD_STALLS_LNK1	Memory Data Request available but no Req Pcrd to send over CCIX per LinkEnd 1 ^b
	Yes	RA_REQ_PCRD_STALLS_LNK2	Memory Data Request available but no Req Pcrd to send over CCIX per LinkEnd 2 ^b

7.2.1 Cycle counter

The cycle counter is used to track time.

You can reset this counter to initiate the time interval over which you want to capture the events.

PMU_CYCLE_COUNTER Cycle counter.

GCLK0 clocks the cycle counter. Therefore, the cycle counter is not incremented during periods of HCG when the clocks are stopped.

^a Can the event be determined to be Secure or Non-secure? If No, the event is considered to be Secure, irrespective of Secure or Non-secure attributes associated with the event.

7.3 HN-F performance events

The HN-F performance analysis counters are used to monitor cache behavior.

For a particular cache, the cache miss or hit rate is used to measure the capacity of the cache, and the location for certain applications. To measure the cache miss rate, the performance monitor counters count the number of instances of cache accesses and cache misses.

This section contains the following subsections:

- [7.3.1 Cache performance on page 7-1899.](#)
- [7.3.2 HN-F counters on page 7-1900.](#)
- [7.3.3 SF events on page 7-1900.](#)
- [7.3.4 System-wide events on page 7-1901.](#)
- [7.3.5 Quality of Service on page 7-1901.](#)
- [7.3.6 HN-F PMU event summary on page 7-1901.](#)

7.3.1 Cache performance

Cache performance events are required to calculate the cache miss rate and the cache allocation.

The following sections describe the cache performance events.

Cache miss rate

The cache events that are required to calculate the cache miss rate are:

PMU_HN_CACHE_MISS_EVENT	Counts the total cache misses. A miss results from a first-time lookup and is high priority.
PMU_HNSLC_SF_CACHE_ACCESS_EVENT	The total number of cache accesses. An access is first-time and high priority.

Note

The performance counter architecture enables only four HNs to collect the cache miss rate. However, because of the CMN-600AE microarchitecture, the cache miss rate that is measured at one HN-F is a good proxy for the cache miss rate of the remaining HN-Fs.

Calculate the cache miss rate as follows:

$$\text{Cache miss rate (\%)} = \frac{\text{Total cache misses}}{\text{Total cache accesses}} \times 100$$

Figure 7-1 Cache miss rate

Certain request types can cause multiple cache accesses:

- Lookup.
- Tag update.
- Victim selection.
- Cache fill.

Event counting is therefore limited to first time accesses only. For example, for a ReadUnique transaction that leads to an SLC hit, PMU_HNSLC_SF_CACHE_ACCESS_EVENT is only counted the first-time cache lookup is performed. The tag update is not counted as a cache access. Similarly, for WriteBack or Write*Unique transactions with an SLC allocate hint, only the first instance of an SLC lookup is counted as an access and hit or miss. The eventual victim selection and cache fill are not counted as further accesses.

Cache allocations

The cache allocation event counts the number of times an HN-F SLC cache is allocated. It provides an approximate cache usage for this particular application over a specific time slice. This event does not check whether the application has any hot sets.

PMU_HN_CACHE_FILL_EVENT Counts all cache line allocations to SLC cache.

All cache line writes, that is, Write*Unique, WriteBack, and Evictions that are allocated in SLC cache, are counted towards this event.

7.3.2 HN-F counters

Applications can bottleneck on one or more HN-Fs because they frequently target an address or a stream of addresses.

The following POCQ occupancy and request retry events are used to monitor possible performance loss in the system:

PMU_HN_POCQ_RETRY_EVENT The total number of requests that have been retried.

PMU_HN_POCQ_REQS_RECVD_EVENT The total number of requests that the HN-F receives.

Requests that cannot be queued in the POCQ, because of lack of credits, are retried. The HN-F responds with a RetryAck response, and the request waits for a static credit. This wait period indicates whether a lack of credits is causing the bottlenecks, and also shows if the latency of requests is very high.

Calculate the message retry rate as follows:

$$\text{HN-F message retry rate (\%)} = \frac{\text{HN-F total messages retried}}{\text{HN-F total messages received}} \times 100$$

Figure 7-2 HN-F message retry rate

7.3.3 SF events

There are three snoop events that can be counted.

The following sections describe the SF performance events.

SF miss rate

This event measures the amount of memory controller traffic that is generated. It can also be used to measure the efficiency of the SF.

PMU_HN_SF_HIT_EVENT Measures the number of SF hits.

Calculate the SF hit rate as follows:

$$\text{Snoop filter hit rate (\%)} = \frac{\text{Total snoop filter hits}}{\text{Total SLC lookups}} \times 100$$

Figure 7-3 SF hit rate

SF accesses are only counted for first-time lookups, and not for the victim selection accesses or SF fills. Because the SLC lookup and SF lookups are parallel, the SLC lookups can be used to calculate the SF hit rate.

SF evictions

This event measures the frequency of SF evictions.

PMU_HN_SF_EVICTIONS_EVENT Measures the number of SF evictions when cache invalidations are initiated.

Snoops sent and received with hit rate

These events measure the amount of shared data across clusters for a specific application, using snoop hits or misses.

PMU_HN_SNOOPS_SENT_EVENT Number of snoops sent. Does not differentiate between broadcast or directed snoops.

PMU_HN_SNOOPS_BROADCAST_EVENT Number of snoop broadcasts sent.

Calculate the snoops sent and received rate as follows:

$$\text{Shared data (\%)} = \frac{\text{Total snoops broadcast}}{\text{Total snoops sent}} \times 100$$

Figure 7-4 Sent and received snoops rate

The number of broadcast and total snoops measures the shared data invalidations.

7.3.4 System-wide events

The memory controller request retries determine whether the memory controller is the bottleneck in the system, which can cause higher request latencies.

The following events can be counted:

PMU_HN_MC_RETRIES_EVENT Number of requests that are retried to the memory controller.

PMU_HN_MC_REQS_EVENT Total number of requests that are sent to the memory controller.

Calculate the retry rate for requests to the memory controller as follows:

$$\text{MC message retry rate (\%)} = \frac{\text{MC total messages retried}}{\text{MC total messages received}} \times 100$$

Figure 7-5 MC message retry rate

7.3.5 Quality of Service

Requests with a HighHigh QoS must be allocated and processed from the POCQ with the highest priority compared to High, Medium, and Low QoS requests.

If the HighHigh requests are retried too frequently, there could be a bottleneck at a particular HN-F, or the POCQ reservation for HighHigh requests requires adjustment.

PMU_HN_QOS_HH_RETRY How often a HighHigh request is retried.

7.3.6 HN-F PMU event summary

The following table shows a summary of the HN-F PMU events.

Table 7-2 HN-F events

Number	Name	Description
1	PMU_HN_CACHE_MISS_EVENT	Counts total cache misses in first lookup result (high priority).
2	PMU_HNSLC_SF_CACHE_ACCESS_EVENT	Counts number of cache accesses in first access (high priority).
3	PMU_HN_CACHE_FILL_EVENT	Counts total allocations in HN SLC (all cache line allocations to SLC).

Table 7-2 HN-F events (continued)

Number	Name	Description
4	PMU_HN_POCQ_RETRY_EVENT	Counts number of retried requests.
5	PMU_HN_POCQ_REQS_RECVD_EVENT	Counts number of requests that HN receives.
6	PMU_HN_SF_HIT_EVENT	Counts number of SF hits.
7	PMU_HN_SF_EVICTIONS_EVENT	Counts number of SF eviction cache invalidations initiated.
8	PMU_HN_DIR_SNOOPS_SENT_EVENT	Counts number of directed snoops sent (not including SF back invalidation).
9	PMU_HN_BRD_SNOOPS_SENTEVENT	Counts number of multicast snoops sent (not including SF back invalidation).
10	PMU_HN_SLC_EVICTION_EVENT	Counts number of SLC evictions (dirty only).
11	PMU_HN_SLC_FILL_INVALID_WAY_EVENT	Counts number of SLC fills to an invalid way.
12	PMU_HN_MC_RETRIES_EVENT	Counts number of retried transactions by the MC.
13	PMU_HN_MC_REQS_EVENT	Counts number of requests that are sent to MC.
14	PMU_HN_QOS_HH_RETRY_EVENT	Counts number of times a HighHigh priority request is protocol-retried at the HN-F.
15	PMU_HNF_POCQ_OCCUPANCY_EVENT	Counts the POCQ occupancy in HN-F. Occupancy filtering is programmed in pmu_occup1_id.
16	PMU_HN_POCQ_ADDRHAZ_EVENT	Counts number of POCQ address hazards on allocation.
17	PMU_HN_POCQ_ATOMICS_ADDRHAZ_EVENT	Counts number of POCQ address hazards on allocation for atomic operations.
18	PMU_HN_LD_ST_SWP_ADQ_FULL_EVENT	Counts number of times ADQ is full for Ld/St/SWP type atomic operations while POCQ has pending operations.
19	PMU_HN_CMP_ADQ_FULL_EVENT	Counts number of times ADQ is full for CMP type atomic operations while POCQ has pending operations.
20	PMU_HN_TXDAT_STALL_EVENT	Counts number of times HN-F has a pending TXDAT flit but no credits to upload.
21	PMU_HN_TXRSP_STALL_EVENT	Counts number of times HN-F has a pending TXRSP flit but no credits to upload.
22	PMU_HN_SEQ_FULL_EVENT	Counts number of times requests are replayed in SLC pipe due to SEQ being full.
23	PMU_HN_SEQ_HIT_EVENT	Counts number of times a request in SLC hit a pending SF eviction in SEQ.
24	PMU_HN_SNP_SENT_EVENT	Counts number of snoops sent including directed, multicast, and SF back invalidation.
25	PMU_HN_SFBI_DIR_SNP_SENT_EVENT	Counts number of times directed snoops were sent due to SF back invalidation.
26	PMU_HN_SFBI_BRD_SNP_SENT_EVENT	Counts number of times multicast snoops were sent due to SF back invalidation.
27	PMU_HN_SNP_SENT_UNTRK_EVENT	Counts number of times snoops were sent due to untracked RNFs.
28	PMU_HN_INTV_DIRTY_EVENT	Counts number of times SF back invalidation resulted in dirty line intervention from the RN.

Table 7-2 HN-F events (continued)

Number	Name	Description
29	PMU_HN_STASH_SNP_SENT_EVENT	Counts number of times stash snoops were sent.
30	PMU_HN_STASH_DATA_PULL_EVENT	Counts number of times stash snoops resulted in data pull from the RN.
31	PMU_HN_SNP_FWDED_EVENT	Counts number of times data forward snoops were sent.

7.4 RN-I performance events

External devices connect at an RN-I bridge.

This section contains the following subsections:

- [7.4.1 Bandwidth at RN-I bridges on page 7-1904.](#)
- [7.4.2 Bottleneck analysis at RN-I bridges on page 7-1905.](#)
- [7.4.3 RN-I PMU event summary on page 7-1906.](#)

7.4.1 Bandwidth at RN-I bridges

External devices connect at an RN-I bridge.

The following events measure bandwidth at the RN-I bridges:

- [Requested read bandwidth at RN-I bridges on page 7-1904.](#)
- [Actual read bandwidth on interconnect on page 7-1904.](#)
- [Write bandwidth at RN-I bridges on page 7-1905.](#)

Requested read bandwidth at RN-I bridges

External devices connect to CMN-600AE at an RN-I bridge.

To monitor the behavior of the system, the following events measure the read bandwidth at each RN-I bridge:

- RDataBeats_Port0** Number of RData beats, **RVALID** and **RREADY**, dispatched on port 0. This is a measure of the read bandwidth.
- RDataBeats_Port1** Number of RData beats, **RVALID** and **RREADY**, dispatched on port 1. This is a measure of the read bandwidth.
- RDataBeats_Port2** Number of RData beats, **RVALID** and **RREADY**, dispatched on port 2. This is a measure of the read bandwidth.

Because CMOs are sent through the read channel, their responses are included in these events.

Calculate the read bandwidth as follows:

$$\text{Read bandwidth} = \frac{\text{Number RDataBeats_Port}n \times \text{AXIDataBeatSize}}{\text{Cycles}} \times \text{Frequency}$$

Where AXIDataBeatSize is the number of bytes for each AXI beat. In most cases, this is the same size as the AXI bus.

Actual read bandwidth on interconnect

RXDATFLITV measures the bandwidth that an RN-I bridge sends to the interconnect.

This event counts the number of received data flit requests that the bridge receives through the data channel. Therefore, this event measure the actual bandwidth that an RN-I bridge sends to the interconnect, and not the useful bandwidth the external devices can use.

- RXDATFLITV** Number of **RXDAT** flits received. This event is a measure of the true read data bandwidth. It excludes CMOs, because CMO completions return to the RN-I through the response channel, but includes replayed requests.

This event includes the replayed requests because of the read data buffer decoupled scheme.

Calculate the actual read bandwidth as follows:

$$\text{Actual read bandwidth} = \frac{\text{RXDATFLITV} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Figure 7-6 Actual read bandwidth

Write bandwidth at RN-I bridges

TXDATFLITV monitors the number of data flits that the RN-I bridge sends out.

In a similar way to the read actual bandwidth event, this event monitors the number of data flits that the RN-I bridge sends out. Therefore, this event measures the actual write bandwidth that is sent to the interconnect:

TXDATFLITV Number of **TXDAT** flits dispatched. This event is a measure of the write bandwidth.

Calculate the write bandwidth as follows:

$$\text{Actual write bandwidth} = \frac{\text{TXDATFLITV} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Figure 7-7 Actual write bandwidth

7.4.2 Bottleneck analysis at RN-I bridges

CMN-600AE provides events that observe the locations where the nodes or bridges are full, which can cause delays in the rest of the system.

This feature enables you to monitor the current bottlenecks in the system, and checks multiple events in the RN-Is, HN-Fs, and memory controllers. In the RN-I bridges, the events monitor the following:

- The number of times the bridge is forced to retry because of the lack of dynamic credits.
- The number of times the read and write tracker is full and therefore cannot accept new requests in the system. This condition can cause delays in the AXI masters.
- The number of read request replays, because of decoupling of the read request buffers and read data buffers in the RN-I system.

Request retry rate at RN-I bridges

TXREQFLITV_RETRIED monitors the efficiency of using dynamic credits in the system.

It does this task by measuring the request retry rate:

TXREQFLITV_RETRIED Number of retried **TXREQ** flits dispatched. This event is a measure of the retry rate.

Calculate the request retry rate as follows:

$$\text{Retry rate} = \frac{\text{TXREQFLITV_RETRIED}}{\text{TXREQFLITV_TOTAL}}$$

Figure 7-8 Retry rate

Read and write delays at RN-I bridges

To monitor the delays for both reads and writes, CMN-600AE enables you to monitor how full the read and write trackers are in the RN-I bridges.

When one of the trackers is full, the bridge cannot accept new requests from the AXI master. This condition delays the I/O devices that connect to the AXI master.

There are two measures that, together, can help you to isolate the source of bottlenecks in the system. These measures are: how full the trackers are, and the read and write bandwidth from the RN-I bridge to the interconnect. For example, consider the following situations:

- The read tracker of a specific RN-I bridge is full but the effective read bandwidth from the bridge is not close to the maximum expected. In this case, the interconnect cannot keep up with the read traffic from the specific device.
- The bandwidth is close to maximum, the I/O device can send requests to the maximum of its port bandwidth. In this case, the tracker is full for this reason.

You can also use the measure of how full the trackers are with AXI PMUs to monitor delays to the AXI masters.

The following events monitor the read and write trackers:

RRT_OCCUPANCY All entries in the read request tracker are occupied. This event is a measure of oversubscription in the read request tracker.

WRT_OCCUPANCY All entries in the write request tracker are occupied. This event is a measure of oversubscription in the write request tracker.

7.4.3 RN-I PMU event summary

There are 16 RN-I PMU events.

The following table shows a summary of the RN-I PMU events.

Table 7-3 RN-I PMU event summary

Number	Name	Description
1	PMU_RNI_RDATABASEATS_P0	Number of RData beats, RVALID and RREADY , dispatched on port 0. This event measures the read bandwidth, including CMO responses.
2	PMU_RNI_RDATABASEATS_P1	Number of RData beats, RVALID and RREADY , dispatched on port 1. This event measures the read bandwidth, including CMO responses.
3	PMU_RNI_RDATABASEATS_P2	Number of RData beats, RVALID and RREADY , dispatched on port 2. This event measures the read bandwidth, including CMO responses.
4	PMU_RNI_RXDATFLITV	Number of RXDAT flits received. This event measures the true read data bandwidth, excluding CMOs.
5	PMU_RNI_TXDATFLITV	Number of TXDAT flits dispatched. This event measures the write bandwidth.
6	PMU_RNI_TXREQFLITV	Number of TXREQ flits dispatched. This event measures the total request bandwidth.
7	PMU_RNI_TXREQFLITV_RETRIED	Number of retried TXREQ flits dispatched. This event measures the retry rate.
8	PMU_RNI_RRT_OCCUPANCY	All entries in the read request tracker are occupied. This event measures oversubscription in the read request tracker.
9	PMU_RNI_WRT_OCCUPANCY	All entries in the write request tracker are occupied. This event measures oversubscription in the write request tracker.
10	PMU_RNI_TXREQFLITV_REPLAYED	Number of replayed TXREQ flits. This event measures the replay rate.
11	PMU_RNI_WRCANCEL_SENT	Number of write data cancels sent. This event measures the write cancel rate.
12	PMU_RNI_WDATABASEAT_P0	Number of WData beats, WVALID and WREADY , dispatched on port 0. This event measures write bandwidth on AXI port 0.
13	PMU_RNI_WDATABASEAT_P1	Number of WData beats, WVALID and WREADY , dispatched on port 1. This event measures the write bandwidth on AXI port 1.
14	PMU_RNI_WDATABASEAT_P2	Number of WData beats, WVALID and WREADY , dispatched on port 2. This event measures the write bandwidth on AXI port 2.
15	PMU_RNI_RRTALLOC	Number of allocations in the read request tracker. This event measures the read transaction count.
16	PMU_RNI_WRTALLOC	Number of allocations in the write request tracker. This event measures the write transaction count.
17	PMU_RNI_RDB_UNORD	Number of cycles for which Read Data Buffer state machine is in Unordered Mode.

Table 7-3 RN-I PMU event summary (continued)

Number	Name	Description
18	PMU_RNI_RDB_REPLAY	Number of cycles for which Read Data Buffer state machine is in Replay mode.
19	PMU_RNI_RDB_HYBRID	Number of cycles for which Read Data Buffer state machine is in hybrid mode. Hybrid mode is where there is a mix of ordered and unordered traffic.
20	PMU_RNI_RDB_ORD	Number of cycles for which Read Data Buffer state machine is in ordered Mode.

7.5 SBSX performance events

This section contains SBSX performance event information.

This section contains the following subsections:

- [7.5.1 Bandwidth at SBSX bridges on page 7-1908.](#)
- [7.5.2 Bottleneck analysis at SBSX bridges on page 7-1909.](#)
- [7.5.3 SBSX PMU event summary on page 7-1911.](#)

7.5.1 Bandwidth at SBSX bridges

This section contains SBSX bridge bandwidth information.

The following events are used to measure bandwidth at the SBSX bridges:

- [Read bandwidth on interconnect at SBSX bridges on page 7-1908.](#)
- [Write bandwidth at SBSX bridges on page 7-1908.](#)
- [Total requested bandwidth at SBSX bridges on page 7-1909.](#)

Read bandwidth on interconnect at SBSX bridges

This section contains information on read bandwidth on interconnect at SBSX bridges.

This event counts the number of received data flits at the SBSX and interconnect:

PMU_SBSX_RXDAT Number of RXDAT flits received at XP from SBSX. This event is a measure of the read data bandwidth.

Calculate the actual read bandwidth as follows:

$$\text{Actual read bandwidth} = \frac{\text{PMU_SBSX_RXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Figure 7-9 Actual read bandwidth

Note

This event is tracked in the DWM, not in the SBSX, and is defined from the XP's perspective.

Write bandwidth at SBSX bridges

This section contains information on write bandwidth at SBSX bridges.

In a similar way to the read actual bandwidth event, this event monitors the number of data flits that the SBSX receives. Therefore, this event measures the actual write bandwidth that is received from the interconnect:

PMU_SBSX_TXDAT Number of TXDAT flits dispatched from XP to SBSX. This event is a measure of the write bandwidth.

Calculate the write bandwidth as follows:

$$\text{Actual write bandwidth} = \frac{\text{PMU_SBSX_TXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Figure 7-10 Actual write bandwidth

Note

This event is tracked in the DWM, not in the SBSX design. The event is defined from the perspective of the XP.

Total requested bandwidth at SBSX bridges

This section contains information on total requested bandwidth at SBSX bridges.

To improve efficiency when using PMU events and signals, this event combines the read and write bandwidth estimation in a single event. The PMU_SBSX_TXREQ_TOTAL event monitors the number of REQ flits that an SBSX bridge receives:

PMU_SBSX_TXREQ_TOTAL

Number of **TXREQ** flits dispatched from XP to SBSX. This event is a measure of the total request bandwidth.

Calculate the total bandwidth as follows:

$$\text{Total requested bandwidth} = \frac{\text{PMU_SBSX_TXREQ_TOTAL} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Figure 7-11 Total requested bandwidth

Note

This event is tracked in the DWM, not in the SBSX design, and is defined from the perspective of the XP.

7.5.2 Bottleneck analysis at SBSX bridges

This section contains information on bottleneck analysis at SBSX bridges.

CMN-600AE provides events that observe the locations where the nodes or bridges are full, which can cause delays in the rest of the system. This feature enables you to monitor the current bottlenecks in the system, and checks multiple events in all CMN-600AE components. The events monitor the following:

- The number of times the bridge is forced to retry because of the lack of dynamic credits.
- The number of cycles the bridge is forced to stall due to backpressures on AXI or CHI interface.

The following events are used to measure bottlenecks at the SBSX bridges:

- [7.5 SBSX performance events on page 7-1908](#).

Request retry rate at SBSX bridges

This section contains information on the request retry rate at SBSX bridges.

RXREQFLITV_RETRIED monitors the efficiency of using dynamic credits in the system. It does this task by measuring the request retry rate:

RXREQFLITV_RETRIED

Number of **RXREQ** flits dispatched. This event is a measure of the retry rate. Calculate the retry rate as follows:

$$\text{Retry rate} = \text{RXREQFLITV_RETRIED} / \text{RXREQFLITV_TOTAL}$$

Delays at SBSX bridges due to backpressure

To analyze the delays in SBSX bridges, CMN-600AE enables you to monitor the source of backpressure.

SBSX might have requests that are ready to be sent to the downstream AXI or ACE-Lite device. However, it cannot send them due to backpressure from the downstream device. In this situation, SBSX holds the request in the *Receive Request Tracker* (RRT). This condition results in the RRT getting full and so the SBSX bridge cannot accept any new requests from RNs impacting system performance.

The following table contains events that monitor such backpressure from the downstream AXI or ACE-Lite device:

Table 7-4 AXI or ACE-Lite downstream monitoring events

Events	Description
ARVALID_NO_ARREADY	Number of cycles the SBSX bridge is stalled due to backpressure on AR channel.
AWVALID_NO_AWREADY	Number of cycles the SBSX bridge is stalled due to backpressure on AW channel.
WVALID_NO_WREADY	Number of cycles the SBSX bridge is stalled due to backpressure on W channel.

If a mesh is congested with many DAT or RSP flits, it might not give link credits to SBSX in timely manner. This situation can cause DAT flits for Reads or RSP flits for Writes to be stalled in SBSX. The following table describes events monitor in such cases where SBSX bridge is not able to upload DAT/RSP flits on the mesh.

Table 7-5 CHI events monitor information

Events	Description
TXDATFLITV_NO_LINKCRD	Number of cycles the TXDAT flit in SBSX bridge is waiting for link credits.
TXRSPFLITV_NO_LINKCRD	Number of cycles the TXRSP flit in SBSX bridge is waiting for link credits.

Tracker occupancy analysis

To debug performance issues, more events are provided to measure occupancy of various trackers in SBSX. These trackers include the *Request Received Tracker* (RRT), *Request Dispatch Tracker* (RDT), and *Write Data Buffers* (WDB).

Read, Write, and CMO transactions occupy RRT before they are dispatched on the AXI interface. When Read/CMO transactions are dispatched on AXI, they move from RRT to RDT. Writes remain on RRT until the write response is obtained from AXI interface and then deallocated from RRT. Knowing the occupancy of RRT and RDT independently can inform you better about the bottleneck source. In the PMU event register description section, RRT is called request tracker, while RDT is called AXI pending tracker.

The following table contains tracker occupancy information.

Table 7-6 Tracker occupancy information

Events	Description
RRT_RD_OCCUPANCY_CNT_OVFL	Read request tracker occupancy count overflow
RRT_WR_OCCUPANCY_CNT_OVFL	Write request tracker occupancy count overflow
RRT_CMO_OCCUPANCY_CNT_OVFL	CMO request tracker occupancy count overflow
WDB_OCCUPANCY_CNT_OVFL	WDB occupancy count overflow
RDT_RD_OCCUPANCY_CNT_OVFL	Read AXI pending tracker occupancy count overflow
RDT_CMO_OCCUPANCY_CNT_OVFL	CMO AXI pending tracker occupancy count overflow

7.5.3 SBSX PMU event summary

This section contains SBSX PMU event summary information.

For more information, see [por_sbsx_pmu_event_sel](#) on page 4-899.

7.6 HN-I performance events

This section contains HN-I performance event information.

This section contains the following subsections:

- [7.6.1 Bandwidth at HN-I bridges on page 7-1912.](#)
- [7.6.2 Bottleneck analysis at HN-I bridges on page 7-1913.](#)
- [7.6.3 HN-I PMU event summary on page 7-1915.](#)

7.6.1 Bandwidth at HN-I bridges

This section contains HN-I bridge bandwidth information.

The following events are used to measure bandwidth at the HN-I bridges:

- [Read bandwidth on interconnect at HN-I bridges on page 7-1912.](#)
- [Write bandwidth at HN-I bridges on page 7-1912.](#)
- [Total requested bandwidth at HN-I bridges on page 7-1913.](#)

Read bandwidth on interconnect at HN-I bridges

This section contains information on read bandwidth on interconnect at HN-I bridges.

This event counts the number of received data flits at the HN-I and interconnect:

PMU_HNI_RXDAT Number of **RXDAT** flits received at XP from HN-I. This event is a measure of the read data bandwidth.

Calculate the actual read bandwidth as follows:

$$\text{Actual read bandwidth} = \frac{\text{PMU_HNI_RXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Figure 7-12 Actual read bandwidth

Note

This event is tracked in the DWM, not in the HN-I design. The event is defined from the XP's perspective.

Write bandwidth at HN-I bridges

This section contains information on write bandwidth at HN-I bridges.

In a similar way to the read actual bandwidth event, this event monitors the number of data flits that the HN-I receives. Therefore this event measures the actual write bandwidth that is received from the interconnect:

PMU_HNI_TXDAT Number of **TXDAT** flits dispatched from XP to HN-I. This event is a measure of the write bandwidth.

Calculate the write bandwidth as follows:

$$\text{Actual write bandwidth} = \frac{\text{PMU_HNI_TXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Figure 7-13 Actual write bandwidth

Note

This event is tracked in the DWM, not in the HN-I design. The event is defined from the perspective of the XP.

Total requested bandwidth at HN-I bridges

This section contains information on total requested bandwidth at HN-I bridges.

To improve efficiency when using PMU events and signals, this event combines the read and write bandwidth estimation in a single event. The PMU_HNI_TXREQ_TOTAL event monitors the number of REQ flits that an HN-I bridge receives:

PMU_HNI_TXREQ_TOTAL

Number of **TXREQ** flits dispatched from XP to HN-I. This event is a measure of the total request bandwidth.

Calculate the total bandwidth as follows:

$$\text{Total requested bandwidth} = \frac{\text{PMU_HNI_TXREQ} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Figure 7-14 Total requested bandwidth

Note

This event is tracked in the DWM, not in the HN-I design. The event is defined from the perspective of the XP.

7.6.2 Bottleneck analysis at HN-I bridges

This section contains information on bottleneck analysis at HN-I bridges.

Locations where the nodes or bridges are full can cause delays in the rest of the system. CMN-600AE provides events that observe locations where the nodes or bridges are full. This feature enables you to monitor the current bottlenecks in the system, and checks multiple events in all CMN-600AE components. The events monitor the following:

- The number of times the bridge is forced to retry because of the lack of dynamic credits.
- The number of times requests are serialized due to ordering requirements.
- The number of cycles the bridge is forced to stall due to backpressures.

The following events are used to measure bottlenecks at the HN-I bridges:

- [7.6 HN-I performance events on page 7-1912](#).

Request retry rate at HN-I bridges

This section contains information on the request retry rate at HN-I bridges.

RXREQFLITV_RETRIED monitors the efficiency of using dynamic credits in the system. It does this task by measuring the request retry rate:

RXREQFLITV_RETRIED

Number of **RXREQ** flits dispatched. This event is a measure of the retry rate. Calculate the retry rate as follows:

$$\text{Retry rate} = \text{RXREQFLITV_RETRIED} / \text{RXREQFLITV_TOTAL}$$

Delays at HN-I bridges because of ordering requirements

When requests are received at an HN-I, there are different ordering guarantees the HN-I bridge must maintain based on the source and attributes of the request.

The requests are sometimes serialized, indicating a lower than expected bandwidth at HN-I, as the following table shows.

Table 7-7 PCIe and non-PCIe RN request information

Request	Description
NONPCIE_SERIALIZED	Number of non-PCIe RN requests that are serialized.
PCIE_SERIALIZED	Number of PCIe RN requests that are serialized.

Delays at HN-I bridges because of backpressure

To analyze the delays in HN-I bridges, CMN-600AE enables you to monitor the source of backpressure.

HN-I might have requests that are ready to be sent to AXI or ACE-Lite downstream. However, it cannot send them due to backpressure from AXI or ACE-Lite downstream. In this situation, HN-I holds the request in the RRT. As a result, the RRT gets full. Therefore, the HN-I bridge cannot accept any new requests from RNs, impacting system performance.

This table describes the events that monitor such backpressure from AXI or ACE-Lite downstream:

Table 7-8 AXI and ACE-Lite downstream events monitor information

Events	Description
ARVALID_NO_ARREADY	Number of cycles the HN-I bridge is stalled due to backpressure on AR channel.
AWVALID_NO_AWREADY	Number of cycles the HN-I bridge is stalled due to backpressure on AW channel.
WVALID_NO_WREADY	Number of cycles the HN-I bridge is stalled due to backpressure on W channel.

Even if the AXI or ACE-Lite downstream is ready to accept new requests, the HN-I bridge cannot send them downstream while the RDT is full. The lifetime of a request in the RDT depends on response latency from AXI or ACE-Lite downstream and backpressure on TXDAT channel.

This table describes the events that monitor cases where an HN-I bridge is unable to send new requests to AXI or ACE-Lite downstream:

Table 7-9 AXI and ACE-Lite downstream events monitor information (no new requests sent)

Events	Description
ARREADY_NO_ARVALID	Number of cycles the AR channel is waiting for new requests from HN-I bridge.
AWREADY_NO_AWVALID	Number of cycles the AW channel is waiting for new requests from HN-I bridge.

If the mesh is congested with many DAT flits, then there might be a delay before it gives link credits to HN-I. This delay results in the stalling of DAT flits for Reads in HN-I. This table describes events that monitor cases where an HN-I bridge is not able to upload a DAT flit on the mesh.

Table 7-10 CHI events monitor information

Events	Description
TXDATFLITV_NO_LINKCRD	Number of cycles the TXDAT flit in HN-I bridge is waiting for link credits.

Tracker occupancy analysis in HN-I

To debug performance issues, more events are provided to measure occupancy of various trackers in HN-I such as RRT, RDT, and WDB.

Read and Write transactions occupy RRT before they are dispatched on the AXI interface. When Read and Write transactions are dispatched on AXI, they move from RRT to RDT. Reads and Writes remain on RDT until all the responses are obtained from the AXI interface. The transactions are then deallocated from RDT. Knowing the occupancy of RRT and RDT independently can inform you better about the bottleneck source. In the PMU event register description section, RRT is called request tracker while RDT is called AXI pending tracker.

The following table contains tracker occupancy information:

Table 7-11 Tracker occupancy information

Events	Description
RRT_RD_OCCUPANCY_CNT_OVFL	Read occupancy count overflow event in RRT
RRT_WR_OCCUPANCY_CNT_OVFL	Write occupancy count overflow event in RRT
RDT_RD_OCCUPANCY_CNT_OVFL	Read occupancy count overflow event in RDT
RDT_WR_OCCUPANCY_CNT_OVFL	Write occupancy count overflow event in RDT
WDB_OCCUPANCY_CNT_OVFL	WDB occupancy count overflow event

7.6.3 HN-I PMU event summary

This section contains HN-I PMU event summary information.

Refer to [por_hni_pmu_event_sel](#) on page 4-637 for more information.

7.7 DN performance events

This section contains DN performance event information.

The following table shows a summary of the DN PMU events.

Table 7-12 DN PMU event summary

Number	Name	Description
1	PMU_DN_RXREQ_DVMOP	Number of DVMOP requests received. This includes all the sub-types include TLB invalidate, Branch predictor invalidate, instruction cache (physical and virtual) invalidate.
2	PMU_DN_RXREQ_DVMSYNC	Number of DVM Sync requests received.
3	PMU_DN_RXREQ_DVMOP_VMID_FILTERED	Number of incoming DVMOP requests that are subject to VMID based filtering. This is a measure of the effectiveness of VMID based filtering and potential reduction in DVM snoops.
4	PMU_DN_RXREQ_RETRIED	Number of incoming requests that are retried. This is a measure of the retry rate.
5	PMU_DN_TRK_OCCUPANCY	Counts the tracker occupancy in DN.

The `pmu_occup1_id` field in the `por_dn_pmu_event_sel` register is used to program the occupancy counter for specific operations types. The following table summarizes the options.

Table 7-13 Field values for `pmu_occup1_id`

<code>pmu_occup1_id</code> values	Description
<code>0b0000</code>	All
<code>0b0001</code>	DVM Ops
<code>0b0010</code>	DVM Syncs

Note

In HN-D, DN PMU events can be accessed only when the corresponding HN-I PMU select is 0 (NONE).

DN events can be accessed through the HN-D. The `por_dn_pmu_event_sel` register outputs on corresponding TXPMU output only if `por_hni_pmu_event_sel` bits [5], [13], [21], and [29] are set to 0. Otherwise the value on the HN-I PMU is available.

7.8 XP PMU event summary

This section contains XP PMU event summary information.

Each of the XP PMU events is associated with:

- One of six XP ports - East, West, North, South, device port0 or device port1.
- One of four CHI channels - REQ, RSP, SNP, or DAT.

You can specify up to four XP PMU events using the `por_mxp_pmu_event_sel` register. For more information about this register, see [por_mxp_pmu_event_sel on page 4-677](#).

The following table shows a summary of the XP PMU events.

Table 7-14 XP PMU event summary

Number	Name	Description
1	PMU_XP_TXFLIT_VALID	<p>Number of flits transmitted on a specified port and CHI channel. This is a measure of the flit transfer bandwidth from an XP.</p> <p>———— Note ————</p> <p>On device ports, this event also includes link flit transfers.</p> <p>————</p>
2	PMU_XP_TXFLIT_STALL	<p>Number of cycles when a flit is stalled at an XP waiting for link credits at a specified port and CHI channel. This is a measure of the flit traffic congestion on the mesh and at the flit download ports.</p>
3	PMU_XP_PARTIAL_DAT_FLIT_VALID	<p>Number of times when a partial DAT flit is uploaded on to the mesh from a RN-F_CHIA port. Partial DAT flit transmission occurs when XP is not able to combine two 128b DAT flits and send them over the 256b DAT channel. This can happen under 2 circumstances:</p> <ol style="list-style-type: none"> 1. Only one 128b DAT flit is received within a transmission time window. 2. Two 128b DAT flits are received but they are not two halves of a single 256b word.

7.9 Occupancy and lifetime measurement using PMU events

CMN-600AE has PMU events to measure the average occupancy of a tracker and measure the average lifetime of the requests in that tracker.

This event is implemented for many of the trackers in CMN-600AE units (HN-F, RN-I, RN-D, HN-I, and others). The following formula measures the average occupancy and lifetime and can be applied to all the trackers where this event is supported:

Occupancy measurement

The formula to measure the occupancy is:

$$\text{Average Occupancy (entries)} = \frac{\text{PMU_OCCUPANCY_EVENT} \ll 8}{\text{PMU_CYCLE_COUNTER}}$$

Figure 7-15 Average occupancy

For example, for RN-I RRT average occupancy, the formula is:

$$\text{Average RRT Occupancy (entries)} = \frac{\text{PMU_RNI_RRT_OCCUPANCY_EVENT} \ll 8}{\text{PMU_CYCLE_COUNTER}}$$

Figure 7-16 Average RRT occupancy

Lifetime measurement

If a tracker supports lifetime event, the formula to measure the lifetime is:

$$\text{Average Lifetime (cycles)} = \frac{\text{PMU_OCCUPANCY_EVENT} \ll 8}{\text{PMU_NUM_TRACKER_ALLOCATIONS}}$$

Figure 7-17 Average lifetime

For example, for RN-I RRT average lifetime, the formula is:

$$\text{Average Lifetime (cycles)} = \frac{\text{PMU_RNI_RRT_OCCUPANCY} \ll 8}{\text{PMU_RNI_RRTALLOC}}$$

Figure 7-18 Average RRT lifetime

7.10 DEVEVENT

CMN-600AE HN-Fs support device-specific events that are collectively called DEVEVENT. These events are sent along with the completion of a transaction.

The completion of a transaction can be a data response (DAT) or completion response (RSP). These events contain information regarding the transaction encountering an SLC hit or miss. The events also include information about snoops sent to resolve coherency actions. You can measure these events using watchpoints on the XP that the RN-F is connected to. Refer to [6.1.1 DTM watchpoint on page 6-1870](#) for watchpoint usage.

The following table describes the DEVEVENT encodings from HN-F.

Table 7-15 DEVEVENT encodings from HN-F

Encoding	Description
2'b00	Line missed in SLC and no snoops sent
2'b01	Line missed in SLC and directed snoop sent
2'b10	Line missed in SLC and broadcast snoops sent
2'b11	Line hit in SLC and no snoops sent

Other CMN-600AE device responses have the default 2'b00 encoding as the DEVEVENT value.

Appendix A

Signal descriptions

This section describes the CMN-600AE I/O signals.

It contains the following sections:

- *A.1 About the signal descriptions* on page Appx-A-1921.
- *A.2 Clock and reset signals* on page Appx-A-1922.
- *A.3 Clock management signals* on page Appx-A-1923.
- *A.4 Power management signals* on page Appx-A-1926.
- *A.5 Interrupt and event signals* on page Appx-A-1928.
- *A.6 Configuration input signals* on page Appx-A-1929.
- *A.7 Device population signals* on page Appx-A-1930.
- *A.8 CHI interface signals* on page Appx-A-1931.
- *A.9 AXI and ACE-Lite interface signals* on page Appx-A-1937.
- *A.10 CGL interface signals* on page Appx-A-1947.
- *A.11 Debug, trace, and PMU interface signals* on page Appx-A-1954.
- *A.12 DFT and MBIST interface signals* on page Appx-A-1956.
- *A.13 Processor event interface signals* on page Appx-A-1958.
- *A.14 AXI4-Stream interface signals* on page Appx-A-1959.
- *A.15 FMU interface signals* on page Appx-A-1961.
- *A.16 APB interface signals* on page Appx-A-1962.

A.1 About the signal descriptions

CMN-600AE signals are composed of a base name along with identifiers that indicate unique product configuration.

Because there are multiple identical interfaces in CMN-600AE, the signal names that this appendix describes are only root names, in many cases. The actual signal name includes a port-specific identifier suffix. The system configuration determines which of the signals that this appendix describes are used in a particular system.

Note

Check signals, when present at safe interfaces, have inverse polarity relative to the associated primary signal unless stated otherwise.

A.2 Clock and reset signals

The following table shows the CMN-600AE clock and reset signals.

Table A-1 CMN-600AE clock and reset signals

Signal	Check signal	Type	Description	Connection information
GCLK0	GCLK0CHK	Input	Primary CMN-600AE clock input.	Connect to global clock for CMN-600AE.
nSRESET	nSRESETCHK	Input	CMN-600AE reset, active-LOW.	Connect to global reset for CMN-600AE. ———— Note ———— nSRESETCHK has the same polarity as nSRESET . ————
nFMURESET	nFMURESETCHK	Input	CMN-600AE reset, active-LOW.	Connect to global FMU reset for CMN-600AE. ———— Note ———— nFMURESETCHK has the same polarity as nFMURESET . ————

A.3 Clock management signals

This section contains information on clock management signals.

The following table shows the CMN-600AE clock management signals.

Table A-2 CMN-600AE clock management signals

Signal	Check signal	Type	Description	Connection information
QACTIVE_CLKCTL	QACTIVECHK_CLKCTL	Output	Indication that CMN-600AE is active, and that the <i>External Clock Controller</i> (ExtCC) must not make a request for CMN-600AE to prepare to stop the clocks.	Connect to ExtCC.
QREQN_CLKCTL	QREQCHK_CLKCTL	Input	Request from the ExtCC for the CMN-600AE to prepare to stop the clocks.	Connect to ExtCC or tie HIGH if unused.
QACCEPTN_CLKCTL	QACCEPTCHK_CLKCTL	Output	Positive acknowledgment after receiving QREQN assertion indicating that CMN-600AE has completed preparation to stop the clocks and that the ExtCC can stop the clocks.	Connect to ExtCC.
QDENY_CLKCTL	QDENYCHK_CLKCTL	Output	Negative acknowledgment after receiving QREQN assertion indicating that CMN-600AE has refused the request from the ExtCC to prepare to stop the clocks.	

The following table shows the clock management signals for CML configurations.

Table A-3 Additional clock management signals for CML configurations

Signal	Check signal	Type	Description	Connection information
QACTIVE_CGLCLKCTL	QACTIVECHK_CGLCLKCTL	Output	Indication that the CGL side of CMN-600AE is active, and that the ExtCC must not make a request for CMN-600AE and corresponding CXG device to prepare to stop the clocks.	OR with QACTIVE_CGLCLKCTL (CXLA) and connect to ExtCC.
QREQN_CGLCLKCTL	QREQCHK_CGLCLKCTL	Input	Request from the ExtCC for the CMN-600AE to prepare to stop the clock CLK_CGL.	Connect to ExtCC or tie HIGH if unused.

Table A-3 Additional clock management signals for CML configurations (continued)

Signal	Check signal	Type	Description	Connection information
QACCEPTN_CGLCLKCTL	QACCEPTCHK_CGLCLKCTL	Output	Positive acknowledgment after receiving QREQN assertion indicating that CMN-600AE has completed preparation to stop the clock CLK_CGL and that the ExtCC can stop the clock CLK_CGL.	Connect to ExtCC.
QDENY_CGLCLKCTL	QDENYCHK_CGLCLKCTL	Output	Negative acknowledgment after receiving QREQN assertion indicating that CMN-600AE has refused the request from the ExtCC to prepare to stop the clock CLK_CGL.	

The following table shows the clock management signals for CDB.

Table A-4 Additional clock management signals for CDB

Signal	Check signal	Type	Description	Connection information
CLK_QACTIVE_ICN	CLK_QACTIVECHK_ICN	Output	Indication that the interconnect side of the domain bridge is active, and if the CMN-600AE is in the Q_STOPPED state, the ExtCC should bring it out of the Q_STOPPED state.	OR with QACTIVE_CLKCTL and connect to the ExtCC.
CLK_QACTIVE_DEV	CLK_QACTIVECHK_DEV	Output	Indication that the device side of the domain bridge is active, and if the CMN-600AE is in the Q_STOPPED state, the ExtCC should bring it out of the Q_STOPPED state.	OR with the QACTIVE signal that belongs to the device and connect to the ExtCC.

The following table shows the clock management signals for ADB.

Table A-5 Additional clock management signals for ADB

Signal	Check signal	Type	Description	Connection information
CLK_QACTIVE_M	CLK_QACTIVECHK_M	Output	Indication that the master side of the domain bridge is active, and that if the CMN-600AE is in the Q_STOPPED state, the ExtCC should bring the master out of the Q_STOPPED state.	OR with the QACTIVE signal that belongs to the slave and connect to the ExtCC.
CLK_QACTIVE_S	CLK_QACTIVECHK_S	Output	Indication that the slave side of the domain bridge is active, and if the device is in the Q_STOPPED state, the ExtCC should bring the slave out of the Q_STOPPED state.	OR with the QACTIVE signal that belongs to the master and connect to the ExtCC.

A.4 Power management signals

This section contains information on power management signals.

The following table shows the power management signals for the logic power domain.

Table A-6 Power management signals for logic power domain

Signal	Check signal	Type	Description	Connection information
PREQ_LOGIC	PREQCHK_LOGIC	Input	Indicates a request for a power state transition.	Connect to External Power Management Controller or tie LOW if unused.
PSTATE_LOGIC[4:0]	PSTATECHK_LOGIC	Input	The power state to which a transition is requested. ^c	Connect to External Power Management Controller or tie to 5'b01000 if unused. ————— Note ————— PSTATECHK_LOGIC is the Odd parity bit of PSTATE_LOGIC[4:0] . —————
PACCEPT_LOGIC	PACCEPTCHK_LOGIC	Output	Indicates acknowledgment of the power state transition and completion of the power state transition within the CMN-600AE.	Connect to External Power Management Controller.
PDENY_LOGIC	PDENYCHK_LOGIC	Output	Indicates denial of the power state transition.	
PACTIVE_LOGIC	PACTIVECHK_LOGIC	Output	Hint that indicates activity across the CMN-600AE. When LOW, indicates the possibility of entering static retention or the OFF state.	

————— **Restriction** —————

The system cannot be powered down if **PACTIVE_LOGIC** is asserted.

The following table shows the power management signals for the CDB.

^c If *MultiCycle Path* (MCP), the MCP duration must be no more than eight cycles to the last flop to receive this signal. This is a requirement for implementation.

Table A-7 Additional power management signals for CDB

Signal	Check signal	Type	Description	Connection information
PWR_QREQN_DEV	PWR_QREQCHK_DEV	Input	Indicates a request for the domain bridge to enter a power-off state.	Connect to External Power Management Controller.
PWR_QACTIVE_DEV	PWR_QACTIVECHK_DEV	Output	Indication that there is activity in the domain bridge, and that the ExtCC must not make a request for the domain bridge device to prepare to power down.	
PWR_QACCEPTN_DEV	PWR_QACCEPTCHK_DEV	Output	Indicates an acknowledgement and completion of the power state transition inside the domain bridge.	
PWR_QDENY_DEV	PWR_QDENYCHK_DEV	Output	Indicates a denial of the power state transition.	

The following table shows the power management signals for the ADB.

Table A-8 Additional power management signals for ADB

Signal	Check signal	Type	Description	Connection information
PWR_QREQN_<M/S>	PWR_QREQCHK_<M/S>	Input	Indicates a request for the domain bridge to enter a power-off state.	Connect to External Power Management Controller.
PWR_QACTIVE_<M/S>	PWR_QACTIVECHK_<M/S>	Output	Indication that there is activity in the domain bridge, and that ExtCC must not make a request for the domain bridge device to prepare to power down.	
PWR_QACCEPTN_<M/S>	PWR_QACCEPTNCHK_<M/S>	Output	Indicates an acknowledgement and completion of the power state transition inside the domain bridge.	
PWR_QDENY_<M/S>	PWR_QDENYCHK_<M/S>	Output	Indicates a denial of the power state transition.	

A.5 Interrupt and event signals

The following table shows the interrupt and event signals.

————— **Note** —————

All signal names in this section are only a root name that is indicated as **RootName**. CMN-600AE interfaces use **RootName** within a more fully specified signal name as follows:

CMN-600AE interface signal name == **RootName_NID#**, where # represents the node ID corresponding to the specific interface.

Table A-9 Interrupt and event signals

Signal	Check signal	Type	Description	Connection information
INTREQPPU	INTREQPPUCHK	Output	Power state transition complete.	Connect to external interrupt control logic or Generic Interrupt Controller. ————— Note ————— There is no check signal for INTREQPMU .
INTREQPMU	-	Output	PMU count overflow interrupt. NID indicates node ID where <x> represents the NodeID number for that HN-D/DTC or HN-T/DTC.	
INTREQERRNS	INTREQERRNSCHK	Output	Non-secure error handling interrupt.	
INTREQERRS	INTREQERRSCHK	Output	Secure error handling interrupt.	
INTREQFAULTNS	INTREQFAULTNSCHK	Output	Non-secure fault handling interrupt.	
INTREQFAULTS	INTREQFAULTSCHK	Output	Secure fault handling interrupt.	

A.6 Configuration input signals

The following table shows the configuration input signals.

All of these signals must be stable at least ten cycles before deassertion of reset and must remain stable throughout the operation of the CMN-600AE, until a following reset assertion or power down, if any.

Table A-10 General configuration input signals

Signal	Check signal	Type	Description	Connection information
CFGM_PERIPHBASE[21:0]	CFGM_PERIPHBASECHK[21:0]	Input	Base address [21:0] of the CMN-600AE configuration register space	Tie as required for system memory map.
GCID_DESTID[15:0]	GCID_DESTIDCHK[15:0]	Input	PUB Destination ID corresponding to the A4S port to which the local GIC is connected.	

A.7 Device population signals

The following table shows the RN-D ACE-Lite-with-DVM device population signals.

These signals are present only when CMN-600AE has been configured to include the relevant RN-D bridge.

Table A-11 RN-D ACE-Lite-with-DVM device population signals

Signal	Check signal	Type	Description	Connection information
ACCHANNELEN_S0_NID<x>	ACCHANNELENCHK_S0_NID<x>	Input	Indicates that the RN-D bridge at NodeID <x> is populated and AMBA slave port 0 for NodeID <x> is of type ACE-Lite-with-DVM and includes a device which responds to DVM messages on the AC channel. 0 DVM-capable device is not populated. 1 DVM-capable device is populated.	Tie as required for system configuration.
ACCHANNELEN_S1_NID<x>	ACCHANNELENCHK_S1_NID<x>	Input	Indicates that the RN-D bridge at NodeID <x> is populated and AMBA slave port 1 for NodeID <x> is of type ACE-Lite-with-DVM and includes a device which responds to DVM messages on the AC channel. 0 DVM-capable device is not populated. 1 DVM-capable device is populated.	
ACCHANNELEN_S2_NID<x>	ACCHANNELENCHK_S2_NID<x>	Input	Indicates that the RN-I bridge at NodeID <x> is populated and AMBA slave port 2 for NodeID <x> is of type ACE-Lite-with-DVM and includes a device which responds to DVM messages on the AC channel. 0 DVM-capable device is not populated. 1 DVM-capable device is populated.	

A.8 CHI interface signals

CMN-600AE uses channels that form an inbound and outbound CHI interface for each device using signals that form each channel in a specific interface.

The *Arm AMBA® 5 CHI Architecture Specification* defines four channels:

- *Request* (REQ).
- *Response* (RSP).
- *Snoop* (SNP).
- *Data* (DAT).

Note

All signal names in this section are only a root name, **RootName**. CMN-600AE interfaces use **RootName** within a more fully specified signal name as follows:

- CMN-600AE interface signal name == **RootName_NID#**, where # is the node ID corresponding to the specific interface.
- When a CHI safe interface is disabled, the corresponding check signals are removed from the interface, except where noted.

This section contains the following subsections:

- [A.8.1 Per-device interface definition on page Appx-A-1931.](#)
- [A.8.2 Per-channel interface signals on page Appx-A-1932.](#)
- [A.8.3 Non-channel-specific interface signals on page Appx-A-1935.](#)

A.8.1 Per-device interface definition

Each CHI device included in a CMN-600AE system has distinct functionality, and the requirements and configuration of its respective CHI interfaces differ.

The requirements and configuration for the CHI interfaces are as follows:

External RN-F interface

The RN-F interface consists of a request channel, snoop channel, and two response channels, one in each direction, as the following figure shows.

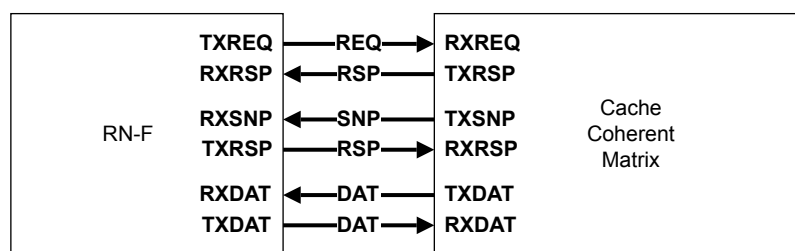


Figure A-1 External RN-F interface

It also has two data channels, one in each direction, for data transfers. CMN-600AE receives request messages from the RN-F and sends responses to it. In addition, CMN-600AE sends snoop messages to the RN-F and receives snoop response messages.

External SN-F interface

The SN-F interface consists of a request channel and a response channel as the following figure shows.

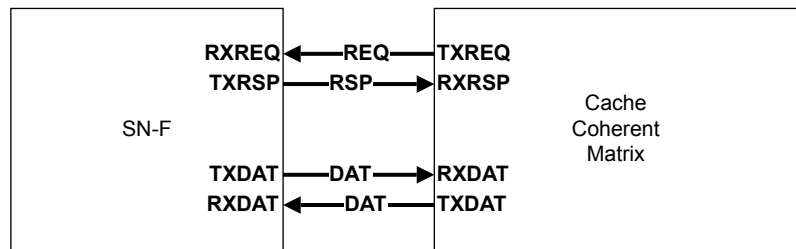


Figure A-2 External SN-F interface

It also has two data channels, one in each direction, for data transfers. The SN-F receives request messages from CMN-600AE and returns response messages.

A.8.2 Per-channel interface signals

For communication between devices, each channel includes a *Transmit* (TX) and a *Receive* (RX) port, with various interface signals traveling from TX to RX.

Note

Connection of CHI interfaces between two devices requires cross-coupling of the **TX*** and **RX*** signals between the two devices, as required by the CHI architecture.

The following table shows the Transmit Request channel signals.

Table A-12 Transmit Request channel signals

Signal	Check signal	Type	Description	Connection information
TXREQFLITPEND	TXREQFLITPENDCHK	Output	Transmit Request Early Flit Valid hint.	Connect to RXREQFLITPEND and RXREQFLITPENDCHK of the corresponding CHI device, if populated.
TXREQFLITV	TXREQFLITVCHK	Output	Transmit Request Flit Valid.	Connect to RXREQFLITV and RXREQFLITVCHK of the corresponding CHI device, if populated.
TXREQFLIT[n:0] ^d	TXREQFLITCHK[m:0] ^e	Output	Transmit Request Flit.	Connect to RXREQFLIT and RXREQFLITCHK of the corresponding CHI device, if populated.
TXREQLCRDV	TXREQLCRDVCHK	Input	Transmit Request channel link layer credit.	Connect to RXREQLCRDV and RXREQLCRDVCHK of the corresponding CHI device, if populated, otherwise tie LOW.

The following table shows the Transmit Response channel signals.

^d The value of n is configuration-dependent.
^e $m = \text{ceil}((n+1)/8) - 1$.

Table A-13 Transmit Response channel signals

Signal	Check signal	Type	Description	Connection information
TXRSPFLITPEND	TXRSPFLITPENDCHK	Output	Transmit Response Early Flit Valid hint.	Connect to RXRSPFLITPEND and RXRSPFLITPENDCHK of the corresponding CHI device, if populated.
TXRSPFLITV	TXRSPFLITVCHK	Output	Transmit Response Flit Valid.	Connect to RXRSPFLITV and RXRSPFLITVCHK of the corresponding CHI device, if populated.
TXRSPFLIT[n:0]^d	TXRSPFLITCHK[m:0]^e	Output	Transmit Response Flit.	Connect to RXRSPFLIT and RXRSPFLIT of the corresponding CHI device, if populated.
TXRSPLCRDV	TXRSPLCRDVCHK	Input	Transmit Response channel link layer credit.	Connect to RXRSPLCRDV and RXRSPLCRDV of the corresponding CHI device, if populated, otherwise tie LOW.

The following table shows the Transmit Snoop channel signals.

Table A-14 Transmit Snoop channel signals

Signal	Check signal	Type	Description	Connection information
TXSNPFLITPEND	TXSNPFLITPENDCHK	Output	Transmit Snoop Early Flit Valid hint.	Connect to RXSNPFLITPEND and TXSNPFLITPENDCHK of the corresponding CHI device, if populated.
TXSNPFLITV	TXSNPFLITVCHK	Output	Transmit Snoop Flit Valid.	Connect to RXSNPFLITV and TXSNPFLITVCHK of the corresponding CHI device, if populated.
TXSNPFLIT[n:0]^d	TXSNPFLITCHK[m:0]^e	Output	Transmit Snoop Flit.	Connect to RXSNPFLIT and RXSNPFLITCHK of the corresponding CHI device, if populated.
TXSNPLCRDV	TXSNPLCRDVCHK	Input	Transmit Snoop channel link layer credit.	Connect to RXSNPLCRDV and RXSNPLCRDVCHK of the corresponding CHI device, if populated, otherwise tie LOW.

The following table shows the Transmit Data channel signals.

Table A-15 Transmit Data channel signals

Signal	Check signal	Type	Description	Connection information
TXDATFLITPEND	TXDATFLITPENDCHK	Output	Transmit Data Early Flit Valid hint.	Connect to RXDATFLITPEND of the corresponding CHI device, if populated.
TXDATFLITV	TXDATFLITVCHK	Output	Transmit Data Flit Valid.	Connect to RXDATFLITV of the corresponding CHI device, if populated.
TXDATFLIT[n:0]^d	TXDATFLITCHK[m:0]	Output	Transmit Data Flit.	Connect to RXDATFLIT of the corresponding CHI device, if populated.
TXDATLCRDV	TXDATLCRDVCHK	Input	Transmit Data channel link layer credit.	Connect to RXDATLCRDV of the corresponding CHI device, if populated, otherwise tie LOW.

The following table shows the Receive Request channel signals.

^f The value of m is configuration-dependent.

Table A-16 Receive Request channel signals

Signal	Check signal	Type	Description	Connection information
RXREQFLITPEND	RXREQFLITPENDCHK	Input	Receive Request Early Flit Valid hint.	Connect to TXREQFLITPEND of the corresponding CHI device, if populated, otherwise tie LOW.
RXREQFLITV	RXREQFLITVCHK	Input	Receive Request Flit Valid.	Connect to TXREQFLITV of the corresponding processor, if populated, otherwise tie LOW.
RXREQFLIT[n:0]^d	RXREQFLITCHK[m:0]^f	Input	Receive Request Flit.	Connect to TXREQFLIT of the corresponding CHI device, if populated, otherwise tie LOW.
RXREQLCRDV	RXREQLCRDVCHK	Output	Receive Request channel link layer credit.	Connect to TXREQLCRDV of the corresponding CHI device, if populated.

The following table shows the Receive Response channel signals.

Table A-17 Receive Response channel signals

Signal	Check signal	Type	Description	Connection information
RXRSPFLITPEND	RXRSPFLITPENDCHK	Input	Receive Response Early Flit Valid hint.	Connect to TXRSPFLITPEND of the corresponding CHI device, if populated, otherwise tie LOW.
RXRSPFLITV	RXRSPFLITVCHK	Input	Receive Response Flit Valid.	Connect to TXRSPFLITV of the corresponding processor, if populated, otherwise tie LOW.
RXRSPFLIT[n:0]^d	RXRSPFLITCHK[m:0]^f	Input	Receive Response Flit.	Connect to TXRSPFLIT of the corresponding CHI device, if populated, otherwise tie LOW.
RXRSPLCRDV	RXRSPLCRDVCHK	Output	Receive Response channel link layer credit.	Connect to TXRSPLCRDV of the corresponding CHI device, if populated.

The following table shows the Receive Snoop channel signals.

Table A-18 Receive Snoop channel signals

Signal	Check signal	Type	Description	Connection information
RXSNPFLITPEND	RXSNPFLITPENDCHK	Input	Receive Snoop Early Flit Valid hint.	Connect to TXSNPFLITPEND of the corresponding CHI device, if populated, otherwise tie LOW.
RXSNPFLITV	RXSNPFLITVCHK	Input	Receive Snoop Flit Valid.	Connect to TXSNPFLITV of the corresponding processor, if populated, otherwise tie LOW.
RXSNPFLIT[n:0]^d	RXSNPFLITCHK[m:0]^f	Input	Receive Snoop Flit.	Connect to TXSNPFLIT of the corresponding CHI device, if populated, otherwise tie LOW.
RXSNPLCRDV	RXSNPLCRDVCHK	Output	Receive Snoop channel link layer credit.	Connect to TXSNPLCRDV of the corresponding CHI device, if populated.

The following table shows the Receive Data channel signals.

Table A-19 Receive Data channel signals

Signal	Check signal	Type	Description	Connection information
RXDATFLITPEND	RXDATFLITPENDCHK	Input	Receive Data Early Flit Valid hint.	Connect to TXDATFLITPEND of the corresponding CHI device, if populated, otherwise tie LOW.
RXDATFLITV	RXDATFLITVCHK	Input	Receive Data Flit Valid.	Connect to TXDATFLITV of the corresponding processor, if populated, otherwise tie LOW.
RXDATFLIT[n:0]^d	RXDATFLITCHK[m:0]^f	Input	Receive Data Flit.	Connect to TXDATFLIT of the corresponding CHI device, if populated, otherwise tie LOW.
RXDATLCRDV	RXDATLCRDVCHK	Output	Receive Data channel link layer credit.	Connect to TXDATLCRDV of the corresponding CHI device, if populated.

A.8.3 Non-channel-specific interface signals

Every transmit and receive link layer interface includes additional signals that exist only at the interface level and are not channel specific.

The following table shows the LinkActive interface signals.

Table A-20 Receive LinkActive interface signals

Signal	Check signal	Type	Description	Connection information
RXLINKACTIVEREQ	RXLINKACTIVEREQCHK	Input	Receive channel LinkActive request from adjacent transmitter device	Connect to TXLINKACTIVEREQ of the corresponding CHI device, if populated, otherwise tie LOW.
RXLINKACTIVEACK	RXLINKACTIVEACKCHK	Output	Receive channel LinkActive acknowledgment to adjacent transmitter device	Connect to TXLINKACTIVEACK of the corresponding CHI device, if populated.
TXLINKACTIVEREQ	TXLINKACTIVEREQCHK	Output	Transmit channel LinkActive request to adjacent receiver device	Connect to RXLINKACTIVEREQ of the corresponding CHI device, if populated.
TXLINKACTIVEACK	TXLINKACTIVEACKCHK	Input	Transmit channel LinkActive acknowledgment from adjacent receiver device	Connect to RXLINKACTIVEACK of the corresponding CHI device, if populated, otherwise tie LOW.

The following table shows the Sactive interface signals.

Table A-21 Sactive interface signals

Signal	Check signal	Type	Description	Connection information
RXSACTIVE	RXSACTIVECHK	Input	Indication from the adjacent CHI device that it has one or more outstanding protocol-layer transactions. RXSACTIVE must remain asserted throughout the lifetime of the transaction.	Connect to TXSACTIVE of the corresponding CHI device.
TXSACTIVE	TXSACTIVECHK	Output	Indication to the adjacent CHI device that CMN-600AE has one or more outstanding protocol-layer transactions. TXSACTIVE remains asserted throughout the lifetime of the transaction.	Connect to RXSACTIVE of the corresponding CHI device.

The following table shows the hardware coherency interface signals.

Table A-22 Hardware coherency interface signals

Signal	Check signal	Type	Description	Connection information
SYSCOREQ	SYSCOREQCHK	Input	Request to enter CHI coherence domain when asserted and to exit the CHI coherence domain when deasserted. SYSCOREQ and SYSCOACK implement a four-phase handshake protocol.	Connect to SYSCOREQ of corresponding CHI device, if populated, otherwise tie LOW.
SYSCOACK	SYSCOACKCHK	Output	Acknowledge CHI coherence domain entry/exit request	Connect to SYSCOACK of corresponding CHI device, if populated.

A.9 AXI and ACE-Lite interface signals

All AXI and ACE-Lite interface signal names contain a RootName, which is used within a fully specified signal name.

The fully specified signal name is **RootName_[S|M][#a]_NID#b**, where:

S|M Indicates either a slave or master interface.

#a Defines an optional interface identifier for a node that can support multiple AMBA interfaces.

#b Defines the node ID corresponding to the specific interface.

Multi-bit signals append the bit-range identifier that is included in the RootName to the end of the full signal name.

Note

Unless stated otherwise, the corresponding check signals are removed from the interface when the AXI/ACE-Lite safe interface is disabled.

This section contains the following subsections:

- [A.9.1 ACE-Lite-with-DVM slave interface signals on page Appx-A-1937.](#)
- [A.9.2 AXI/ACE-Lite master interface signals on page Appx-A-1942.](#)

A.9.1 ACE-Lite-with-DVM slave interface signals

This interface is present as the ACE-Lite-with-DVM slave port for an RN-D bridge. The signal descriptions show which signals specific to DVM functionality are not present in an ACE-Lite interface without DVM.

The following table shows the clock and power management signals.

Table A-23 Clock and power management signals

Signal	Check signal	Type	Description	Connection information
ACLKEN_S	ACLKENCHK_S	Input	AXI bus clock enable.	Connect to clock enable logic. Tie HIGH if RN-I port is unused.
ACWAKEUP_S	ACWAKEUPCHK_S	Output	Indication that the interconnect is starting a transaction that is being sent to the DVM master (SMMU).	Connect to corresponding master device, if populated.
AWAKEUP_S	AWAKEUPCHK_S	Input	Indication that the master is starting a transaction that is being sent to the interconnect.	Connect to corresponding master device, if populated, otherwise tie LOW.
RNID_SAM_STALL_DIS	RNID_SAM_STALL_DISCHK	Input	Disables RN SAM programming stall for specified RN.	Tie HIGH if boot programming, including RN SAM, is done through this RN-I port. Otherwise, tie LOW.

Table A-23 Clock and power management signals (continued)

Signal	Check signal	Type	Description	Connection information
SYSCOREQ_S	SYSCOREQCHK_S	Input	Request to enter DVM domain when asserted and to exit the DVM domain when deasserted. SYSCOREQ and SYSCOACK implement a four-phase handshake protocol.	Connect to corresponding master device. Tie LOW if master is not populated or does have port.
SYSCOACK_S	SYSCOACKCHK_S	Output	Acknowledge for DVM domain entry or exit.	Connect to corresponding master device, if populated.

The following table shows the slave interface Write Address Channel signals.

Table A-24 Slave interface Write Address Channel signals

Signal	Check signal	Type	Description	Connection information
AWREADY_S	AWREADYCHK_S	Output	Write address ready.	Connect to corresponding master device, if populated.
AWVALID_S	AWVALIDCHK_S	Input	Write address valid.	Connect to corresponding master device, if populated, otherwise tie LOW.
AWID_S[10:0]	AWIDCHK_S[1:0]	Input	Write address ID.	
AWADDR_S[n:0]^g	AWADDRCHK_S[m:0]^h	Input	Write address.	
AWLEN_S[7:0]	AWLENCHK_S	Input	Write burst length.	
AWSIZE_S[2:0]	AWCTLCHK0_S	Input	Write burst size.	
AWBURST_S[1:0]		Input	Write burst type.	
AWLOCK_S		Input	Write lock type.	
AWPROT_S[2:0]		Input	Write protection type.	
AWCACHE_S[3:0]	AWCTLCHK1_S	Input	Write memory type.	
AWQOS_S[3:0]		Input	Write QoS identifier.	
AWSNOOP_S[3:0]	AWCTLCHK2_S	Input	Write transaction type.	
AWDOMAIN_S[1:0]		Input	Write shareability domain.	
AWATOP_S[5:0]	AWCTLCHK3_S	Input	Atomic operation.	Tie LOW.

^g The value of n is configuration-dependent.

^h The value of m = $\text{ceil}((n + 1)/8) - 1$.

Table A-24 Slave interface Write Address Channel signals (continued)

Signal	Check signal	Type	Description	Connection information
AWUSER_S[n:0]^g	AWUSERCHK_S[m:0]^h	Input. ⁱ	User-defined signal.	Connect to corresponding master device, if populated, otherwise tie LOW.
AWSTASHNID_S[10:0]	AWSTASHNIDCHK_S	Input	Indicates the node identifier of the physical interface that is the target interface for the cache stash operation.	
AWSTASHNIDEN_S		Input	When asserted, indicates that the AWSTASHNID signal is valid and should be used.	
AWSTASHLPID_S[4:0]	AWSTASHLPIDCHK_S	Input	Indicates the logical processor sub-unit that is associated with the physical interface that is the target for the cache stash operation.	
AWSTASHLPIDEN_S		Input	When asserted, indicates that the AWSTASHLPID signal is enabled and should be used.	
AWTRACE_S	AWTRACECHK_S	Input	Trace signal that is associated with the AW Write Address channel.	

The following table shows the slave interface Write Data Channel signals.

Table A-25 Slave interface Write Data Channel signals

Signal	Check signal	Type	Description	Connection information
WREADY_S	WREADYCHK_S	Output	Write data ready.	Connect to corresponding master device, if populated.
WVALID_S	WVALIDCHK_S	Input	Write data valid.	Connect to corresponding master device, if populated, otherwise tie LOW.
WDATA_S[n:0]^j	WDATACHK_S[m:0]^k	Input	Write data.	
WSTRB_S[m:0]^k	WSTRBCHK_S[e:0]^l	Input	Write byte lane strobes.	
WLAST_S	WLASTCHK_S	Input	Write data last transfer indication.	
WUSER_S[0:0]	WUSERCHK_S[0:0]	Input	User signal that is associated with the Write Data channel.	
WTRACE_S	WTRACECHK_S	Input	Trace signal that is associated with the Write Data channel.	
WPOISON_S[p:0]^m	WPOISONCHK_S[q:0]ⁿ	Input	Poison signal that is associated with the W Write Data channel.	

ⁱ If REQ_RSVD_WIDTH == 0, n = 3. Otherwise, n = REQ_RSVD_WIDTH - 1.

^j The value of n is configuration-dependent.

^k The value of m = ceil((n + 1)/8) - 1.

^l The value of e = ceil((d + 1)/8) - 1.

^m The value of p = ceil((n + 1)/64) - 1, where n + 1 = width of **WDATA**.

ⁿ The value of q = ceil((p + 1)/8) - 1.

The following table shows the slave interface Write Response Channel signals.

Table A-26 Slave interface Write Response Channel signals

Signal	Check signal	Type	Description	Connection information
BREADY_S	BREADYCHK_S	Input	Write response ready.	Connect to corresponding master device, if populated, otherwise tie LOW.
BVALID_S	BVALIDCHK_S	Output	Write response valid.	
BID_S[10:0]	BIDCHK_S[1:0]	Output	Write response ID.	
BRESP_S[1:0]	BRESPCHK_S	Output	Write response.	
BUSER_S[3:0]	BUSERCHK_S	Output	User response signal.	
BTRACE_S	BTRACECHK_S	Output	Trace signal that is associated with the Write Response channel.	

The following table shows the slave interface Read Address Channel signals.

Table A-27 Slave interface Read Address Channel signals

Signal	Check signal	Type	Description	Connection information
ARREADY_S	ARREADYCHK_S	Output	Read address ready.	Connect to corresponding master device, if populated.
ARVALID_S	ARVALIDCHK_S	Input	Read address valid.	
ARID_S[10:0]	ARID_S[1:0]	Input	Read address ID.	Connect to corresponding master device, if populated, otherwise tie LOW.
ARADDR_S[n:0] ^o	ARADDRCHK_S[m:0] ^p	Input	Read address.	
ARLEN_S[7:0]	ARLENCHK_S	Input	Read burst length.	
ARSIZE_S[2:0]	ARCTLCHK0_S	Input	Read burst size.	
ARBURST_S[1:0]		Input	Read burst type.	
ARLOCK_S		Input	Read lock type.	
ARPROT_S[2:0]		Input	Read protection type.	
ARCACHE_S[3:0]	ARCTLCHK1_S	Input	Read cache type.	
ARQOS_S[3:0]		Input	Read QoS value.	
ARSNOOP_S[3:0]	ARCTLCHK2_S	Input	Read transaction type.	
ARDOMAIN_S[1:0]		Input	Read shareability domain.	
ARUSER_S[n:0] ^o	ARUSERCHK_S[m:0] ^o	Input. ⁱ	User-defined signal.	
ARTRACE_S	ARTRACECHK_S	Input	Trace signal that is associated with the Read Address channel.	

The following table shows the slave interface Read Data Channel signals.

^o The value of n is configuration-dependent.
^p The value of m = $\text{ceil}((n + 1)/8) - 1$.

Table A-28 Slave interface Read Data Channel signals

Signal	Check signal	Type	Description	Connection information
RREADY_S	RREADYCHK_S	Input	Read data ready.	Connect to corresponding master device, if populated, otherwise tie LOW.
RVALID_S	RVALIDCHK_S	Output	Read data valid.	Connect to corresponding master device, if populated.
RID_S[10:0]	RIDCHK_S[1:0]	Output	Read data ID.	
RDATA_S[n:0] ^q	RDATACHK_S[d:0] ^r	Output	Read data.	
RRESP_S[1:0]	RRESPCHK_S	Output	Read data response.	
RLAST_S	RLASTCHK_S	Output	Read data last transfer indication.	
RUSER_S	RUSERCHK_S	Output	User signal that is associated with the Read Data channel.	
RTRACE_S	RTRACECHK_S	Output	Trace signal that is associated with the Read Data channel.	
RPOISON_S[p-1:0] ^s	RPOISONCHK_S[q:0] ^t	Output	Poison signal that is associated with the Read Data channel.	

The following table shows the slave interface Snoop Address Channel signals. These signals are not included in an ACE-Lite interface without DVM.

Table A-29 Slave interface Snoop Address Channel signals

Signal	Check signal	Type	Description	Connection information
ACREADY_S	ACREADYCHK_S	Input	Snoop address ready.	Connect to corresponding master device, if populated, otherwise tie LOW.
ACVALID_S	ACVALIDCHK_S	Output	Snoop address valid.	Connect to corresponding master device, if populated.
ACADDR_S[n:0] ^u	ACADDRCHK_S[m:0] ^v	Output	Snoop address.	
ACSNOOP_S[3:0]	ACSNOOPCHK_S	Output	Snoop transaction type.	
ACPROT_S[2:0]	ACPROTCHK_S	Output	Snoop protection type.	
ACVMIDEXT_S[3:0]	ACVMIDEXTCHK_S	Output	Snoop address VMID extension.	
ACTRACE_S	ACTRACECHK_S	Output	Snoop address trace.	

The following table shows the slave interface Snoop Response Channel signals. These signals are not included in an ACE-Lite interface without DVM.

^q The value of n is configuration-dependent.
^r The value of d = $\text{ceil}((n + 1)/8) - 1$.
^s The value of p = $\text{ceil}((n + 1)/64) - 1$, where n + 1 is the width of WDATA.
^t The value of q = $\text{ceil}((p + 1)/8) - 1$.
^u The value of n is configuration-dependent.
^v The value of m = $\text{ceil}((n + 1)/8) - 1$.

Table A-30 Slave interface Snoop Response Channel signals

Signal	Check signal	Type	Description	Connection information
CRREADY_S	CRREADYCHK_S	Output	Snoop response ready.	Connect to corresponding master device, if populated.
CRVALID_S	CRVALIDCHK_S	Input	Snoop response valid.	Connect to corresponding master device, if populated, otherwise tie LOW.
CRRESP_S[4:0]	CRRESPCHK_S	Input	Snoop response.	
CRTRACE_S	CRTRACECHK_S	Input	Snoop response trace.	

Note

WUSER_S[0] acts as a **WDATACHK** valid signal when the **DATACHECK_EN** parameter is enabled.

- If **WUSER_S[0]** == 0, RN-I or RN-D synthesizes the correct **WDATACHK** value before sending it on CHI write request.
- If **WUSER_S[0]** == 1, RN-I or RN-D uses the **WDATACHK** pin value to drive on CHI write request.

The **WUSER_S[0]** input is ignored if **DATACHECK_EN** is not enabled.

Note

RUSER_S[0] acts as an **RDATACHK** valid signal. Because RN-I or RN-D always drives the **RDATACHK** value, **RUSER_S[0]** is set to 1 when **DATACHECK_EN** is enabled.

The **RUSER_S[0]** output is set to 0 if **DATACHECK_EN** is not enabled.

A.9.2 AXI/ACE-Lite master interface signals

HN-I and SBSX have an AXI/ACE-Lite master interface.

The following table shows the clock enable signal.

Table A-31 Clock enable signal

Signal	Check signal	Type	Description	Connection information
ACLKEN_M	ACLKENCHK_M	Input	AXI master bus clock enable.	Connect to clock-enable logic.
AWAKEUP_M	AWAKEUPCHK_M	Output	Indication that CMN-600AE is starting an AXI transaction.	Connect to corresponding slave device, if populated.

The following table shows the master interface Write Address Channel signals.

Table A-32 Master interface Write Address Channel signals

Signal	Check signal	Type	Description	Connection information
AWREADY_M	AWREADYCHK_M	Input	Write address ready.	Connect to corresponding slave device, if populated, otherwise tie LOW.
AWVALID_M	AWVALIDCHK_M	Output	Write address valid.	
AWID_M[10:0]	AWIDCHK_M[1:0]	Output	Write address ID.	
AWADDR_M[n:0] ^w	AWADDR_M[m:0] ^x	Output	Write address.	
AWLEN_M[7:0]	AWLENCHK_M	Output	Write burst length.	
AWSIZE_M[2:0]	AWCTLCHK0_M	Output	Write burst size.	
AWBURST_M[1:0]		Output	Write burst type.	
AWLOCK_M		Output	Write lock type.	
AWPROT_M[2:0]		Output	Write protection type.	
AWCACHE_M[3:0]	AWCTLCHK1_M	Output	Write cache type.	
AWQOS_M[3:0]		Output	Write QoS value.	
AWSNOOP_M[3:0]	AWCTLCHK2_M	Output	Shareable write transaction type.	
AWDOMAIN_M[1:0]		Output	Write shareability domain.	
AWUSER_M[n:0] ^w	AWUSERCHK_M[m:0] ^x	Output. ^y	User signal.	
AWTRACE_M	AWTRACECHK_M	Output	-	

The following table shows the master interface Write Data Channel signals.

^w The value of n is configuration-dependent.
^x The value of m = $\text{ceil}((n + 1)/8) - 1$.
^y If REQ_RSVD_WIDTH == 0, n = 3. Otherwise, n = REQ_RSVD_WIDTH - 1.

Table A-33 Master interface Write Data Channel signals

Signal	Check signal	Type	Description	Connection information
WREADY_M	WREADYCHK_M	Input	Write data ready.	Connect to corresponding slave device, if populated, otherwise tie LOW.
WVALID_M	WVALIDCHK_M	Output	Write data valid.	Connect to corresponding slave device, if populated.
WDATA_M [n:0] ^z	WDATACHK_M [d:0] ^{aa}	Output	Write data.	
WSTRB_M [d:0] ^{aa}	WSTRBCHK_M [e:0] ^{ab}	Output	Write byte lane strobes.	
WLAST_M	WLASTCHK_M	Output	Write data last transfer indication.	
WUSER_M [0:0]	WUSERCHK_M [0:0]	Output	User signal that is associated with the Write Data channel.	
WPOISON_M [p:0] ^{ac}	WPOISONCHK_M [q:0] ^{ad}	Output	Poison signal that is associated with the Write Data channel.	
WTRACE_M	WTRACECHK_M	Output	Trace signal that is associated with the Write Data channel.	

The following table shows the master interface Write Response Channel signals.

Table A-34 Master interface Write Response Channel signals

Signal	Check signal	Type	Description	Connection information
BREADY_M	BREADYCHK_M	Output	Write response ready.	Connect to corresponding slave device, if populated.
BVALID_M	BVALIDCHK_M	Input	Write response valid.	Connect to corresponding slave device, if populated, otherwise tie LOW.
BID_M [10:0]	BIDCHK_M [1:0]	Input	Write response ID.	
BRESP_M [1:0]	BRESPCHK_M	Input	Write response.	
BUSER_M [3:0]	BUSERCHK_M	Input	User signal.	
BTRACE_M	BTRACECHK_M	Input	-	

The following table shows the master interface Read Address Channel signals.

^z **WDATA** is configurable to 128 bits or 256 bits. **WSTRB** scales accordingly.
^{aa} The value of $d = \text{ceil}((n + 1)/8) - 1$, where $(n + 1)$ is the width of **WDATA**.
^{ab} The value of $e = \text{ceil}((d + 1)/8) - 1$.
^{ac} The value of $p = \text{ceil}((n + 1)/64) - 1$, where $(n + 1)$ is the width of **WDATA**.
^{ad} The value of $q = \text{ceil}((p + 1)/8) - 1$.

Table A-35 Master interface Read Address Channel signals

Signal	Check signal	Type	Description	Connection information
ARREADY_M	ARREADYCHK_M	Input	Read address ready.	Connect to corresponding slave device, if populated, otherwise tie LOW.
ARVALID_M	ARVALIDCHK_M	Output	Read address valid.	
ARID_M[10:0]	ARIDCHK_M[1:0]	Output	Read address ID.	
ARADDR_M[n:0] ^{ae}	ARADDRCHK_M[m:0] ^{af}	Output	Read address.	
ARLEN_M[7:0]	ARLENCHK_M	Output	Read burst length.	
ARSIZE_M[2:0]	ARCTLCHK0_M	Output	Read burst size.	
ARBURST_M[1:0]		Output	Read burst type.	
ARLOCK_M		Output	Read lock type.	
ARPROT_M[2:0]		Output	Read protection type.	
ARCACHE_M[3:0]	ARCTLCHK1_M	Output	Read cache type.	
ARQOS_M[3:0]		Output	Read QoS value.	
ARSNOOP_M[3:0]	ARCTLCHK2_M	Output	Shareable read transaction type.	
ARDOMAIN_M[1:0]		Output	Read shareability domain.	
ARUSER_M[n:0]	ARUSERCHK_M[m:0] ^{af}	Output. ^y	User signal.	
ARTRACE_M	ARTRACECHK_M	Output	-	

The following table shows the master interface Read Data Channel signals.

^{ae} The value of n is configuration-dependent.
^{af} The value of m = $\text{ceil}((n + 1)/8) - 1$.

Table A-36 Master interface Read Data Channel signals

Signal	Check signal	Type	Description	Connection information
RREADY_M	RREADYCHK_M	Output	Read data ready.	Connect to corresponding slave device, if populated. Connect to corresponding slave device, if populated, otherwise tie LOW.
RREADY_M	RREADYCHK_M	Input	Read data valid.	
RID_M[10:0]	RIDCHK_M[1:0]	Input	Read data ID.	
RDATA_M[127:0]/[255:0]	RDATACHK_M[15:0]/[31:0]	Input	Read data.	
RRESP_M[1:0]	RRESPCHK_M	Input	Read data response.	
RLAST_M	RLASTCHK_M	Input	Read data last transfer indication.	
RUSER_M[0:0]	RUSERCHK_M[0:0]	Input	User signal that is associated with the Read Data channel.	
RPOISON_M[p:0]^{ag}	RPOISONCHK_M[q:0]^{ah}	Input	Poison signal that is associated with the Read Data channel.	
RTRACE_M	RTRACECHK_M	Input	Trace signal that is associated with the Read Data channel.	

Note

RUSER_M[0] acts as an **RDATACHK** valid signal when the **DATACHECK_EN** parameter is enabled.

- If **RUSER_M[0]** == 0, SBSX or HN-I synthesizes the correct **RDATACHK** value before sending it on CHI read data response.
- If **RUSER_M[0]** == 1, SBSX or HN-I uses the **RDATACHK** pin value to drive on CHI read data response.

If **DATACHECK_EN** is not enabled, the **RUSER_M[0]** input is ignored.

Note

WUSER_M[0] acts as a **WDATACHK** valid signal. Because SBSX or HN-I always drives the **WDATACHK** value, **WUSER_M[0]** is set to 1 when **DATACHECK_EN** is enabled.

If **DATACHECK_EN** is not enabled, the **WUSER_M[0]** output is driven to 0.

^{ag} The value of $p = \text{ceil}((n + 1)/64) - 1$, where $(n + 1)$ is the width of **RDATA**.
^{ah} The value of $q = \text{ceil}((p + 1)/8) - 1$.

A.10 CGL interface signals

The following tables describe the CCIX Gateway Link interface signals.

Note

The signal names in this section are only a RootName. CMN-600AE interfaces use the RootName within a more fully specified signal name, **RootName_NID#**, where # represents the node ID corresponding to the specific interface.

Transmit signals

Note

Values for n and m transmit signals ***REQDATFLIT** and ***SNPFLIT** are configuration-dependent.

The following table contains Transmit Memory Request interface signals.

Table A-37 Transmit Memory Request interface signals

Signal	Check signal	Type	Description	Connection information
TXCGLREQDATFLITPEND	TXCGLREQDATFLITPENDCHK	Output	Transmit Memory Request Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the TX* signal to the matching RX* signal. Connect the TX*CHK signal to the matching RX*CHK signal.
TXCGLREQDATFLITV	TXCGLREQDATFLITVCHK	Output	Transmit Memory Request Flit Valid.	
TXCGLREQDATFLIT[n:0]	TXCGLREQDATFLITCHK[n:0]	Output	Transmit Memory Request Flit.	
TXCGLREQDATLCRDV	TXCGLREQDATLCRDVCHK	Input	Transmit Memory Request channel link layer credit.	

The following table contains Transmit Snoop Request interface signals.

Table A-38 Transmit Snoop Request interface signals

Signal	Check signal	Type	Description	Connection information
TXCGLSNPFLITPEND	TXCGLSNPFLITPENDCHK	Output	Transmit Snoop Request Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the TX* signal to the matching RX* signal. Connect the TX*CHK signal to the matching RX*CHK signal.
TXCGLSNPFLITV	TXCGLSNPFLITVCHK	Output	Transmit Snoop Request Flit Valid.	
TXCGLSNPFLIT[m:0]	TXCGLSNPFLITCHK[m:0]	Output	Transmit Snoop Request Flit.	
TXCGLSNPLCRDV	TXCGLSNPLCRDVCHK	Input	Transmit Snoop Request channel link layer credit.	

The following table contains Transmit Memory Response interface signals.

Table A-39 Transmit Memory Response interface signals

Signal	Check signal	Type	Description	Connection information
TXCGLREQRSPFLITPEND	TXCGLREQRSPFLITPENDCHK	Output	Transmit Memory Response Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the TX* signal to the matching RX* signal. Connect the TX*CHK signal to the matching RX*CHK signal.
TXCGLREQRSPFLITV	TXCGLREQRSPFLITVCHK	Output	Transmit Memory Response Flit Valid.	
TXCGLREQRSPFLIT[35:0]	TXCGLREQRSPFLITCHK[35:0]	Output	Transmit Memory Response Flit.	
TXCGLREQRSPLCRDV	TXCGLREQRSPLCRDVCHK	Input	Transmit Memory Response channel link layer credit.	

The following table contains Transmit Snoop Response interface signals.

Table A-40 Transmit Snoop Response interface signals

Signal	Check signal	Type	Description	Connection information
TXCGLSNPRSPFLITPEND	TXCGLSNPRSPFLITPENDCHK	Output	Transmit Snoop Response Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the TX* signal to the matching RX* signal. Connect the TX*CHK signal to the matching RX*CHK signal.
TXCGLSNPRSPFLITV	TXCGLSNPRSPFLITVCHK	Output	Transmit Snoop Response Flit Valid.	
TXCGLSNPRSPFLIT[35:0]	TXCGLSNPRSPFLITCHK[35:0]	Output	Transmit Snoop Response Flit.	
TXCGLSNPRSPLCRDV	TXCGLSNPRSPLCRDVCHK	Input	Transmit Snoop Response channel link layer credit.	

The following table contains Transmit Snoop Data interface signals.

Table A-41 Transmit Snoop Data interface signals

Signal	Check signal	Type	Description	Connection information
TXCGLSNPDATFLITPEND	TXCGLSNPDATFLITPENDCHK	Output	Transmit Snoop Data Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the TX* signal to the matching RX* signal. Connect the TX*CHK signal to the matching RX*CHK signal.
TXCGLSNPDATFLITV	TXCGLSNPDATFLITVCHK	Output	Transmit Snoop Data Flit Valid.	
TXCGLSNPDATFLIT[559:0]	TXCGLSNPDATFLITCHK[559:0]	Output	Transmit Snoop Data Flit.	
TXCGLSNPDATLCRDV	TXCGLSNPDATLCRDVCHK	Input	Transmit Snoop Data channel link layer credit.	

The following table contains Transmit Memory Response interface signals.

Table A-42 Transmit Memory Response interface signals

Signal	Check signal	Type	Description	Connection information
TXCGLRSPDATFLITPEND	TXCGLRSPDATFLITPENDCHK	Output	Transmit Memory Response Data Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the TX* signal to the matching RX* signal. Connect the TX*CHK signal to the matching RX*CHK signal.
TXCGLRSPDATFLITV	TXCGLRSPDATFLITVCHK	Output	Transmit Memory Response Data Flit Valid.	
TXCGLRSPDATFLIT[559:0]	TXCGLRSPDATFLITCHK[559:0]	Output	Transmit Memory Response Data Flit.	
TXCGLRSPDATLCRDV	TXCGLRSPDATLCRDVCHK	Input	Transmit Memory Response Data channel link layer credit.	

The following table contains Transmit Protocol Credit interface signals.

Table A-43 Transmit Protocol Credit interface signals

Signal	Check signal	Type	Description	Connection information
TXCGLPCRDFLITPEND	TXCGLPCRDFLITPENDCHK	Output	Transmit Protocol Credit Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the TX* signal to the matching RX* signal. Connect the TX*CHK signal to the matching RX*CHK signal.
TXCGLPCRDFLITV	TXCGLPCRDFLITVCHK	Output	Transmit Protocol Credit Flit Valid.	
TXCGLPCRDFLIT[50:0]	TXCGLPCRDFLITCHK[50:0]	Output	Transmit Protocol Credit Flit.	
TXCGLPCRDLCDV	TXCGLPCRDLCDVCHK	Input	Transmit Protocol Credit channel link layer credit.	

Receive signals

————— **Note** —————

Values for n and m receive signals *REQDATFLIT and *SNPFLIT are configuration-dependent.

The following table contains Receive Memory Request interface signals.

Table A-44 Receive Memory Request interface signals

Signal	Check signal	Type	Description	Connection information
RXCGLREQDATFLITPEND	RXCGLREQDATFLITPENDCHK	Input	Receive Memory Request Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the RX* signal to the matching TX* signal. Connect the RX*CHK signal to the matching TX*CHK signal.
RXCGLREQDATFLITV	RXCGLREQDATFLITVCHK	Input	Receive Memory Request Flit Valid.	
RXCGLREQDATFLIT[n:0]	RXCGLREQDATFLITCHK[n:0]	Input	Receive Memory Request Flit.	
RXCGLREQDATLCRDV	RXCGLREQDATLCRDVCHK	Output	Receive Memory Request channel link layer credit.	

The following table contains Receive Snoop Request interface signals.

Table A-45 Receive Snoop Request interface signals

Signal	Check signal	Type	Description	Connection information
RXCGLSNPFLITPEND	RXCGLSNPFLITPENDCHK	Input	Receive Snoop Request Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the RX* signal to the matching TX* signal. Connect the RX*CHK signal to the matching TX*CHK signal.
RXCGLSNPFLITV	RXCGLSNPFLITVCHK	Input	Receive Snoop Request Flit Valid.	
RXCGLSNPFLIT[m:0]	RXCGLSNPFLITCHK[m:0]	Input	Receive Snoop Request Flit.	
RXCGLSNPLCRDV	RXCGLSNPLCRDVCHK	Output	Receive Snoop Request channel link layer credit.	

The following table contains Receive Memory Response interface signals.

Table A-46 Receive Memory Response interface signals

Signal	Check signal	Type	Description	Connection information
RXCGLREQRSPFLITPEND	RXCGLREQRSPFLITPENDCHK	Input	Receive Memory Response Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the RX* signal to the matching TX* signal. Connect the RX*CHK signal to the matching TX*CHK signal.
RXCGLREQRSPFLITV	RXCGLREQRSPFLITVCHK	Input	Receive Memory Response Flit Valid.	
RXCGLREQRSPFLIT[35:0]	RXCGLREQRSPFLITCHK[35:0]	Input	Receive Memory Response Flit.	
RXCGLREQRSPLCRDV	RXCGLREQRSPLCRDVCHK	Output	Receive Memory Response channel link layer credit.	

The following table contains Receive Snoop Response interface signals.

Table A-47 Receive Snoop Response interface signals

Signal	Check signal	Type	Description	Connection information
RXCGLSNPRSPFLITPEND	RXCGLSNPRSPFLITPENDCHK	Input	Receive Snoop Response Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the RX* signal to the matching TX* signal. Connect the RX*CHK signal to the matching TX*CHK signal.
RXCGLSNPRSPFLITV	RXCGLSNPRSPFLITVCHK	Input	Receive Snoop Response Flit Valid.	
RXCGLSNPRSPFLIT[35:0]	RXCGLSNPRSPFLITCHK[35:0]	Input	Receive Snoop Response Flit.	
RXCGLSNPRSPLCRDV	RXCGLSNPRSPLCRDVCHK	Output	Receive Snoop Response channel link layer credit.	

The following table contains Receive Snoop Data interface signals.

Table A-48 Receive Snoop Data interface signals

Signal	Check signal	Type	Description	Connection information
RXCGLSNPDATFLITPEND	RXCGLSNPDATFLITPENDCHK	Input	Receive Snoop Data Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the RX* signal to the matching TX* signal. Connect the RX*CHK signal to the matching TX*CHK signal.
RXCGLSNPDATFLITV	RXCGLSNPDATFLITVCHK	Input	Receive Snoop Data Flit Valid.	
RXCGLSNPDATFLIT[559:0]	RXCGLSNPDATFLITCHK[559:0]	Input	Receive Snoop Data Flit.	
RXCGLSNPDATLCRDV	RXCGLSNPDATLCRDVCHK	Output	Receive Snoop Data channel link layer credit.	

The following table contains Receive Memory Response interface signals.

Table A-49 Receive Memory Response interface signals

Signal	Check signal	Type	Description	Connection information
RXCGLRSPDATFLITPEND	RXCGLRSPDATFLITPENDCHK	Input	Receive Memory Response Data Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the RX* signal to the matching TX* signal. Connect the RX*CHK signal to the matching TX*CHK signal.
RXCGLRSPDATFLITV	RXCGLRSPDATFLITVCHK	Input	Receive Memory Response Data Flit Valid.	
RXCGLRSPDATFLIT[559:0]	RXCGLRSPDATFLITCHK[559:0]	Input	Receive Memory Response Data Flit.	
RXCGLRSPDATLCRDV	RXCGLRSPDATLCRDVCHK	Output	Receive Memory Response Data channel link layer credit.	

The following table contains Receive Protocol Credit interface signals.

Table A-50 Receive Protocol Credit interface signals

Signal	Check signal	Type	Description	Connection information
RXCGLPCRDFLITPEND	RXCGLPCRDFLITPENDCHK	Input	Receive Protocol Credit Early Flit Valid hint.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the RX* signal to the matching TX* signal. Connect the RX*CHK signal to the matching TX*CHK signal.
RXCGLPCRDFLITV	RXCGLPCRDFLITVCHK	Input	Receive Protocol Credit Flit Valid.	
RXCGLPCRDFLIT[50:0]	RXCGLPCRDFLITCHK[50:0]	Input	Receive Protocol Credit Flit.	
RXCGLPCRDLCDV	RXCGLPCRDLCDVCHK	Output	Receive Protocol Credit channel link layer credit.	

The following table contains Receive and Transmit channel LinkActive interface signals.

Table A-51 Receive and Transmit channel LinkActive interface signals

Signal	Check signal	Type	Description	Connection information
RXCGLLINKACTIVEREQ	RXCGLLINKACTIVEREQCHK	Input	Receive channel LinkActive request from CXLA.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the RX* signal to the matching TX* signal. Connect the RX*CHK signal to the matching TX*CHK signal.
RXCGLLINKACTIVEACK	RXCGLLINKACTIVEACKCHK	Output	Receive channel LinkActive acknowledgement to CXLA.	
TXCGLLINKACTIVEREQ	TXCGLLINKACTIVEREQCHK	Output	Transmit channel LinkActive request to CXLA.	
TXCGLLINKACTIVEACK	TXCGLLINKACTIVEACKCHK	Input	Transmit channel LinkActive acknowledgement from CXLA.	

The following table contains RXCGLSACTIVE and TXCGLSACTIVE interface signals.

Table A-52 RXCGLSACTIVE and TXCGLSACTIVE interface signals

Signal	Check signal	Type	Description	Connection information
RXCGLSACTIVE	RXCGLSACTIVECHK	Input	Indication from CXLA that it has one or more outstanding protocol-layer transactions. RXSACTIVE must remain asserted throughout the lifetime of the transaction.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the RX* signal to the matching TX* signal. Connect the RX*CHK signal to the matching TX*CHK signal.
TXCGLSACTIVE	TXCGLSACTIVECHK	Output	Indication to CXLA that CXRH has one or more outstanding protocol-layer transactions. TXSACTIVE remains asserted throughout the lifetime of the transaction.	In the corresponding CXLA: <ul style="list-style-type: none"> Connect the TX* signal to the matching RX* signal. Connect the TX*CHK signal to the matching RX*CHK signal.

The *AMBA® CXS Protocol Specification* describes the CXS interface signals in CXLA.

A.11 Debug, trace, and PMU interface signals

Signals that aid debugging are included in CMN-600AE.

The following table shows the debug, trace, and PMU interface signals.

Note

- All signal names in this section are only a root name indicated as RootName. CMN-600AE interfaces use **RootName** within a more fully specified signal name, **RootName_NID#**, where # represents the node ID corresponding to the specific interface.
- Debug signals do not have a check signal equivalent.

Table A-53 Debug, trace, and PMU interface signals

Signal	Check signal	Type	Description	Connection information
ATCLKEN_NID<x>	-	Input	ATB clock enable, where <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
ATREADY_NID<x>	-	Input	ATB device ready: 0 = not ready, 1 = ready. <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
AFVALID_NID<x>	-	Input	FIFO flush request, where <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
ATDATA[31:0]_NID<x>	-	Output	ATB data bus, where <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
ATVALID_NID<x>	-	Output	ATB valid data: 0 = no valid data, 1 = valid data. <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
ATBYTES[1:0]_NID<x>	-	Output	CoreSight ATB device data size: 0b00 = 1 byte, 0b01 = 2 bytes, 0b10 = 3 bytes, 0b11 = 4 bytes. <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
AFREADY_NID<x>	-	Output	FIFO flush acknowledge: 0 = FIFO flush not complete, 1 = FIFO flush complete. <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
ATID[6:0]_NID<x>	-	Output	ATB trace source identification, where <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
DBGWATCHTRIGREQ_NID<x>	-	Output	Trigger output from DEM indicating assertion of a DT event. DBGWATCHTRIGREQ is asynchronous-safe, and operates in a four-phase handshake with DBGWATCHTRIGACK . <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	Connect to external debug and trace control logic.

Table A-53 Debug, trace, and PMU interface signals (continued)

Signal	Check signal	Type	Description	Connection information
DBGWATCHTRIGACK_NID<x>	-	Input	External acknowledgment of receipt of DBGWATCHTRIGREQ . DBGWATCHTRIGACK must be asynchronous-safe, and operates in a four-phase handshake with DBGWATCHTRIGREQ . <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	Connect to external debug and trace control logic, or tie LOW if DBGWATCHTRIGREQ is unused.
PMUSNAPSHOTREQ	-	Input	External request that the live PMU counters are snapshot to the shadow registers. PMUSNAPSHOTREQ must be asynchronous-safe, and operates in a four-phase handshake with PMUSNAPSHOTACK .	Connect to external debug and trace control logic, or tie LOW if unused.
PMUSNAPSHOTACK	-	Output	Indication that all live PMU counters have been copied to shadow registers and the contents can be read. PMUSNAPSHOTACK is asynchronous-safe, and operates in a four-phase handshake with PMUSNAPSHOTREQ .	Connect to external debug and trace control logic.
NIDEN	-	Input	Global enable for all debug, trace, and PMU functionality. 0 Disabled. 1 Enabled.	Tie or drive as appropriate to meet system security requirements.
SPNIDEN	-	Input	Global enable for secure debug, trace, and PMU capability. Only applicable when NIDEN is enabled. 0 Disabled. 1 Enabled.	
TSVALUEB[63:0]	-	Input	Global system timestamp value in binary format.	Connect to external system timestamp counter output.

A.12 DFT and MBIST interface signals

Signals that support DFT and MBIST capabilities are included in CMN-600AE.

The following table shows the DFT signals.

Table A-54 DFT signals

Signal	Check signal	Type	Description	Connection information
DFTCLKBYPASS	DFTCLKBYPASSCHK	Input	Select the SLC RAM clock to follow the CMN-600AE input clock, as applicable for each clock region.	Tie LOW if unused. <hr/> Note The DFT check signal has the same polarity as the corresponding DFT signal.
DFTCLKDISABLE[3:0]	DFTCLKDISABLECHK[3:0]	Input	Disable clock regions during scan shift.	
DFTRAMHOLD	DFTRAMHOLDCHK	Input	Disable the RAM chip select during scan shift.	
DFTMCPHOLD	DFTMCPHOLDCHK	Input	Assert to prevent HN-F multicycle RAMs from clocking during capture cycles.	
DFTRSTDISABLE[1:0]	DFTRSTDISABLECHK[1:0]	Input	Disable internal synchronized reset during scan shift.	
DFTCGEN	DFTCGENCHK	Input	Scan shift enable. Forces on the clock grids during scan shift.	

Table A-55 DFT signals continued

Signal	Check signal	Type	Description	Connection information
DFTSCANMODE	DFTSCANMODECHK	Input	<p>During functional mode, the HN-F SLC and SF RAM set address and write data inputs satisfy RAM hold timing constraints using pipeline behavior. The set address and write data are only clocked and enabled the cycle before the RAMs are accessed, and are held the cycle that the RAM clock asserts.</p> <p>The RAM hold constraints are not guaranteed during ATPG test, because random data is shifted into the flops that control the set address and write data flop enables. This allows the set address and write data to change in the same cycle as a RAM access, violating the RAM hold constraints.</p> <p>This signal addresses the hold constraints during ATPG test. It is used to force the RAM set address and write data flop enables LOW in the cycle that RAM clocks are enabled during ATPG test.</p> <p>The combination of the functional pipeline behavior and this override logic enable holds MCPs to be used on the RAM set address and write data inputs in the implementation flow and during static timing analysis.</p>	<p>Tie LOW if unused.</p> <p>————— Note —————</p> <p>The DFT check signal has the same polarity as the corresponding DFT signal.</p>

The following table shows the MBIST signals.

Table A-56 MBIST signals

Signal	Check signal	Type	Description	Connection information
nMBISTRESET	nMBISTRESETCHK	Input	Primary reset to enter MBIST. Must be HIGH during functional non-MBIST operation.	Tie HIGH if unused.
MBISTREQ	-	Input	SLC MBIST mode request	Tie LOW if unused.

A.13 Processor event interface signals

Signals that support processor event interface capabilities are included in CMN-600AE.

The following table shows the processor event interface signals.

Note

All signal names in this section are only a root name indicated as RootName. CMN-600AE interfaces use RootName within a more fully specified signal name, **RootName_NID#**, where # represents the node ID corresponding to the specific interface.

Processor event interface signals are present at RN-F, RN-I, and RN-D node locations.

Table A-57 Processor event interface signals

Signal	Check signal	Type	Description	Connection information
EVENTIREQ	EVENTIREQCHK	Output	Event input request for processor wake up from WFE state. Remains asserted until EVENTIACK is asserted, and is not reasserted until EVENTIACK is LOW.	Connect to EVENTIREQ input of processor.
EVENTIACK	EVENTIACKCHK	Input	Event input request acknowledge. Must not be asserted until EVENTIREQ is HIGH, and then must remain asserted until after EVENTIREQ goes LOW.	Connect to EVENTIACK output of processor, or tie to EVENTIREQ output of CMN-600AE if unused.
EVENTOREQ	EVENTOREQCHK	Input	Event output request for processor wake up, triggered by SEV instruction. Must only be asserted when EVENTOACK is LOW, and then must remain HIGH until after EVENTOACK goes HIGH.	Connect to EVENTOREQ output of processor, or tie LOW if unused.
EVENTOACK	EVENTOACKCHK	Output	Event output request acknowledge. Is not asserted until EVENTOREQ is HIGH, and then remains asserted until after EVENTOREQ goes LOW.	Connect to EVENTOACK input of processor.

A.14 AXI4-Stream interface signals

Signals that support AXI4-Stream are included in CMN-600AE.

The following table shows the receive interface AXI4-Stream signals.

Table A-58 Receive interface AXI4-Stream signals

Signal	Check signal	Type	Description	Connection information
RXA4STVALID	RXA4STVALIDCHK	Input	Indicates that the master is driving a valid transfer.	Connect to corresponding AXI4-Stream TX ports on external device.
RXA4STREADY	RXA4STREADYCHK	Output	Indicates that the slave can accept a transfer in the current cycle.	
RXA4STDATA[63:0]	RXA4STDATACHK[7:0]	Input	Data payload.	
RXA4STSTRB[7:0]	RXA4STSTRBCHK	Input	Byte qualifier that indicates whether the content of the associated byte of TDATA is processed as a data byte or a position byte.	
RXA4STKEEP[7:0]	RXA4STKEEPCHK	Input	Byte qualifier that indicates null bytes when deasserted.	
RXA4STLAST	RXA4STLASTCHK	Input	Packet boundary indicator.	
RXA4STID[7:0]	RXA4STIDCHK	Input	Data stream identifier.	
RXA4STDEST[7:0]	RXA4STDESTCHK	Input	Routing information.	
RXA4STRI[7:0]	RXA4STRICHK	Input	Data stream resource identifier for CCIX transfer.	

The following table shows the transmit interface AXI4-Stream signals.

Table A-59 Transmit interface AXI4-Stream signals

Signal	Check signal	Type	Description	Connection information
TXA4STVALID	TXA4STVALIDCHK	Output	Indicates that the master is driving a valid transfer.	Connect to corresponding AXI4-Stream RX ports on external device.
TXA4STREADY	TXA4STREADYCHK	Input	Indicates that the slave can accept a transfer in the current cycle.	
TXA4STDATA[63:0]	TXA4STDATACHK[7:0]	Output	Data payload.	
TXA4STSTRB[7:0]	TXA4STSTRBCHK	Output	Byte qualifier that indicates whether the content of the associated byte of TDATA is processed as a data byte or a position byte.	
TXA4STKEEP[7:0]	TXA4STKEEPCHK	Output	Byte qualifier that indicates null bytes when deasserted.	
TXA4STLAST	TXA4STLASTCHK	Output	Packet boundary indicator.	
TXA4STID[7:0]	TXA4STIDCHK	Output	Data stream identifier.	
TXA4STDEST[7:0]	TXA4STDESTCHK	Output	Routing information.	

The following table shows the AXI4-Stream miscellaneous signals.

Table A-60 AXI4-Stream miscellaneous signals

Signal	Check signal	Type	Description	Connection information
GICD_DESTID[15:0]	GICD_DESTIDCHK[15:0]	Input	PUB_DESTID that is associated with the A4S port to which GICD is connected.	See <i>Arm® CoreLink™ CMN-600AE Release Note</i> for information on determining the PUB_DESTID of the GICD A4S port.

A.15 FMU interface signals

Signals that support FMU capabilities are included in CMN-600AE.

The following table shows the FMU signals.

Table A-61 FMU signals

Signal	Check signal	Type	Description	Connection information
FMU_ERI_NID<x> ^{ai}	FMU_ERICHK_NID<x> ^{ai}	Output	Critical error interrupt.	Connect to ERI input of external FMU
FMU_FHI_NID<x> ^{ai}	FMU_FHCHK	Output	Non-critical error interrupt.	Connect to FHI input of external FMU.
RXERRAGINFO_NID<y>[9:0] ^{aj}	RXERRAGINFOCHK_NID<y>[9:0] ^{aj}	Input	FuSa error bus from external components that are connected to CMN-600AE such as CXLA or CDB.	Connect to TXERRAGGINFO output port of CXLA or CDB, when present.

^{ai} Where x is the node ID of the HN-D.

^{aj} Where y is the node ID that corresponds to the device port to which CXLA or CDB is connected.

A.16 APB interface signals

Signals that support APB capabilities are included in CMN-600AE.

The following table shows the APB signals.

Table A-62 APB signals

Signal	Check signal	Type	Description	Connection information
PADDR[31:0]	PADDRCHK[3:0]	Input	Address that is associated with the APB transaction.	Connect to corresponding ports on external APB master device.
PPROT[2:0]	PCTRLCHK	Input	Protection type of the transaction.	
PWRITE		Input	Indicates write access when HIGH. Indicates read access when LOW.	
PSEL	PSELCHK	Input	Indicates that the slave device is selected and that a data transfer is required.	
PENABLE	PENABLECHK	Input	Enable. Indicates the second and subsequent cycles of an APB transfer.	
PWDATA[31:0]	PWDATACHK[3:0]	Input	Write data.	
PSTRB[3:0]	PSTRBCHK	Input	Write strobes.	
PREADY	PREADYCHK	Output	Ready.	
PRDATA[31:0]	PRDATACHK[3:0]	Output	Read data.	
PSLVERR	PSLVERRCHK	Output	Indicates a transfer failure.	

Appendix B

Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

- [B.1 Revisions on page Appx-B-1964](#).

B.1 Revisions

Differences between released versions of the document are listed in this appendix.

Table B-1 Issue 0000-00 LAC

Change	Location	Affects
First release for r0p0 LAC.	-	-

Table B-2 Differences between Issue 0000-00 LAC and Issue 0100-01 EAC

Change	Location	Affects
Changed instances of ACE-Lite+DVM to ACE-Lite-with-DVM.	Throughout document	All revisions
Updated additional reading to include RAS Architecture Specification.	Additional reading on page 10	All revisions
Reorganized subsections.	1.3 Features on page 1-16	All revisions
Updated REQ_RSVDC_WIDTH parameter description.	<i>Mesh sizing and top level configuration</i> , removed in a subsequent release	All revisions
Added information about the User Guide.	1.7 Product documentation and design flow on page 1-33	All revisions
Updated product revisions for r1p0.	1.8 Product revisions on page 1-35	r1p0
Clarified width of NodeID REQ flit field on internal and external CHI interfaces.	2.4 Node ID mapping on page 2-51	All revisions
Updated ERRGSR numbering in diagrams.	2.14 Reliability, Availability, and Serviceability on page 2-80	All revisions
Added information about MPU access violations and clarified poison errors on DAT flits.	2.14.5 HN-F error handling on page 2-89	All revisions
Updated information about error handling at the RN-I.	2.14.8 RN-I error handling on page 2-93	All revisions
Added section.	Illegal MPU Access Errors on page 2-91	All revisions
Added information about MPU access errors.	HN-I summary on sending NDE and DE on page 2-92	All revisions
Updated information about error handling at the XP.	2.14.9 XP error handling on page 2-94	All revisions
Added section.	2.15 CCIX Port Aggregation Groups on page 2-96	All revisions
Removed table.	SN contiguous address spaces	All revisions
Added note about Non-hashed Region 7 for RN SAM CPA programming sequence.	2.20.4 Support for CCIX Port Aggregation on page 2-117	All revisions
Removed section.	<i>RN and HN-F SAM R2 Support</i>	All revisions
Removed section.	<i>Global clock</i>	All revisions
Removed section.	<i>Timing closure with credited slices</i>	All revisions
Added constraints for power states and transitions.	2.26.7 HN-F power domains on page 2-145	All revisions
Added assumptions of use for FuSa error reporting and the External Clock Controller.	3.2.2 Asynchronous interface signals on page 3-161	All revisions
Added note about CXHA RAMs.	3.5 Shared RAM protection on page 3-170	All revisions
Updated diagrams.	3.5.2 Address protection on page 3-170	All revisions
Updated transaction trackers.	Table 3-1 Device transaction trackers with hang detection on page 3-176	All revisions
Updated description for ERRSTATUS.	Table 3-3 FDC register set on page 3-185	All revisions

Table B-2 Differences between Issue 0000-00 LAC and Issue 0100-01 EAC (continued)

Change	Location	Affects
Added section.	3.9.5 Clearing the ERRSTATUS on page 3-185	All revisions
Removed <i>por_cxg_ra_sam_mem_region{0-7}_limit_reg</i> registers.	4.2.12 CXRA register summary on page 4-210	All revisions
Removed section due to redundancy.	<i>CFGM register summary</i>	All revisions
Updated bit [57] assignment. Updated description for <i>hnf_excl_snp_fwd_en</i> .	por_hnf_aux_ctl on page 4-385	r1p0
Updated bit [3] assignment.	por_hnf_r2_aux_ctl on page 4-389	r1p0
Updated bit [15:10] assignments.	rdf_hnf_aux_ctl on page 4-390	r1p0
Updated bit [29:28] assignments.	por_hni_unit_info on page 4-612	r1p0
Updated bit [25:24] assignments.	por_mxp_p0_info on page 4-663	r1p0
Updated bit [25:24] assignments.	por_mxp_p1_info on page 4-664	r1p0
Updated bit [1] assignment.	por_mxp_secure_register_groups_override on page 4-666	r1p0
Updated bit [45:44] assignments.	por_rnd_unit_info on page 4-734	r1p0
Updated bit [45:44] assignments.	por_rni_unit_info on page 4-766	r1p0
Updated bit [21] assignment.	por_sbsx_unit_info on page 4-883	r1p0
Updated bit [22] assignment.	por_cxla_unit_info on page 4-1049	r1p0
Updated bit [3] assignment.	por_fmu_ctl on page 4-1090	r1p0
Updated bit [3:0] assignments.	por_fdc_aux_ctl_mxp on page 4-1783	r1p0
Updated description for <i>HANG_DET_CONFIG</i> .	por_fdc_aux_ctl_p0_d0 on page 4-1788 por_fdc_aux_ctl_p0_d1 on page 4-1794 por_fdc_aux_ctl_p0_d2 on page 4-1800 por_fdc_aux_ctl_p0_d3 on page 4-1806 por_fdc_aux_ctl_p1_d0 on page 4-1812 por_fdc_aux_ctl_p1_d1 on page 4-1818 por_fdc_aux_ctl_p1_d2 on page 4-1824 por_fdc_aux_ctl_p1_d3 on page 4-1830	r1p0
Added <i>ReadNotSharedDirty</i> to list of Cacheable transactions.	5.5 Cacheable and Non-cacheable exclusives on page 5-1853	All revisions
Added tables for CDB and ADB clock management signals.	Table A-4 Additional clock management signals for CDB on page Appx-A-1924 Table A-5 Additional clock management signals for ADB on page Appx-A-1925	All revisions
Added tables for CDB and ADB power management signals.	Table A-7 Additional power management signals for CDB on page Appx-A-1927 Table A-8 Additional power management signals for ADB on page Appx-A-1927	All revisions
Removed section due to redundancy.	<i>A4S Signal list</i>	All revisions

Table B-2 Differences between Issue 0000-00 LAC and Issue 0100-01 EAC (continued)

Change	Location	Affects
Clarified configuration-dependent width of AxUSER signals.	<ul style="list-style-type: none"> A.9.1 ACE-Lite-with-DVM slave interface signals on page Appx-A-1937 A.9.2 AXI/ACE-Lite master interface signals on page Appx-A-1942 	All revisions
Removed appendix.	<i>CXS Specification</i>	All revisions

Table B-3 Differences between Issue 0000-00 LAC and Issue 0100-01 EAC

Change	Location	Affects
Added a section on error handling.	3.10.4 Example FuSa error handling on page 3-187	All revisions
Updated information on CMOs.	5.4 Cache maintenance operations on page 5-1852	All revisions
Removed note about FDC logical ID.	por_fdc_node_info on page 4-1774	All revisions
Updated references to GIC-600 to GIC-600AE.	Throughout	All revisions

Table B-4 Differences between Issue 0010-01 EAC and Issue 0100-03 EAC

Change	Location	Affects
Updates to language for clarification	Throughout	All revisions
Additional information on PA width restrictions and a possible truncation error that can result.	2.6 Addressing capabilities on page 2-64	All revisions
Clarification of CHI feature support for CML	1.3.3 CHI feature support for CML on page 1-17	All revisions
Clarification that CMN-600AE does not support 6-SN mode.	Throughout, particularly 2.19 HN-F SAM on page 2-105 and RN and HN-F SAM .	All revisions

Table B-5 Differences between Issue 0010-01 EAC and Issue 0100-03 EAC

Change	Location
Updates to language for clarification.	Throughout
Extended information on RN and HN-F SAM programming.	2.20 RN and HN-F SAM additional features and programming on page 2-110
Removal of information on unsupported 6-SN mode.	Throughout, particularly 2.19 HN-F SAM on page 2-105 and 2.20 RN and HN-F SAM additional features and programming on page 2-110.
Clarification of truncation error and avoidance.	2.6 Addressing capabilities on page 2-64
Added information about APB interfaces, including a note on silent fails.	3.10.3 APB Interface on page 3-187
Correction of descriptions and reset values for MPU programmable limit address and programmable base address registers, for bit ranges [47:32] and [31:12].	4.3.15 MPU register descriptions on page 4-1162